8-Bit Shift Register/Latch (3-State)

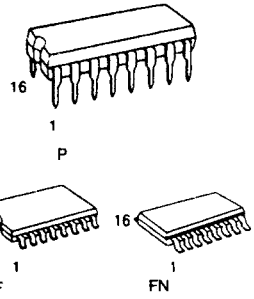
The TC74HC595A is a high speed CMOS 8-BIT SHIFT REGISTER/LATCH fabricated with silicon gate C^2MOS technology.

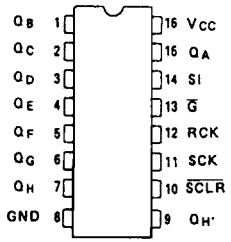
It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC595A contains an 8-bit static shift register which feeds an 8-bit storage register.

Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stabler during the shift operation. And, since the parallel outputs are 3-state, it can be directly connected to 8-bit bus. This register can be used in serial-to-parallel conversion, data receivers, etc.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

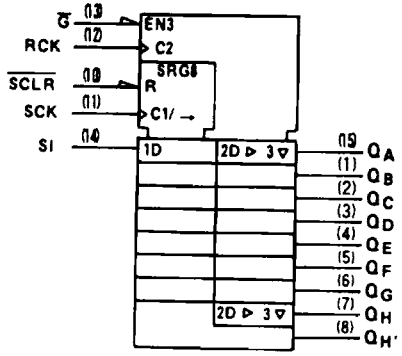




Pin Assignment

Features

- High Speed: f_{MAX} = 55MHz(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Output Drive Capability: 15 LSTTL Loads For QA ~ QH
  10 LSTTL Loads For QA'
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 6mA(Min.)
  For QA ~ QH
  $|I_{OH}| = I_{OL}$ = 4mA(Min.)
  For QH'
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS595

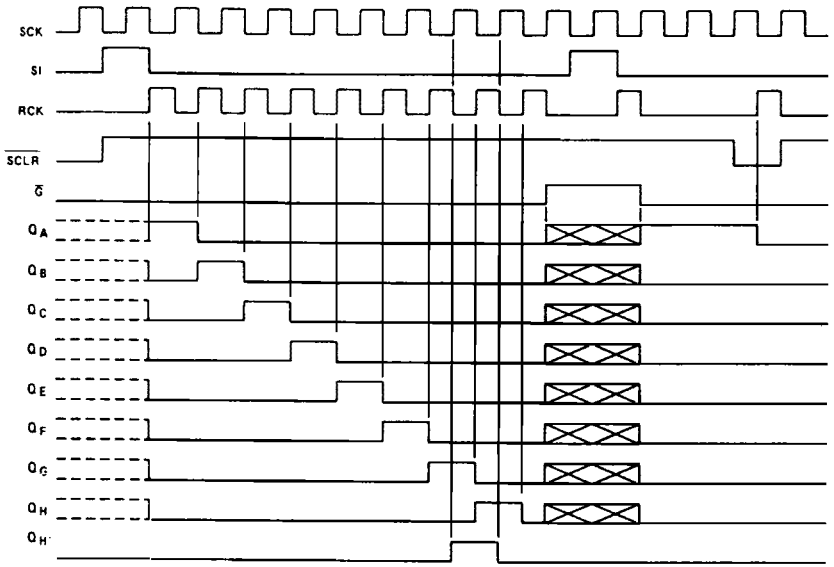


IEC Logic Symbol

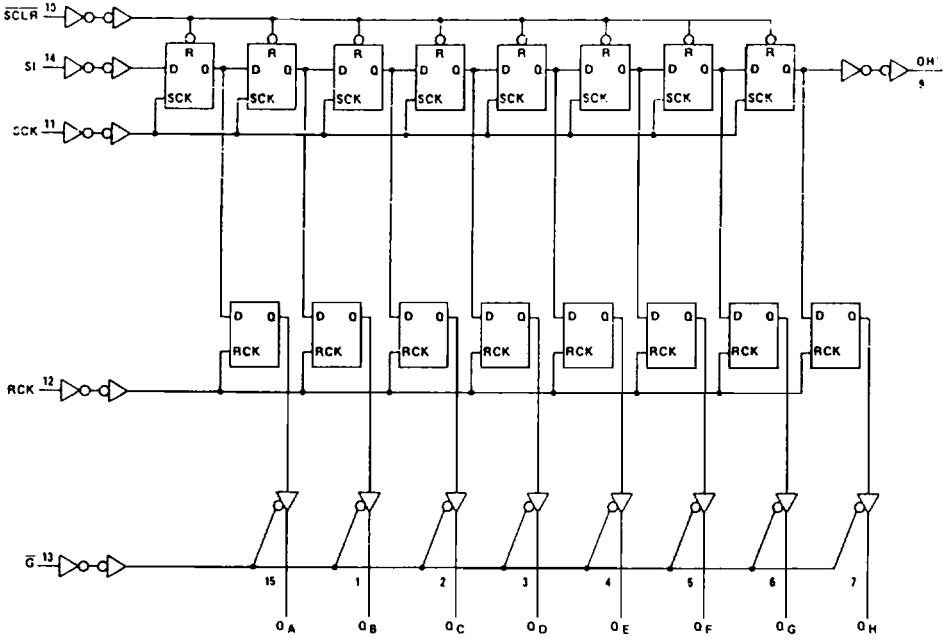
Truth Table

Inputs					Function
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA through QH outputs disable
X	X	X	X	L	QA through QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First of S.R. becomes "L". Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S.R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register state is not changed.

X: Don't Care



Timing Chart



Logic Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current (Q_H') (Q_A ~ Q_H)	I_{OUT}	±25 ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition			Ta = 25°C			Ta = -40 ~ 85°C		Unit
				V_{CC}	Min.	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
		Q_H'	I_{OH} = -4 mA I_{OH} = -5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
		Q_A ~ Q_H	I_{OH} = -6 mA I_{OH} = -7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
		Q_H'	I_{OH} = 4 mA I_{OH} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
		Q_A ~ Q_H	I_{OL} = 6 mA I_{OL} = 7.8mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	

DC Electrical Characteristics

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	6.0	–	–	±0.5	–	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	–	–	±0.1	–	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	–	–	4.0	–	40.0	

Timing Requirements (Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (SCK, RCK)	$t_{W(H)}$ $t_{W(L)}$	–	2.0 4.5 6.0	– – –	75 15 13	95 19 16	ns
Minimum Pulse Width ($\overline{SCLR}$)	$t_{W(L)}$	–	2.0 4.5 6.0	– – –	75 15 13	95 19 16	
Minimum Setup Time (SI-SCK)	t_s	–	2.0 4.5 6.0	– – –	50 10 9	165 13 11	
Minimum Setup Time (SCK-RCK))	t_s	–	2.0 4.5 6.0	– – –	75 15 13	95 19 16	
Minimum Setup Time ($\overline{SCLR}$-RCK)	t_s	–	2.0 4.5 6.0	– – –	100 20 17	125 25 21	
Minimum Hold Time	t_h	–	2.0 4.5 6.0	– – –	0 0 0	0 0 0	
Minimum Removal Time ($\overline{SCLR}$)	t_{rem}	–	2.0 4.5 6.0	– – –	50 10 9	65 13 11	
Clock Frequency	f	–	2.0 4.5 6.0	– – –	6 30 35	5 25 28	MHz

AC Electrical Characteristics (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time (Q_H')	t_{TLH} t_{THL}	–	–	4	8	ns
Propagation Delay Time (SCK-Q_H')	t_{pLH} t_{pHL}	–	–	12	21	
Propagation Delay Time ($\overline{SCLR}$-Q_H')	t_{pHL}	–	–	15	30	
Maximum Clock Frequency	f_{MAX}	–	35	77	–	MHz

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition			Ta = 25°C			Ta = -40 ~ 85°C		Unit
			CL	V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time (Qn)	t_{TLH} t_{THL}	–	50	2.0	–	25	60	–	75	ns
				4.5	–	7	12	–	15	
				6.0	–	6	10	–	13	
Output Transition Time (Q_H')	t_{TLH} t_{THL}	–	50	2.0	–	30	75	–	95	
				4.5	–	8	15	–	19	
				6.0	–	7	13	–	16	
Propagation Delay Time (SCK-Q_H')	t_{pLH} t_{pHL}	–	50	2.0	–	45	125	–	155	
				4.5	–	15	25	–	31	
				6.0	–	13	21	–	26	
Propagation Delay Time ($\overline{SCLR}$-Q_H')	t_{pHL}	–	50	2.0	–	60	175	–	220	
				4.5	–	18	35	–	44	
				6.0	–	15	30	–	37	
Propagation Delay Time (RCK-Qn)	t_{pLH} t_{pHL}	–	50	2.0	–	60	150	–	190	
				4.5	–	20	30	–	38	
				6.0	–	17	26	–	32	
			150	2.0	–	75	190	–	240	
				4.5	–	25	38	–	48	
				6.0	–	22	32	–	41	
Output Enable Time	t_{pZL} t_{pZH}	R_L = 1kΩ	50	2.0	–	45	135	–	170	
				4.5	–	15	27	–	34	
				6.0	–	13	23	–	29	
			150	2.0	–	60	175	–	220	
				4.5	–	20	35	–	44	
				6.0	–	17	30	–	37	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L = 1kΩ	50	2.0	–	30	150	–	190	
				4.5	–	15	30	–	38	
				6.0	–	14	26	–	32	
Maximum Clock Frequency	f_{MAX}	–	50	2.0	6	17	–	5	–	MHz
				4.5	30	50	–	25	–	
				6.0	35	59	–	28	–	
Input Capacitance	C_{IN}	–			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	–			–	184	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$