SIEMENS

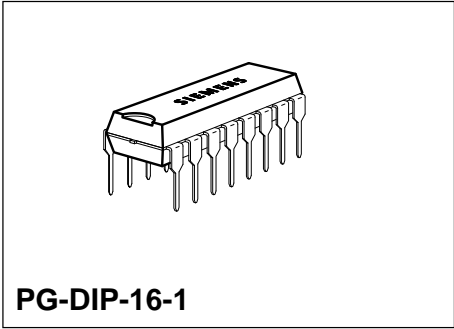## Phase Control IC   TCA 785

Pb-free lead plating; RoHS compliant   **Bipolar IC**

Features

- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
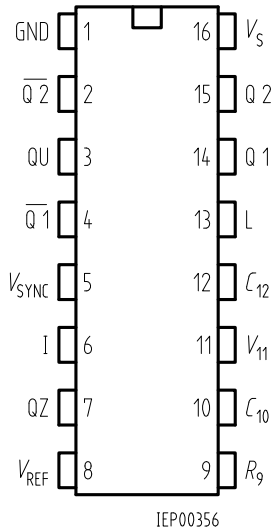- Large ramp current range
- Wide temperature range

PG-DIP-16-1

Type	Ordering Code	Package
TCA 785	Q67000-A2321	PG-DIP-16-1

This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0 ° and 180 °. Typical applications include converter circuits, AC controllers and three-phase current controllers.

This IC replaces the previous types TCA 780 and TCA 780 D.

Pin Configuration
(top view)

```
GND     1        16   V_S
Q2      2        15   Q 2
QU      3        14   Q 1
Q1      4        13   L
V_SYNC  5        12   C_12
I       6        11   V_11
QZ      7        10   C_10
V_REF   8        9    R_9
```
IEP00356

Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	$\overline{Q2}$	Output 2 inverted
3	Q U	Output U
4	$\overline{Q2}$	Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6	I	Inhibit
7	Q Z	Output Z
8	V_{REF}	Stabilized voltage
9	R_9	Ramp resistance
10	C_{10}	Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14	Q 1	Output 1
15	Q 2	Output 2
16	V_S	Supply voltage

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Functional Description

The synchronization signal is obtained via a high-ohmic resistance from the line voltage (voltage V_5). A zero voltage detector evaluates the zero passages and transfers them to the synchronization register.

This synchronization register controls a ramp generator, the capacitor C_{10} of which is charged by a constant current (determined by R_9). If the ramp voltage V_{10} exceeds the control voltage V_{11} (triggering angle φ), a signal is processed to the logic. Dependent on the magnitude of the control voltage V_{11}, the triggering angle φ can be shifted within a phase angle of $0°$ to $180°$.

For every half wave, a positive pulse of approx. 30 μs duration appears at the outputs Q 1 and Q 2. The pulse duration can be prolonged up to $180°$ via a capacitor C_{12}. If pin 12 is connected to ground, pulses with a duration between φ and $180°$ will result.
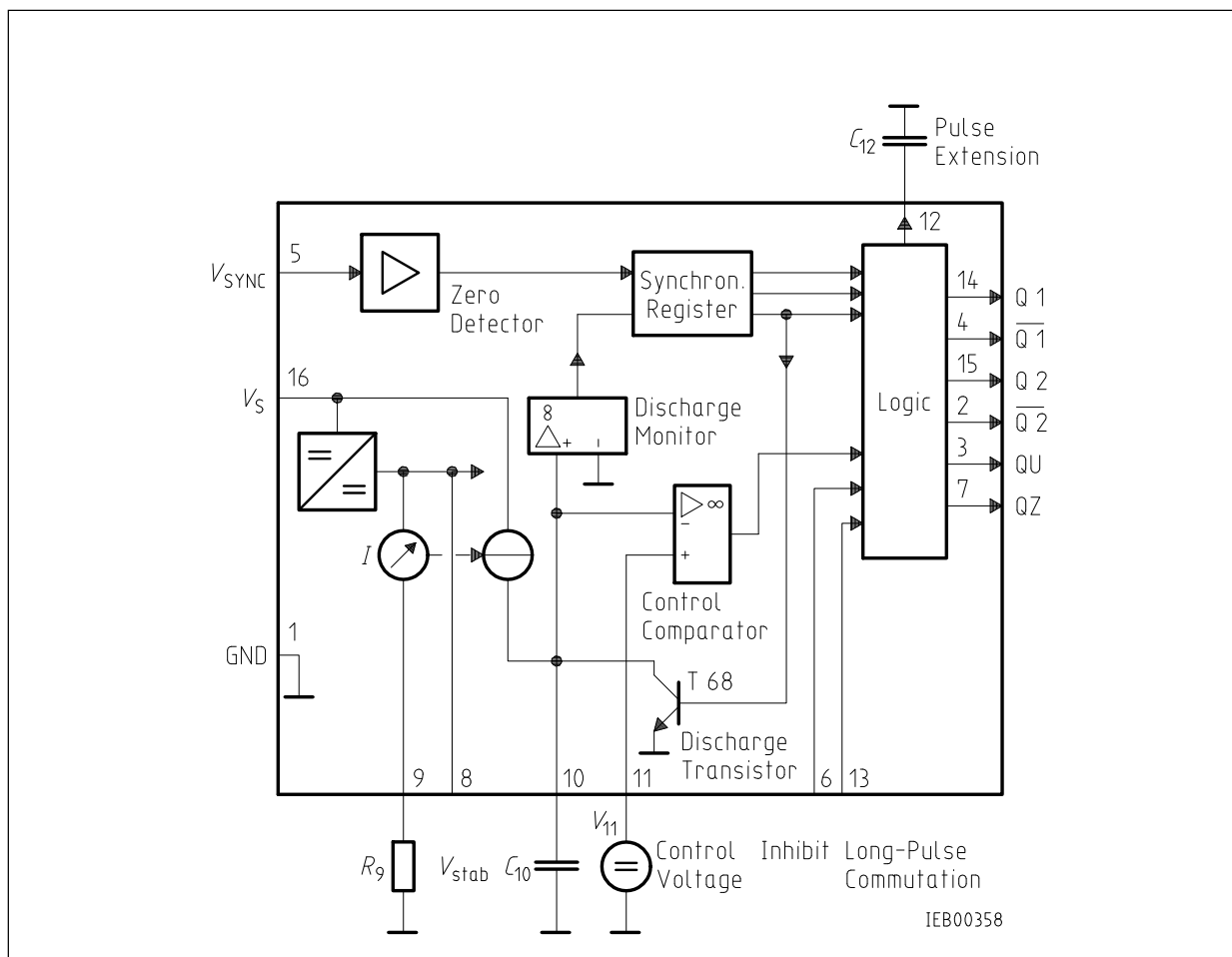
Outputs $\overline{Q1}$ and $\overline{Q2}$ supply the inverse signals of Q 1 and Q 2.

A signal of $\varphi + 180°$ which can be used for controlling an external logic, is available at pin 3.
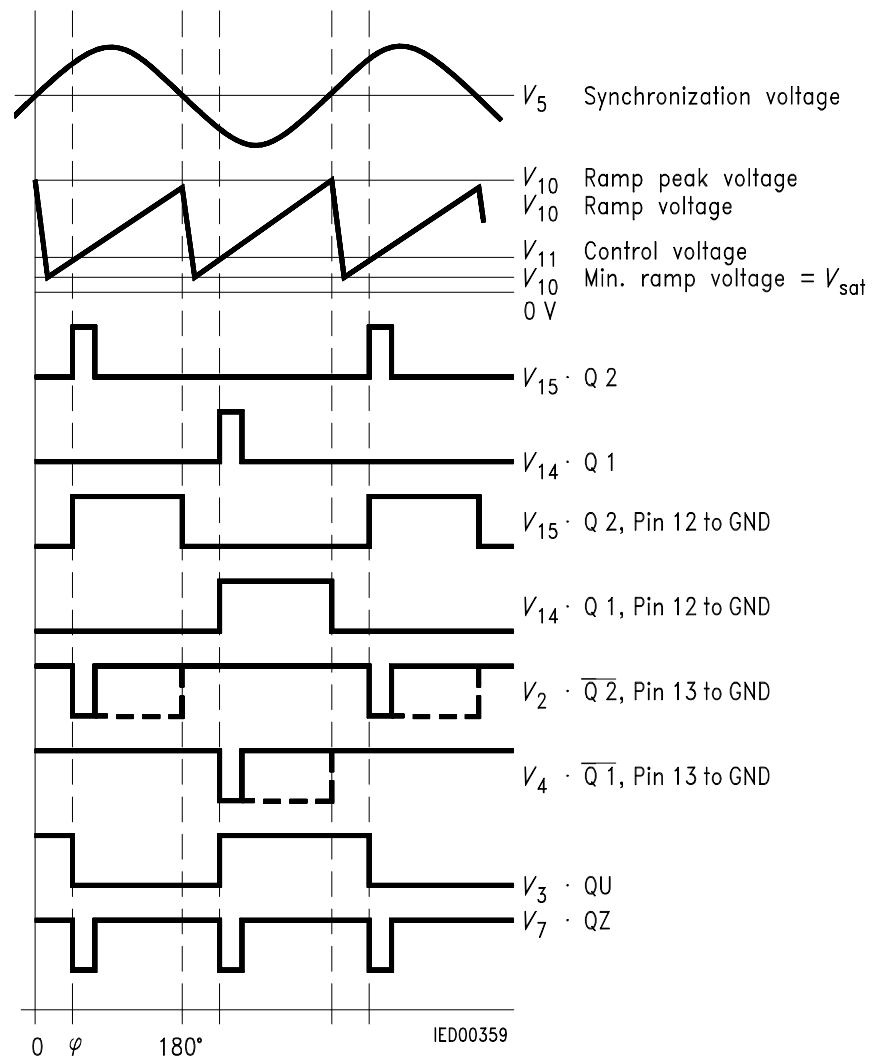
A signal which corresponds to the NOR link of Q 1 and Q 2 is available at output Q Z (pin 7).

The inhibit input can be used to disable outputs Q1, Q2 and $\overline{Q1}$, $\overline{Q2}$.

Pin 13 can be used to extend the outputs $\overline{Q1}$ and $\overline{Q2}$ to full pulse length ($180° - \varphi$).

Block Diagram

V_5 Synchronization voltage

V_{10} Ramp peak voltage
V_{10} Ramp voltage

V_{11} Control voltage
V_{10} Min. ramp voltage = V_{sat}
0 V

$V_{15} \cdot$ Q 2

$V_{14} \cdot$ Q 1

$V_{15} \cdot$ Q 2, Pin 12 to GND

$V_{14} \cdot$ Q 1, Pin 12 to GND

$V_2 \cdot \overline{Q\ 2}$, Pin 13 to GND

$V_4 \cdot \overline{Q\ 1}$, Pin 13 to GND

$V_3 \cdot$ QU
$V_7 \cdot$ QZ

0   φ 180°   IED00359

Pulse Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	− 0.5	18	V
Output current at pin 14, 15	I_Q	− 10	400	mA
Inhibit voltage	V_6	− 0.5	V_S	V
Control voltage	V_{11}	− 0.5	V_S	V
Voltage short-pulse circuit	V_{13}	− 0.5	V_S	V
Synchronization input current	V_5	− 200	± 200	μA
Output voltage at pin 14, 15	V_Q		V_S	V
Output current at pin 2, 3, 4, 7	I_Q		10	mA
Output voltage at pin 2, 3, 4, 7	V_Q		V_S	V
Junction temperature	T_j		150	˚C
Storage temperature	T_{stg}	− 55	125	˚C
Thermal resistance system - air	$R_{th\ SA}$		80	K/W

Operating Range

Parameter	Symbol	Limit Values		Unit
Supply voltage	V_S	8	18	V
Operating frequency	f	10	500	Hz
Ambient temperature	T_A	− 25	85	˚C

Characteristics

$8 \leq V_S \leq 18$ V; $− 25$ ˚C $\leq T_A \leq 85$ ˚C; $f = 50$ Hz

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Supply current consumption S1 … S6 open $V_{11} = 0$ V $C_{10} = 47$ nF; $R_9 = 100$ kΩ	I_S	4.5	6.5	10	mA	1
Synchronization pin 5 Input current R_2 varied	$I_{5\ rms}$	30		200	μA	1
Offset voltage	ΔV_5		30	75	mV	4
Control input pin 11 Control voltage range	V_{11}	0.2		$V_{10\ peak}$	V	1
Input resistance	R_{11}		15		kΩ	5

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Characteristics (cont'd)

$8 \le V_S \le 18$ V; $-25\ ^{\circ}$C $\le T_A \le 85\ ^{\circ}$C; $f = 50$ Hz

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Ramp generator						
Charge current	I_{10}	10		1000	μA	
Max. ramp voltage	V_{10}			$V_2 - 2$	V	1
Saturation voltage at capacitor	V_{10}	100	225	350	mV	1.6
Ramp resistance	R_9	3		300	kΩ	1
Sawtooth return time	t_f		80		μs	1
Inhibit pin 6						
switch-over of pin 7						
Outputs disabled	$V_{6\,L}$		3.3	2.5	V	1
Outputs enabled	$V_{6\,H}$	4	3.3		V	1
Signal transition time	t_r	1		5	μs	1
Input current	$I_{6\,H}$		500	800	μA	1
$V_6 = 8$ V						
Input current	$-I_{6\,L}$	80	150	200	μA	1
$V_6 = 1.7$ V						
Deviation of I_{10}	I_{10}	-5		5	%	1
$R_9 =$ const.						
$V_S = 12$ V; $C_{10} = 47$ nF						
Deviation of I_{10}	I_{10}	-20		20	%	1
$R_9 =$ const.						
$V_S = 8$ V to 18 V						
Deviation of the ramp voltage						
between 2 following						
half-waves, $V_S =$ const.	$\Delta V_{10\,max}$		± 1		%	
Long pulse switch-over						
pin 13						
switch-over of S8						
Short pulse at output	$V_{13\,H}$	3.5	2.5		V	1
Long pulse at output	$V_{13\,L}$		2.5	2	V	1
Input current	$I_{13\,H}$			10	μA	1
$V_{13} = 8$ V						
Input current	$-I_{13\,L}$	45	65	100	μA	1
$V_{13} = 1.7$ V						
Outputs pin 2, 3, 4, 7						
Reverse current	I_{CEO}			10	μA	2.6
$V_Q = V_S$						
Saturation voltage	V_{sat}	0.1	0.4	2	V	2.6
$I_Q = 2$ mA						

Characteristics (cont'd)
$8 \leq V_S \leq 18$ V; $-25 \,^{\circ}$C $\leq T_A \leq 85 \,^{\circ}$C; $f = 50$ Hz

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Outputs pin 14, 15 H-output voltage $-I_Q = 250$ mA	$V_{14/15\,H}$	$V_S - 3$	$V_S - 2.5$	$V_S - 1.0$	V	3.6
L-output voltage $I_Q = 2$ mA	$V_{14/15\,L}$	0.3	0.8	2	V	2.6
Pulse width (short pulse) S9 open	t_p	20	30	40	μs	1
Pulse width (short pulse) with C_{12}	t_p	530	620	760	μs/ nF	1
Internal voltage control Reference voltage Parallel connection of 10 ICs possible	V_{REF}	2.8	3.1	3.4	V	1
TC of reference voltage	α_{REF}		2×10^{-4}	5×10^{-4}	1/K	1

Application Hints for External Components

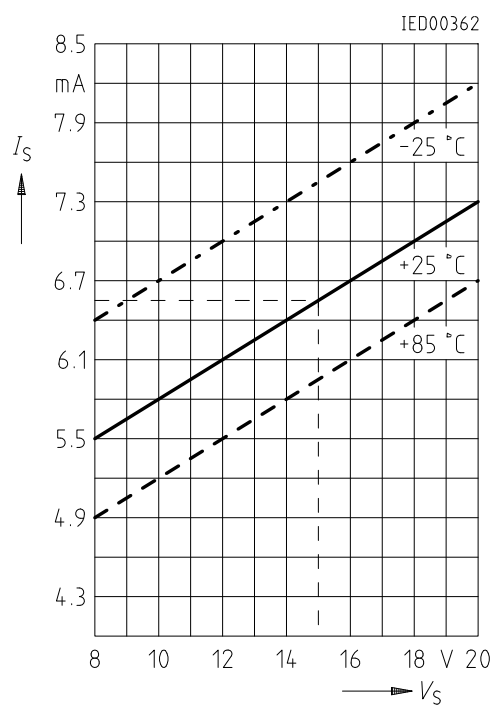|		min	max

Ramp capacitance C_{10} 500 pF   1 μF[1]   The minimum and maximum values of I_{10} are to be observed

Triggering point $t_{Tr} = \dfrac{V_{11} \times R_9 \times C_{10}}{V_{REF} \times K}$ [2]

Charge current $I_{10} = \dfrac{V_{REF} \times K}{R_9}$ [2]

Ramp voltage
$V_{10\,max} = V_S - 2\ \text{V}$ $V_{10} = \dfrac{V_{REF} \times K \times t}{R_9 \times C_{10}}$ [2]
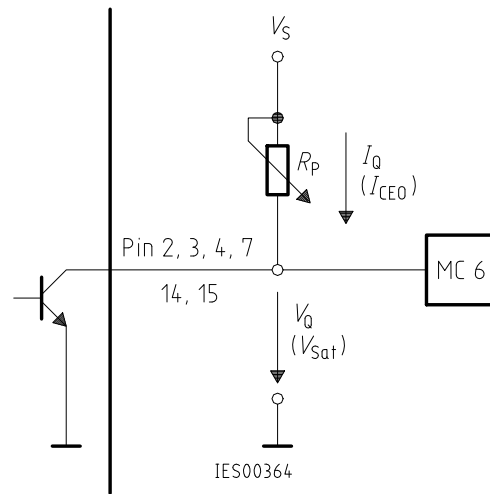
Pulse Extension versus Temperature

$V_S = 15\ \text{V}$
$C_{12} = 1\,\text{nF}$

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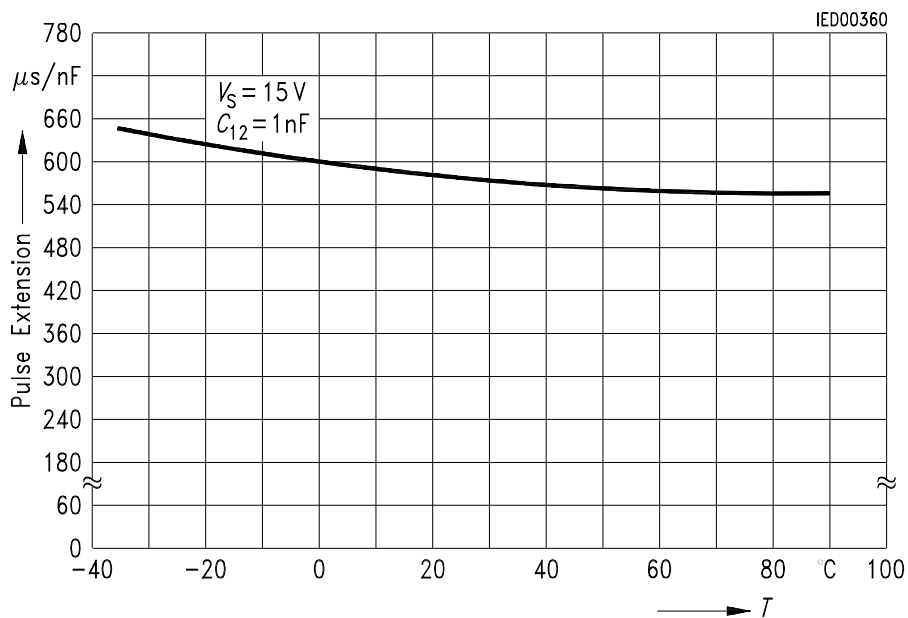
[1] Attention to flyback times
[2] $K = 1.10 \pm 20\ \%$

Output Voltage measured to + V_S
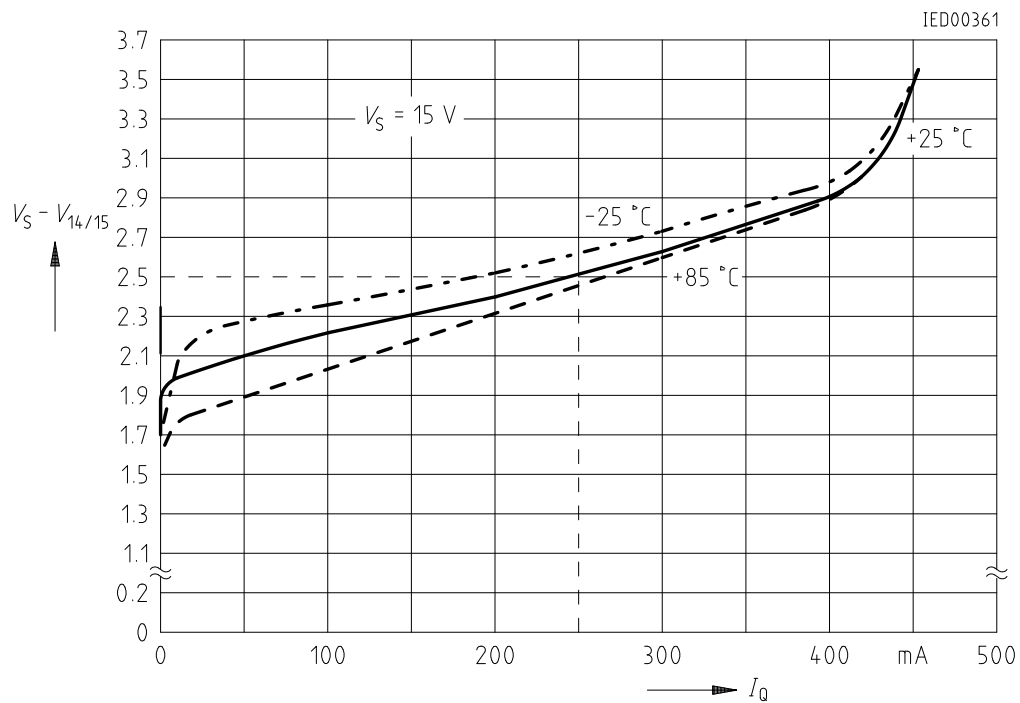
Supply Current versus Supply Voltage

It is necessary for all measurements to adjust the ramp with the aid of C_{10} and R_9 in the way that $3\,V \le V_{\text{ramp max}} \le V_S - 2\,V$ e.g. C_{10} = 47 nF; 18 V: R_9 = 47 kΩ; 8 V: R_9 = 120 kΩ
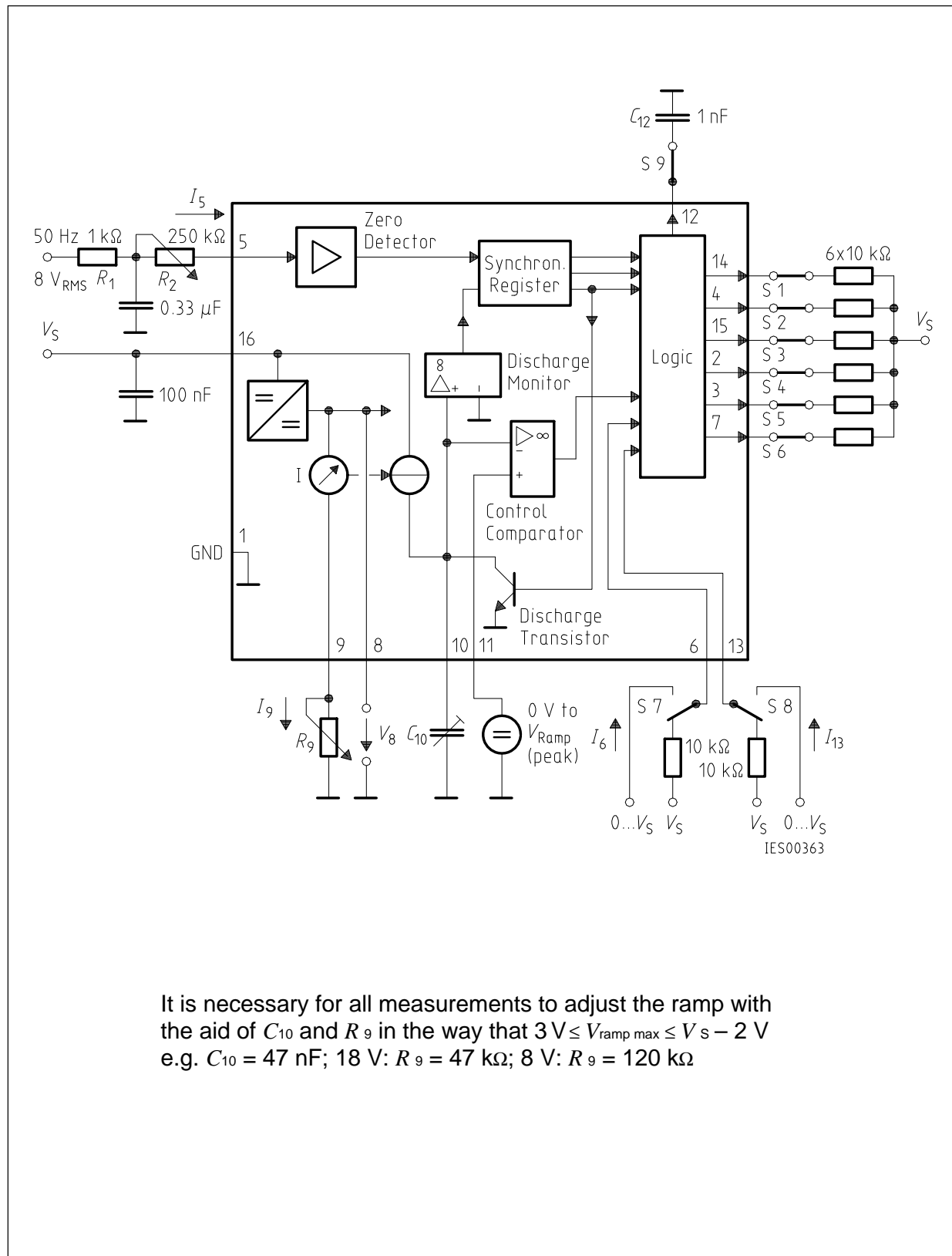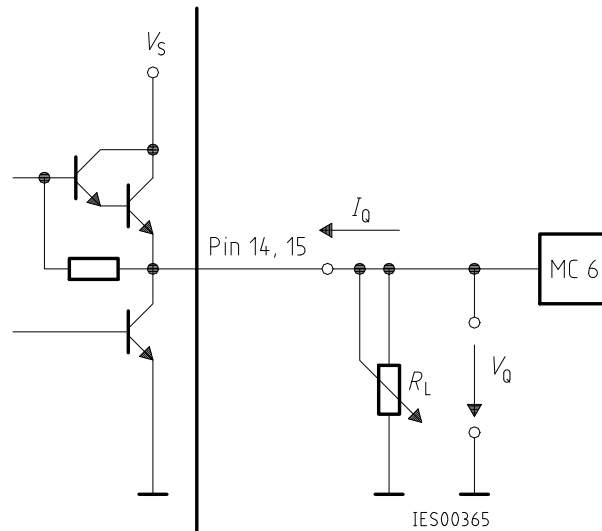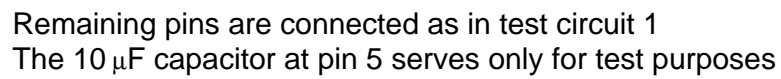
Test Circuit 1

The remaining pins are connected as in test circuit 1

Test Circuit 2

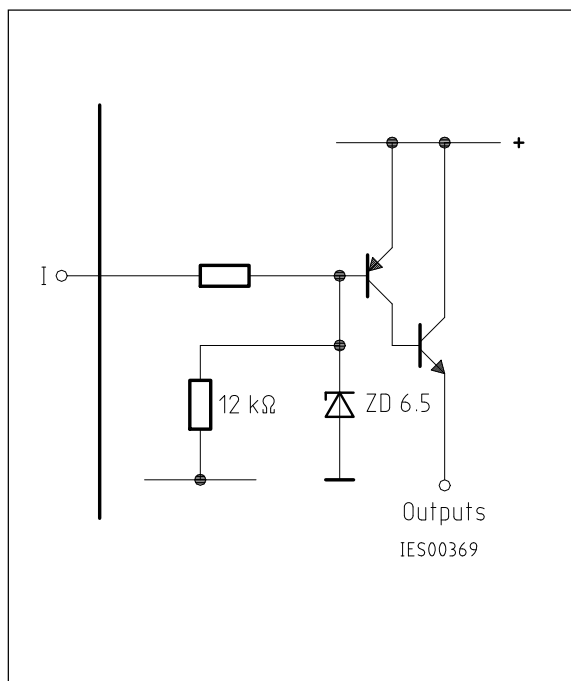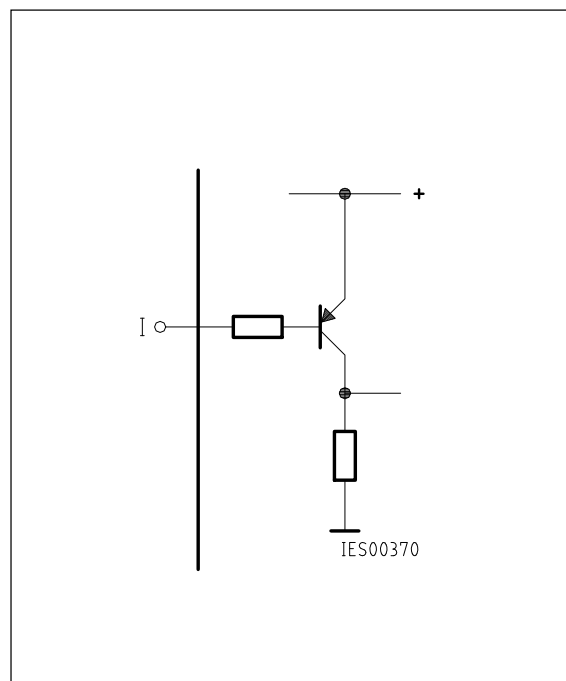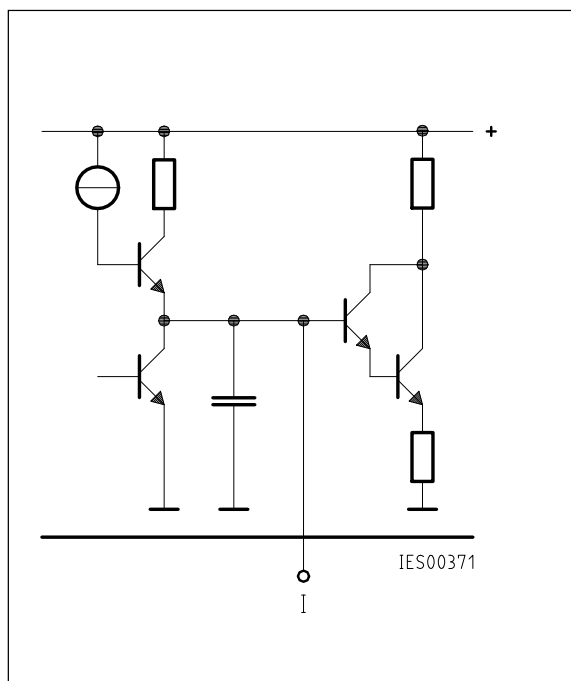The remaining pins are connected as in test circuit 1

Test Circuit 3

Remaining pins are connected as in test circuit 1
The 10 µF capacitor at pin 5 serves only for test purposes

Test Circuit 4

Test Circuit 5

Test Circuit 6

Inhibit 6

Long Pulse 13

Pulse Extension 12
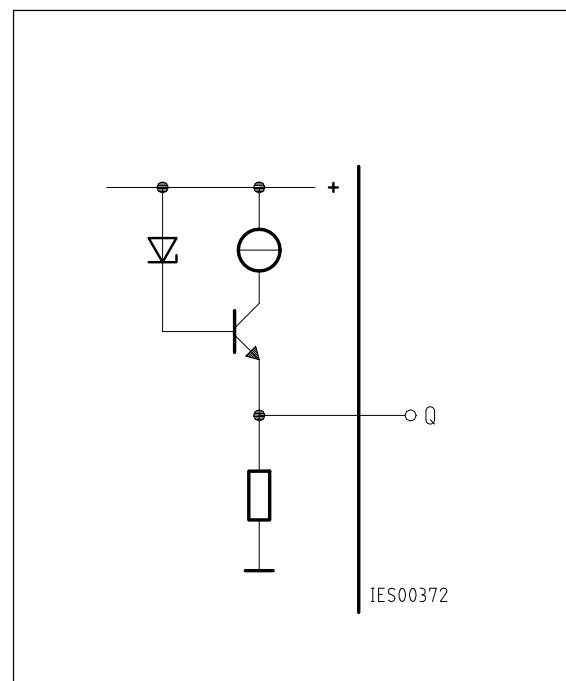
Reference Voltage 8
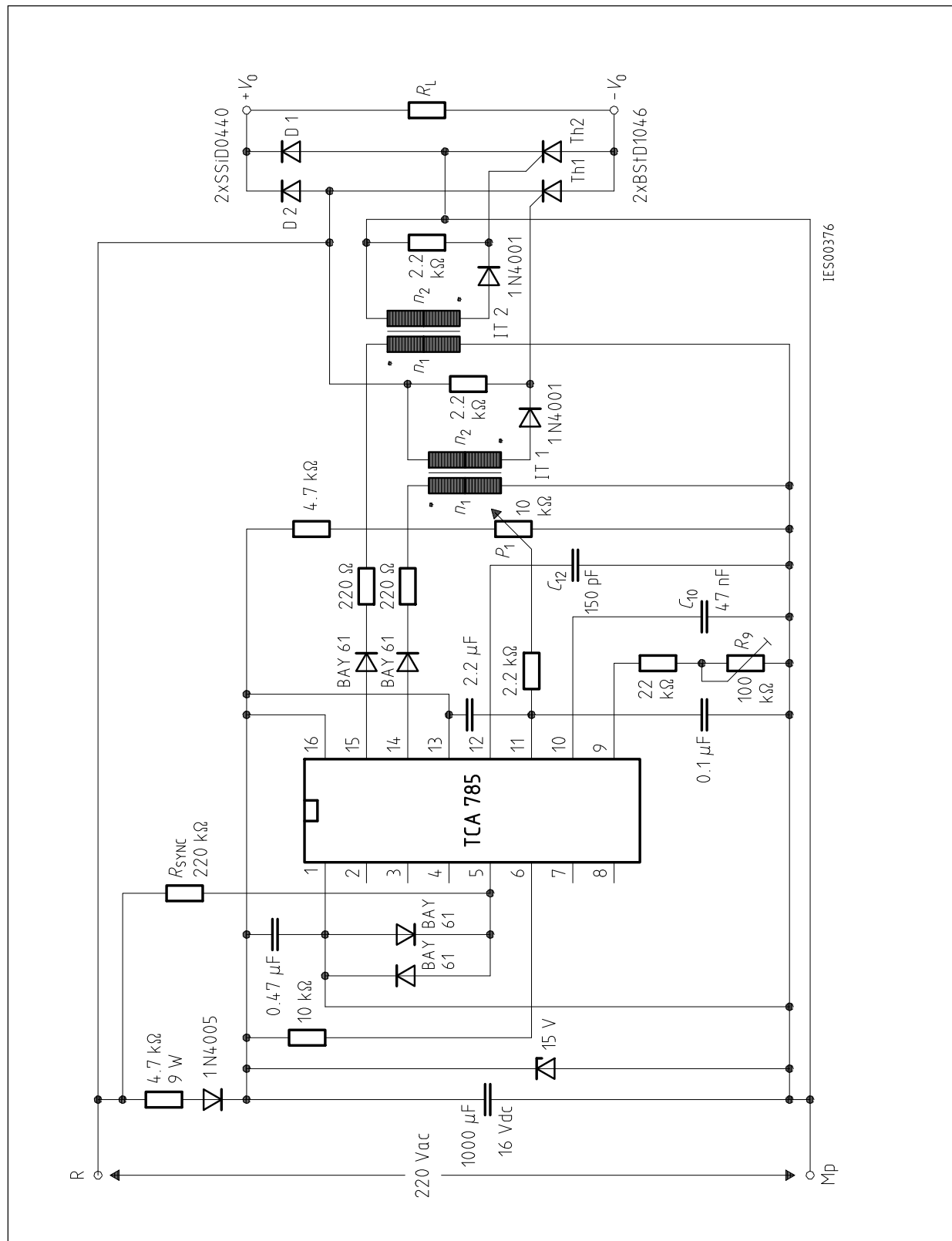
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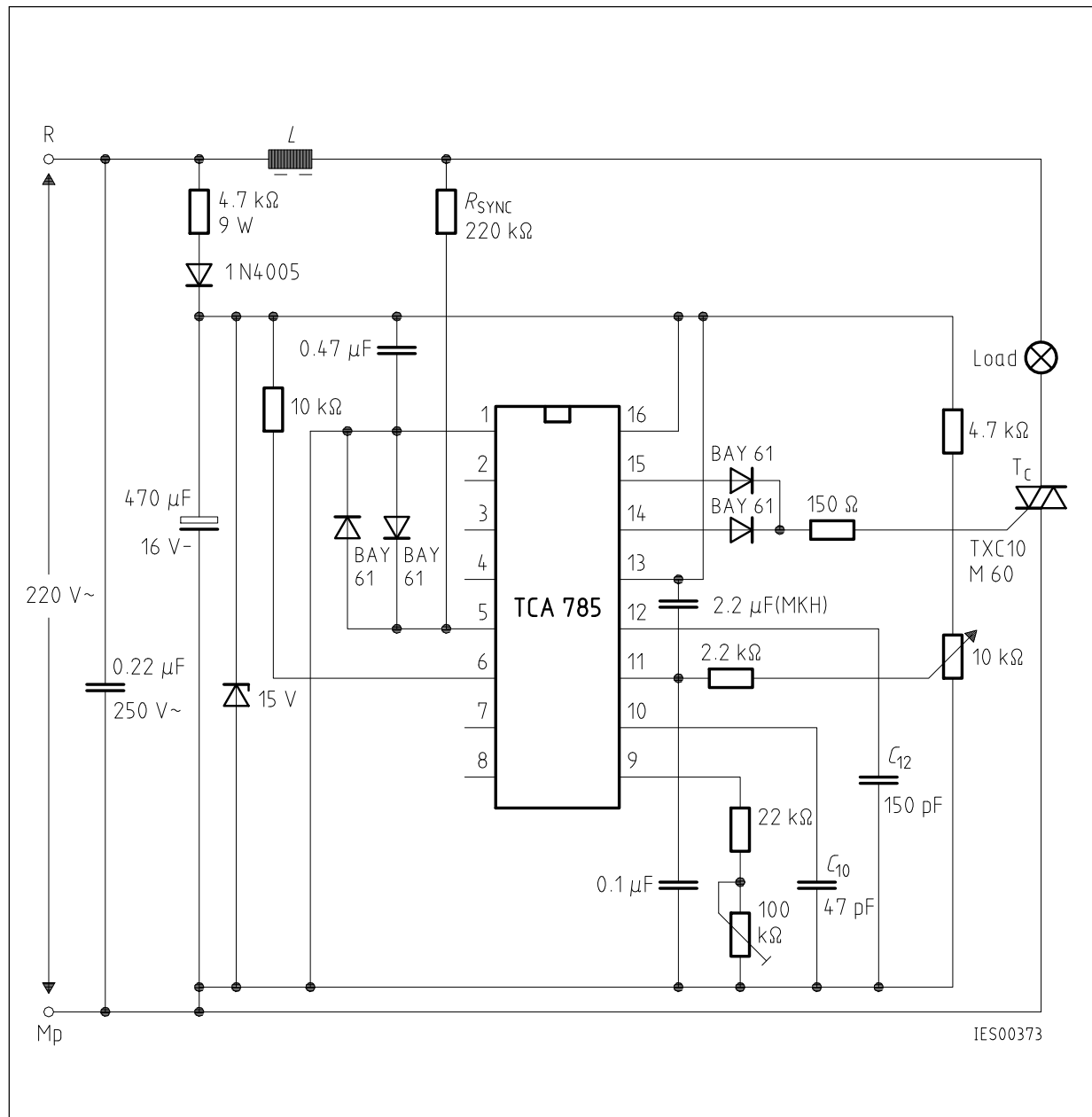
Application Examples
Triac Control for up to 50 mA Gate Trigger Current

A phase control with a directly controlled triac is shown in the figure. The triggering angle of the triac can be adjusted continuously between 0° and 180° with the aid of an external potentiometer. During the positive half-wave of the line voltage, the triac receives a positive gate pulse from the IC output pin 15. During the negative half-wave, it also receives a positive trigger pulse from pin 14. The trigger pulse width is approx. 100 μs.

**Fully Controlled AC Power Controller
Circuit for Two High-Power Thyristors**

Shown is the possibility to trigger two antiparalleled thyristors with one IC TCA 785. The trigger pulse can be shifted continuously within a phase angle between 0° and 180° by means of a potentiometer. During the negative line half-wave the trigger pulse of pin 14 is fed to the relevant thyristor via a trigger pulse transformer. During the positive line half-wave, the gate of the second thyristor is triggered by a trigger pulse transformer at pin 15.

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IES00375

Half-Controlled Single-Phase Bridge Circuit with Trigger Pulse Transformer and Direct Control for Low-Power Thyristors

IES00376

Half-Controlled Single-Phase Bridge Circuit with Two Trigger Pulse Transformers for Low-Power Thyristors