DATA SHEET

TDA3608Q; TDA3608TH
Multiple voltage regulators with switch

Product specification
Supersedes data of 2001 Jun 29

2003 Nov 28

Philips Semiconductors

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FEATURES

General

- Two V_P-state controlled regulators (regulator 1 and regulator 3) and a power switch
- Regulator 2 and reset circuit operate during load dump and thermal shutdown
- Separate control pins for switching regulator 1, regulator 3 and power switch
- Supply voltage range from –18 to +50 V
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1, regulator 3 and power switch are switched off)
- Hold output circuit for regulator 1 (only valid when regulator 3 output voltage >1.3 V)
- Reset and hold outputs (open-collector outputs)
- Adjustable reset delay time
- High ripple rejection
- Backup capacitor connection to supply regulator 2 and reset circuit up to 25 V.

Protections

- Reverse polarity safe (down to –18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short circuited)
- ESD protection on all pins
- Thermal protection
- Load dump protection
- Foldback current limit protection for regulator 1, regulator 2 and regulator 3
- Delayed foldback current limit protection for power switch (at short-circuit); delay time fixed by reset delay capacitor
- All regulator outputs and power switch are DC short-circuited safe to ground and V_P.

GENERAL DESCRIPTION

The TDA3608 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. It contains:

- Two fixed output voltage regulators with a foldback current protection (regulator 1 and regulator 3) and one fixed output voltage regulator (regulator 2) intended to supply a microcontroller, which also operates during load dump and thermal shutdown
- A power switch with protections, operated by an enable input
- Reset and hold outputs that can be used to interface with the microcontroller; the reset output can be used to call up the microcontroller and the hold output indicates that the regulator 1 output voltage is available and within the range
- A supply pin which can withstand load dump pulses and negative supply voltages
- Regulator 2 which is switched on at a backup voltage higher than 6.5 V and switched off when the regulator 2 output drops below 1.9 V
- A provision for the use of a reserve (backup) supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3608Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6
TDA3608TH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-3

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	operating	9.5	14.4	18	V
		regulator 2 on	2.4	14.4	18	V
		reverse polarity; non-operating	–	–	–18	V
		jump start for t ≤ 10 minutes	–	–	30	V
		load dump protection for $t \leq 50$ ms and $t_r \geq 2.5$ ms	–	–	50	V
I_q	quiescent supply current	standby mode; V_P = 12.4 V	–	500	600	µA
T_j	junction temperature		–40	–	+150	°C
Voltage regulators						
V_{REG1}	output voltage of regulator 1	1 mA ≤ I_{REG1} ≤ 600 mA	8.15	8.5	8.85	V
V_{REG2}	output voltage of regulator 2	0.5 mA ≤ I_{REG2} ≤ 150 mA	4.75	5.0	5.25	V
V_{REG3}	output voltage of regulator 3	1 mA ≤ I_{REG3} ≤ 400 mA	4.75	5.0	5.25	V
Power switch						
V_{drop}	dropout voltage	I_{SW} = 1 A	–	0.45	0.7	V
		I_{SW} = 1.8 A	–	1.0	1.8	V
I_M	peak current		2	–	–	A

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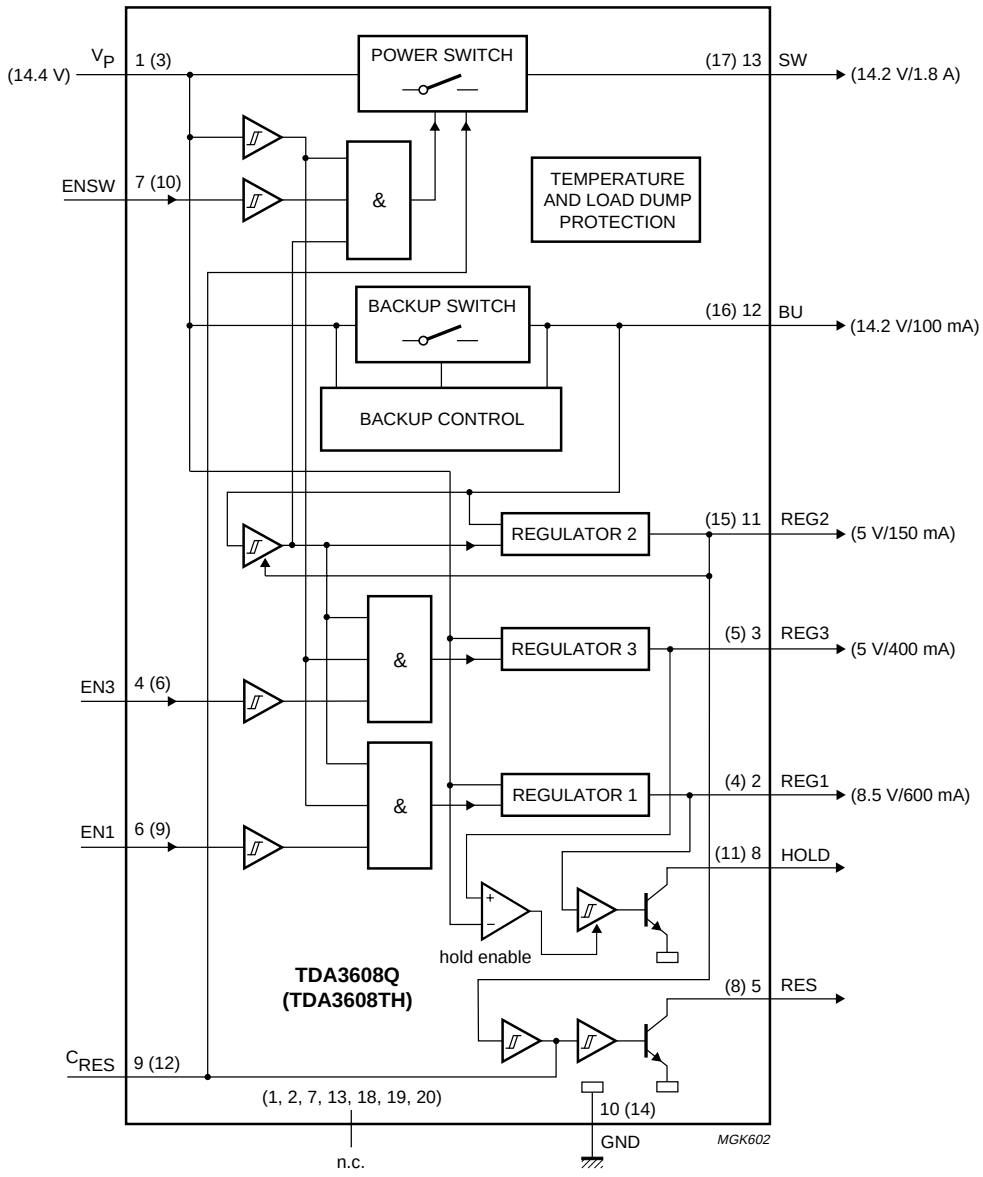
BLOCK DIAGRAM



Numbers in parenthesis refer to type number TDA3608TH.

Fig.1 Block diagram.

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PINNING

SYMBOL	PIN		DESCRIPTION
	TDA3608Q	TDA3608TH	
V_P	1	3	supply voltage
REG1	2	4	regulator 1 output
REG3	3	5	regulator 3 output
EN3	4	6	regulator 3 enable input
RES	5	8	reset output
EN1	6	9	regulator 1 enable input
ENSW	7	10	power switch enable input
HOLD	8	11	hold output
C_{RES}	9	12	reset delay capacitor connection
GND	10	14	ground
REG2	11	15	regulator 2 output
BU	12	16	backup capacitor connection
SW	13	17	power switch output
n.c.	–	1, 2, 7, 13, 18,19 and 20	not connected

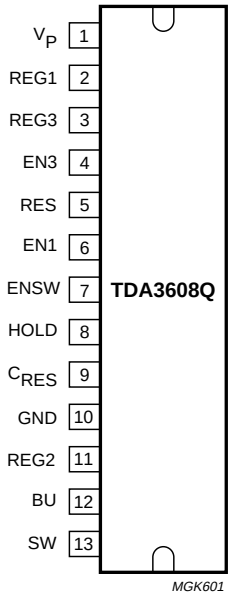

Fig.2 Pin configuration of TDA3608Q.

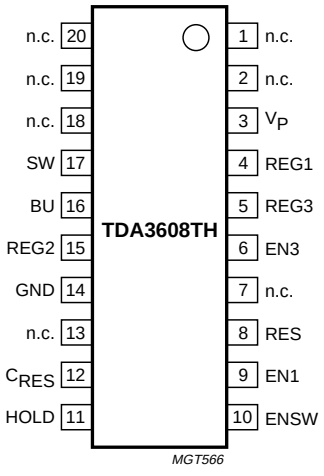

Fig.3 Pin configuration of TDA3608TH.

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FUNCTIONAL DESCRIPTION

The TDA3608 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of low-voltage operation of the car radio, low-voltage drop regulators are used in the TDA3608.

Backup supply

The charge of the backup capacitor connected to pin BU can be used to supply regulator 2 for a short period when the supply voltage V_P drops to 0 V (the time depends on the value of the capacitor).

Regulator 1

When the output voltage of regulator 2 and the supply voltage (V_P > 4.5 V) are both available, regulator 1 can be operated by means of enable pin EN1 (see Fig.4).

Regulator 2

Regulator 2 switches on (see Fig.5) when the backup voltage exceeds 6.5 V for the first time and switches off when the output voltage of regulator 2 drops below 1.9 V (this is far below an engine start).

Regulator 3

When the output voltage of regulator 2 and the supply voltage (V_P > 4.5 V) are both available, regulator 3 can be operated by means of enable pin EN3 (see Fig.4).

Reset

When regulator 2 is switched on and the output voltage of this regulator is within its voltage range, the reset output (see Fig.5) will be enabled (pin RES goes HIGH through an external pull-up resistor) to generate a reset to the microcontroller.

The reset cycles can be extended by means of an external capacitor connected to pin C_{RES}. This start-up feature is included to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

Hold

Regulator 1 has an open-collector hold output (see Fig.4) indicating that the output voltage is settled at 8.5 V. Pin HOLD is held HIGH by an external pull-up resistor. When the supply voltage V_P drops or during high load, the output voltage drops out-of-regulation and pin HOLD goes LOW.

The hold output is only activated when V_{REG3} > 1.3 V. When pin HOLD is connected via a pull-up resistor to the output of regulator 3 spikes will be minimized to 1.3 V (maximum value) because the hold output is only disabled when V_{REG3} < 1.3 V.

Pin HOLD will be forced LOW when the load dump protection is activated and also in the standby mode.

Power switch

The power switch can be controlled by means of enable pin ENSW (see Fig.6).

Protections

All output pins are fully protected.

The regulators are protected against load dump (regulator 1 and regulator 3 switch off at V_P > 18 V) and short-circuit (foldback current protection).

The power switch contains a foldback current protection, but this protection is delayed at a short-circuit condition by the reset delay capacitor. During this time the output current is limited to at least 2 A (peak value) and 1.8 A (continuous value) at $V_P \leq 18$ V. During the foldback mode the current is limited to 0.5 A (typical value).

The timing diagram is shown in Fig.7.

The foldback protection is activated when V_{SW} < 4 V. When regulator 2 is out-of-regulation and generates a reset, the power switch is in the foldback mode immediately when V_{SW} < 4 V.

In the standby mode the voltage on the reset delay capacitor is about 4 V and the voltage on the power switch output is V_P – 0.45 V (typical value) at I_{SW} = 1 A. During an overload condition or short-circuit the reset delay capacitor will be charged to a higher voltage. The power switch is in the high current mode while the capacitor is charged, after this the switch is in the foldback mode (V_{SW} < 4 V). While the reset delay capacitor is charged the power switch output can reach its correct output voltage. Now the voltage on the reset delay capacitor is decreased rapidly to 4 V. The reset output voltage is not influenced by this change of voltages. The time of the high current mode depends on the value of the reset delay capacitor.

At V_P > 18 V the power switch is clamped at maximum 17.2 V (to avoid that external connected circuitry is being damaged by an overvoltage) and the power switch will switch off at load dump.

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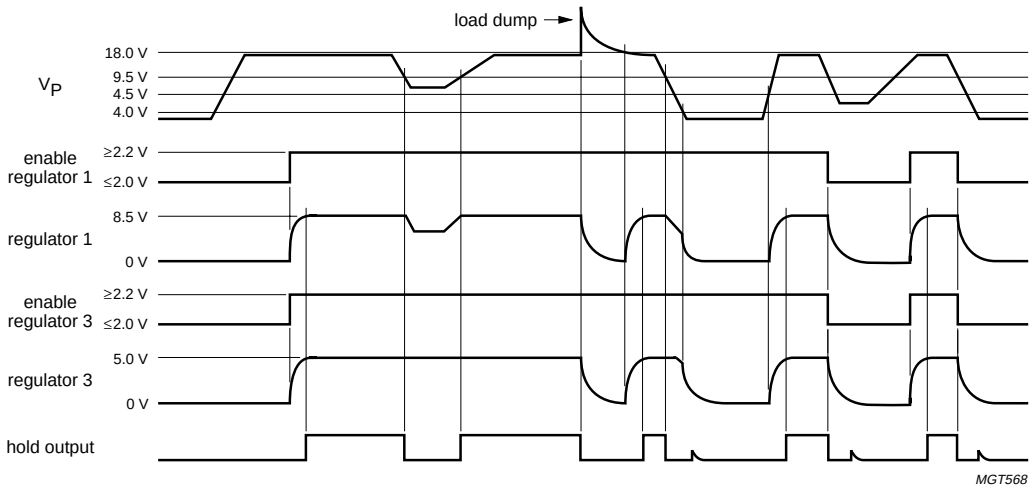

Fig.4 Timing diagram of regulator 1, regulator 3 and hold output.

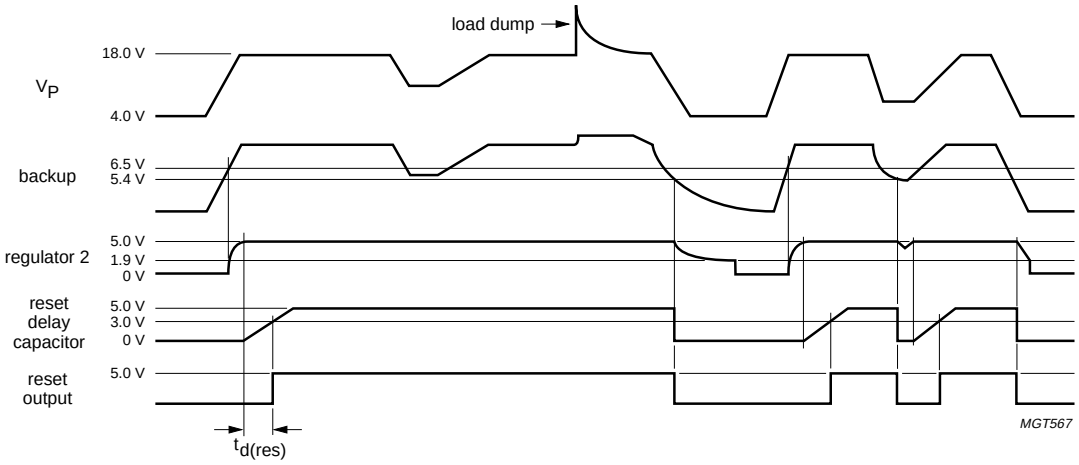

Fig.5 Timing diagram of backup, regulator 2 and reset output.

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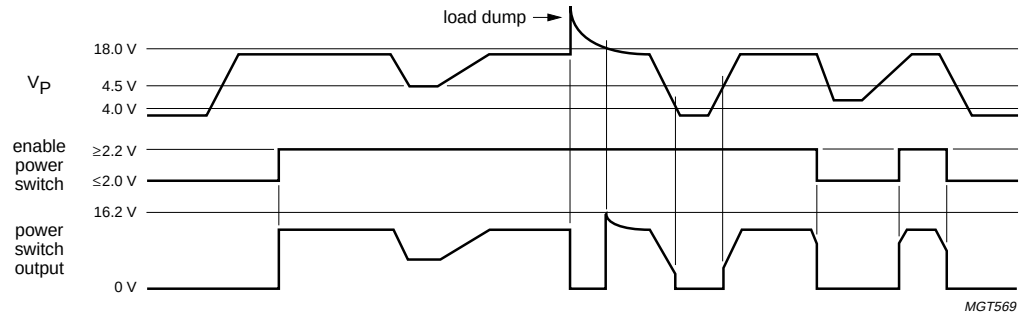

Fig.6 Timing diagram of power switch output.

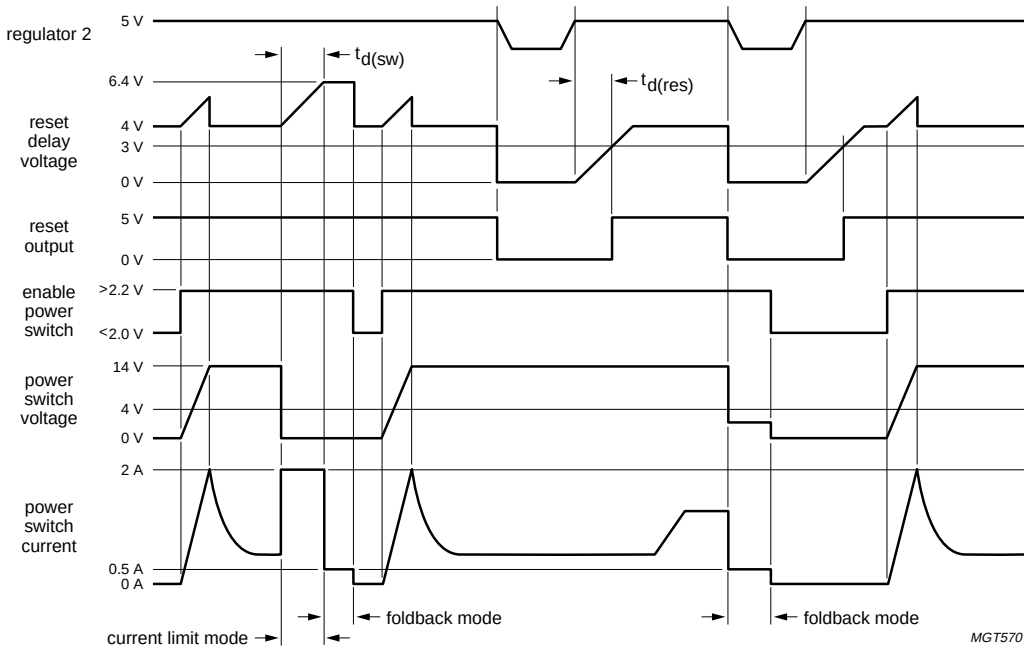

Fig.7 Timing diagram of current protection of power switch.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		reverse polarity; non-operating	–	–18	V
		jump start for t ≤ 10 minutes	–	30	V
		load dump protection for t ≤ 50 ms and $t_r \geq 2.5$ ms	–	50	V
P_{tot}	total power dissipation		–	62	W
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
T_j	junction temperature	operating	–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case			
	TDA3608Q		2	K/W
	TDA3608TH		3.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	50	K/W

CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	operating	9.5	14.4	18	V
		regulator 2 on; note 1	2.4	14.4	18	V
		jump start for t ≤ 10 minutes	–	–	30	V
		load dump protection for t ≤ 50 ms and $t_r \geq 2.5$ ms	–	–	50	V
I_q	quiescent supply current	standby mode; note 2				
		V_P = 12.4 V	–	500	600	µA
		V_P = 14.4 V	–	520	–	µA
Schmitt trigger supply voltage for regulator 1, regulator 3 and power switch						
V_{thr}	rising threshold voltage		4.0	4.5	5.0	V
V_{thf}	falling threshold voltage		3.5	4.0	4.5	V
V_{hys}	hysteresis voltage		–	0.5	–	V
Schmitt trigger supply voltage for regulator 2						
V_{thr}	rising threshold voltage		6.0	6.5	7.1	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{thf}	falling threshold voltage		1.7	1.9	2.2	V
V_{hys}	hysteresis voltage		–	4.6	–	V
Schmitt trigger voltage for enable input (regulator 1, regulator 3 and power switch)						
V_{thr}	rising threshold voltage		1.7	2.2	2.7	V
V_{thf}	falling threshold voltage		1.5	2.0	2.5	V
V_{hys}	hysteresis voltage	$I_{REG} = I_{SW} = 1$ mA	0.1	0.2	0.5	V
I_{LI}	input leakage current	$V_{EN} = 5$ V	1	5	10	µA
Schmitt trigger voltage for reset						
V_{thr}	rising threshold voltage of regulator 2	V_P rising; $I_{REG2} = 50$ mA; note 3	–	$V_{REG2} - 0.15$	$V_{REG2} - 0.075$	V
V_{thf}	falling threshold voltage of regulator 2	V_P falling; $I_{REG2} = 50$ mA; note 3	4.3	$V_{REG2} - 0.35$	–	V
V_{hys}	hysteresis voltage		0.1	0.2	0.3	V
Schmitt trigger voltage for hold						
V_{thr}	rising threshold voltage of regulator 1	V_P rising; note 3	–	$V_{REG1} - 0.15$	$V_{REG1} - 0.075$	V
V_{thf}	falling threshold voltage of regulator 1	V_P falling; note 3	7.7	$V_{REG1} - 0.35$	–	V
V_{hys}	hysteresis voltage		0.1	0.2	0.3	V
Reset and hold output						
I_{sinkL}	LOW-level sink current	$V_o \leq 0.8$ V	2	–	–	mA
I_{LO}	output leakage current	$V_o = 5$ V; $V_P = 14.4$ V	–	–	2	µA
t_r	rise time	note 4	–	7	50	µs
t_f	fall time	note 4	–	1	50	µs
Reset delay capacitor circuit						
I_{ch}	charge current		2	3	4	µA
I_{dch}	discharge current		500	800	–	µA
$V_{thr(res)}$	rising threshold voltage for delayed reset pulse		2.8	3.0	3.2	V
$V_{thr(sw)}$	rising threshold voltage for delayed power switch foldback mode	note 5	–	6.4	–	V
$t_{d(res)}$	reset delay time	C7 = 47 nF; note 6	32	47	70	ms

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Regulator 1; I_{REG1} = 5 mA; unless otherwise specified						
$V_{REG1(off)}$	output voltage with regulator off		–	1	400	mV
V_{REG1}	output voltage	1 mA ≤ I_{REG1} ≤ 600 mA	8.15	8.5	8.85	V
		9.5 V ≤ V_P ≤ 18 V	8.15	8.5	8.85	V
ΔV_{line}	line regulation	9.5 V ≤ V_P ≤ 18 V	–	2	75	mV
ΔV_{load}	load regulation	1 mA ≤ I_{REG1} ≤ 600 mA	–	20	50	mV
I_q	quiescent current	I_{REG1} = 600 mA	–	25	60	mA
SVRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)	60	70	–	dB
V_{drop}	dropout voltage	V_P = 8.5 V; I_{REG1} = 550 mA; note 7	–	0.4	0.7	V
I_m	current limit	V_{REG1} > 7.5 V; see Fig.8; note 8	0.65	1.2	–	A
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω; see Fig.8; note 9	250	800	–	mA
Regulator 2; I_{REG2} = 5 mA; unless otherwise specified						
V_{REG2}	output voltage	0.5 mA ≤ I_{REG2} ≤ 150 mA	4.75	5.0	5.25	V
		I_{REG2} = 300 mA; note 10	4.75	5.0	5.25	V
		7 V ≤ V_P ≤ 18 V	4.75	5.0	5.25	V
		18 V ≤ V_P ≤ 50 V; I_{REG2} ≤ 150 mA	4.75	5.0	5.25	V
ΔV_{line}	line regulation	6 V ≤ V_P ≤ 18 V	–	2	50	mV
		18 V ≤ V_P ≤ 50 V	–	15	75	mV
ΔV_{load}	load regulation	1 mA ≤ I_{REG2} ≤ 150 mA	–	20	50	mV
		1 mA ≤ I_{REG2} ≤ 300 mA	–	–	100	mV
SVRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)	60	70	–	dB
V_{drop}	dropout voltage	normal supply; note 7				
		V_P = 4.75 V; I_{REG2} = 100 mA	–	0.4	0.6	V
		V_P = 5.75 V; I_{REG2} = 200 mA	–	0.8	1.2	V
		backup supply; note 11				
		V_{BU} = 4.75 V; I_{REG2} = 100 mA	–	0.2	0.5	V
		V_{BU} = 5.75 V; I_{REG2} = 200 mA	–	0.8	1.0	V
I_m	current limit	V_{REG2} > 4.5 V; see Fig.9; note 8	0.32	0.37	–	A
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω; see Fig.9; note 9	20	100	–	mA
Regulator 3; I_{REG3} = 5 mA; unless otherwise specified						
$V_{REG3(off)}$	output voltage with regulator off		–	1	400	mV
V_{REG3}	output voltage	1 mA ≤ I_{REG3} ≤ 400 mA	4.75	5.0	5.25	V
		7 V ≤ V_P ≤ 18 V	4.75	5.0	5.25	V
ΔV_{line}	line regulation	7 V ≤ V_P ≤ 18 V	–	2	50	mV
ΔV_{load}	load regulation	1 mA ≤ I_{REG3} ≤ 400 mA	–	20	50	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_q	quiescent current	I_{REG3} = 400 mA	–	15	40	mA
SVRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)	60	70	–	dB
V_{drop}	dropout voltage	V_P = 5.75 V; I_{REG3} = 400 mA; note 7	–	1	1.5	V
I_m	current limit	V_{REG3} > 4.5 V; see Fig.10; note 8	0.45	0.70	–	A
I_{sc}	short-circuit current	$R_L \leq 0.5\ \Omega$; see Fig.10; note 9	100	400	–	mA
Power switch						
V_{drop}	dropout voltage	I_{SW} = 1 A; note 12	–	0.45	0.7	V
		I_{SW} = 1.8 A; note 12	–	1.0	1.8	V
V_{cl}	clamping voltage	$V_P \geq 18$ V	15	16.2	17.2	V
V_{fb}	flyback voltage behaviour	I_{SW} = –100 mA	–	V_P + 3	22	V
I_{dc}	continuous current	V_P = 16 V; V_{SW} = 13.5 V	1.8	2.0	–	A
I_M	peak current	V_P = 17 V; see Fig.11; note 13	2	–	–	A
I_{sc}	short-circuit current	V_P = 14.4 V; V_{SW} < 3.5 V; see Fig.11; note 14	–	0.5	–	A
Backup switch						
I_{dc}	continuous current		0.3	0.35	–	A
V_{cl}	clamping voltage	$V_P \geq 16.7$ V	–	–	16	V
I_r	reverse current	V_P = 0; V_{BU} = 12.4 V; note 15	–	–	900	mA

Notes

1. The minimum value is the minimum operating voltage, only if V_P has exceeded 6.5 V.
2. The quiescent current is measured in the standby mode. Therefore, the enable inputs of regulator 1, regulator 3 and the power switch are grounded and $R_{L(REG2)} = \infty$.
3. The voltage of the regulator drops as a result of a V_P drop.
4. The rise and fall time is measured with a 10 kΩ pull-up resistor and C_L = 50 pF.
5. This is the threshold voltage for the delay time of the power switch. The voltage on the reset delay capacitor increases only at low output voltage of the power switch (for example at short circuit). When the voltage on this capacitor exceeds this threshold voltage, the power switch is set to the foldback mode. The power switch is also protected by the temperature protection.
6. Delay time calculation:

   a) Reset pulse delay: $t_{d(res)} = \frac{C}{I_{ch}} \times V_{C(th1)} = C \times 1000 \times 10^3$ [sec] The delay time is 47 ms for C = 47 nF.

   b) Power switch delay: $t_{d(sw)} = \frac{C}{I_{ch}} \times V_{C(th2)} = C \times 500 \times 10^3$ [sec] The delay time is 23.5 ms for C = 47 nF.
7. The dropout voltage of regulator 1, regulator 2 and regulator 3 is measured between pin V_P and pins REG1, REG2 or REG3 respectively.
8. During current limit, current I_m is held constant.
9. The foldback current protection limits the dissipated power at short-circuit.

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10. The peak current of 300 mA can only be applied for short periods (t < 100 ms).
11. The dropout voltage is measured between pins BU and REG2.
12. The dropout voltage of the power switch is measured between pins V_P and SW.
13. The maximum output current of the power switch is limited to 1.8 A when V_P > 18 V.
14. During short-circuit, current I_{sc} of the power switch is held constant to a lower value than the continuous current after a delay of at least 10 ms. Furthermore, a foldback function is activated after the delay. When V_{SW} < 3.5 V, the short-circuit current is reduced to 0.5 A (typical value). The short-circuit protection of the power switch functions best when C1 = 220 μF and C2 = 10 μF.
15. The reverse current of the backup switch is the current which is flowing out of pin V_P at V_P = 0 V.

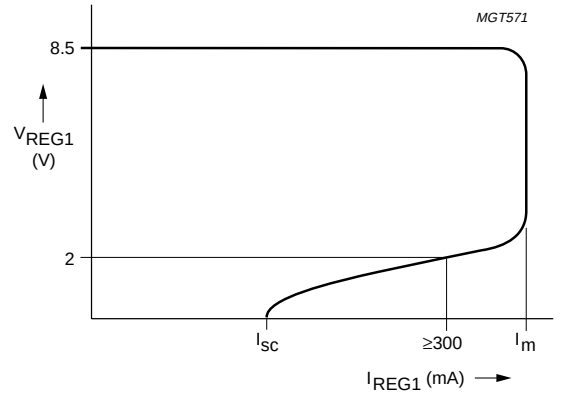


Fig.8 Foldback current protection of regulator 1.

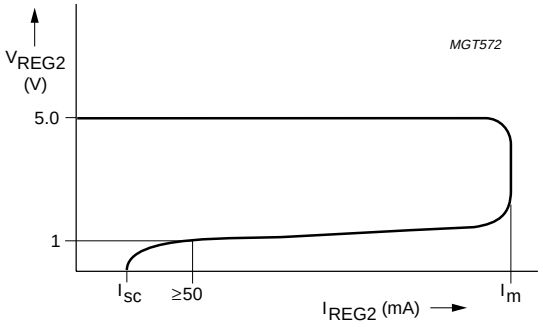


Fig.9 Foldback current protection of regulator 2.

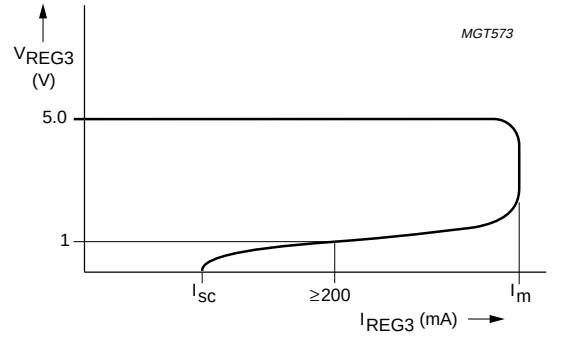
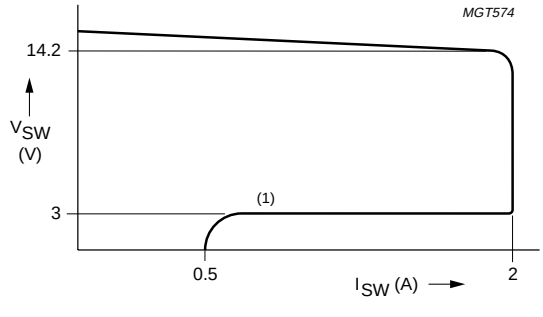


Fig.10 Foldback current protection of regulator 3.



(1) Delayed; time depends on value of capacitor C7.

Fig.11 Current protection of power switch.

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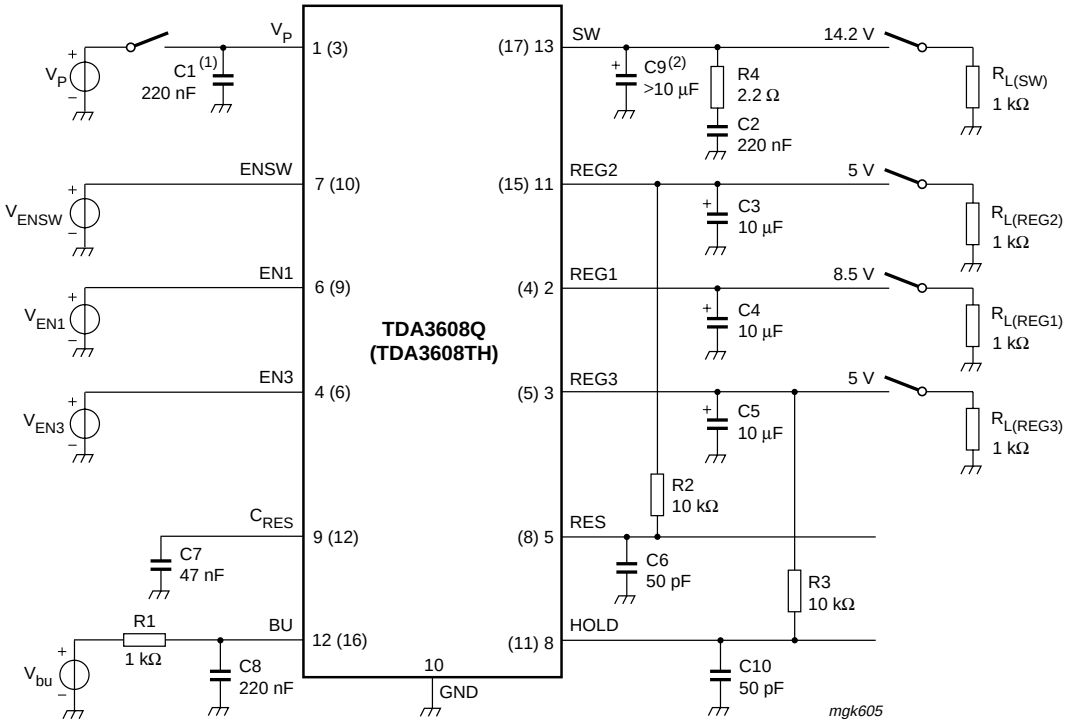
TEST AND APPLICATION INFORMATION

Test information



Numbers in parenthesis refer to type number TDA3608TH.

(1) Capacitor not required for stability.

(2) Value depends on application.

Fig.12 Test circuit.

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Application information

NOISE

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (the output noise of the regulators is translated into a current noise by means of the output capacitors). Table 1 shows the noise figure with the corresponding output capacitor C_o for each regulator. The noise is minimal when a high frequency capacitor of 220 nF in parallel with an electrolytic capacitor of 100 μF is connected directly to pins V_P and GND.

Table 1 Noise figure; note 1

REGULATOR	NOISE FIGURE (μV)		
	C_o = 10 μF	C_o = 47 μF	C_o = 100 μF
1	225	150	135
2	225	150	135
3	255	200	180

Note

1. Measured at a bandwidth of 200 kHz.

STABILITY

The regulators are made stable with the externally connected output capacitors. The output capacitors can be selected using the graphs of Figs 13 and 14. When an electrolytic capacitor is used, the temperature behaviour of this output capacitor can cause oscillations at low temperature. The next two examples show how an output capacitor value is selected.

Example 1

The regulator 1 is made stable with an electrolytic output capacitor of 220 μF with ESR = 0.15 Ω. At T_{amb} = –30 °C the capacitor value is decreased to 73 μF and the ESR is increased to 1.1 Ω. The regulator remains stable at T_{amb} = –30 °C (see Fig.13).

Example 2

The regulator 2 is made stable with an electrolytic capacitor of 10 μF with ESR = 3 Ω. At T_{amb} = –30 °C the capacitor value is decreased to 3 μF and the ESR is increased to 23.1 Ω. The regulator will be instable at T_{amb} = –30 °C (see Fig.14).

Solution

Use a tantalum capacitor of 10 μF or a larger electrolytic capacitor. The use of tantalum capacitors is recommended to avoid problems with stability at low temperatures.

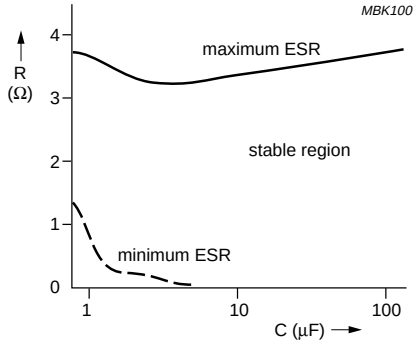

Fig.13 Curves for selecting value of output capacitor for regulator 1 and regulator 3.

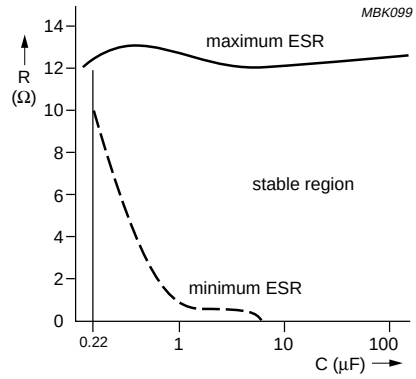

Fig.14 Curves for selecting value of output capacitor for regulator 2.

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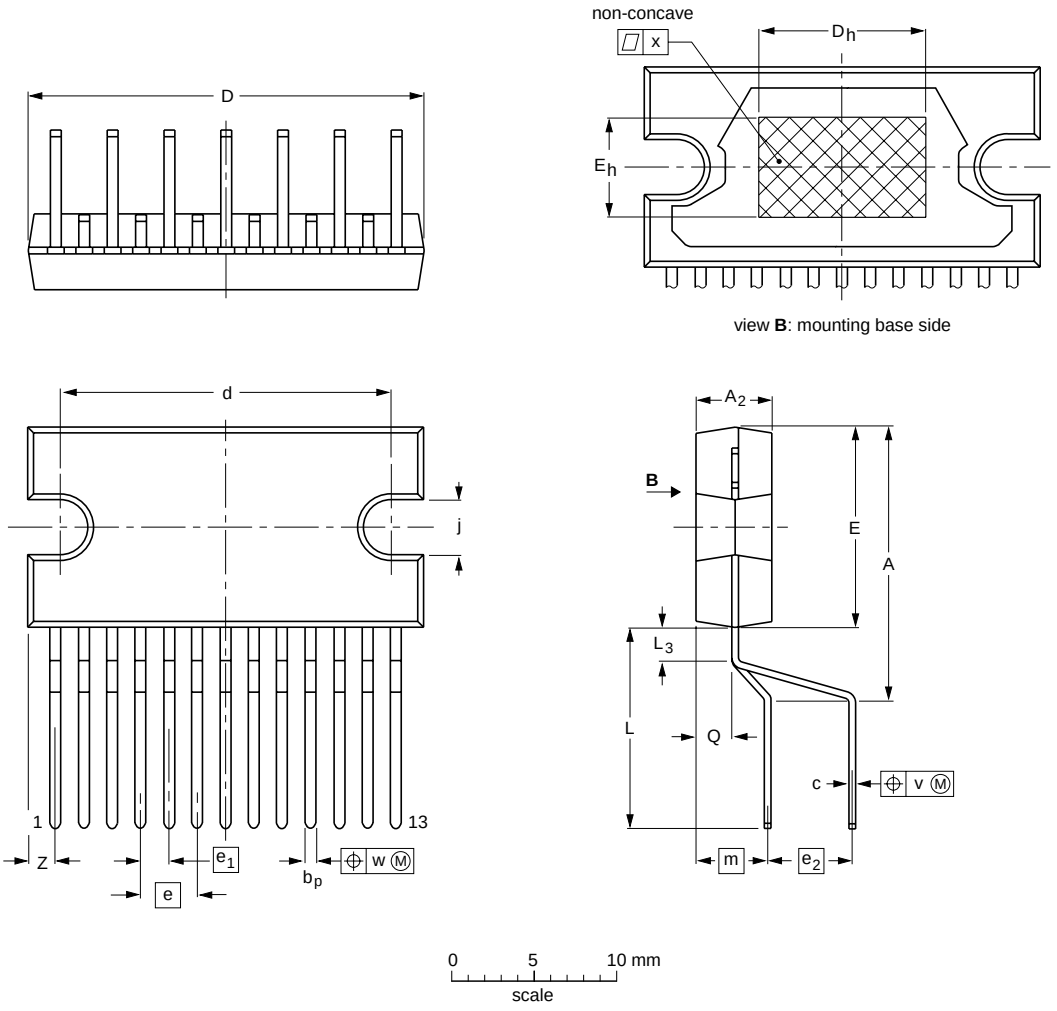
PACKAGE OUTLINES

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) **SOT141-6**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT141-6						~~99-12-17~~ 03-03-12

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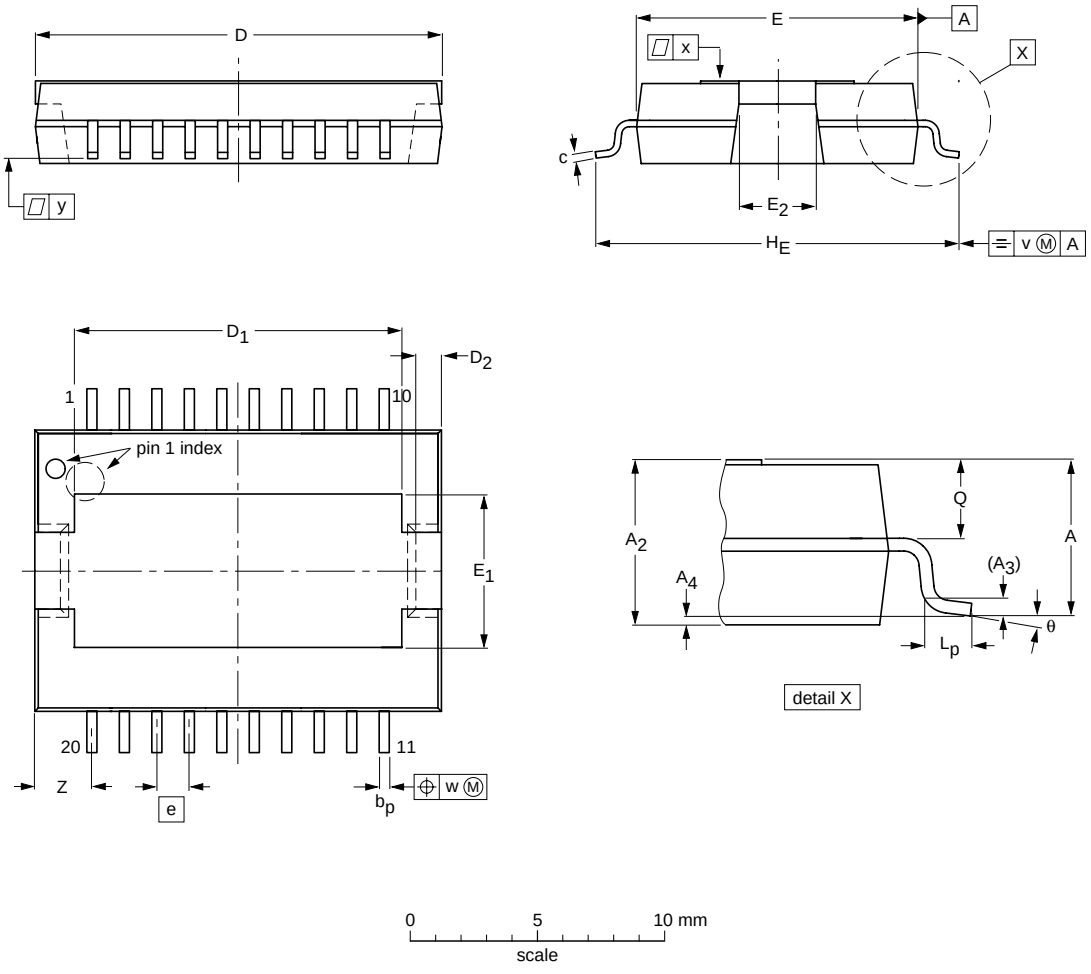
HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height **SOT418-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 −0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT418-3						~~02-02-12~~ 03-07-23

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SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA, HTSSON..T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

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During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE[1]	SOLDERING METHOD		
		WAVE	REFLOW[2]	DIPPING
Through-hole mount	CPGA, HCPGA	suitable	–	suitable
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable[3]	–	–
Through-hole-surface mount	PMFP[4]	not suitable	not suitable	–
Surface mount	BGA, HTSSON..T[5], LBGA, LFBGA, SQFP, SSOP-T[5], TFBGA, USON, VFBGA	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[6]	suitable	–
	PLCC[7], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[7][8]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended[9]	suitable	–
	CWQCCN..L[11], PMFP[10], WQCCN32L[11]	not suitable	not suitable	–

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
4. Hot bar soldering or manual soldering is suitable for PMFP packages.
5. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
6. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
7. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
8. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
9. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
10. Hot bar or manual soldering is suitable for PMFP packages.
11. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands R32/04/pp22 Date of release: 2003 Nov 28 Document order number: 9397 750 12339

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