DATA SHEET

I²C BUS

TDA8444; TDA8444T; TDA8444AT

Octuple 6-bit DACs with I²C-bus

Product specification
Supersedes data of March 1991
File under Integrated Circuits, IC01

1999 Apr 29

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Octuple 6-bit DACs with I^{2}C-bus

TDA8444; TDA8444T; TDA8444AT

FEATURES

- Eight DACs with 6-bit resolution
- Adjustable common output swing
- Push-pull outputs
- Outputs short-circuit protected
- Three programmable slave address bits
- Large supply voltage range
- Low temperature coefficient.

GENERAL DESCRIPTION

The interface circuit is a bipolar IC in a DIP16, SO16, or SO20 package made in an I2L-compatible 18 V process.

The TDA8444 contains eight programmable 6-bit DAC outputs, an I^{2}C-bus slave receiver with three (two for SO16) programmable address bits and one input (V_{MAX}) to set the maximum output voltage. Each DAC can be programmed separately by a 6-bit word to 64 values, but V_{MAX} determines the maximum output voltage for all DACs. The resolution will be approximately $\frac{1}{64}V_{MAX}$.

At power-on all DACs are set to their lowest value.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	12	13.2	V
I_{CC}	supply current	$V_{CC} = 12$ V	–	14	–	mA
P	power dissipation		–	170	–	mW
V_{VMAX}	input effective voltage		1	–	$V_{CC} - 2.0$	V
$V_{o(DACn)}$	DAC output voltage	$V_{MAX} = V_{CC}$	0.1	–	$V_{CC} - 0.5$	V
$V_{o(DACn)(max)}$	maximum DAC output voltage	$1 < V_{MAX} < V_{CC} - 2.0$	–	$V_{MAX} + 0.3$	–	V
$I_{source(min)}$	minimum DAC source current	data = 1FH	2	–	–	mA
$I_{sink(min)}$	minimum DAC sink current	data = 1FH	2	–	–	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8444	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA8444T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
TDA8444AT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

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                                                                                    TDA8444AT

BLOCK DIAGRAM

Fig.1 Block diagram.
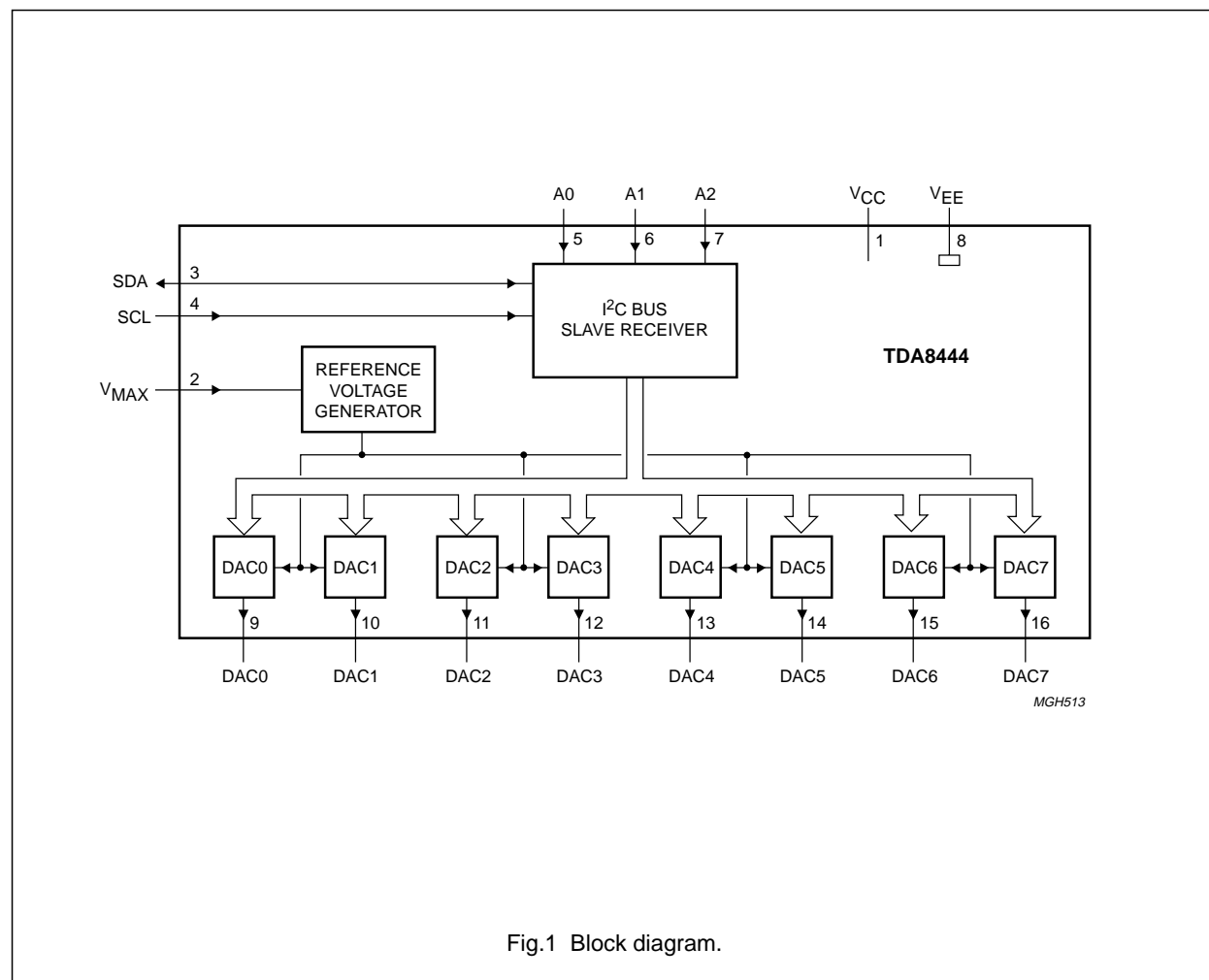
Octuple 6-bit DACs with I^{2}C-bus

TDA8444; TDA8444T;
TDA8444AT

PINNING

| SYMBOL	PIN			DESCRIPTION
	TDA8444 (DIP16)	TDA8444T (SO16)	TDA8444AT (SO20)	
V$_{CC}$	1	1	1	supply voltage
V$_{MAX}$	2	2	2	control input for DAC maximum output voltage
SDA	3	3	3	I^{2}C-bus serial data input/output
SCL	4	4	4	I^{2}C-bus serial clock
A0	5	6	7	programmable address bit 0 for I^{2}C-bus slave receiver
A1	6	7	8	programmable address bit 1 for I^{2}C-bus slave receiver
A2	7	–	9	programmable address bit 2 for I^{2}C-bus slave receiver
V$_{EE}$	8	8	10	ground
DAC0	9	9	11	analog voltage output 0
DAC1	10	10	13	analog voltage output 1
DAC2	11	11	14	analog voltage output 2
DAC3	12	12	15	analog voltage output 3
DAC4	13	13	16	analog voltage output 4
DAC5	14	14	17	analog voltage output 5
DAC6	15	15	18	analog voltage output 6
DAC7	16	16	20	analog voltage output 7
n.c.	–	5	5, 6, 12, 19	not connected
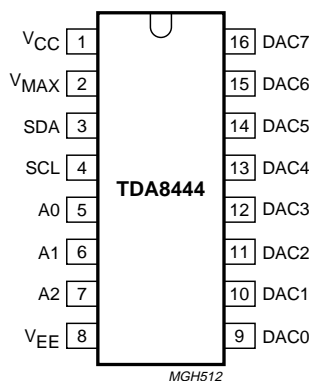
Fig.2 Pin configuration (TDA8444; DIP16).
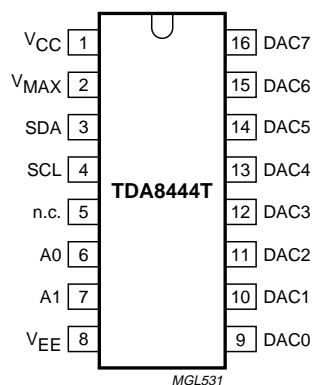
Fig.3 Pin configuration (TDA8444T; SO16).

Octuple 6-bit DACs with I^{2}C-bus

TDA8444; TDA8444T;
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Fig.4 Pin configuration (TDA8444AT; SO20).
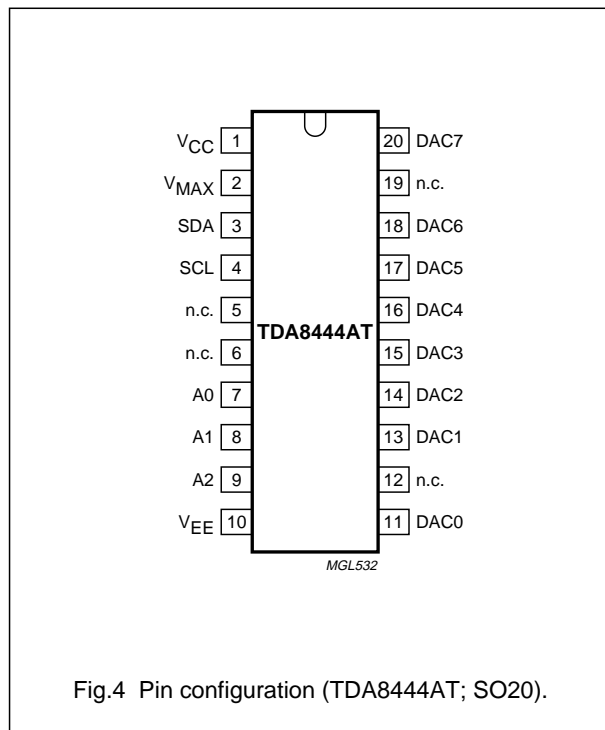
FUNCTIONAL DESCRIPTION

I^{2}C-bus interface

The I^{2}C-bus interface is a receive-only slave, which accepts data according the format shown in Table 1.

Table 1 I^{2}C-bus format (see note 1)

| S | 0 1 0 0 A2 A1 A0 0 | A | I3 I2 I1 I0 SD SC SB SA | A | X X D5 D4 D3 D2 D1 D0 | A | P |

Note

1. S = START condition; A2 to A0 = programmable address bits; A = Acknowledge; I3 to I0 = Instruction bits;
    SD to SA = subaddress bits; X = don't care; D5 to D0 = data bits; P = STOP condition.

Valid addresses are:

TDA8444 and TDA8444AT: 40H, 42H, 44H, 46H, 48H, 4AH, 4CH and 4EH

TDA8444T: 48H, 4AH, 4CH and 4EH (A2 is always logic 1).

All other addresses cannot be acknowledged by the circuit. The actual slave address depends on the programmable address bits A2, A1 and A0. This way up to eight circuits can be used on one I^{2}C-bus.

Valid instructions are: 00H to 0FH; F0H to FFH.

Octuple 6-bit DACs with I^{2}C-bus

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The circuit will not react to other combinations of the 4 instruction bits I3 to I0 than 0 or F, but will still generate an acknowledge. The difference between instruction 0 and F is only important when more than one data byte is sent within one transmission. Instruction 0 causes the data bytes to be written into the DAC-latches with consecutive subaddresses starting with the subaddress given in the instruction byte (auto-increment of subaddress), while instruction F will cause a consecutive writing of the data bytes into the same DAC-latch whose subaddress was given in the instruction byte. In case of only one data byte the DAC-latch with the subaddress equal to the subaddress in the instruction byte will receive the data.

Valid subaddresses are: 0H to 7H.

The subaddresses correspond to DAC0 to DAC7. The Auto-Increment (AI) function of instruction 0, however, works on all possible subaddresses 0 to F in such a way that next to subaddress F, subaddress 0 will follow, and so on.

The data will be latched into the DAC-latch on the positive-going edge of the acknowledge related clock pulse.

The specification of the SCL and SDA I/O meets the I^{2}C-bus specification. For protection against positive voltage pulses on pins 3 and 4, zener diodes are connected between these pins and V_{EE}. This means that normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1 and A2 can be easily programmed by either a connection to V_{EE} (An = 0) or V_{CC} (An = 1). If the inputs are left floating the result will be An = 1.

V_{MAX}

The V_{MAX} input gives a means of compressing the DAC output voltage swing. The maximum DAC output voltage will be equal to $V_{MAX} + V_{DAC(min)}$, while the 6-bit resolution is maintained. This enables a higher voltage resolution for smaller output swings.

DACs

The DACs consist of a 6-bit data-latch, current switches and an opamp. The current sources connected to the switches have values with weights 2^0 to 2^5. The sum of the switched on currents is converted by the opamp into a voltage between approximately 0.5 and 10.5 V if $V_{MAX} = V_{CC} = 12$ V. The DAC outputs are short-circuit protected against V_{CC} and V_{EE}. Capacitive load on the DAC outputs should not exceed 2 nF in order to prevent possible oscillations at certain levels. The temperature coefficient for each of the outputs remains in all possible conditions well below 0.1 LSB per Kelvin.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.5	+18	V
I_{CC}	supply current	−10	+40	mA
$P_{(max)}$	maximum power dissipation	–	500	mW
$V_{i(n)}$	input voltage	−0.5	+5.9	V
	pins SDA and SCL	−0.5	+5.9	V
	pins V_{MAX}, A0 to A2 and DAC0 to DAC7	−0.5	V_{CC} + 0.5	V
I_n	current in all pins except V_{CC} and V_{EE}	–	±10	mA
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−20	+70	°C

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA8444		75	K/W
	TDA8444T	note 1	100	K/W
	TDA8444AT	note 1	85	K/W

Note

1. When mounted on a Printed-Circuit Board (PCB).

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		4.5	12	13.2	V
I_{CC}	supply current	V_{MAX} = V_{CC} = 12 V; data = 00H	12	14	19	mA
P	power dissipation		–	170	250	mW
V_{rst}	power reset voltage		1	–	4	V
Pin V_{MAX}						
$V_{i(VMAX)}$	input effective voltage		1	–	V_{CC} – 2.0	V
I_i	input current	V_{MAX} = V_{CC}	–	–	10	µA
		V_{MAX} = 1 V	–	–	10	µA
Pins SDA and SCL						
V_I	input voltage		0	–	5.5	V
V_{IL}	LOW-level input voltage		–	–	1.0	V
V_{IH}	HIGH-level input voltage		3.0	–	–	V
I_{IL}	LOW-level input current	V_{SDA} = V_{SCL} = −0.3 V	–	–	−10	µA
I_{IH}	HIGH-level input current	V_{SDA} = V_{SCL} = 6 V	–	–	±10	µA
PIN SDA						
V_{OL}	LOW-level output voltage	I_L = 3 mA	–	–	0.4	V
$I_{o(sink)}$	output sink current		3	8	–	mA
Address bits (A0 to A2)						
V_I	input voltage		0	–	V_{CC}	V
V_{IL}	LOW-level input voltage		–	–	1.0	V
V_{IH}	HIGH-level input voltage		2.2	–	–	V
I_{IL}	LOW-level input current	V_{An} = V_{EE}	−10	−15	–	µA
I_{IH}	HIGH-level input current	V_{An} = V_{CC}	–	–	1	µA

Octuple 6-bit DACs with I²C-bus

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DACs (DAC0 to DAC7)						
V_o	DAC output voltage	$V_{MAX} = V_{CC}$	0.1	–	$V_{CC} - 0.5$	V
$V_{o(min)}$	minimum output voltage	data = 00H; $I_L = -2$ mA	0.1	0.28	0.5	V
$V_{o(max)}$	maximum output voltage	data = 3FH; $I_L = -2$ mA				
		$V_{MAX} = V_{CC}$	10.0	10.5	11.5	V
		$1 < V_{MAX} < 10$ V	–	note 1	–	V
$I_{o(sink)}$	output sink current	$V_{DAC} = V_{CC}$; data = 1FH	2	8	15	mA
$I_{o(source)}$	output source current	$V_{DAC} = V_{EE}$; data = 1FH	−2	–	−6	mA
Z_o	output impedance	$-2 \le I_L \le +2$ mA; data = 1FH	–	4	50	Ω
DNL	differential non-linearity	$V_{MAX} = V_{CC}$; $I_L = -2$ mA	–	–	±0.5	LSB
INL	integral non-linearity	$V_{MAX} = V_{CC}$; $I_L = -2$ mA	–	–	±0.5	LSB
ΔG_{FS}	DC gain match at full-scale	data = 3FH; $I_L = -2$ mA	–	–	5	%
$\Delta G/\Delta data$	DC gain versus other DAC data change	data = 3FH; $I_L = -2$ mA	–	<±0.5	–	LSB
TC	temperature coefficient	data = 3FH; $I_L = -2$ mA	–	<±0.1	–	LSB/K

Note

1. The output voltage is typically: $\dfrac{V_{swing}}{(V_{CC} - 2.0)} \times V_{MAX} + V_{o\,(00H)}$ with $V_{swing} = V_{o(3FH)} - V_{o(00H)}$ for $V_{MAX} = V_{CC}$.

Octuple 6-bit DACs with I²C-bus

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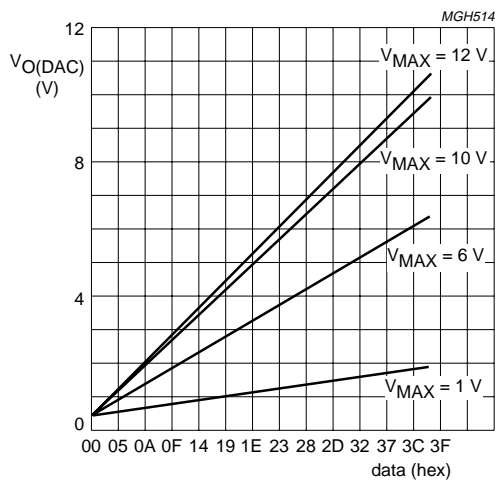TDA8444AT

TEST AND APPLICATION INFORMATION

V_{CC} = 12 V.

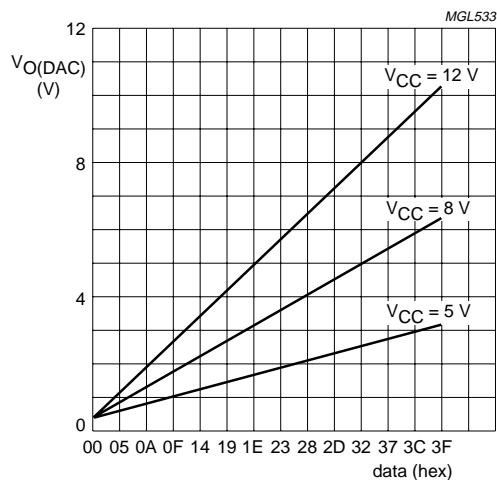Fig.5   DAC output voltage as a function of
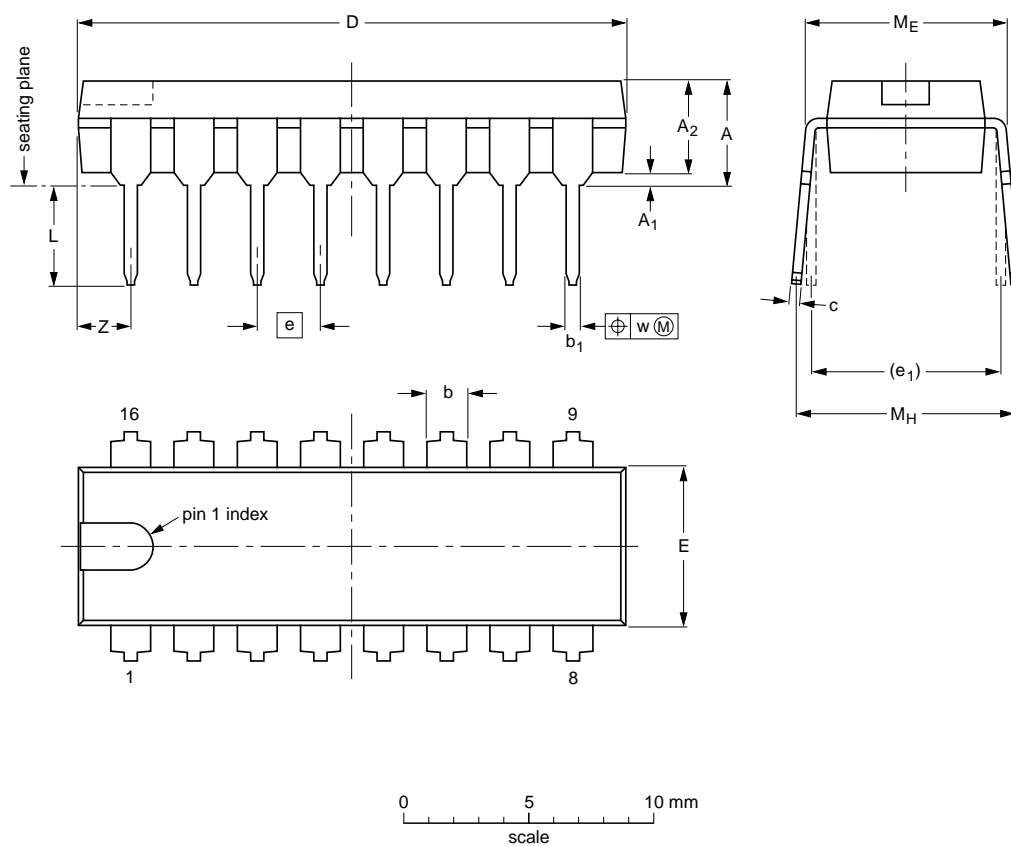programmed value.

V_{MAX} = V_{CC}.

Fig.6   DAC output voltage as a function of
programmed value.

Octuple 6-bit DACs with I^{2}C-bus

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PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1

0   5   10 mm

scale

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

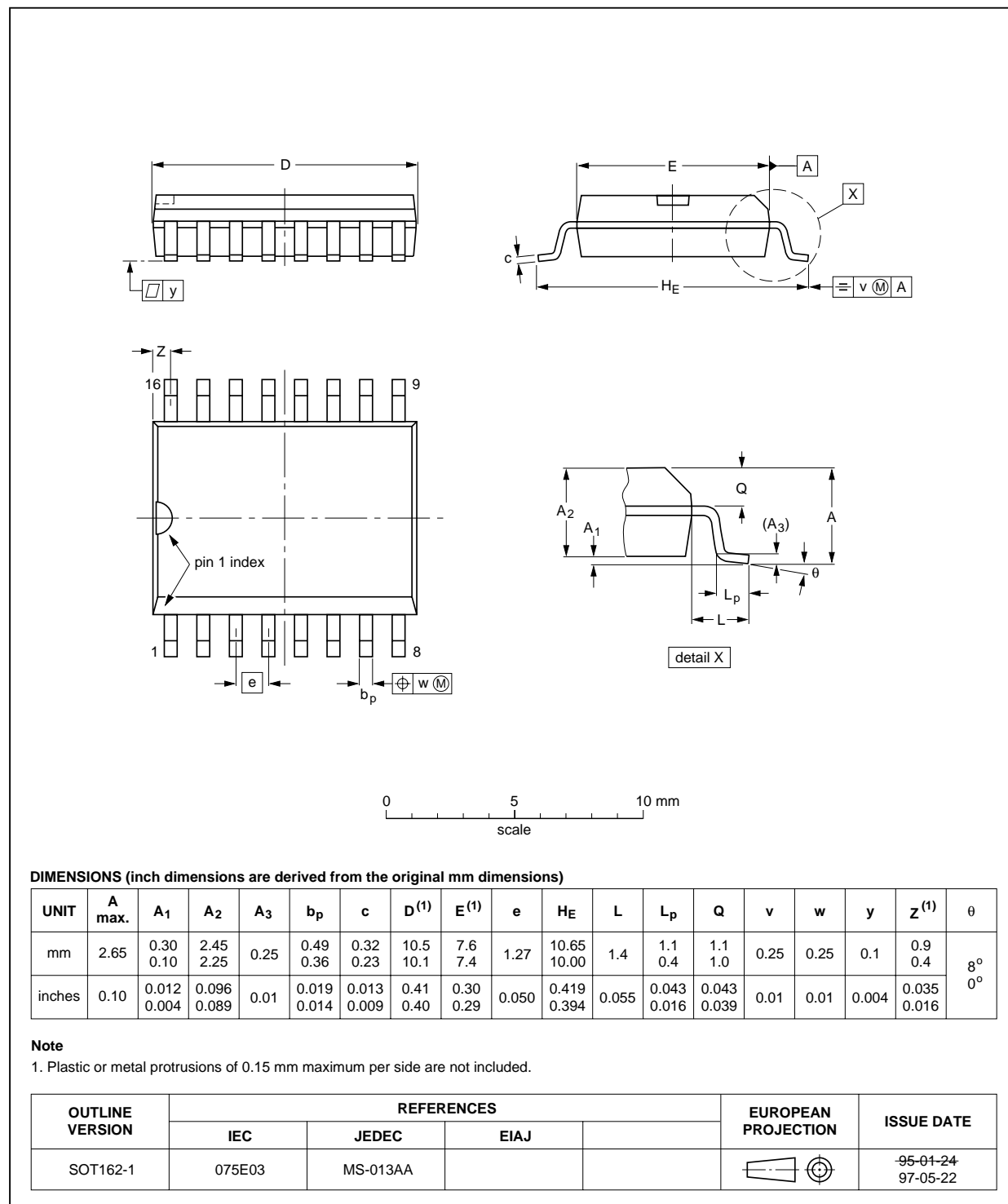| UNIT	A max.	A$_1$ min.	A$_2$ max.	b	b$_1$	c	D$^{(1)}$	E$^{(1)}$	e	e$_1$	L	M$_E$	M$_H$	w	Z$^{(1)}$ max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

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SO16: plastic small outline package; 16 leads; body width 7.5 mm   **SOT162-1**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A$_1$	A$_2$	A$_3$	b$_p$	c	D$^{(1)}$	E$^{(1)}$	e	H$_E$	L	L$_p$	Q	v	w	y	Z$^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

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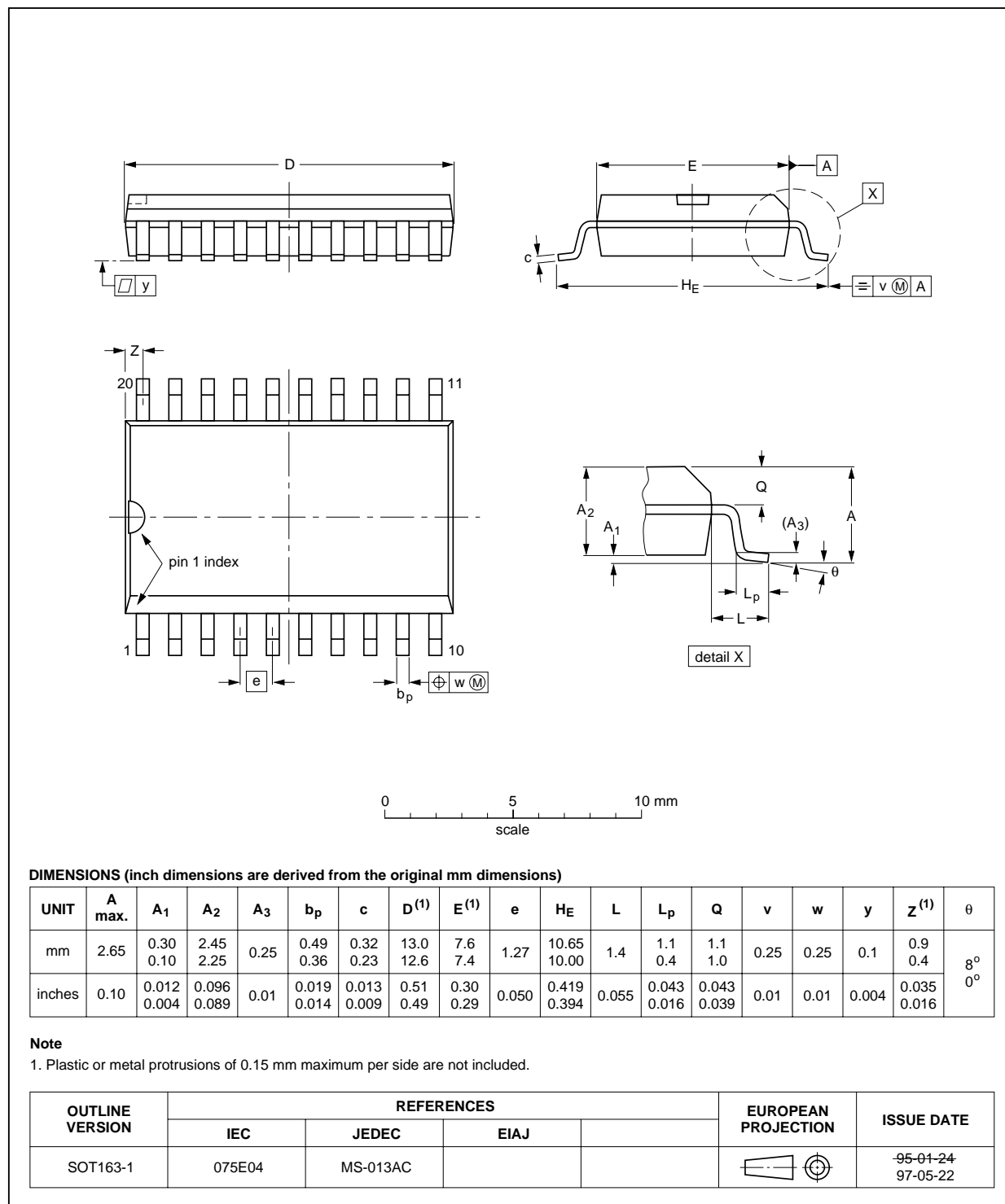
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Octuple 6-bit DACs with I^{2}C-bus

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TDA8444AT

SO20: plastic small outline package; 20 leads; body width 7.5 mm　　　　　　**SOT163-1**

scale

0　　　　5　　　　10 mm

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A$_1$	A$_2$	A$_3$	b$_p$	c	D$^{(1)}$	E$^{(1)}$	e	H$_E$	L	L$_p$	Q	v	w	y	Z$^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

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Octuple 6-bit DACs with I²C-bus

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

* A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
* The longitudinal axis of the package footprint must be parallel to the solder flow.
* The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I^{2}C COMPONENTS

Purchase of Philips I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C system provided the system conforms to the I^{2}C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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