TDA8566

2 × 40 W/2 Ω stereo BTL car radio power amplifier with differential inputs and diagnostic outputs

Rev. 06 — 15 October 2007 Product data sheet

1. General description

The TDA8566 is an integrated class-B output amplifier which is available in several packages. TDA8566TH is contained in a 20-lead small outline plastic package. The TDA8566TH1 is a 24-lead small outline plastic package which is pin compatible with the I^2C-bus controlled amplifier TDA1566TH for one board layout. TDA8566Q is a 17-pin DIL-bent-SIL package.

The device contains 2 amplifiers in a Bridge-Tied Load (BTL) configuration. The output power is 2 × 25 W in a 4 Ω load or 2 × 40 W in a 2 Ω load. It has a differential input stage and 2 diagnostic outputs. The device is primarily developed for car radio applications.

2. Features

- Differential inputs
- Very high Common Mode Rejection Ratio (CMRR)
- High common mode input signal handling
- Requires very few external components
- High output power
- 4 Ω and 2 Ω load driving capability
- Low offset voltage at output
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature pre-warning)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit proof to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Protected against electrostatic discharge
- No switch-on/switch-off plops
- Low thermal resistance
- TDA8566TH1 is pin compatible with TDA1566TH

3. Quick reference data

Table 1. Quick reference data

V_P = 14.4 V; T_{amb} = 25 °C; f_i = 1 kHz; measured in test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_P	supply voltage		[1]	6	14.4	18	V
I_{ORM}	repetitive peak output current			-	-	7.5	A
I_q	quiescent current	R_L = ∞ Ω		-	115	180	mA
I_{stb}	standby current			-	0.1	10	μA
Z_i	input impedance	differential		100	120	150	kΩ
P_o	output power	R_L = 4 Ω; THD = 10 %		21	25	-	W
		R_L = 2 Ω; THD = 10 %		33	40	-	W
SVRR	supply voltage ripple rejection	operating	[2]	50	60	-	dB
α_{cs}	channel separation	P_o = 25 W; R_s = 10 kΩ		45	50	-	dB
CMRR	common mode rejection ratio	R_s = 0 Ω	[3]	60	75	-	dB
G_v	closed loop voltage gain			25	26	27	dB
$V_{n(o)}$	noise output voltage	operating; R_s = 0 Ω	[4]	-	85	120	μV

[1] The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.

[2] $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.

[3] Common mode rejection ratio measured at the output (over R_L) with both inputs tied together; $V_{common} \leq 3.5$ V (RMS); f_i = 100 Hz to 10 kHz; R_s = 0 Ω.

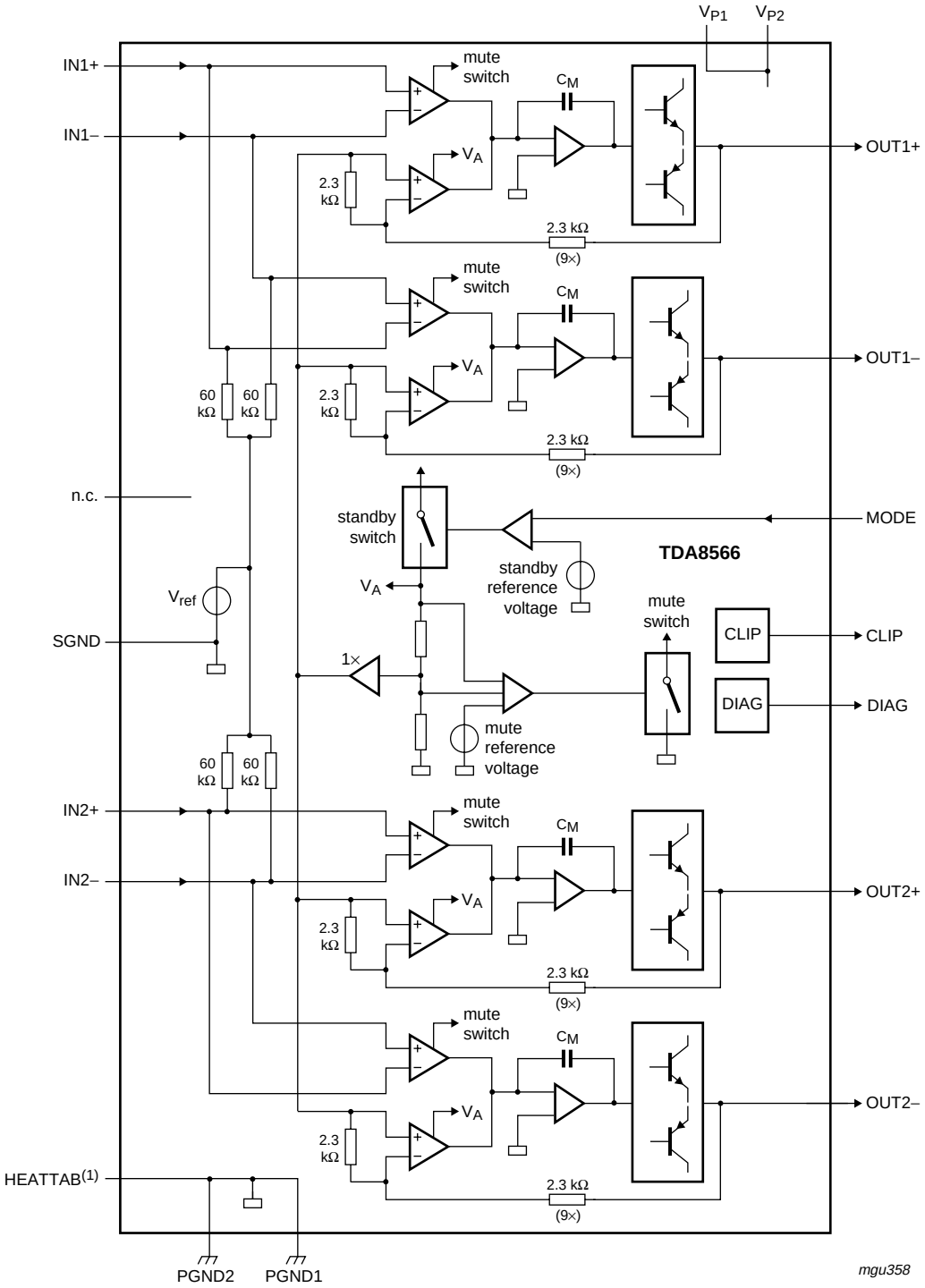
[4] Noise measured in a bandwidth of 20 Hz to 20 kHz.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8566TH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-3
TDA8566TH1	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3
TDA8566Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

5. Block diagram



(1) Pin HEATTAB is available in TDA8566TH1 only.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

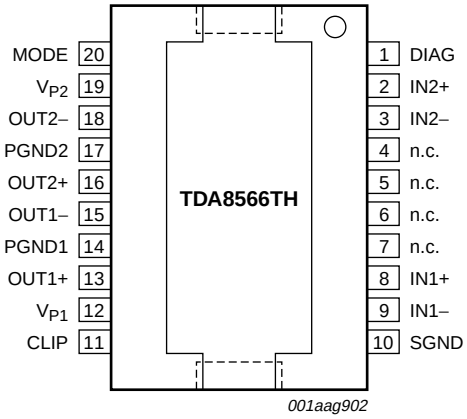


Fig 2. Pin configuration TDA8566TH

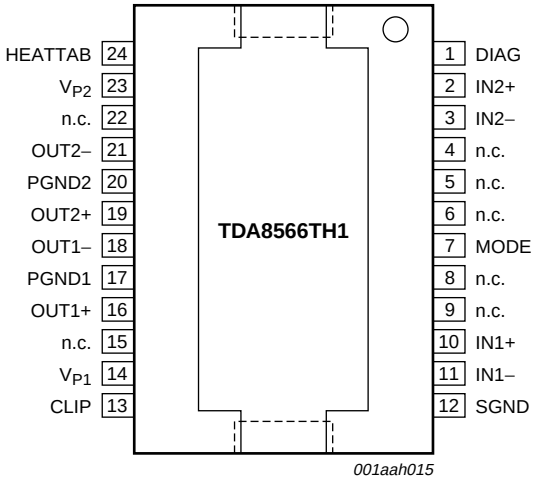


Fig 3. Pin configuration TDA8566TH1

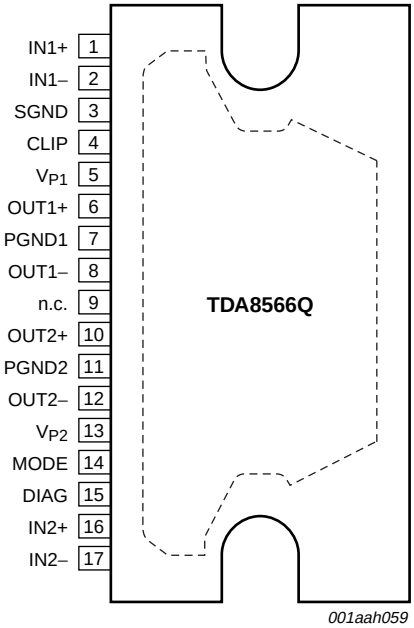


Fig 4. Pin configuration TDA8566Q

6.2 Pin description

Table 3. Pin description TDA8566TH and TDA8566TH1

Symbol	Pin		Description
	TDA8566TH	TDA8566TH1	
DIAG	1	1	short-circuit and temperature pre-warning diagnostic output
IN2+	2	2	channel 2 input positive
IN2–	3	3	channel 2 input negative
n.c.	4	4	not connected
n.c.	5	5	not connected
n.c.	6	6	not connected
n.c.	7	-	not connected
n.c.	-	8	not connected
n.c.	-	9	not connected
IN1+	8	10	channel 1 input positive
IN1–	9	11	channel 1 input negative
SGND	10	12	signal ground
CLIP	11	13	clip detection output
V_{P1}	12	14	supply voltage 1
n.c.	-	15	not connected
OUT1+	13	16	channel 1 output positive
PGND1	14	17	power ground 1
OUT1–	15	18	channel 1 output negative
n.c.	-	-	not connected
OUT2+	16	19	channel 2 output positive
PGND2	17	20	power ground 2
OUT2–	18	21	channel 2 output negative
n.c.	-	22	not connected
V_{P2}	19	23	supply voltage 2
MODE	20	7	mode select switch input (standby/mute/operating)
HEATTAB	-	24	connect to ground, used for test purposes only

Table 4. Pin description TDA8566Q

Symbol	Pin	Description
IN1+	1	channel 1 input positive
IN1–	2	channel 1 input negative
SGND	3	signal ground
CLIP	4	clip detection output
V_{P1}	5	supply voltage 1
OUT1+	6	channel 1 output positive
PGND1	7	power ground 1
OUT1–	8	channel 1 output negative
n.c.	9	not connected

Table 4. Pin description TDA8566Q *…continued*

Symbol	Pin	Description
OUT2+	10	channel 2 output positive
PGND2	11	power ground 2
OUT2–	12	channel 2 output negative
V_{P2}	13	supply voltage 2
MODE	14	mode select switch input (standby/mute/operating)
DIAG	15	short-circuit and temperature pre-warning diagnostic output
IN2+	16	channel 2 input positive
IN2–	17	channel 2 input negative

7. Functional description

The TDA8566 contains 2 identical amplifiers and can be used for BTL applications. The gain of each amplifier is fixed at 26 dB. Special features of this device are:

- Mode select switch
- Clip detection
- Short-circuit diagnostic
- Temperature pre-warning
- Open-collector diagnostic outputs
- Differential inputs

7.1 Mode select switch (pin MODE)

- Standby: low supply current
- Mute: input signal suppressed
- Operating: normal on condition

Since this pin has a very low input current (< 40 μA), a low-cost supply switch can be applied. To avoid switch-on plops, it is advisable to keep the amplifier in the mute mode for a period of ≥ 150 ms (charging the input capacitors at pins IN1+, IN1–, IN2+ and IN2–). This can be realized by using a microcontroller or by using an external timing circuit as illustrated in Figure 8.

7.2 Clip detection (pin CLIP)

When clipping occurs at one or more output stages, the dynamic distortion detector becomes active and pin CLIP goes LOW. This information can be used to drive a sound processor or a DC volume control to attenuate the input signal and so limit the level of distortion. The output level of pin CLIP is independent of the number of channels that are being clipped. The clip detection circuit is disabled in a short-circuit condition, so if a fault condition occurs at the outputs, pin CLIP will remain at a HIGH level. The clip detection waveforms are illustrated in Figure 5.

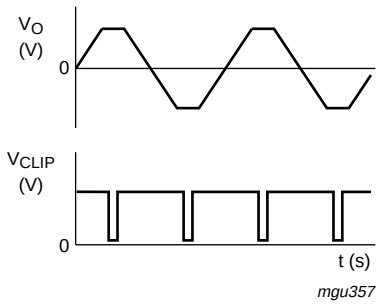


Fig 5. Clip detection waveforms

7.3 Short-circuit diagnostic (pin DIAG)

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again (with a delay of approximately 20 ms after the removal of the short-circuit). During this short-circuit condition, pin DIAG is continuously LOW.

When a short-circuit occurs across the load of one or both channels, the output stages are switched off for approximately 20 ms. After that time the load condition is checked during approximately 50 µs to see whether the short-circuit is still present. Due to this duty cycle of 50 µs/20 ms the average current consumption during the short-circuit condition is very low (approximately 40 mA). During this condition, pin DIAG is LOW for 20 ms and HIGH for 50 µs; see Figure 6. The power dissipation in any short-circuit condition is very low.

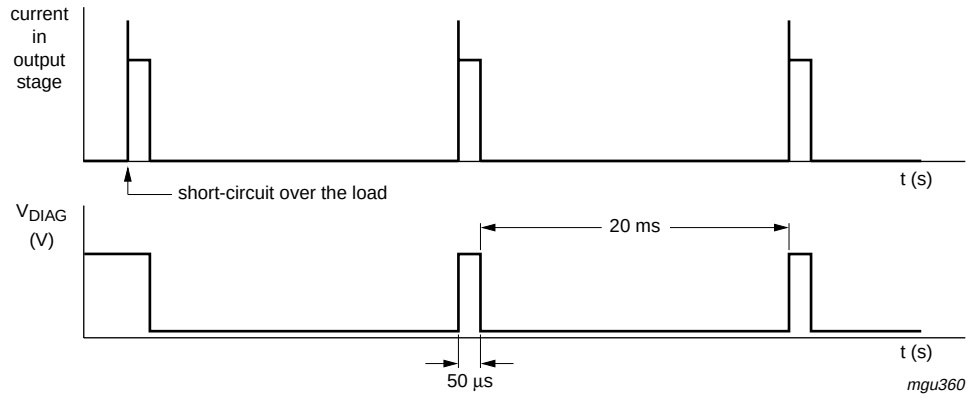


Fig 6. Short-circuit diagnostic timing diagram

7.4 Temperature pre-warning (pin DIAG)

When the virtual junction temperature (T_{vj}) reaches 145 °C, pin DIAG will become continuously LOW.

7.5 Open-collector diagnostic outputs

Pins DIAG and CLIP are open-collector outputs, therefore more devices can be tied together. Pins DIAG and CLIP can also be tied together. An external pull-up resistor is required.

7.6 Differential inputs

The input stage is a high-impedance fully differential balanced input stage that is also capable of operating in a single-ended mode with one of the inputs capacitively coupled to an audio ground. It should be noted that if a source resistance is added (input voltage dividers) the CMRR degrades to lower values.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage	operating	-	18	V
		non-operating	-	30	V
		load dump protection; during 50 ms; $t_r \geq 2.5$ ms	-	45	V
I_{OSM}	non-repetitive peak output current		-	10	A
I_{ORM}	repetitive peak output current		-	7.5	A
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		-	150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{psc}	short-circuit safe voltage		-	18	V
V_{rp}	reverse polarity voltage		-	6.0	V
P_{tot}	total power dissipation		-	60	W

9. Thermal characteristics

Table 6. Thermal characteristics

Thermal characteristics in accordance with IEC 60747-1.

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	see Figure 7	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

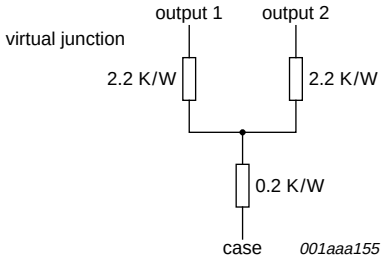


Fig 7. Equivalent thermal resistance network

10. Static characteristics

Table 7. Static characteristics

V_P = 14.4 V; T_{amb} = 25 °C; measured in test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	supply voltage		[1]	6	14.4	18	V
I_q	quiescent current	R_L = ∞ Ω		-	115	180	mA
Operating condition							
V_{MODE}	mode select switch level			8.5	-	V_P	V
I_{MODE}	mode select switch current	V_{MODE} = 14.4 V		-	15	40	µA
V_O	output voltage		[2]	-	7.0	-	V
V_{OO}	output offset voltage			-	-	100	mV
Mute condition							
V_{MODE}	mode select switch level			3.3	-	6.4	V
V_O	output voltage		[2]	-	7.0	-	V
V_{OO}	output offset voltage			-	-	60	mV
ΔV_{OO}	output offset voltage difference	with respect to operating condition		-	-	60	mV
Standby condition							
V_{MODE}	mode select switch level			0	-	2	V
I_{stb}	standby current			-	0.1	10	µA
Diagnostic							
V_{DIAG}	diagnostic output voltage	during any fault condition		-	-	0.6	V

[1] The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.

[2] At V_P = 18 V to 30 V the DC output voltage is ≤ 0.5V_P.

11. Dynamic characteristics

Table 8. Dynamic characteristics

V_P = 14.4 V; T_{amb} = 25 °C; R_L = 2 Ω; f_i = 1 kHz; measured in test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD = 0.5 %		25	30	-	W
		THD = 10 %		33	40	-	W
		THD = 30 %		45	55	-	W
		V_P = 13.5 V; THD = 0.5 %		-	25	-	W
		V_P = 13.5 V; THD = 10 %		-	35	-	W
		THD = 0.5 %; R_L = 4 Ω		16	19	-	W
		THD = 10 %; R_L = 4 Ω		21	25	-	W
		THD = 30 %; R_L = 4 Ω		28	35	-	W
		V_P = 13.5 V; THD = 0.5 %; R_L = 4 Ω		-	14	-	W
		V_P = 13.5 V; THD = 10 %; R_L = 4 Ω		-	22	-	W
THD	total harmonic distortion	P_o = 1 W		-	0.1	-	%
		V_{CLIP} = 0.6 V	[1]	-	8	-	%
		P_o = 1 W; R_L = 4 Ω		-	0.05	-	%
B	power bandwidth	THD = 0.5 %; P_o = −1 dB with respect to 25 W		-	20 to 20000	-	Hz
$f_{ro(l)}$	low frequency roll off	−1 dB	[2]	-	25	-	Hz
$f_{ro(h)}$	high frequency roll off	−1 dB		20	-	-	kHz
G_v	closed loop voltage gain			25	26	27	dB
SVRR	supply voltage ripple rejection	operating	[3]	50	60	-	dB
		mute	[3]	50	-	-	dB
		standby	[3]	80	-	-	dB
Z_i	input impedance	differential		100	120	150	kΩ
		single-ended		50	60	75	kΩ
$\lvert\Delta Z_i\rvert$	input impedance mismatch			-	2	-	%
$V_{n(o)}$	noise output voltage	operating; R_S = 0 Ω	[4]	-	85	120	μV
		operating; R_S = 10 kΩ	[4]	-	100	-	μV
		mute; independent of R_S	[4]	-	60	-	μV
α_{cs}	channel separation	P_o = 25 W; R_S = 10 kΩ		45	50	-	dB
$\lvert\Delta G_v\rvert$	channel unbalance			-	-	1	dB

Table 8. Dynamic characteristics *...continued*

V_P = 14.4 V; T_{amb} = 25 °C; R_L = 2 Ω; f_i = 1 kHz; measured in test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{o(mute)}$	output signal voltage in mute	V_{in} = $V_{in(max)}$ = 1 V (RMS)		-	-	2	mV
CMRR	common mode rejection ratio	R_s = 0 Ω	[5]	60	75	-	dB
		R_s = 45 kΩ	[6]	40	-	-	dB

[1] Dynamic distortion detector active; pin CLIP is LOW.

[2] Frequency response externally fixed.

[3] V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.

[4] Noise measured in a bandwidth of 20 Hz to 20 kHz.

[5] Common mode rejection ratio measured at the output (over R_L) with both inputs tied together; V_{common} ≤ 3.5 V (RMS); f_i = 100 Hz to 10 kHz; R_s = 0 Ω.

[6] Common mode rejection ratio measured at the output (over R_L) with both inputs tied together; V_{common} ≤ 3.5 V (RMS); f_i = 1 kHz; R_s = 45 kΩ. The mismatch of the input coupling capacitors is excluded.

12. Application information

12.1 Diagnostic output

Special care must be taken in the PCB layout to separate pin CLIP from pins IN1+, IN1–, IN2+ and IN2– to minimize the crosstalk between the CLIP output and the inputs.

12.2 Mode select switch

To avoid switch-on plops, it is advisable to keep the amplifier in the mute mode during ≥ 150 ms (charging of the input capacitors at pins IN1+, IN1–, IN2+ and IN2–). The circuit in Figure 8 slowly ramps-up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

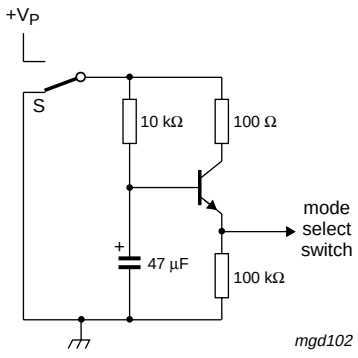


Fig 8. Mode select switch circuit

13. Test information

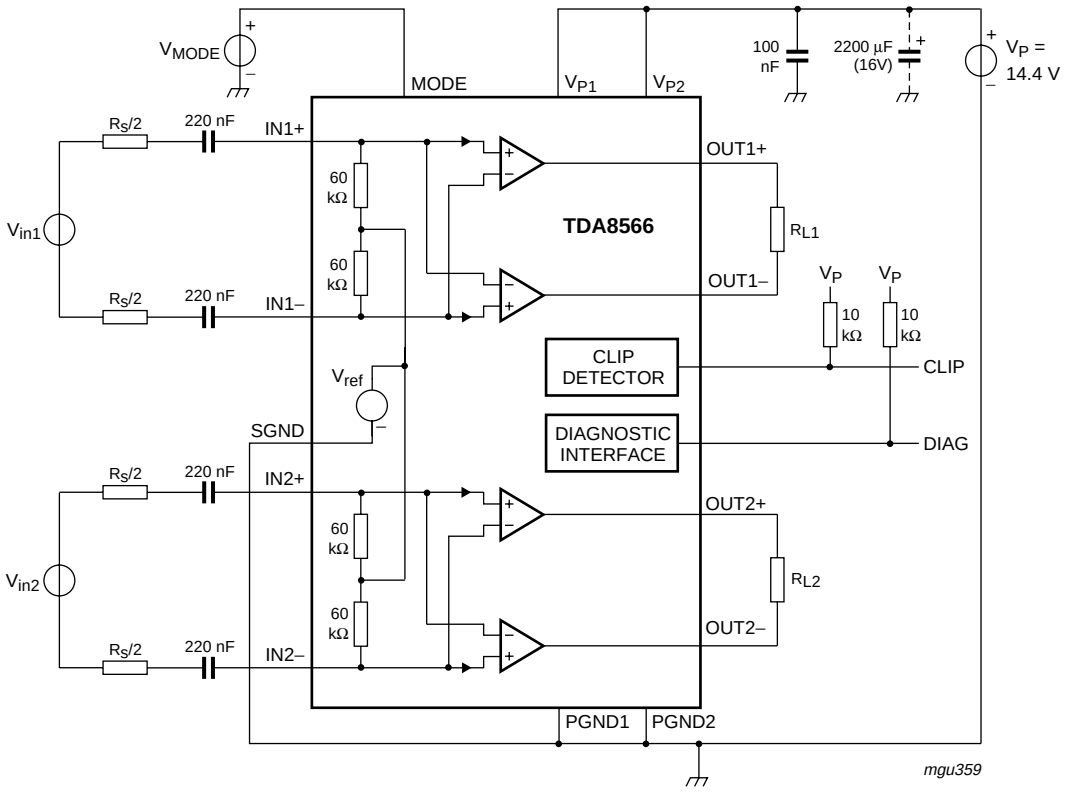
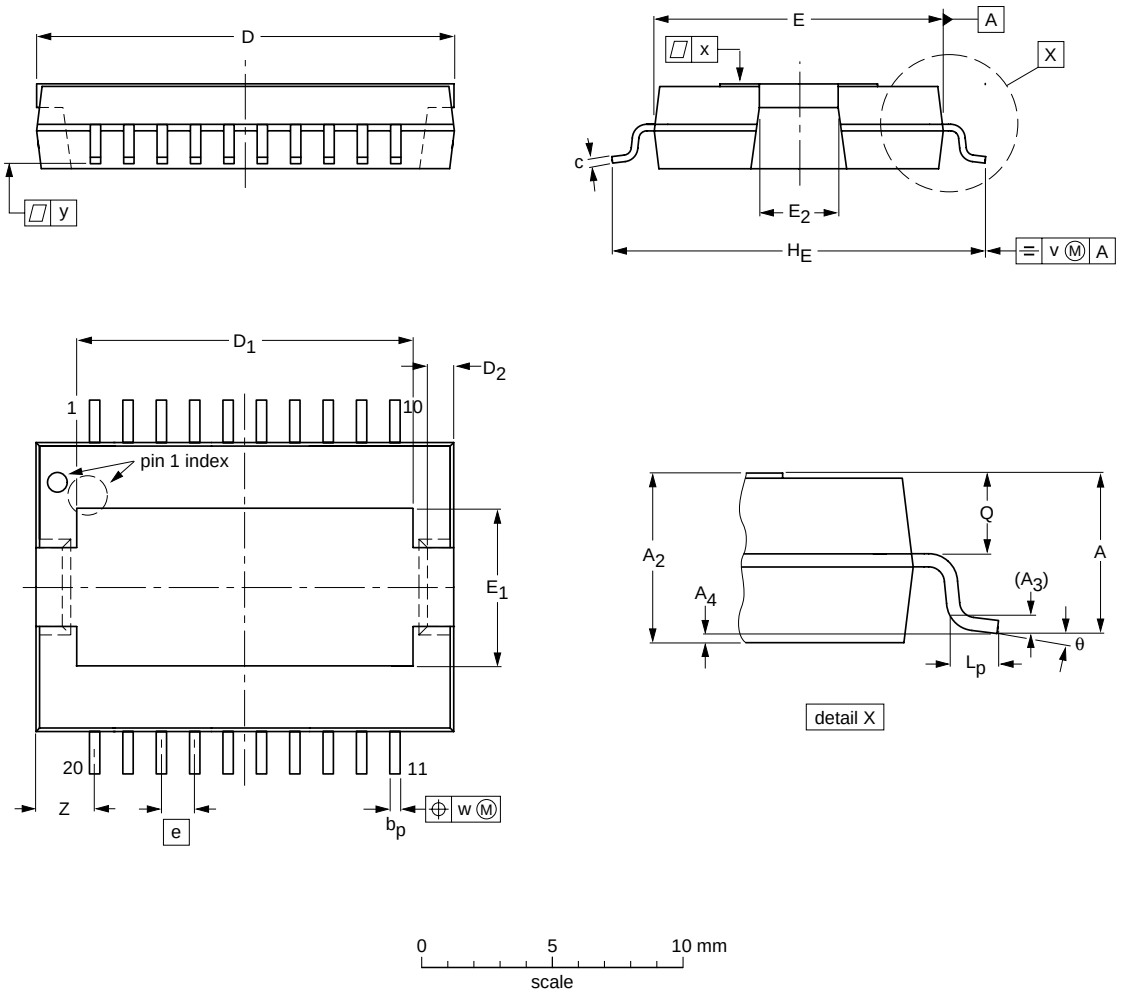


Fig 9. Stereo BTL test diagram

14. Package outline

HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height **SOT418-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4[1]	b_p	c	D[2]	D_1	D_2	E[2]	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 –0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

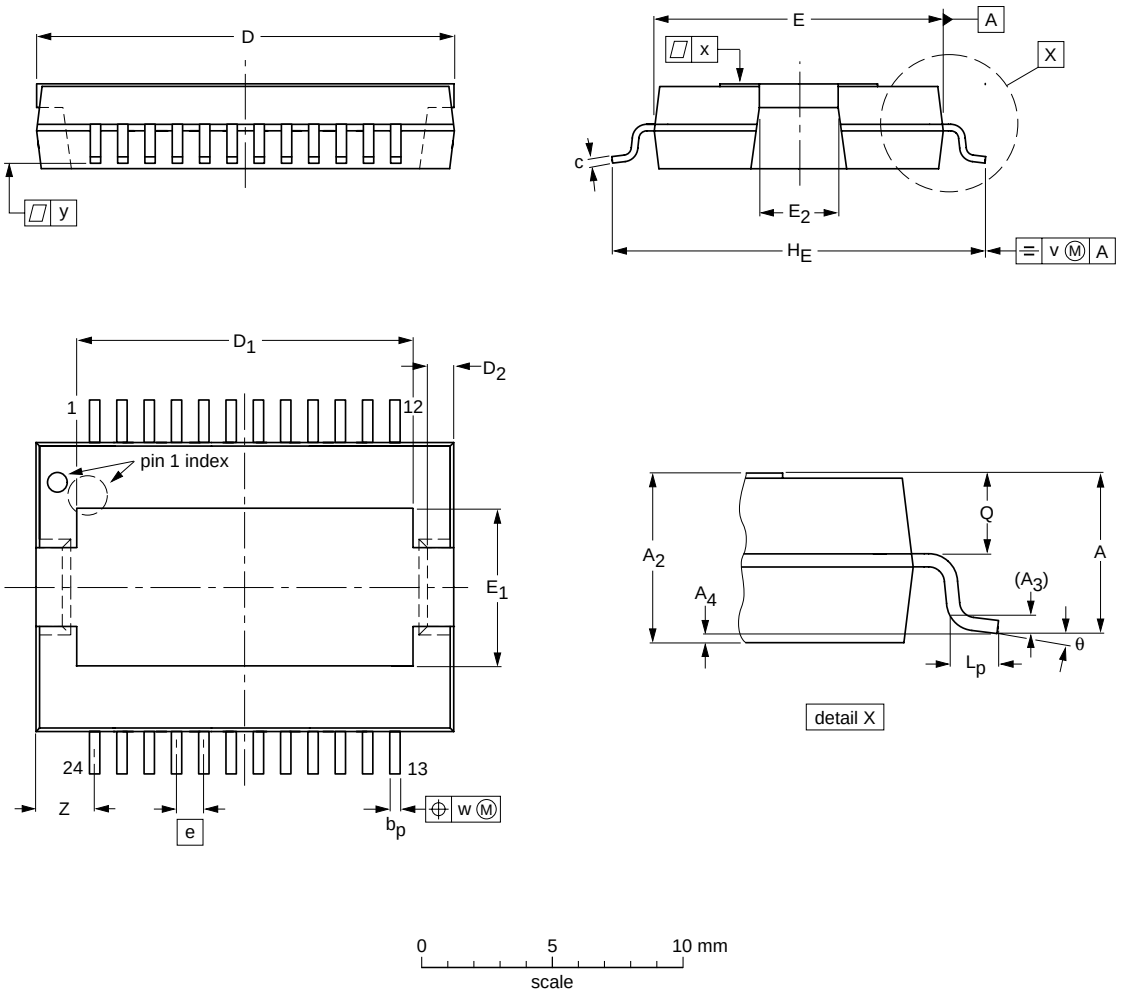
Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT418-3						~~02-02-12~~ 03-07-23

Fig 10. Package outline SOT418-3 (HSOP20)

HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off height **SOT566-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4[1]	b_p	c	D[2]	D_1	D_2	E[2]	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 –0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.7 2.2	8° 0°

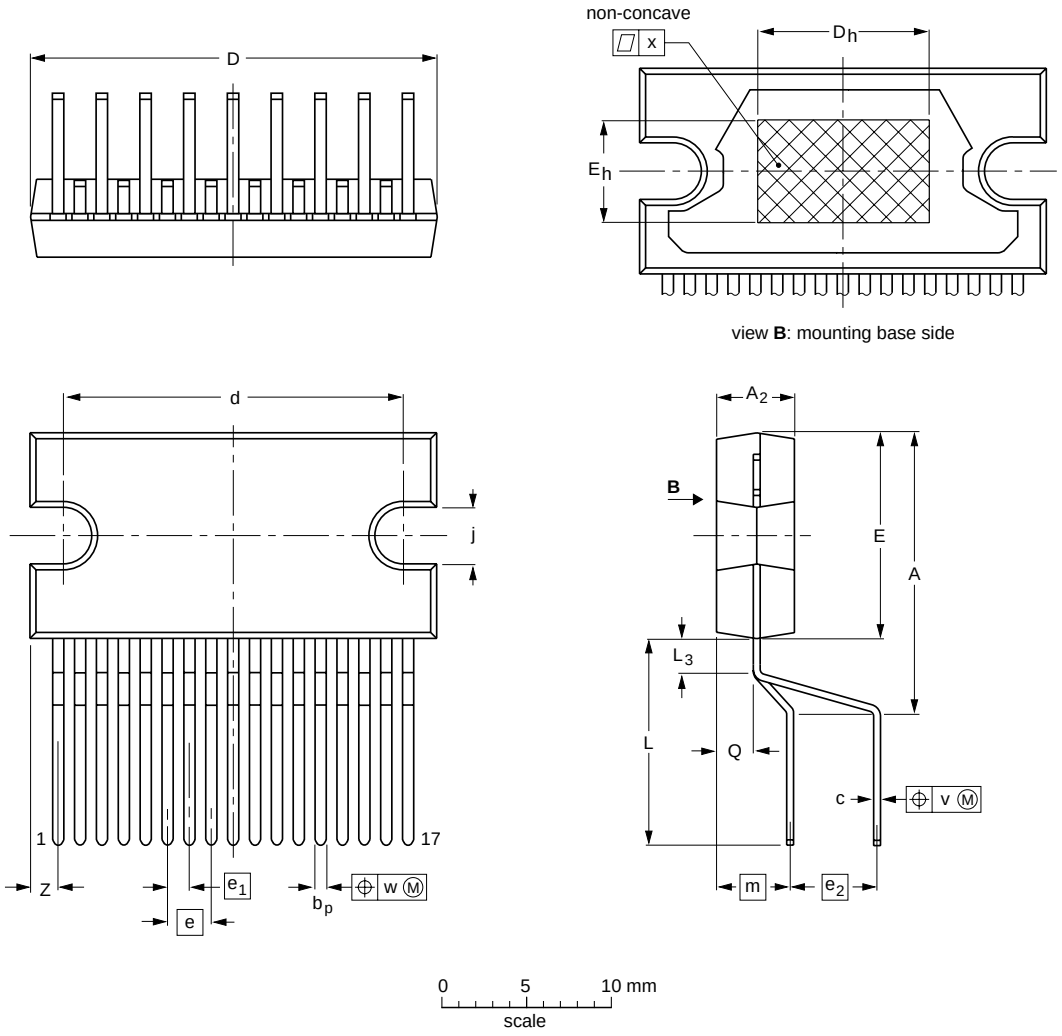
Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT566-3						~~03-02-18~~ 03-07-23

Fig 11. Package outline SOT566-3 (HSOP24)

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT243-1						~~99-12-17~~ 03-03-12

Fig 12. Package outline SOT243-1 (DBS17P)

15. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

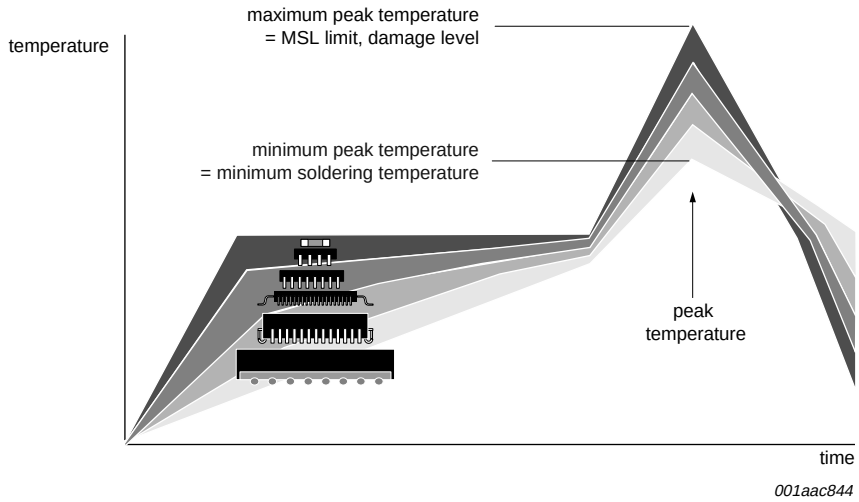
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8566_6	20071015	Product data sheet	-	TDA8566Q_5 TDA8566TH_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 9 “Thermal characteristics”: changed value of $R_{th(j-c)}$ to 1.3 K/W • Figure 7: values updated • Included TDA8566TH1 and TDA8566Q in the data sheet			
TDA8566Q_5	20010221	Product specification	-	-
TDA8566TH_2	20030708	Product specification	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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