TDF8599A

I²C-bus controlled dual channel 135 W/4 Ω, single channel 250 W/2 Ω class-D power amplifier with load diagnostics

Rev. 3 — 2 May 2013 Product data sheet

1. General description

The TDF8599A is a dual Bridge-Tied Load (BTL) car audio amplifier comprising an NDMOST-NDMOST output stage based on SOI BCDMOS technology. Low power dissipation enables the TDF8599A high-efficiency, class-D amplifier to be used with a smaller heat sink than those normally used with standard class-AB amplifiers.

The TDF8599A can operate in either non-I²C-bus mode or I²C-bus mode. When in I²C-bus mode, DC load detection results and fault conditions can be easily read back from the device. Up to 15 I²C-bus addresses can be selected depending on the value of the external resistor connected to pins ADS and MOD.

When pin ADS is short circuited to ground, the TDF8599A operates in non-I²C-bus mode. Switching between Operating mode and Mute mode in non-I²C-bus mode is only possible using pins EN and SEL_MUTE.

2. Features and benefits

- High-efficiency
- Low quiescent current
- Operating voltage from 8 V to 35 V
- Two 4 Ω/2 Ω capable BTL channels or one 1 Ω capable BTL channel
- Differential inputs
- I²C-bus mode with 15 I²C-bus addresses or non-I²C-bus mode operation
- Clip detect
- Independent short circuit protection for each channel
- Advanced short circuit protection for load, GND and supply
- Load dump protection
- Thermal foldback and thermal protection
- DC offset protection
- Selectable AD or BD modulation
- Parallel channel mode for high current drive capability
- Advanced clocking:
  - Switchable oscillator clock source: internal for Master mode or external for Slave mode
  - Spread spectrum mode
  - Phase staggering
  - Frequency hopping
- No ‘pop noise’ caused by DC output offset voltage

- I²C-bus mode:
  - DC load detection
  - AC load detection
  - Thermal pre-warning diagnostic level setting
  - Identification of activated protections or warnings
  - Selectable diagnostic information available using pins DIAG and CLIP
- Qualified in accordance with AEC-Q100

3. Applications

- Car audio

4. Quick reference data

Table 1. Quick reference data

V_P = 14.4 V unless otherwise stated.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_P	supply voltage		[1]	8	14.4	35	V
I_P	supply current	off state; $T_j \leq 85$ °C; V_P = 14.4 V		-	2	10	μA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, snubbers and filter connected		-	90	120	mA
P_o	output power	Stereo mode:	[2]				
		V_P = 14.4 V; THD = 1 %; R_L = 4 Ω		18	20	-	W
		V_P = 14.4 V; THD = 10 %; R_L = 4 Ω		23	25	-	W
		square wave (EIAJ); R_L = 4 Ω		-	40	-	W
		V_P = 35 V; THD = 10 %; R_L = 4 Ω		-	135	-	W
		V_P = 14.4 V; THD = 1 %; R_L = 2 Ω		26	29	-	W
		V_P = 14.4 V; THD = 10 %; R_L = 2 Ω		34	38	-	W
		square wave (EIAJ); R_L = 2 Ω		-	60	-	W
		Parallel mode:	[2]				
		V_P = 14.4 V; THD = 10 %; R_L = 2 Ω		-	50	-	W
		V_P = 35 V; THD = 10 %; R_L = 2 Ω		-	250	-	W
		V_P = 25 V; THD = 1 %; R_L = 1 Ω		135	150	-	W

[1] In this data sheet supply voltage V_P describes V_{P1}, V_{P2} and V_{PA}.

[2] Output power is measured indirectly based on R_{DSon} measurement.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDF8599ATH	HSOP36	plastic, heatsink small outline package; 36 leads; low stand-off height	SOT851-2

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6. Block diagram

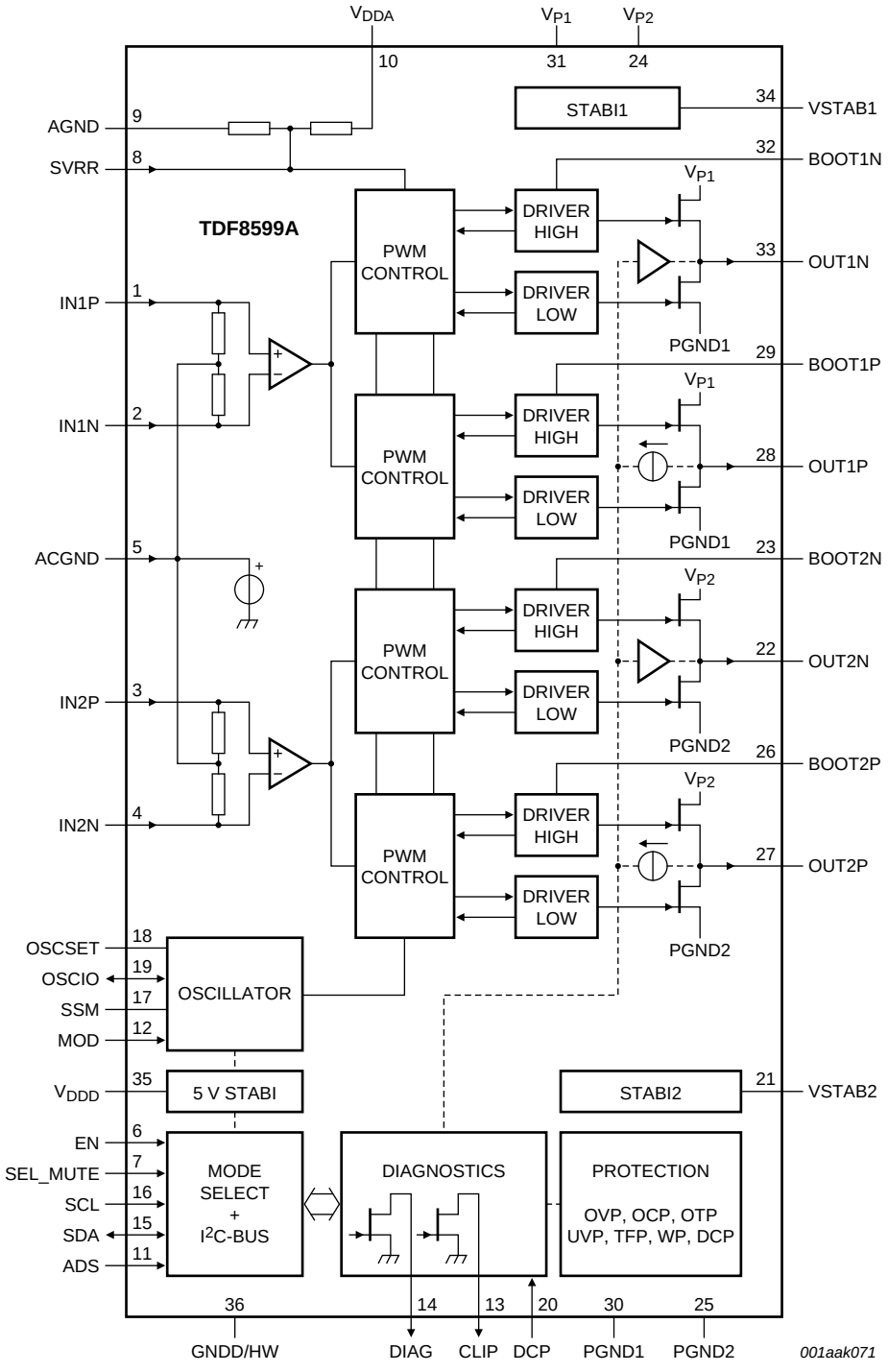

Fig 1. Block diagram

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7. Pinning information

7.1 Pinning

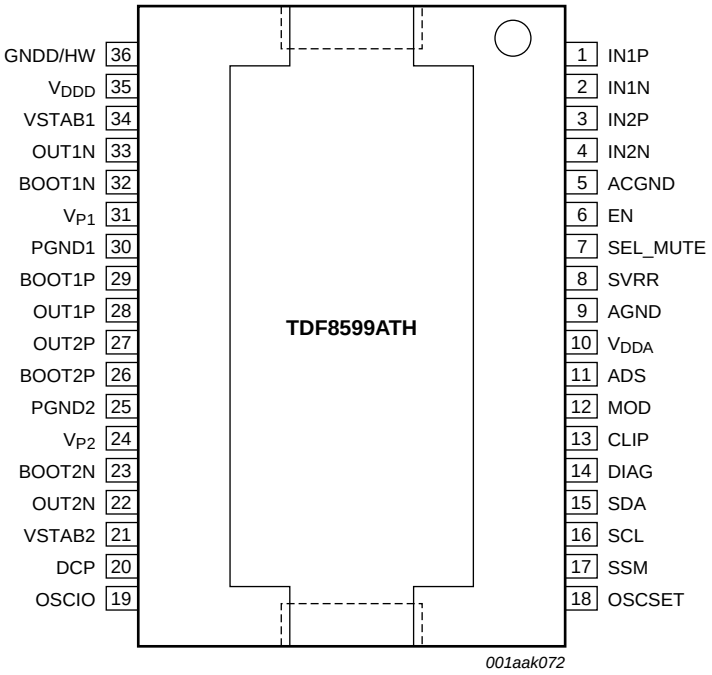

Fig 2. Heatsink up (top view) pin configuration TDF8599ATH

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
IN1P	1	I	channel 1 positive audio input
IN1N	2	I	channel 1 negative audio input
IN2P	3	I	channel 2 positive audio input
IN2N	4	I	channel 2 negative audio input
ACGND	5	I	decoupling for input reference voltage
EN	6	I	enable input: non-I²C-bus mode: switch between off and Mute mode I²C-bus mode: off and Standby mode
SEL_MUTE	7	I	select mute or unmute
SVRR	8	I	decoupling for internal half supply reference voltage
AGND	9	G	analog supply ground
V_{DDA}	10	P	analog supply voltage
ADS	11	I	non-I²C-bus mode: connected to ground I²C-bus mode: selection and address selection pin
MOD	12	I	modulation mode, phase shift and parallel mode select

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Table 3. Pin description *...continued*

Symbol	Pin	Type[1]	Description
CLIP	13	O	clip output; open-drain
DIAG	14	O	diagnostic output; open-drain
SDA	15	I/O	I²C-bus data input and output
SCL	16	I	I²C-bus clock input
SSM	17		master setting: Spread spectrum mode frequency slave setting: phase lock operation
OSCSET	18		master/slave oscillator setting master only setting: set internal oscillator frequency
OSCIO	19	I/O	external oscillator slave setting: input internal oscillator master setting: output
DCP	20	I	DC protection input for the filtered output voltages
VSTAB2	21		decoupling internal stabilizer 2 for DMOST drivers
OUT2N	22	O	channel 2 negative PWM output
BOOT2N	23		boot 2 negative bootstrap capacitor
V_{P2}[2]	24	P	channel 2 power supply voltage
PGND2	25	G	channel 2 power ground
BOOT2P	26		boot 2 positive bootstrap capacitor
OUT2P	27	O	channel 2 positive PWM output
OUT1P	28	O	channel 1 positive PWM output
BOOT1P	29		boot 1 positive bootstrap capacitor
PGND1	30	G	channel 1 power ground
V_{P1}[2]	31	P	channel 1 power supply voltage
BOOT1N	32		boot 1 negative bootstrap capacitor
OUT1N	33	O	channel 1 negative PWM output
VSTAB1	34		decoupling internal stabilizer 1 for DMOST drivers
V_{DDD}	35		decoupling of the internal 5 V logic supply
GNDD/HW	36	G	ground digital supply voltage handle wafer connection

[1] I = input, O = output, I/O = input/output, G = ground and P = power supply.

[2] In this data sheet supply voltage V_P describes V_{P1}, V_{P2} and V_{PA}.

8. Functional description

8.1 General

The TDF8599A is a dual full bridge (BTL) audio power amplifier using class-D technology. The audio input signal is converted into a Pulse-Width Modulated (PWM) signal using the analog input and PWM control stages. A PWM signal is applied to driver circuits for both high-side and low-side enabling the DMOS power output transistors to be driven. An external 2nd order low-pass filter converts the PWM signal into an analog audio signal across the loudspeakers.

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The TDF8599A includes integrated common circuits for all channels such as the oscillator, all reference sources, mode functionality and a digital timing manager. In addition, the built-in protection includes thermal foldback, temperature, overcurrent and overvoltage (load dump).

The TDF8599A operates in either I²C-bus mode or non-I²C-bus mode. In I²C-bus mode, DC load detection, frequency hopping and extended configuration functions are provided together with enhanced diagnostic information.

8.2 Mode selection

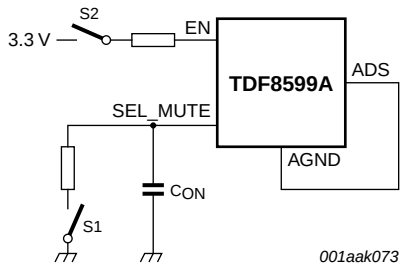
The mode pins EN, ADS and SEL_MUTE enable mute state, I²C-bus mode and Operating mode switching.

Pin SEL_MUTE is used to mute and unmute the device and must be connected to an external capacitor (C_{ON}). This capacitor generates a time constant which is used to ensure smooth fade-in and fade-out of the input signal.

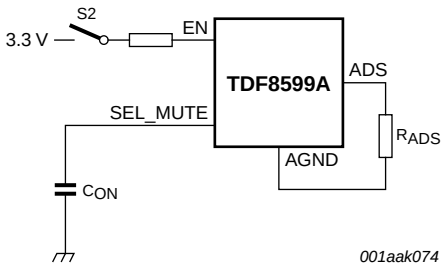
The TDF8599A is enabled when pin EN is HIGH. When pin EN is LOW, the TDF8599A is off and the supply current is at its lowest value (typically 2 μA). When off, the TDF8599A is completely deactivated and will not react to I²C-bus commands.

I²C-bus mode is selected by connecting a resistor between pins ADS and AGND. In I²C-bus mode with pin EN HIGH, the TDF8599A waits for further commands (see Table 4). I²C-bus mode is described in Section 9 on page 23.

Non-I²C-bus mode is selected by connecting pin ADS to pin AGND. In non-I²C-bus mode, the default TDF8599A state is Mute mode. The amplifiers switch idle (50 % duty cycle) and the audio signal is suppressed at the output. In addition, the capacitor (C_{SVRR}) is charged to half the supply voltage. To enter Operating mode, pin SEL_MUTE must be HGH with S1 open, enabling capacitor (C_{ON}) charged by an internal pull-up (see Figure 3). In addition, pin EN must be driven HIGH.



a. Non-I²C-bus mode



b. I²C-bus mode

See Table 13 for detailed information on R_{ADS}.

Fig 3. Mode selection

I²C-bus mode and non-I²C-bus mode control are described in Table 4 on page 7 and Table 5 on page 7. Switches S1 and S2 are shown in Figure 3.

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Table 4. I²C-bus mode operation

Pin EN	Pin SEL_MUTE	Bit IB1[D0]	Bit IB2[D0]	Mode
HIGH (S2 closed)	HIGH	1	0	Operating mode
	LOW	1	1	Mute mode
	LOW	0	X[1]	Standby mode
LOW (S2 open)	X[1]	X[1]	X[1]	off (default)

[1] X = do not care.

Table 5. Non-I²C-bus mode operation

Pin EN	Pin SEL_MUTE	Mode
HIGH (S2 closed)	HIGH (S1 open)	Operating mode
	LOW (S1 closed)	Mute mode (default)
LOW (S2 open)	X[1]	off

[1] X = do not care.

8.3 Pulse-width modulation frequency

The output signal from the amplifier is a PWM signal with a clock frequency of f_{osc}. This frequency is set by connecting a resistor (R_{osc}) between pins OSCSET and AGND. The optimal clock frequency setting is between 300 kHz and 400 kHz. Connecting a resistor with a value of 39 kΩ, for example, sets the clock frequency to 320 kHz (see Figure 5). The external capacitor (C_{osc}) has no influence on the oscillator frequency. It does however, reduce jitter and sensitivity to disturbance. Using a 2nd order LC demodulation filter in the application generates an analog audio signal across the loudspeaker.

8.3.1 Master and slave mode selection

In a master and slave configuration, multiple TDF8599A devices are daisy-chained together in one audio application with a single device providing the clock frequency signal for all other devices. In this situation, it is recommended that the oscillators of all devices are synchronized for optimum EMI behavior as follows:

All OSCIO pins are connected together and one TDF8599A in the application is configured as the clock-master. All other TDF8599A devices are configured as clock-slaves (see Figure 5).

- The clock-master pin OSCIO is configured as the oscillator output. When a resistor (R_{osc}) is connected between pins OSCSET and AGND, the TDF8599A is in Master mode.
- The clock-slave pins OSCIO are configured as the oscillator inputs. When pin OSCSET is directly connected to pin AGND (see Table 6), the TDF8599A is in Slave mode.

Table 6. Mode setting pin OSCIO

Mode	Settings	
	Pin OSCSET	Pin OSCIO
Master	R_{osc} > 26 kΩ	output
Slave	R_{osc} = 0 Ω; shorted to pin AGND	input

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The value of the resistor R_{osc} sets the clock frequency based on Equation 1:

$$f_{osc} = \frac{12.45 \times 10^9}{R_{osc}} [Hz] \quad (1)$$

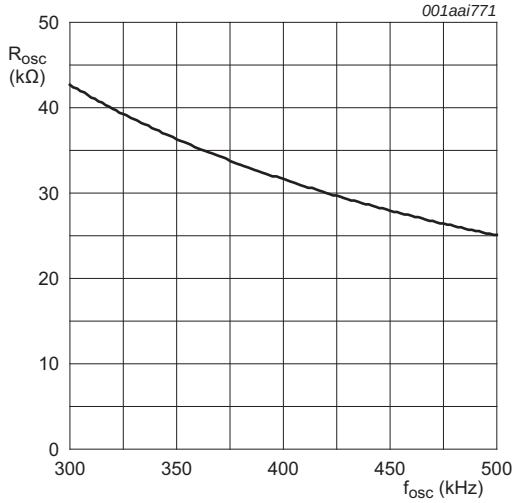

Fig 4. Clock frequency as a function of R_{osc}

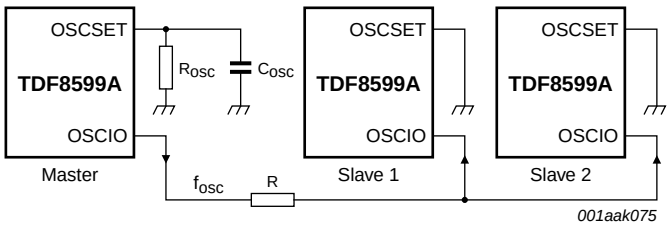

Fig 5. Master and slave configuration

In Master mode, Spread spectrum mode and frequency hopping can be enabled. In Slave mode, phase staggering and phase lock operation can be selected. An external clock can be used as the master-clock on pin OSCIO of the slave devices. When using an external clock, it must remain active during the shutdown sequence to ensure that all devices are switched off and able to enter the off state as described in Section 8.2 on page 6.

In Slave mode, an internal watchdog timer on pin OSCIO is triggered when the TDF8599A is switched off by pulling down pin EN. If the external clock fails, the watchdog timer forces the TDF8599A to switch off.

8.3.2 Spread spectrum mode (Master mode)

Spread spectrum mode is a technique of modulating the oscillator frequency with a slowly varying signal to broaden the switching spectrum, thereby reducing the spectral density of the EMI. Connecting a capacitor (C_{SSM}) to pin SSM enables Spread spectrum mode (see Figure 6). When pin SSM is connected to pin AGND, Spread spectrum mode is disabled.

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The capacitor on pin SSM (C_{SSM}) sets the spreading frequency when Spread spectrum mode is active. The current (I_{SSM}) flowing in and out of pin SSM is typically 5 μA. This gives a triangular voltage on pin SSM that sweeps around the voltage set by pin OSCSET ± 5 %. The voltage on pin SSM is used to modulate the oscillator frequency.

The spread spectrum frequency (f_{SSM}) can be calculated using Equation 2:

$$f_{SSM} = \frac{I_{SSM}}{2 \times C_{SSM} \times V_1 \times 10\ \%}[Hz] \quad (2)$$

where the voltage on pin OSCSET = V_1 and is calculated as 100 μA × R_{osc} (V) with I_{SSM} = 5 μA.

a. Off

b. On

Fig 6. Spread spectrum mode

The frequency swings between 0.95 × f_{osc} and 1.05 × f_{osc}; see Figure 7.

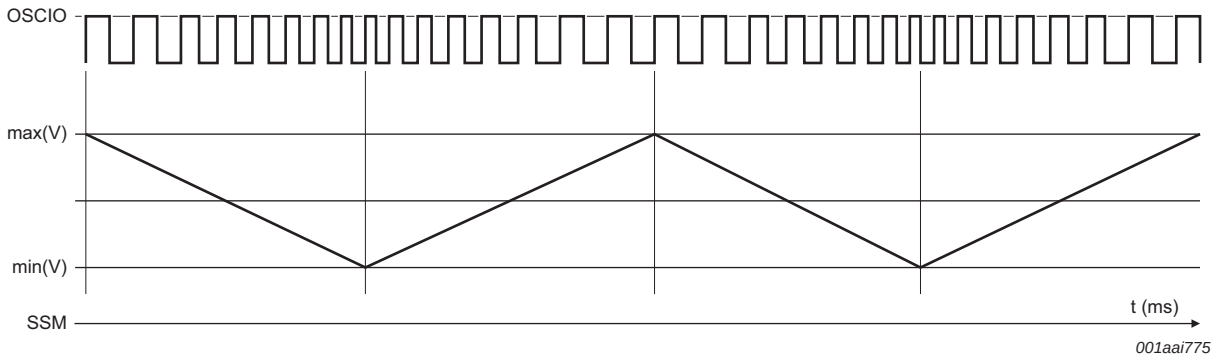

Fig 7. Spread spectrum operation in Master mode

8.3.3 Frequency hopping (Master mode)

Frequency hopping is a technique used to change the oscillator frequency for AM tuner compatibility. In Master mode, the resistor connected between pins OSCSET and AGND sets the oscillator frequency (f_{osc}). In I²C-bus mode, this frequency can be varied by ± 10 %. Set bit IB1[D4] to logic 1 and bit IB1[D3] to either logic 0 (0.9 × f_{osc}) or logic 1 (1.1 × f_{osc}).

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8.3.4 Phase lock operation (Slave mode)

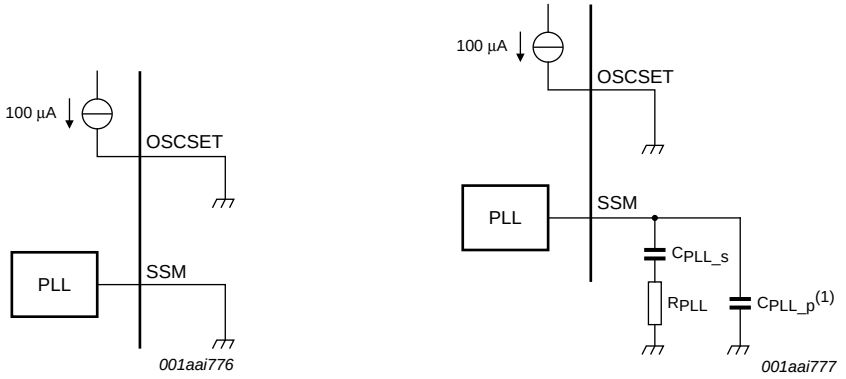
In Slave mode, Phase-Locked Loop (PLL) operation can be used to reduce the jitter effect of the external oscillator signal connected to pin OSCIO. Phase lock operation is also needed to enable phase staggering, see Section 8.4.2 on page 13. Phase lock operation is enabled when the oscillator is in Slave mode by connecting two capacitors (C_{PLL_s} and C_{PLL_p}) and a resistor (R_{PLL}) between pin SSM and pin AGND (see Figure 8). Connecting pin SSM to pin AGND disables phase lock operation and causes the slave to directly use the external oscillator signal. Values for C_{PLL_s}, C_{PLL_p} and R_{PLL} depend on the desired loop bandwidth (B_{PLL}) of the PLL. R_{PLL} is given by: $R_{PLL} = 8.4 \times B_{PLL}\ \Omega$. The corresponding values for C_{PLL_s} and C_{PLL_p} are given by Equation 3 and Equation 4:

$$C_{PLL_p} = \frac{0.032}{R_{PLL} \times B_{PLL}}[F] \quad (3)$$

Remark: C_{PLL_p} is only needed when ¼ π phase shift is selected. See Section 8.4.2 for more detailed information.

$$C_{PLL_s} = \frac{0.8}{R_{PLL} \times B_{PLL}}[F] \quad (4)$$

When pin OSCIO is connected to a clock-master with Spread spectrum mode enabled, the PLL loop bandwidth B_{PLL} should be $100 \times f_{SSM}$.



(1) Only needed when ¼ π phase shift is selected

a. Off

b. On

Fig 8. Phase lock operation

Table 7 lists all oscillator modes.

Table 7. Oscillator modes

OSCSET pin	OSCIO pin	SSM pin	Oscillator modes
R_{osc} > 26 kΩ	output	C_{SSM} to pin AGND	master, spread spectrum
R_{osc} > 26 kΩ	output	shorted to pin AGND	master, no spread spectrum
R_{osc} = 0 Ω	input	C_{PLL} + R_{PLL} to pin AGND	slave, PLL enabled
R_{osc} = 0 Ω	input	shorted to pin AGND	slave, PLL disabled

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8.4 Operation mode selection

Pin MOD is used to select specific operating modes. The resistor (R_{MOD}) connected between pins MOD and AGND together with the non-I²C-bus/I²C-bus mode determine the operating mode (see Table 8). The mode of operation depends on whether non-I²C-bus mode or I²C-bus mode is active. This in turn is determined by the resistor value connected between pins ADS and AGND.

In non-I²C-bus mode, pin MOD is used to select:

- AD or BD modulation (see Section 8.4.1).
- ½ π phase shift when oscillator is used in Slave mode (see Section 8.4.2).
- Parallel mode operation (see Section 8.4.3).

In I²C-bus mode, pin MOD can only select Parallel mode. In addition, the modulation mode and phase shift are programmed using I²C-bus commands.

Table 8. Operation mode selection with the MOD pin

R_{MOD} (kΩ)	I²C-bus mode[1]	Non-I²C-bus mode[2]
0 (short to AGND)	Stereo mode	AD modulation: no phase shift in Slave mode
4.7		BD modulation: no phase shift in Slave mode
13		AD modulation: ½ π phase shift in Slave mode
33	Parallel mode[3]	BD modulation: ½ π phase shift in Slave mode
100		AD modulation: no phase shift in Slave mode
∞ (open)		BD modulation: no phase shift in Slave mode

[1] $R_{ADS} \geq 4.7$ kΩ; See Table 13 on page 23.

[2] $R_{ADS} = 0$ Ω; pin ADS is short circuited to pin AGND.

[3] See Section 8.4.3 on page 14 for more detailed information.

In I²C-bus mode, pin MOD is latched using the I²C-bus command IB3[D7] = 1. This avoids amplifier switching interference generating incorrect information on pin MOD.

In non-I²C-bus mode or when IB3[D7] = 0, the information on pin MOD is latched when one of the TDF8599A's outputs starts switching.

8.4.1 Modulation mode

In non-I²C-bus mode, pin MOD is used to select either AD or BD modulation mode (see Table 8). In I²C-bus mode, the modulation mode is selected using an I²C-bus command.

- AD modulation mode: the bridge halves switch in opposite phase.
- BD modulation mode: the bridge halves switch in phase but the input signal for the modulators is inverted.

Figure 10 and Figure 11 show simplified representations of AD and BD modulation.

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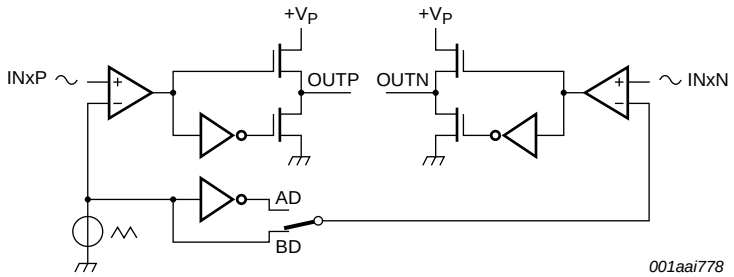
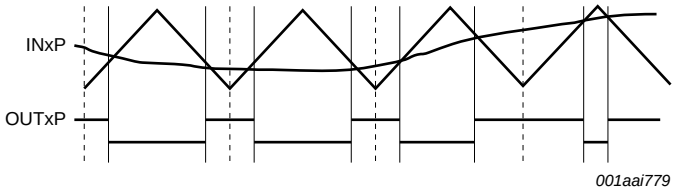
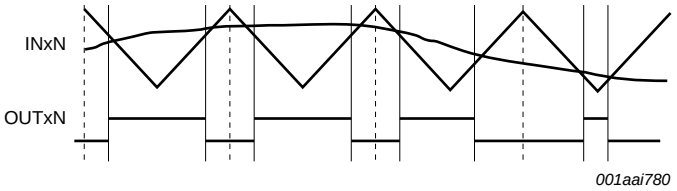


Fig 9. AD/BD modulation switching circuit



a. Bridge half 1.



b. Bridge half 2 switched in the opposite phase to bridge half 1.

Fig 10. AD modulation

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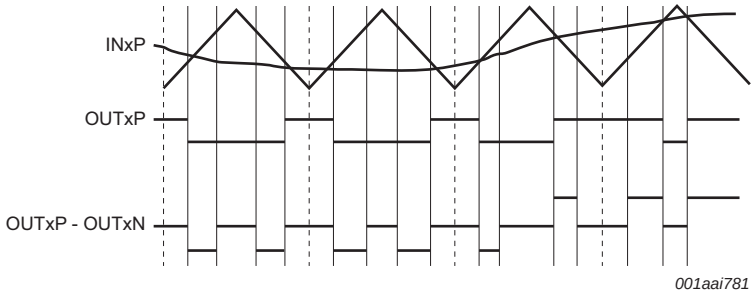
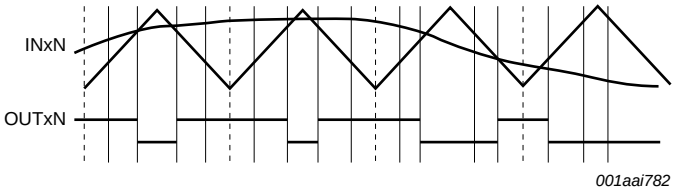


a. Phase switching cycle.



b. Inverted signal to the modulator.

Fig 11. BD modulation

8.4.2 Phase staggering (Slave mode)

In Slave mode with phase lock operation enabled, a phase shift with respect to the incoming clock signal can be selected to distribute the switching moments over time. In non-I²C-bus mode, ½ π phase shift can be programmed using pin MOD. In I²C-bus mode, five different phase shifts (¼ π, ⅓ π, ½ π, ⅔ π, ¾ π) can be selected using the I²C-bus bits (IB3[D1:D3]). See Table 8 for selection of the phase shift in non-I²C-bus mode with pin MOD. An additional capacitor must be connected to pin SSM when ¼ π phase shift is used (see Figure 8). An example of using ½ π phase shift for BD modulation is shown in Figure 12.

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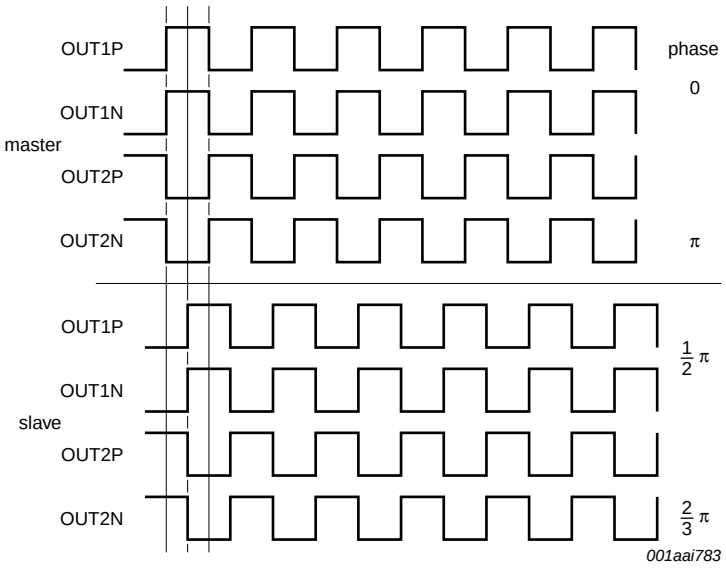

Fig 12. Master and slave operation with ½ π phase shift

8.4.3 Parallel mode

In Parallel mode; the two output stages operate in parallel to enlarge the drive capability. The inputs and outputs for Parallel mode must be connected on the Printed-Circuit Board (PCB) as shown in Figure 13. The parallel connection can be made after the output filter, as shown in Figure 13 or directly to the device output pins (OUTxP and OUTxN).

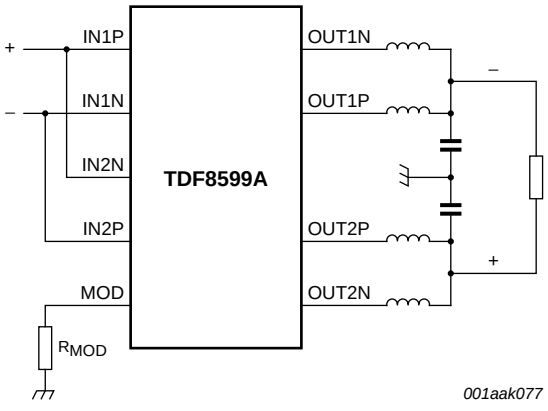

Fig 13. Parallel mode

In Parallel mode, the channel 1 I²C-bus bits can be programmed using the I²C-bus.

8.5 Protection

The TDF8599A includes a range of built-in protection functions. How the TDF8599A manages the various possible fault conditions for each protection is described in the following sections:

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Table 9. Overview of protection types

Protection type	Reference
Thermal foldback	Section 8.5.1
Overtemperature	Section 8.5.2
Overcurrent	Section 8.5.3
Window	Section 8.5.4
DC Offset	Section 8.5.5
Undervoltage	Section 8.5.6
Overvoltage	Section 8.5.6

8.5.1 Thermal foldback

Thermal Foldback Protection (TFP) is tripped when the average junction temperature exceeds the threshold level (145 °C). TFP decreases amplifier gain such that the combination of power dissipation and $R_{th(j-a)}$ create a junction temperature around the threshold level. The device will not completely switch off but remains operational at the lower output power levels. If the average junction temperature continues to increase, a second built-in temperature protection threshold level shuts down the amplifier completely.

8.5.2 Overtemperature protection

If the average junction temperature (T_j) > 160 °C, OverTemperature Protection (OTP) is tripped and the power stage shuts down immediately.

8.5.3 Overcurrent protection

OverCurrent Protection (OCP) is tripped when the output current exceeds the maximum output current of 8 A. OCP regulates the output voltage such that the maximum output current is limited to 8 A. The amplifier outputs keep switching and the amplifier is NOT shutdown completely. This is called current limiting.

OCP also detects when the loudspeaker terminals are short circuited or one of the amplifier's demodulated outputs is short circuited to one of the supply lines. In either case, the shorted channel(s) are switched off.

The amplifier can distinguish between loudspeaker impedance drops and a low-ohmic short across the load or one of the supply lines. This impedance threshold depends on the supply voltage used. When a short is made across the load causing the impedance to drop below the threshold level, the shorted channel(s) are switched off. They try to restart every 50 ms. If the short circuit condition is still present after 50 ms, the cycle repeats. The average power dissipation will be low because of this reduced duty cycle.

When a channel is switched off due to a short circuit on one of the supply lines, Window Protection (WP) is activated. WP ensures the amplifier does not start-up after 50 ms until the supply line short circuit is removed.

8.5.4 Window protection

Window Protection (WP) checks the PWM output voltage before switching from Standby mode to Mute mode (with both outputs switching) and is activated as follows:

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- During the start-up sequence:
  - When the TDF8599A is switched from standby to mute ($t_{d(stb\text{-}mute)}$). When a short circuit on one of the output terminals (i.e. between V_P or GND) is detected, the start-up procedure is interrupted and the TDF8599A waits for open circuit outputs. No large currents flow in the event of a short circuit to the supply lines because the check is performed before the power stages are enabled.
- During operation:
  - A short to one of the supply lines trips OCP causing the amplifier channel to shutdown. After 50 ms the amplifier channel restarts and WP is activated. However, the corresponding amplifier channel will not start-up until the supply line short circuit has been removed.

8.5.5 DC offset protection

DC Protection (DCP) is activated when the DC content in the demodulated output voltage exceeds a set threshold (typically 2 V). DCP is active in both Mute mode and Operating mode. Figure 14 shows how false triggering of the DCP by low frequencies in the audio signal is prevented using the external capacitor (C_F) to generate a cut-off frequency.

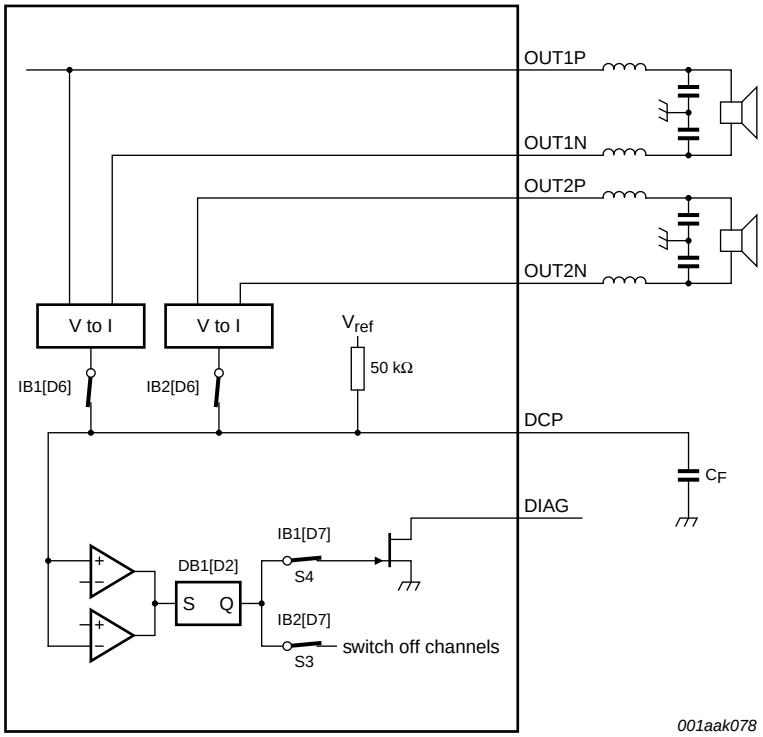

Fig 14. DC offset protection and diagnostic output

In I²C-bus mode, DC offsets generate a voltage shift around the bias voltage. When the voltage shift exceeds threshold values, the offset alarm bit DB1[D2] is set and if bit IB1[D7] is not set, diagnostic information is also given. Any detected offset shuts down both channels when bit IB2[D7] is not set. To restart the TDF8599A in I²C-bus mode, pin EN must be toggled or DCP disabled by connecting pin DCP to pin AGND.

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In non-I²C-bus mode, when an offset is detected, DCP always gives diagnostic information on pin DIAG and shuts down both channels.

Connecting a capacitor between pins DCP and AGND enables DC offset protection. Connecting pin DCP to pin AGND disables DCP in both I²C-bus and non-I²C-bus mode.

8.5.6 Supply voltages

UnderVoltage Protection (UVP) is activated when the supply voltage drops below the UVP threshold. UVP triggers the UVP circuit causing the system to first mute and then stop switching. When the supply voltage rises above the threshold level, the system restarts.

OverVoltage Protection (OVP) is activated when the supply voltage exceeds the OVP threshold. The OVP (or load dump) circuit is activated and the power stages are shutdown.

An overview of all protection circuits and the amplifier states is given in Table 10.

8.5.7 Overview of protection circuits and amplifier states

Table 10. Overview of TDF8599A protection circuits and amplifier states

Protection circuit name	Amplifier state		
	Complete shutdown	Channel shutdown	Restart[1]
TFP	N[2]	N[2]	Y[3]
OTP	Y	N	Y[3]
OCP	N	Y	Y[4]
WP	N	Y	Y
DCP	Y	N	N[5]
UVP	Y	N	Y[6]
OVP	Y	N	Y

[1] When fault is removed.

[2] Amplifier gain depends on the junction temperature and size of the heat sink.

[3] TFP influences restart timing depending on heat sink size.

[4] Shorted load causes a restart of the channel every 50 ms.

[5] Latched protection is reset by toggling pin EN or by disabling DCP in I²C-bus mode.

[6] In I²C-bus mode deep supply voltage drops will cause a Power-On Reset (POR). The restart requires an I²C-bus command.

8.6 Diagnostic output

8.6.1 Diagnostic table

The diagnostic information for I²C-bus mode and non-I²C-bus mode is shown in Table 11. The instruction bitmap and data bytes are described in Table 14 and Table 15.

Pins DIAG and CLIP have an open-drain output which must have an external pull-up resistor connected to an external voltage. Pins CLIP and DIAG can show both fixed and I²C-bus selectable information.

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Pin DIAG goes LOW when a short circuit to one of the amplifier outputs occurs. The microprocessor reads the failure information using the I²C-bus. The I²C-bus bits are set for a short circuit. These bits can be reset with the I²C-bus read command.

Even after the short has been removed, the microprocessor knows what was wrong after reading the I²C-bus. Old information is read when a single I²C-bus read command is used. To read the current information, two read commands must be sent, one after another.

When selected, pin DIAG gives the current diagnostic information. Pin DIAG is released instantly when the failure is removed, independent of the I²C-bus latches.

Table 11. Available data on pins DIAG and CLIP

Diagnostic	I²C-bus mode		Non-I²C-bus mode	
	Pin DIAG	Pin CLIP	Pin DIAG	Pin CLIP
Power-on reset	yes	yes	yes	yes
UVP or OVP	yes	no	yes	no
Clip detection	no	selectable	no	yes
Temperature pre-warning	no	selectable	no	yes
OCP/WP	yes	no	yes	no
DCP	selectable	no	yes	no
OTP	yes	no	yes	no

When OCP is triggered, the open-drain DIAG output is activated. The diagnostic output signal during different short circuit conditions is illustrated in Figure 15.

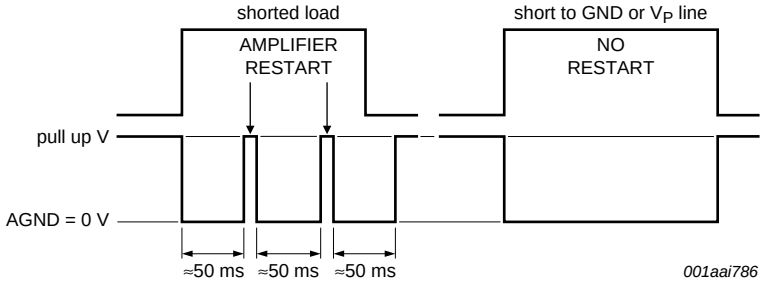

Fig 15. Diagnostic output for short circuit conditions

8.6.2 Load identification (I²C-bus mode only)

8.6.2.1 DC load detection

DC load detection is only available in I²C-bus mode and is controlled using bit IB2[D2]. The default setting is logic 0 for bit IB2[D2] which disables DC load detection. DC load detection is enabled when bit IB2[D2] = 1. Load detection takes place before the class-D amplifier output stage starts switching in Mute mode and the start-up time from Standby mode to Mute mode is increased by $t_{det(DCload)}$ (see Figure 16).

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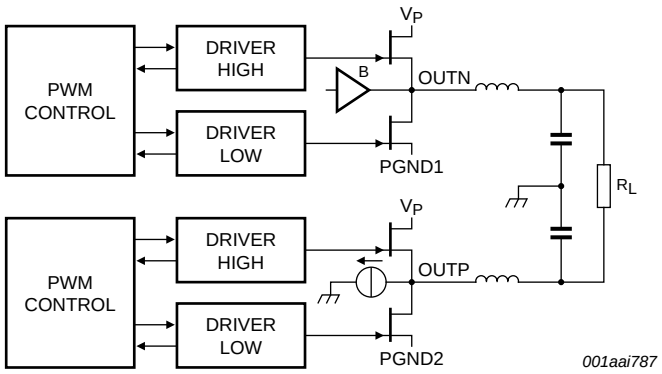

Fig 16. DC load detection circuit

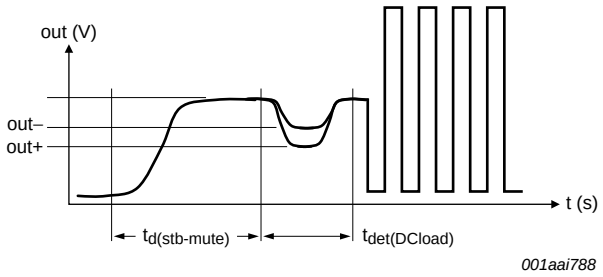

Fig 17. DC load detection procedure

The capacitor connected to pin SEL_MUTE (see Figure 3 on page 6) is used to create an inaudible current test pulse, drawn from the positive amplifier output. The diagnostic ‘speaker load’ (or ‘open load’), based on the voltage difference between pins OUTxP and OUTxN is shown in Figure 18.

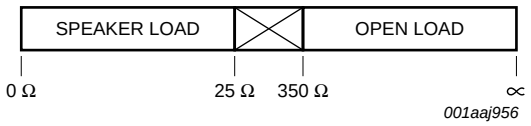

Fig 18. DC load detection limits

Remark: DC load detection identifies a short circuited speaker as a valid speaker load. OCP detection, using byte DB1[D3] for channel 1 and byte DB2[D3] for channel 2, performs diagnostics on shorted loads. However, the diagnostics are performed after the DC load detection cycle has finished and once the amplifier is in Operating mode.

The result of the DC load detection is stored in bits DB1[D4] and DB2[D4].

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Table 12. Interpretation of DC load detection bits

DC load bits DB1[D4] and DB2[D4]	OCP bits DB1[D3] and DB2[D3]	Description
0	0	speaker load
0	1	shorted load
1	0	open load

Remark: After DC load detection has been performed, the DC load valid bit DB1[D6] must be set. The DC load data bits are only valid when bit DB1[D6] = 1. When DC load detection is interrupted by a sudden large change in supply voltage (triggered by UVP or OVP) or if the amplifier hangs up, the DC load valid bit is reset to DB1[D6] = 0. The DC load detection enable bit IB2[D2] must be reset after the DC load protection cycle to release any amplifier hang-up. Once the DC load detection cycle has finished, DC load detection can be restarted by toggling the DC load detection enable bit IB2[D2]. However, this can only be used if both amplifier channels have not been enabled with bit IB1[D1] or bit IB2[D1]. See Section 8.6.2.2 “Recommended start-up sequence with DC load detection enabled” for detailed information.

8.6.2.2 Recommended start-up sequence with DC load detection enabled

The flow diagram (Figure 19) illustrates the TDF8599A’s ability to perform a DC load detection without starting the amplifiers. After a DC load detection cycle finishes without setting the DC load valid bit DB1[D6], DC load detection is repeated (when bit IB2[D2] is toggled).

To limit the maximum number of DC load detection cycle loops, a counter and limit have been added. The loop exits after the predefined number of cycles (COUNTMAX), if the DC load detection cycle finishes with an invalid detection.

Depending on the application needs, the invalid DC load detection cycle can be handled as follows:

- the amplifier can be started without DC load detection
- the DC load detection loop can be executed again

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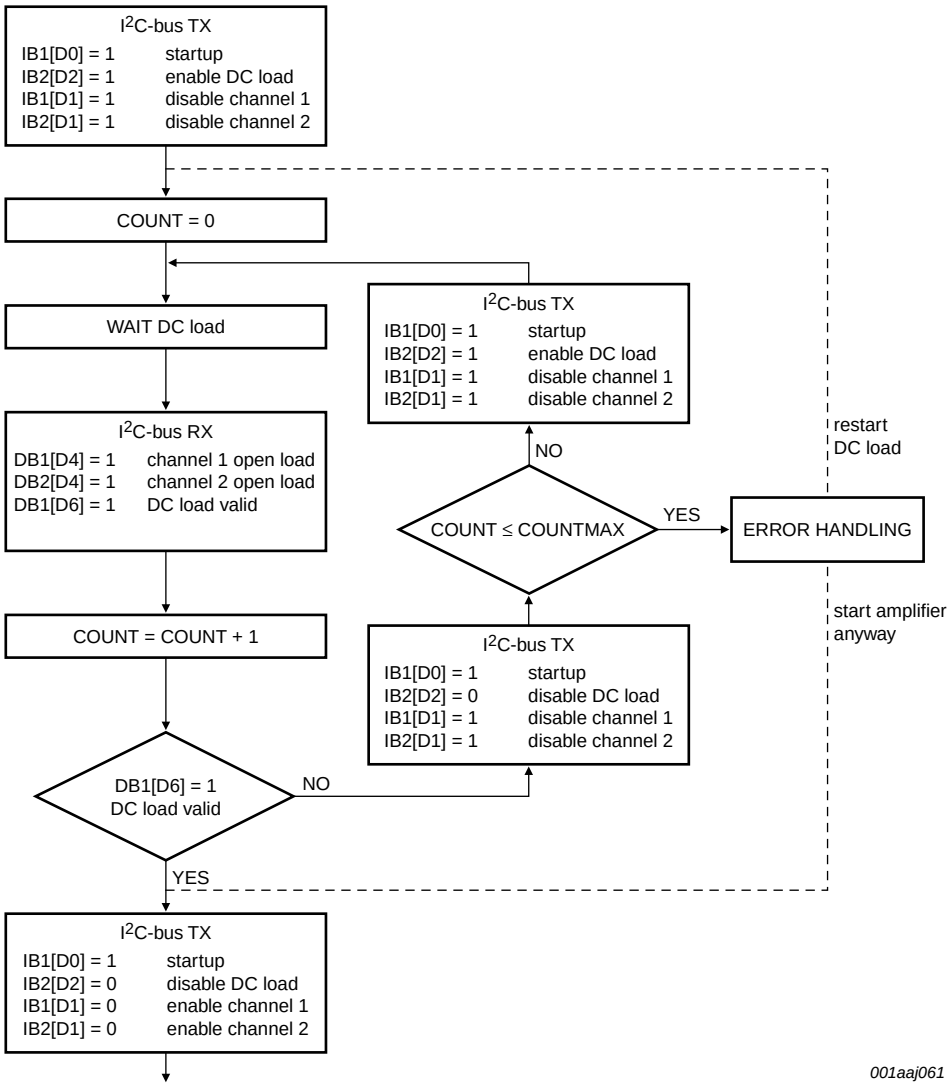

Fig 19. Recommended start-up sequence with DC load detection enabled

8.6.2.3 AC load detection

AC load detection is only available in I²C-bus mode and is controlled using bit IB3[D4]. The default setting for bit IB3[D4] = 0 disables AC load detection. When AC load detection is enabled (bit IB3[D4] = 1), the amplifier load current is measured and compared with a reference level. Pin CLIP is activated when this threshold is reached. Using this information, AC load detection can be performed using a predetermined input signal frequency and level. The frequency and signal level should be chosen so that the load current exceeds the programmed current threshold when the AC coupled load (tweeter) is present.

8.6.2.4 CLIP detection

CLIP detection gives information for clip levels ≥ 0.2 %. Pin CLIP is used as the output for the clip detection circuitry on both channel 1 and channel 2. Setting either bit IB1[D5] or bit IB2[D5] to logic 0 defines which channel reports clip information on the CLIP pin.

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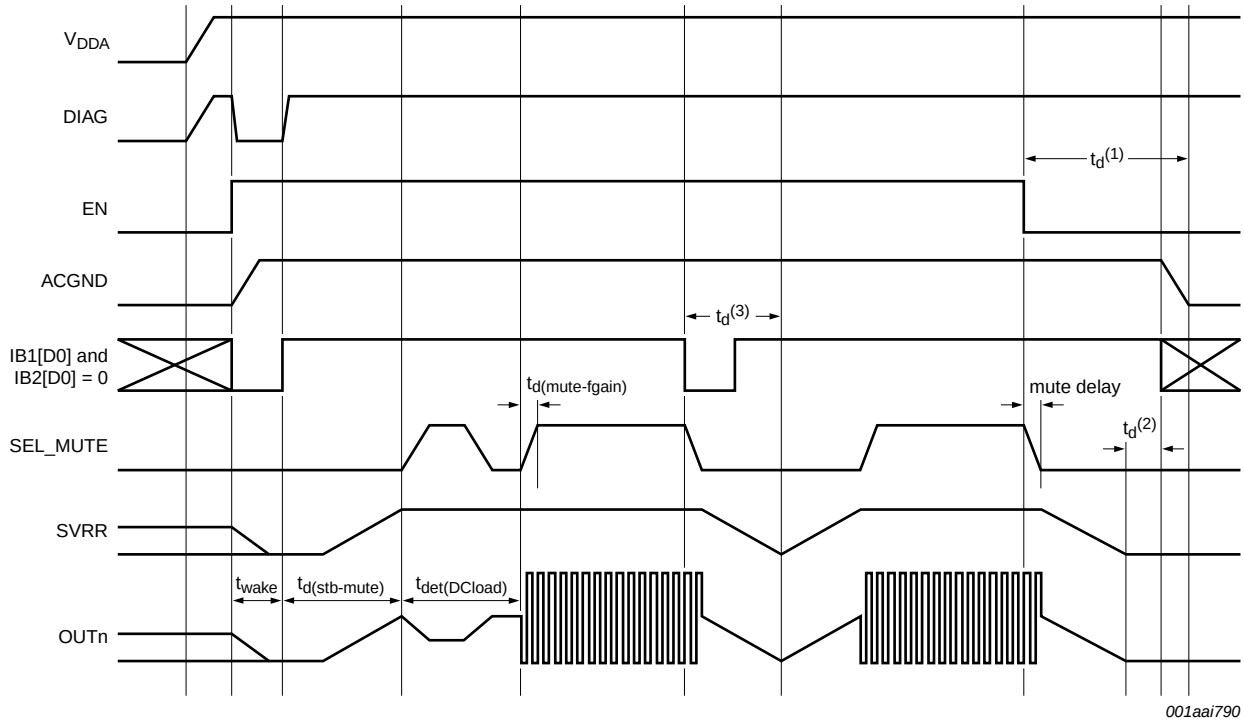
8.6.3 Start-up and shutdown sequence

To prevent switch on or switch off 'pop noises', a capacitor (C_{SVRR}) connected to pin SVRR is used to smooth start-up and shutdown. During start-up and shutdown, the output voltage tracks the voltage on pin SVRR. Increasing C_{SVRR} results in a longer start-up and shutdown time. Enhanced pop noise performance is achieved by muting the amplifier until the SVRR voltage reaches its final value and the outputs start switching. The capacitor value on pin SEL_MUTE (C_{ON}) determines the unmute and mute timing. The voltage on pin SEL_MUTE determines the amplifier gain. Increasing C_{ON} increases the unmute and mute times. In addition, a larger C_{ON} value increases the DC load detection cycle.

When the amplifier is switched off with an I²C-bus command or by pulling pin EN LOW, the amplifier is first muted and then capacitor (C_{SVRR}) is discharged.

In Slave mode, the device enters the off state immediately after capacitor (C_{SVRR}) is discharged. In Master mode, the clock is kept active by an additional delay ($t_d^{(2)}$) of approximately 50 ms to allow slave devices to enter the off state.

When an external clock is connected to pin OSCIO (in Slave mode), the clock must remain active during the shutdown sequence for delay ($t_d^{(1)}$) to ensure that the slaved TDF8599A devices are able to enter the off state.



(1) Shutdown hold delay.

(2) Master mode shutdown delay.

(3) Shutdown delay.

Fig 20. Start-up and shutdown timing in I²C-bus mode with DC load detection

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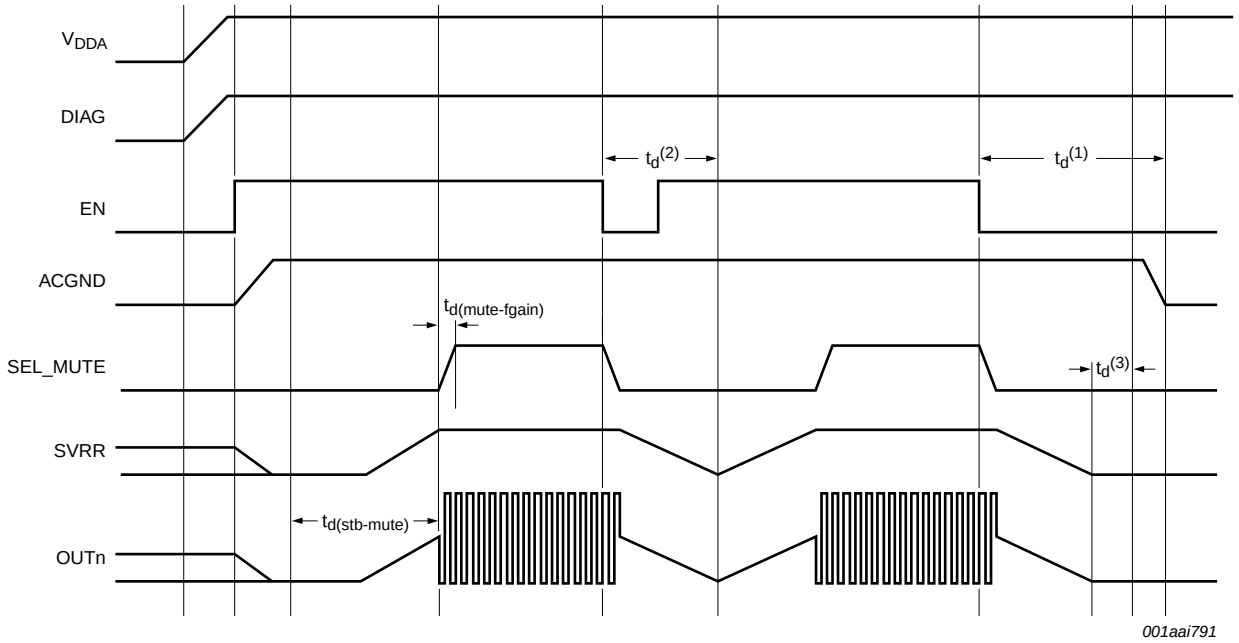

(1) Shutdown hold delay.

(2) Shutdown delay.

(3) Master mode shutdown delay.

Fig 21. Start-up and shutdown timing in non-I²C-bus mode

9. I²C-bus specification

TDF8599A address with hardware address select.

Table 13. I²C-bus write address selection using pins MOD and ADS

R_{ADS}[1] (kΩ)	R_{MOD}[1] (kΩ)						R/W
	Stereo mode			Parallel mode			
	0[2]	4.7	13	33	100	open	
Open	58h	68h	78h	58h	68h	78h	1 = Read from TDF8599A
100	56h	66h	76h	56h	66h	76h	0 = Write to TDF8599A
33	54h	64h	74h	54h	64h	74h	
13	52h	62h	72h	52h	62h	72h	
4.7	50h	60h	70h	50h	60h	70h	
0[2]	non-I²C-bus mode select						

[1] Required external resistor accuracy is 1 %.

[2] Short circuited to ground.

In I²C-bus mode, pins MOD and ADS can be latched using the I²C-bus command IB3[D7] = 1. This avoids disturbances from amplifier outputs of other TDF8599A devices in the same application switching and generating incorrect information on the MOD and ADS pins.

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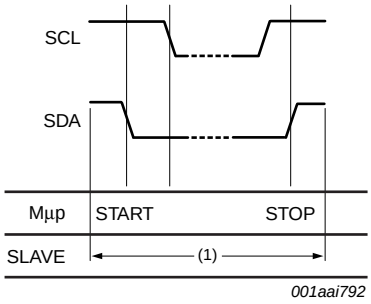
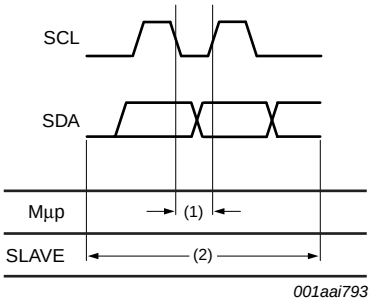
In non-I²C mode or when IB3[D7] = 0, the information on the MOD and ADS pins is latched when one of the TDF8599A's outputs starts switching.



(1) When SCL is HIGH, SDA changes to form the start or stop condition.

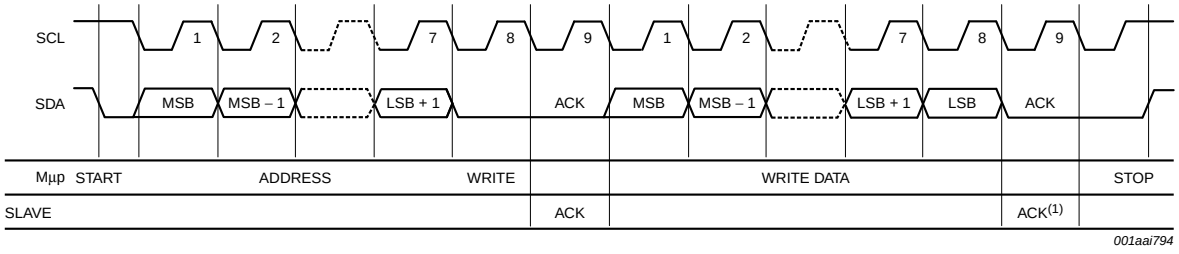
Fig 22. I²C-bus start and stop conditions



(1) SDA is allowed to change.

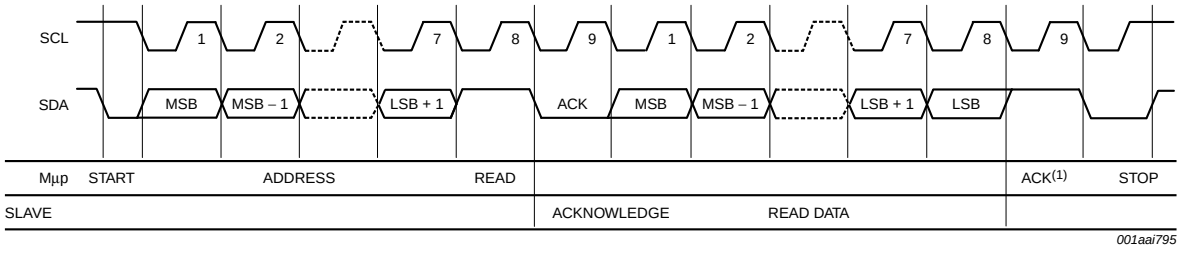
(2) All data bits must be valid on the positive edges of SCL.

Fig 23. Data bits sent from Master microprocessor (Mμp)



(1) To stop the transfer after the last acknowledge a stop condition must be generated.

Fig 24. I²C-bus write



(1) To stop the transfer, the last byte must not be acknowledged (SDA is HIGH) and a stop condition must be generated.

Fig 25. I²C-bus read

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9.1 Instruction bytes

If R/W bit = 0, the TDF8599A expects three instruction bytes: IB1, IB2 and IB3. After a power-on reset, all unspecified instruction bits must be set to zero.

Table 14. Instruction byte descriptions

Bit	Value	Description		
		Instruction byte IB1	**Instruction byte IB2**	**Instruction byte IB3**
D7	0	offset detection on pin DIAG	offset protection on	latch information on pins ADS and MOD when the amplifier starts switching
	1	no offset detection on pin DIAG	offset protection off	latch information on pins ADS and MOD; see Section 9 on page 23
D6	0	channel 1 offset monitoring on	channel 2 offset monitoring on	-
	1	channel 1 offset monitoring off	channel 2 offset monitoring off	-
D5	0	channel 1 clip detect on pin CLIP	channel 2 clip detect on pin CLIP	-
	1	channel 1 no clip detect on pin CLIP	channel 2 no clip detect on pin CLIP	-
D4	0	disable frequency hopping	thermal pre-warning on pin CLIP	disable AC load detection
	1	enable frequency hopping[1]	no thermal pre warning on pin CLIP	enable AC load detection
D3	0	oscillator frequency as set with R_{osc} − 10 %	temperature pre-warning at 140 °C	oscillator phase shift bits IB3[D3] to IB3[D1][2]
	1	oscillator frequency as set with R_{osc} + 10 %	temperature pre-warning at 120 °C	
D2	0	-	DC-load detection disabled	
	1	-	DC-load detection enabled	
D1	0	channel 1 enabled	channel 2 enabled	
	1	channel 1 disabled	channel 2 disabled	
D0	0	TDF8599A in Standby mode	all channels operating	AD modulation
	1	TDF8599A in Mute or Operating modes[3]	all channels muted	BD modulation

[1] See Section 8.3.3 on page 9 for information on IB1[D4] and IB1[D3].

[2] See Table 15 “Phase shift bit settings” for information on IB3[D3] to IB3[D1].

[3] See Table 4 for information on IB1[D0] and IB2[D0].

Table 15. Phase shift bit settings

D3	D2	D1	Phase
0	0	0	0
0	0	1	$\frac{1}{4}\pi$
0	1	0	$\frac{1}{3}\pi$
0	1	1	$\frac{1}{2}\pi$
1	0	0	$\frac{2}{3}\pi$
1	0	1	$\frac{3}{4}\pi$

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9.2 Data bytes

If R/W = 1, the TDF8599A sends two data bytes to the microprocessor (DB1 and DB2). All short diagnostic and offset protection bits are latched. In addition, all bits are reset after a read operation except the DC load detection bits (DBx[D4], DB1[D6]). The default setting for all bits is logic 0.

In Parallel mode, the diagnostic information is stored in byte DB1.

Table 16. Description of data bytes

Bit	Value	DB1 channel 1	DB2 channel 2
D7	0	at least 1 instruction bit set to logic 1	below maximum temperature
	1	all instruction bits are set to logic 0	maximum temperature protection activated
D6	0	invalid DC load data	no temperature warning
	1	valid DC load data	temperature pre-warning active
D5	0	no overvoltage	no undervoltage
	1	overvoltage protection active	undervoltage protection active
D4	0	speaker load channel 1	speaker load channel 2
	1	open load channel 1	open load channel 2
D3	0	no shorted load channel 1	no shorted load channel 2
	1	shorted load channel 1	shorted load channel 2
D2	0	no offset	reserved
	1	offset detected	reserved
D1	0	no short to V_P channel 1	no short to V_P channel 2
	1	short to V_P channel 1	short to V_P channel 2
D0	0	no short to ground channel 1	no short to ground channel 2
	1	short to ground channel 1	short to ground channel 2

Data byte DB1[D7] indicates whether the instruction bits have been set to logic 0. In principle, DB1[D7] is set after a POR or when all the instruction bits are programmed to logic 0. Pin DIAG is driven HIGH when bit DB1[D7] = 1.

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10. Limiting values

Table 17. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage	Operating mode		-	40	V
		off state	[1]	–1	+50	V
		load dump; duration 50 ms; t_r > 2.5 ms		-	50	V
I_{ORM}	repetitive peak output current	maximum output current limiting	[2]	8	-	A
I_{OM}	peak output current	maximum; non-repetitive				
		stereo mode		-	18	A
		parallel mode		-	12	A
V_i	input voltage	pins SCL, SDA, ADS, MOD, SSM, OSCIO, EN and SEL_MUTE		0	5.5	V
		pins IN1N, IN1P, IN2N and IN2P		0	10	V
V_o	output voltage	pins DIAG and CLIP		0	10	V
R_{ESR}	equivalent series resistance	as seen between pins V_P and PGNDn		-	350	mΩ
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
V_{ESD}	electrostatic discharge voltage	HBM	[3]			
		C = 100 pF; R_S = 1.5 kΩ		-	2000	V
		CDM	[4]			
		non-corner pins		-	500	V
		corner pins		-	750	V
$V_{(prot)}$	protection voltage	AC and DC short circuit voltage of output pins across load and to supply and ground	[5]	0	V_P	V

[1] Floating condition assumed for outputs.

[2] Current limiting concept.

[3] Human Body Model (HBM).

[4] Charged-Device Model (CDM).

[5] The output pins are defined as the output pins of the filter connected between the TDF8599A output pins and the load.

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11. Thermal characteristics

Table 18. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	35	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		1	K/W

12. Static characteristics

Table 19. Static characteristics

$V_P = V_{DDA}$ = 14.4 V; f_{osc} = 320 kHz; −40 °C < T_{amb} < +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	supply voltage			8	14.4	35	V
I_P	supply current	off state; $T_j \leq 85$ °C; V_P = 14.4 V		-	2	10	µA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, snubbers and filter connected		-	90	120	mA
Series resistance output switches							
R_{DSon}	drain-source on-state resistance	power switch;					
		T_j = 25 °C		-	170	180	mΩ
		T_j = 100 °C		-	235	250	mΩ
I²C-bus interface: pins SCL and SDA							
V_{IL}	LOW-level input voltage			0	-	1.5	V
V_{IH}	HIGH-level input voltage			2.3	-	5.5	V
V_{OL}	LOW-level output voltage	pin SDA; I_{load} = 5 mA		0	-	0.4	V
Address, phase shift and modulation mode select: pins ADS and MOD							
V_i	input voltage	pins not connected	[1]	1.5	2	2.7	V
I_i	input current	pins shorted to GND	[1]	80	105	160	µA
Enable and SEL_MUTE input: pins EN and SEL_MUTE							
V_i	input voltage	pin EN; off state		0	-	0.8	V
		pin EN; Standby mode; I²C-bus mode		2	-	5	V
		pin EN; Mute mode or Operating mode; non-I²C-bus mode		2	-	5	V
		pin SEL_MUTE; Mute mode; voltage on pin EN > 2 V		0	-	0.8	V
		pin SEL_MUTE; Operating mode; voltage on pin EN > 2 V		3	-	5	V
I_i	input current	pin EN; 2.5 V		-	-	5	µA
		pin SEL_MUTE; Operating mode; 0.8 V		-	-	50	µA

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Table 19. Static characteristics *...continued*

$V_P = V_{DDA} = 14.4$ V; $f_{osc} = 320$ kHz; -40 °C < T_{amb} < $+85$ °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Diagnostic output							
THD_{clip}	total harmonic distortion clip detection level			-	0.2	-	%
$V_{th(offset)}$	threshold voltage for offset detection		[2][3]	1	2	3	V
V_{OL}	LOW-level output voltage	DIAG or CLIP pins activated; I_o = 1 mA		-	-	0.3	V
I_L	leakage current	DIAG and CLIP pins; diagnostic not activated		-	-	50	μA
Audio inputs; pins IN1N, IN1P, IN2N and IN2P							
V_i	input voltage			-	2.45	-	V
SVRR voltage and ACGND input bias voltage in Mute and Operating modes							
V_{ref}	reference voltage	input ACGND pin		2	2.45	3	V
		half supply reference SVRR pin		6.9	7.2	7.5	V
Amplifier outputs; pins OUT1N, OUT1P, OUT2N and OUT2P							
$V_{O(offset)}$	output offset voltage	BTL; Mute mode		-	-	25	mV
		BTL; Operating mode	[4][6]	-	-	70	mV
Stabilizer output; pins VSTAB1 and VSTAB2							
V_o	output voltage	stabilizer output in Mute mode and Operating mode		8	10	12	V
Voltage protections							
$V_{(prot)}$	protection voltage	undervoltage; amplifier is muted		6.8	7.2	8	V
		overvoltage; load dump protection is activated		37	38	-	V
		V_P that a POR occurs at		3	3.7	4.6	V
Current protection							
$I_{O(ocp)}$	overcurrent protection output current	current limiting concept		8	9.5	11	A
Temperature protection							
T_{prot}	protection temperature			155	-	160	°C
$T_{act(th_fold)}$	thermal foldback activation temperature	gain = −1 dB		140	-	150	°C
$T_{j(AV)(warn1)}$	average junction temperature for pre-warning 1	IB2[D3] = 0; non-I²C-bus mode		-	140	150	°C
$T_{j(AV)(warn2)}$	average junction temperature for pre-warning 2	IB2[D3] = 1		-	120	130	°C
DC load detection levels: I²C-bus mode only[7]							
$Z_{th(load)}$	load detection threshold impedance	for normal speaker load; DB1[D4] = 0; DB2[D4] = 0		-	-	25	Ω
$Z_{th(open)}$	open load detection threshold impedance	DB1[D4] = 1; DB2[D4] = 1		350	-	-	Ω
AC load detection levels: I²C-bus mode only							
$I_{th(o)det(load)AC}$	AC load detection output threshold current			250	500	700	mA

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Table 19. Static characteristics *...continued*

$V_P = V_{DDA} = 14.4$ V; $f_{osc} = 320$ kHz; −40 °C < T_{amb} < +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Start-up/shut-down/mute timing							
t_{wake}	wake-up time	on pin EN before first I²C-bus transmission is recognized	[5]	-	-	500	µs
$t_{det(DCload)}$	DC load detection time	C_{ON} = 470 nF	[5]	-	380	-	ms
$t_{d(stb-mute)}$	delay time from standby to mute	measured from amplifier enabling to start of unmute (no DC load detection); C_{SVRR} = 47 µF C_{ON} = 470 nF		-	140	-	ms
$t_{d(mute-fgain)}$	mute to full gain delay time	C_{ON} = 470 nF	[6]	-	15	-	ms
t_d	delay time	shutdown delay time from EN pin LOW to SVRR LOW; voltage on pin SVRR < 0.1 V; C_{SVRR} = 47 µF		200	350	550	ms
		shutdown delay time from EN pin LOW to SVRR LOW; voltage on pin SVRR < 0.1 V; C_{SVRR} = 47 µF; V_P = 35 V		300	400	700	ms
		shutdown hold delay time from pin EN LOW to ACGND LOW; voltage on pin ACGND < 0.1 V; Master mode		-	370	-	ms
		hold delay in Master mode to allow slaved devices to shutdown f_{osc} = 320 kHz		-	50	-	ms
Speaker load impedance							
R_L	load resistance	at supply voltage equal to or below 25 V					
		stereo mode		1.6	4	-	Ω
		parallel mode		0.8	-	-	Ω
		at supply voltage equal to or below 35 V					
		stereo mode		3.2	4	-	Ω
		parallel mode		1.6	-	-	Ω

[1] Required resistor accuracy for pins ADS and MOD is 1 %; see Section 9 on page 23.

[2] Maximum leakage current from DCP pin to ground = 3 µA.

[3] The output offset values can be either positive or negative. The $V_{th(offset)}$ limit values (excluding Typ) are the valid absolute values.

[4] DC output offset voltage is applied to the output gradually during the transition between Mute mode and Operating mode.

[5] I²C-bus mode only.

[6] The transition time between Mute mode and Operating mode is determined by the time constant on the SEL_MUTE pin.

[7] The DC load valid bit DB1[D6] must be used; Section 8.6.2.1 on page 18. The DC load enable bit IB2[D2] must be reset after each load detection cycle to prevent amplifier hang-up incidents.

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12.1 Switching characteristics

Table 20. Switching characteristics

$V_P = V_{DDA}$ = 14.4 V; −40 °C < T_{amb} < +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal oscillator						
f_{osc}	oscillator frequency	external clock frequency; R_{osc} = 39 kΩ	-	320	-	kHz
		internal fixed frequency and Spread spectrum mode frequency based on the resistor value connected to pin OSCSET for the master setting	300	-	450	kHz
Master/slave setting (OSCIO pin)						
R_{osc}	oscillator resistance	resistor value on pin OSCSET; master setting	26	39	49	kΩ
V_{OL}	LOW-level output voltage	output	-	-	0.8	V
V_{OH}	HIGH-level output voltage	output	4	-	-	V
V_{IL}	LOW-level input voltage	input	-	-	0.8	V
V_{IH}	HIGH-level input voltage	input	4	-	-	V
f_{track}	tracking frequency	PLL enabled	300	-	500	kHz
N_{slave}	number of slaves	driven by one master	12	-	-	
Spread spectrum mode setting						
Δf_{osc}	oscillator frequency variation	between maximum and minimum values; Spread spectrum mode activated	-	10	-	%
f_{sw}	switching frequency	Spread spectrum mode activated; C_{SSM} = 1 μF	-	7	-	Hz
Frequency hopping						
$f_{osc(int)}$	internal oscillator frequency	change positive; IB1[D4] = 1; IB1[D3] = 1	-	f_{osc} + 10 %	-	kHz
		change negative; IB1[D4] = 1; IB1[D3] = 0	-	f_{osc} − 10 %	-	kHz
Timing						
t_r	rise time	PWM output; I_o = 0 A	-	10	-	ns
t_f	fall time	PWM output; I_o = 0 A	-	10	-	ns
$t_{w(min)}$	minimum pulse width	I_o = 0 A	-	80	-	ns

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13. Dynamic characteristics

Table 21. Dynamic characteristics

$V_P = V_{DDA}$ = 14.4 V; R_L = 4 Ω; f_i = 1 kHz; f_{osc} = 320 kHz; $R_{s(L)}$ < 0.04 Ω [1]; −40 °C < T_{amb} < +85 °C; Stereo mode; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	Stereo mode:	[2]				
		V_P = 14.4 V; THD = 1 %; R_L = 4 Ω		18	20	-	W
		V_P = 14.4 V; THD = 10 %; R_L = 4 Ω		23	25	-	W
		square wave (EIAJ); R_L = 4 Ω		-	40	-	W
		V_P = 35 V; THD = 10 %; R_L = 4 Ω		-	135	-	W
		V_P = 14.4 V; THD = 1 %; R_L = 2 Ω		26	29	-	W
		V_P = 14.4 V; THD = 10 %; R_L = 2 Ω		34	38	-	W
		square wave (EIAJ); R_L = 2 Ω		-	60	-	W
		Parallel mode:	[2]				
		V_P = 14.4 V; THD = 10 %; R_L = 2 Ω		-	50	-	W
		V_P = 35 V; THD = 10 %; R_L = 2 Ω		-	250	-	W
		V_P = 25 V; THD = 1 %; R_L = 1 Ω		135	150	-	W
THD	total harmonic distortion	f_i = 1 kHz; P_o = 1 W	[3]	-	0.02	0.1	%
		f_i = 10 kHz; P_o = 1 W	[3]	-	0.02	0.1	%
$G_{v(cl)}$	closed-loop voltage gain			25	26	27	dB
α_{cs}	channel separation	f_i = 1 kHz; P_o = 1 W		-	70	-	dB
SVRR	supply voltage rejection ratio	Operating mode					
		f_{ripple} = 100 Hz	[4]	60	70	-	dB
		f_{ripple} = 1 kHz	[4]	60	70	-	dB
		Mute mode					
		f_{ripple} = 1 kHz	[4]	60	70	-	dB
		off state and Standby mode					
		f_{ripple} = 1 kHz	[4]	-	90	-	dB
$\lvert Z_{i(dif)} \rvert$	differential input impedance			60	100	150	kΩ
$V_{n(o)}$	output noise voltage	Operating mode					
		BD mode	[5]	-	60	77	μV
		AD mode	[5]	-	100	140	μV
		Mute mode					
		BD mode	[6]	-	25	32	μV
		AD mode	[6]	-	85	110	μV
$\alpha_{bal(ch)}$	channel balance			-	0	1	dB
α_{mute}	mute attenuation		[7]	66	-	-	dB
CMRR	common mode rejection ratio	$V_{i(cm)}$ = 1 V RMS		65	80	-	dB
η_{po}	output power efficiency	P_o = 20 W		-	90	-	%

[1] $R_{s(L)}$ is the sum of the inductor series resistance from the low-pass LC filter in the application together with all resistance from PCB traces or wiring between the output pin of the TDF8599A and the inductor to the measurement point. LC filter dimensioning is L = 10 μH, C = 1 μF for 4 Ω load and L = 5 μH, C = 2.2 μF for 2 Ω load.

[2] Output power is measured indirectly based on R_{DSon} measurement.

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[3] Total harmonic distortion is measured at the bandwidth of 22 Hz to 20 kHz, AES brick wall. The maximum limit is guaranteed but may not be 100 % tested.

[4] $V_{ripple} = V_{ripple(max)} = 2$ V (p-p); $R_s = 0\ \Omega$.

[5] B = 22 Hz to 20 kHz, AES brick wall, $R_s = 0\ \Omega$.

[6] B = 22 Hz to 20 kHz, AES brick wall, independent of R_s.

[7] $V_i = V_{i(max)} = 0.5$ V RMS.

14. Application information

14.1 Output power estimation (Stereo mode)

The output power, just before clipping, can be estimated using Equation 5:

$$P_o = \frac{\left(\left(\frac{R_L}{R_L + 2 \times (R_{DSon} + R_s)}\right) \times \left(1 - t_{w(min)} \times \frac{f_{osc}}{2}\right) \times V_P\right)^2}{2 \times R_L}[W] \quad (5)$$

Where,

- V_P = supply voltage (V)
- R_L = load impedance (Ω)
- R_{DSon} = drain source on-state resistance (Ω)
- R_S = series resistance of the output inductor (Ω)
- $t_{w(min)}$ = minimum pulse width(s) depending on output current (s)
- f_{osc} = oscillator frequency in Hz (typically 320 kHz)

The output power at 10 % THD can be estimated by: $P_{o(2)} = 1.25 \times P_{o(1)}$ where $P_{o(1)}$ = 0.5 % and $P_{o(2)}$ = 10 %.

Figure 26 and Figure 27 show the estimated output power at THD = 0.5 % and THD = 10 % as a function of supply voltage for different load impedances in stereo mode.

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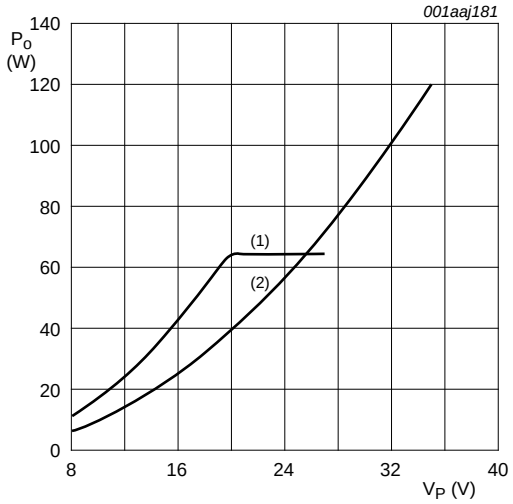


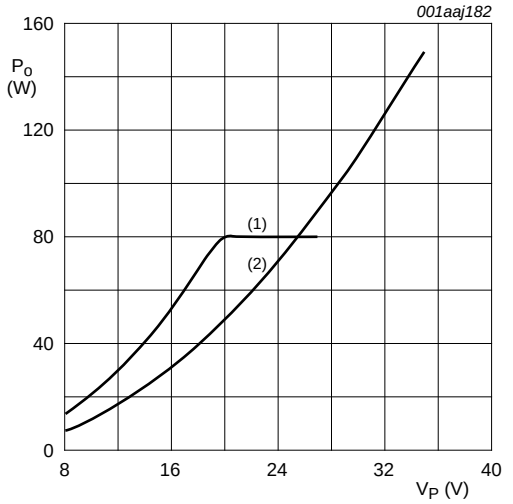
THD = 0.5 %.

R_{DSon} = 0.2 Ω (at T_j = 100 °C), R_s = 0.05 Ω, $t_{w(min)}$ = 190 ns and $I_{O(ocp)}$ = 8 A (minimum).

(1) R_L = 2 Ω.

(2) R_L = 4 Ω.

Fig 26. P_o as a function of V_P in stereo mode with THD = 0.5 %



THD = 10 %.

R_{DSon} = 0.2 Ω (at T_j = 100 °C), R_s = 0.05 Ω, $t_{w(min)}$ = 190 ns and $I_{O(ocp)}$ = 8 A (minimum).

(1) R_L = 2 Ω.

(2) R_L = 4 Ω.

Fig 27. P_o as a function of V_P in stereo mode with THD = 10 %

14.2 Output power estimation (Parallel mode)

Figure 28 and Figure 29 show the estimated output power at THD = 0.5 % and THD = 10 % as a function of the supply voltage for different load impedances in parallel mode.

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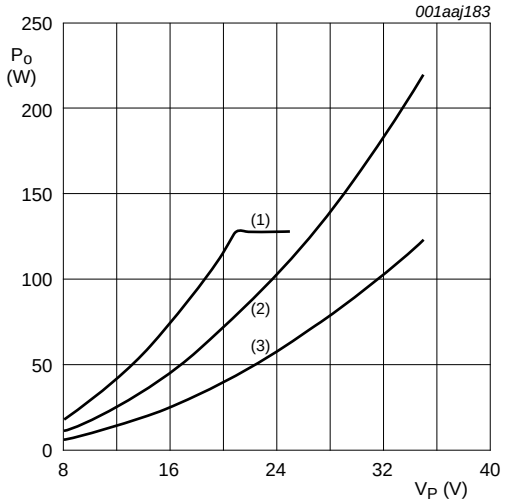


THD = 0.5 %.

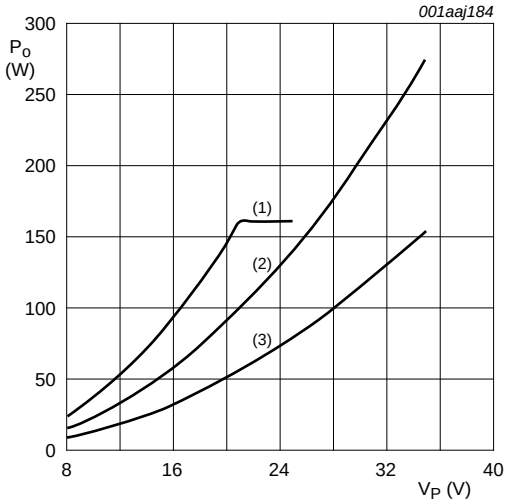
R_{DSon} = 0.1 Ω (at T_j = 100 °C), R_s = 0.025 Ω, $t_{w(min)}$ = 190 ns and $I_{O(ocp)}$ = 16 A (minimum).

(1) R_L = 1 Ω.

(2) R_L = 2 Ω.

(3) R_L = 4 Ω.

Fig 28. P_o as a function of V_P in parallel mode with THD = 0.5 %



THD = 10 %.

R_{DSon} = 0.1 Ω (at T_j = 100 °C), R_s = 0.025 Ω, $t_{w(min)}$ = 190 ns and $I_{O(ocp)}$ = 16 A (minimum).

(1) R_L = 1 Ω.

(2) R_L = 2 Ω.

(3) R_L = 4 Ω.

Fig 29. P_o as a function of V_P parallel mode with THD = 10 %

14.3 Output current limiting

The peak output current is internally limited to 8 A maximum. During normal operation, the output current should not exceed this threshold level otherwise the output signal will be distorted. The peak output current can be estimated using Equation 6:

$$I_o \leq \frac{V_P}{R_L + 2 \times (R_{DSon} + R_s)} \leq 8\ [A] \quad (6)$$

- I_o = output current (A)
- V_P = supply voltage (V)
- R_L = load impedance (Ω)
- R_{DSon} = on-resistance of power switch (Ω)
- R_s = series resistance of output inductor (Ω)

Example: A 2 Ω speaker can be used with a supply voltage of 19 V before current limiting is triggered.

Current limiting (clipping) avoids audio holes but can cause distortion similar to voltage clipping. In Parallel mode, the output current is internally limited above 16 A.

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14.4 Speaker configuration and impedance

A flat-frequency response (due to a 2nd order Butterworth filter) is obtained by changing the low-pass filter components (L_{LC}, C_{LC}) based on the speaker configuration and impedance. Table 22 shows the required values.

Table 22. Filter component values

Load impedance (Ω)	L_{LC} (µH)	C_{LC} (µF)
1	2.5	4.4
2	5	2.2
4	10	1

Remark: When using a 1 Ω load impedance in Parallel mode, the outputs are shorted after the low-pass filter switches two 2 Ω filters in parallel.

14.5 Heat sink requirements

In most applications, it is necessary to connect an external heat sink to the TDF8599A. Thermal foldback activates at T_j = 140 °C. The expression below shows the relationship between the maximum power dissipation before activation of thermal foldback and the total thermal resistance from junction to ambient:

$$R_{th(j\text{-}a)} = \frac{T_{j(max)} - T_{amb}}{P_{max}} [\mathrm{K/W}] \quad (7)$$

P_{max} is determined by the efficiency (η) of the TDF8599A. The efficiency measured as a function of output power is given in Figure 43. The power dissipation can be derived as a function of output power (see Figure 42).

Example 1:

- V_P = 14.4 V
- P_o = 2 × 25 W into 4 Ω (THD = 10 % continuous)
- $T_{j(max)}$ = 140 °C
- T_{amb} = 25 °C
- P_{max} = 5.8 W (from Figure 42)
- The required $R_{th(j\text{-}a)}$ = 115 °C / 5.8 W = 19 K/W

The total thermal resistance $R_{th(j\text{-}a)}$ consists of: $R_{th(j\text{-}c)}$ + $R_{th(c\text{-}h)}$ + $R_{th(h\text{-}a)}$

Where:

- Thermal resistance from junction to case ($R_{th(j\text{-}c)}$) = 1 K/W
- Thermal resistance from case to heat sink ($R_{th(c\text{-}h)}$) = 0.5 K/W to 1 K/W (depending on mounting)
- Thermal resistance from heat sink to ambient ($R_{th(h\text{-}a)}$) would then be 19 − (1 + 1) = 17 K/W.

If an audio signal has a crest factor of 10 (the ratio between peak power and average power = 10 dB) then T_j will be much lower.

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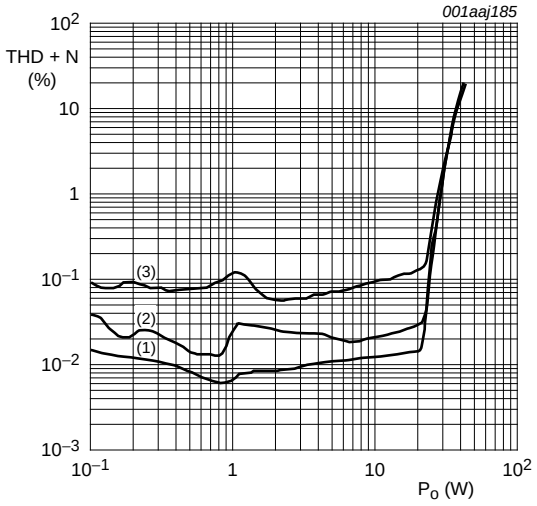
Example 2:

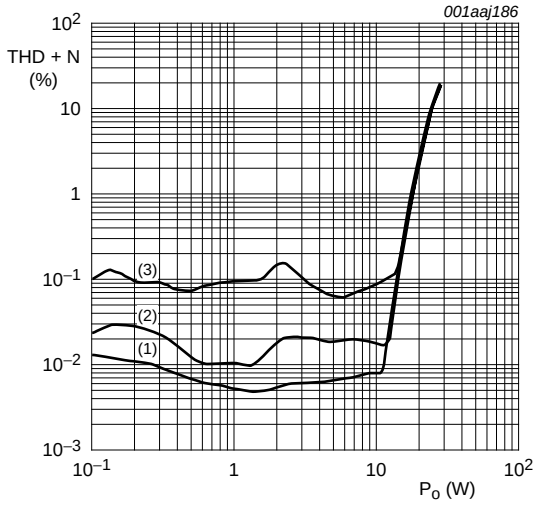
- V_P = 14.4 V
- P_o = 2 × (25 W / 10) = 2 × 2.5 W into 4 Ω (audio with crest factor of 10)
- T_{amb} = 25 °C
- P_{max} = 2.5 W
- $R_{th(j-a)}$ = 19 K/W
- $T_{j(max)}$ = 25 °C + (2.5 W × 19 K/W) = 72 °C

14.6 Curves measured in reference design



(1) V_P = 14.4 V; R_L = 2 Ω at 100 Hz.
(2) V_P = 14.4 V; R_L = 2 Ω at 1 kHz.
(3) V_P = 14.4 V, R_L = 2 Ω at 6 kHz.

Fig 30. THD + N as a function of output power with a 2 Ω load; V_P = 14.4 V



(1) V_P = 14.4 V; R_L = 4 Ω at 100 Hz.
(2) V_P = 14.4 V; R_L = 4 Ω at 1 kHz.
(3) V_P = 14.4 V, R_L = 4 Ω at 6 kHz.

Fig 31. THD + N as a function of output power with a 4 Ω load; V_P = 14.4 V

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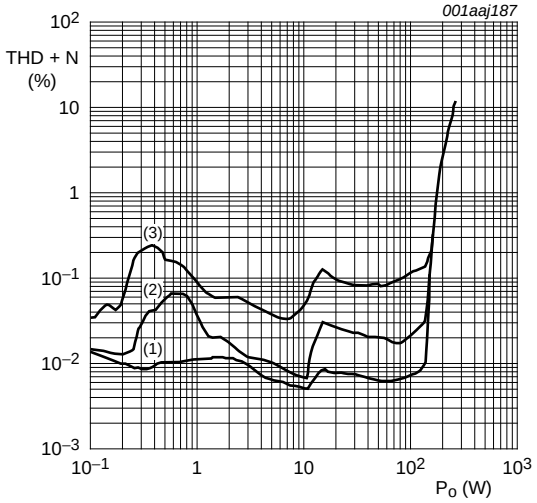
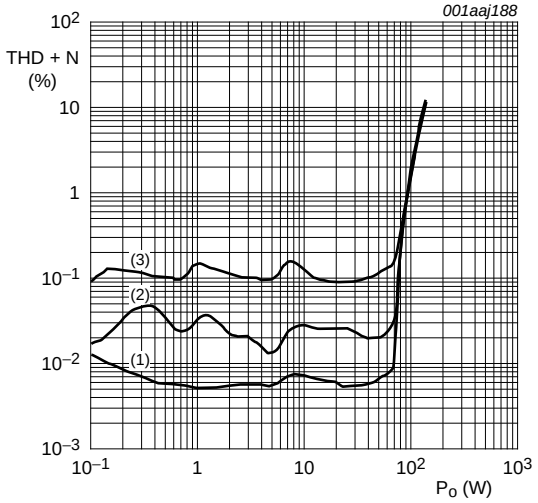


(1) V_P = 35 V; R_L = 2 Ω at 100 Hz.

(2) V_P = 35 V; R_L = 2 Ω at 1 kHz.

(3) V_P = 35 V, R_L = 2 Ω at 6 kHz.

Fig 32. THD + N as a function of output power with a 2 Ω load; V_P = 35 V

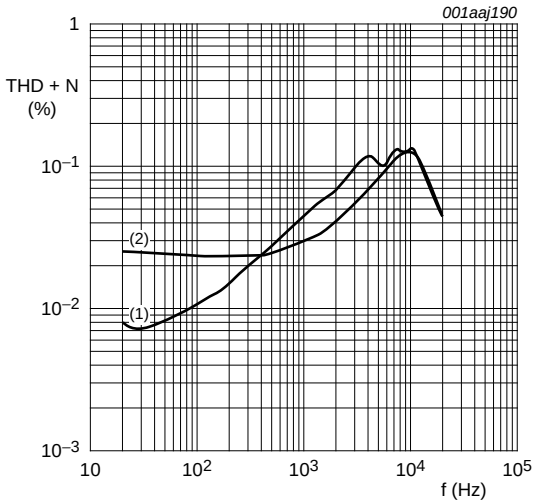


(1) V_P = 35 V; R_L = 4 Ω at 100 Hz.

(2) V_P = 35 V; R_L = 4 Ω at 1 kHz.

(3) V_P = 35 V, R_L = 4 Ω at 6 kHz.

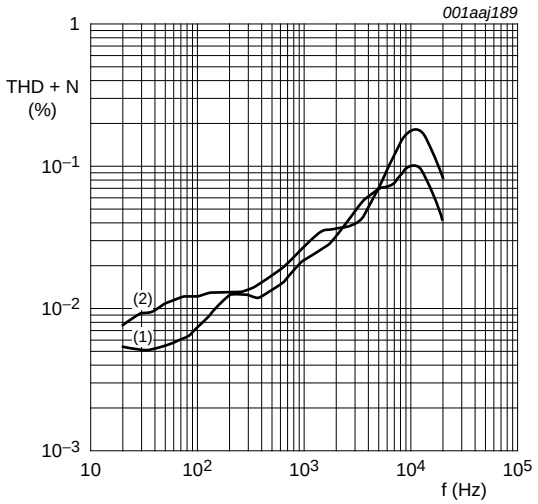
Fig 33. THD + N as a function of output power with a 4 Ω load; V_P = 35 V



(1) V_P = 14.4 V; R_L = 2 Ω at 1 W.

(2) V_P = 14.4 V; R_L = 2 Ω at 10 W.

Fig 34. THD + N as a function of frequency with a 2 Ω load, BD modulation; V_P = 14.4 V



(1) V_P = 14.4 V; R_L = 4 Ω at 1 W.

(2) V_P = 14.4 V; R_L = 4 Ω at 10 W.

Fig 35. THD + N as a function of frequency with a 4 Ω load, BD modulation; V_P = 14.4 V

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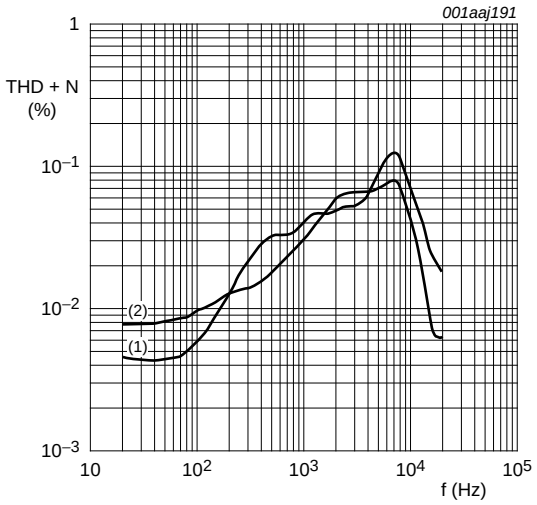


(1) V_P = 35 V; R_L = 2 Ω at 1 W.

(2) V_P = 35 V; R_L = 2 Ω at 10 W.

Fig 36. THD + N as a function of frequency with a 2 Ω load, BD modulation; V_P = 35 V

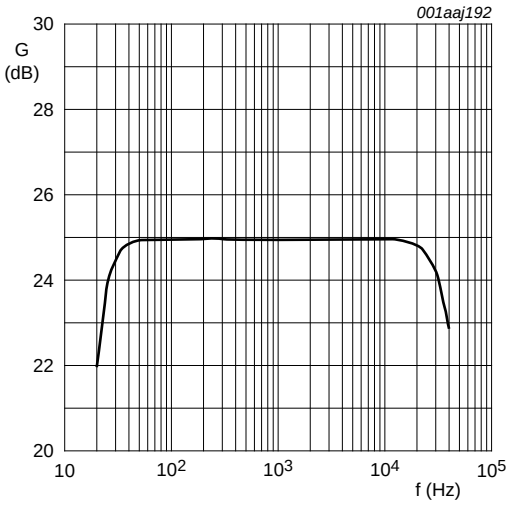
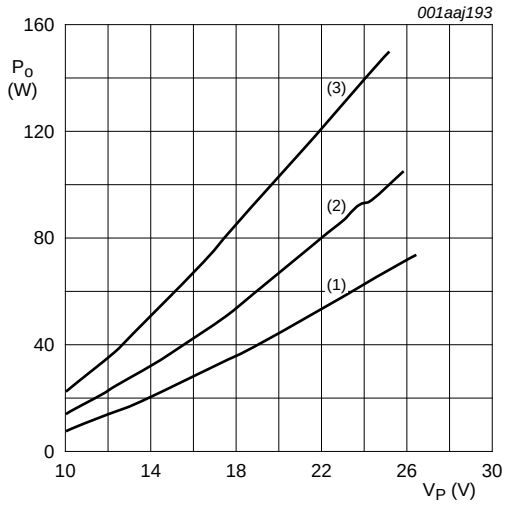


Fig 37. Gain as a function of frequency



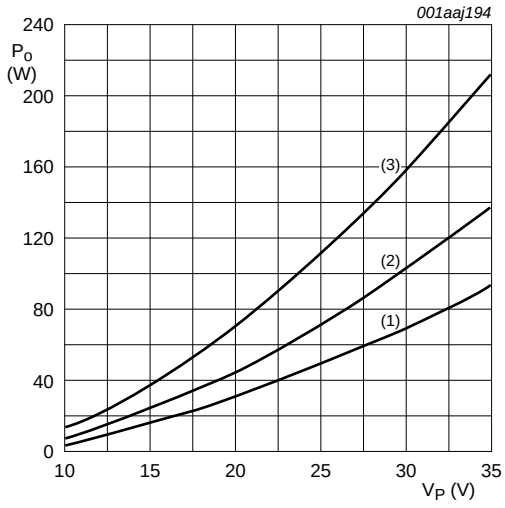
f = 1 kHz; R_L = 2 Ω.

(1) THD = 1 %.

(2) THD = 10 %.

(3) Maximum output power.

Fig 38. Output power as a function of supply voltage with a 2 Ω load



f = 1 kHz; R_L = 4 Ω.

(1) THD = 1 %.

(2) THD = 10 %.

(3) Maximum output power.

Fig 39. Output power as a function of supply voltage with a 4 Ω load

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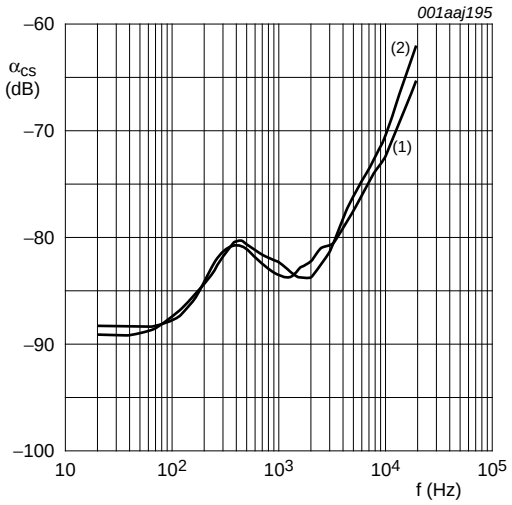
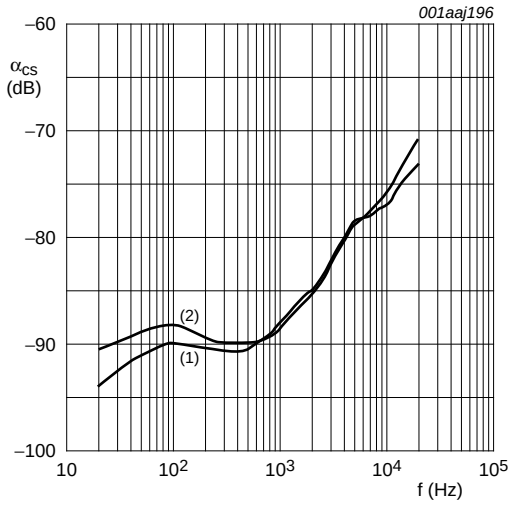


V_P = 14.4 V; R_i = 4 Ω; P_o = 1 W.

(1) Channel 1 to channel 2.

(2) Channel 2 to channel 1.

Fig 40. Channel separation as a function of frequency with 1 W output power

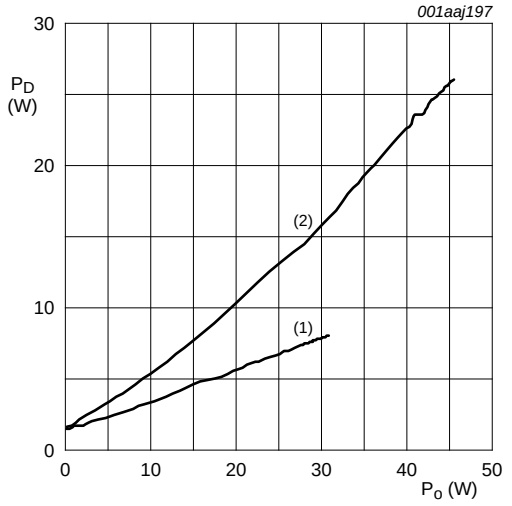


V_P = 14.4 V; R_i = 4 Ω; P_o = 10 W.

(1) Channel 1 to channel 2.

(2) Channel 2 to channel 1.

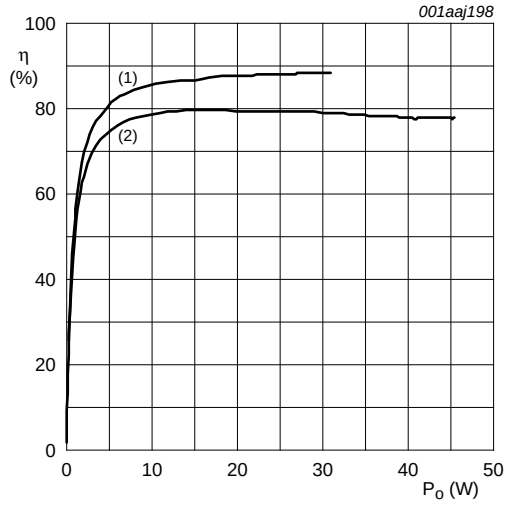
Fig 41. Channel separation as a function of frequency with 10 W output power



(1) V_P = 14.4 V; R_L = 2 Ω at 1 kHz.

(2) V_P = 14.4 V; R_L = 4 Ω at 1 kHz.

Fig 42. Power dissipation as a function of output power



(1) V_P = 14.4 V; R_L = 2 Ω at 1 kHz.

(2) V_P = 14.4 V; R_L = 4 Ω at 1 kHz.

Fig 43. Efficiency as a function of total output power

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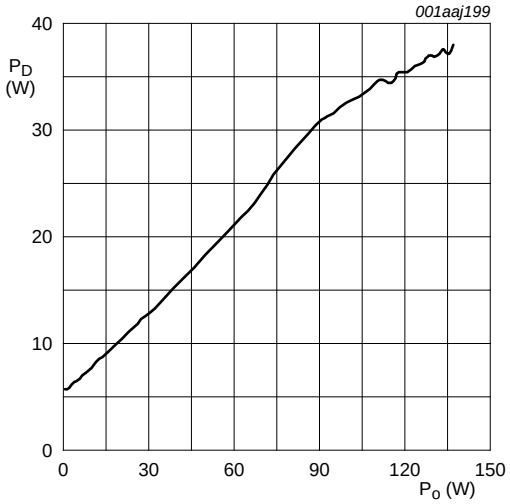
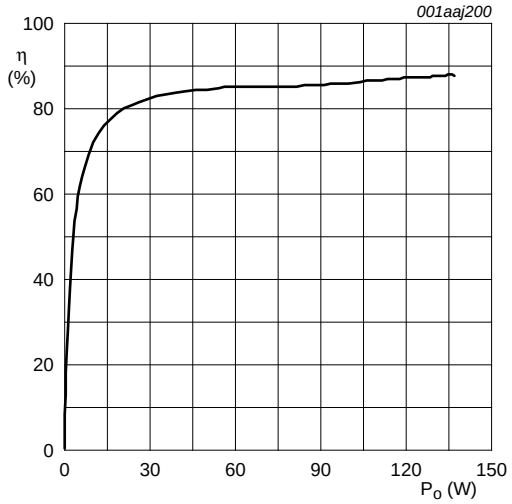


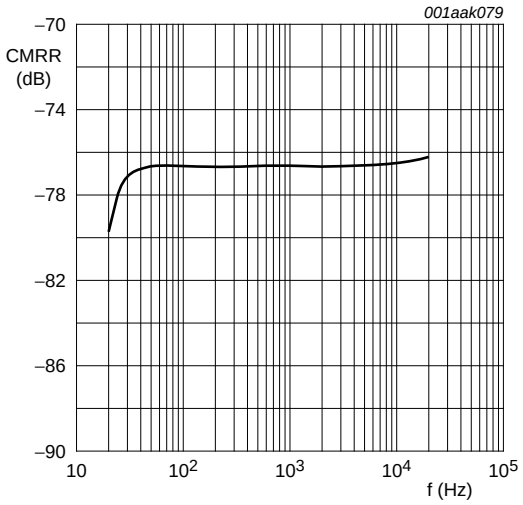
V_P = 35 V; R_L = 4 Ω.

Fig 44. Power dissipation as a function of total output power with both channels driven



V_P = 35 V; R_L = 4 Ω.

Fig 45. Efficiency as a function of output power of one channel with both channels driven



V_P = 14.4 V; V_i = 1 V RMS.

Fig 46. CMRR as a function of frequency

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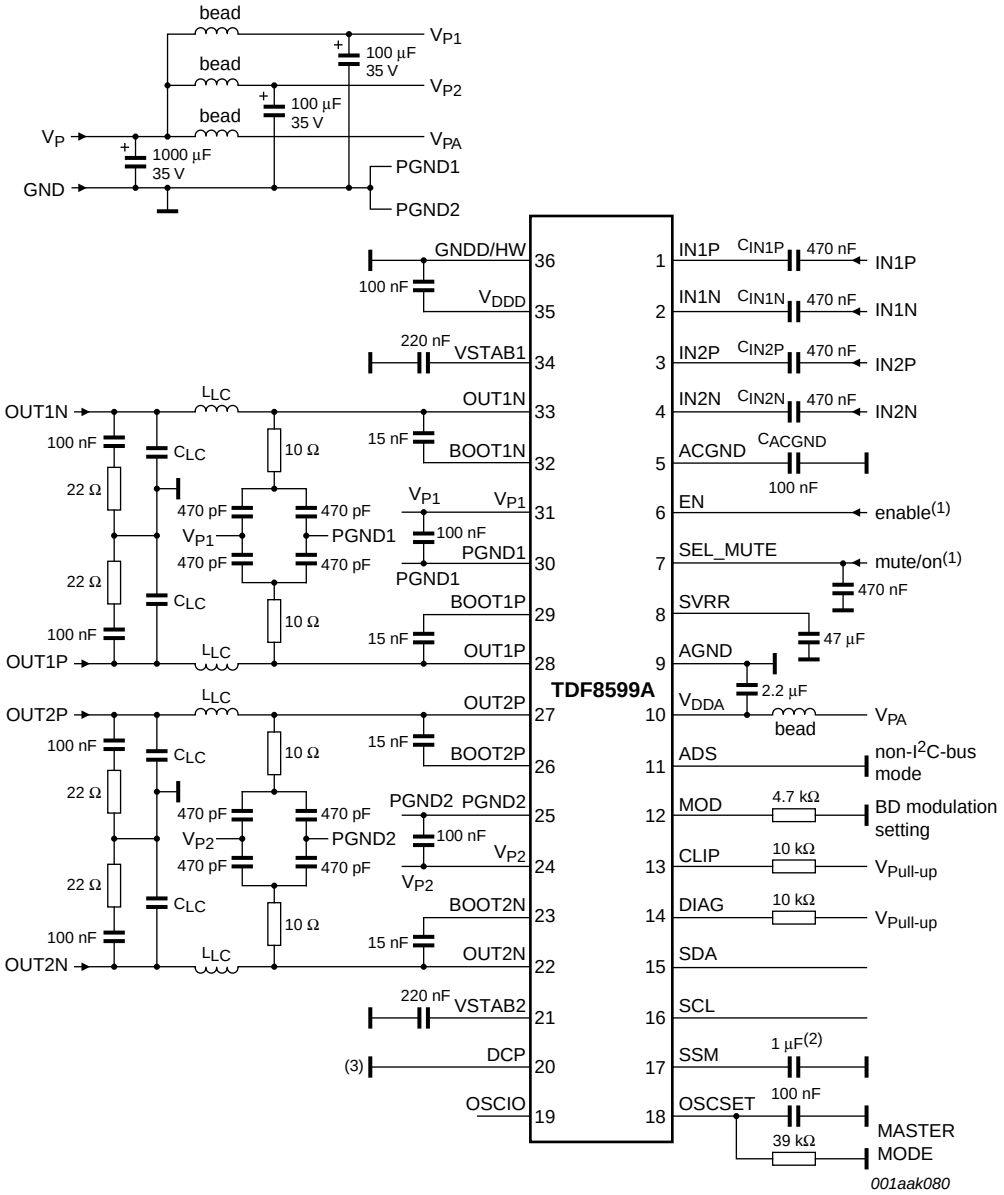
14.7 Typical application schematics



Dual BTL mode (stereo) in non-I²C-bus mode with DC offset protection disabled, Spread spectrum mode enabled BD modulation.

(1) See Figure 3 on page 6 for a diagram of the connection for pins EN and SEL_MUTE.

(2) See Section 8.3.2 on page 8 for detailed information.

(3) See Section 8.5.5 on page 16 for detailed information on DC offset protection.

Fig 47. Example application diagram: dual BTL in non-I²C-bus mode

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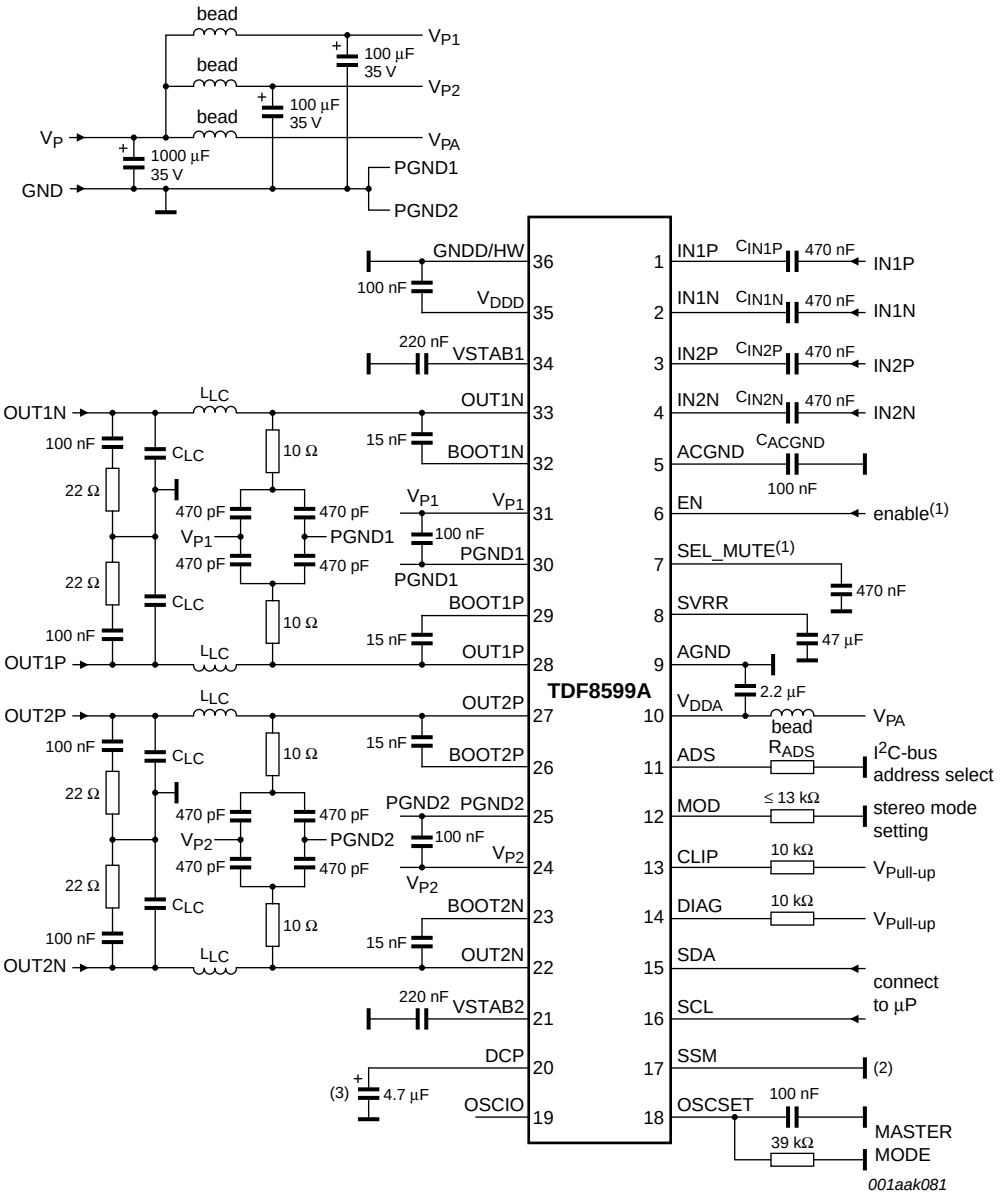

Dual BTL mode (stereo) in I²C-bus mode with DC offset protection enabled, Spread spectrum mode disabled.

(1) See Figure 3 on page 6 for a diagram of the connection for pins EN and SEL_MUTE.

(2) See Section 8.3.2 on page 8 for detailed information.

(3) See Section 8.5.5 on page 16 for detailed information on DC offset protection.

Fig 48. Example application diagram: dual BTL in I²C-bus mode

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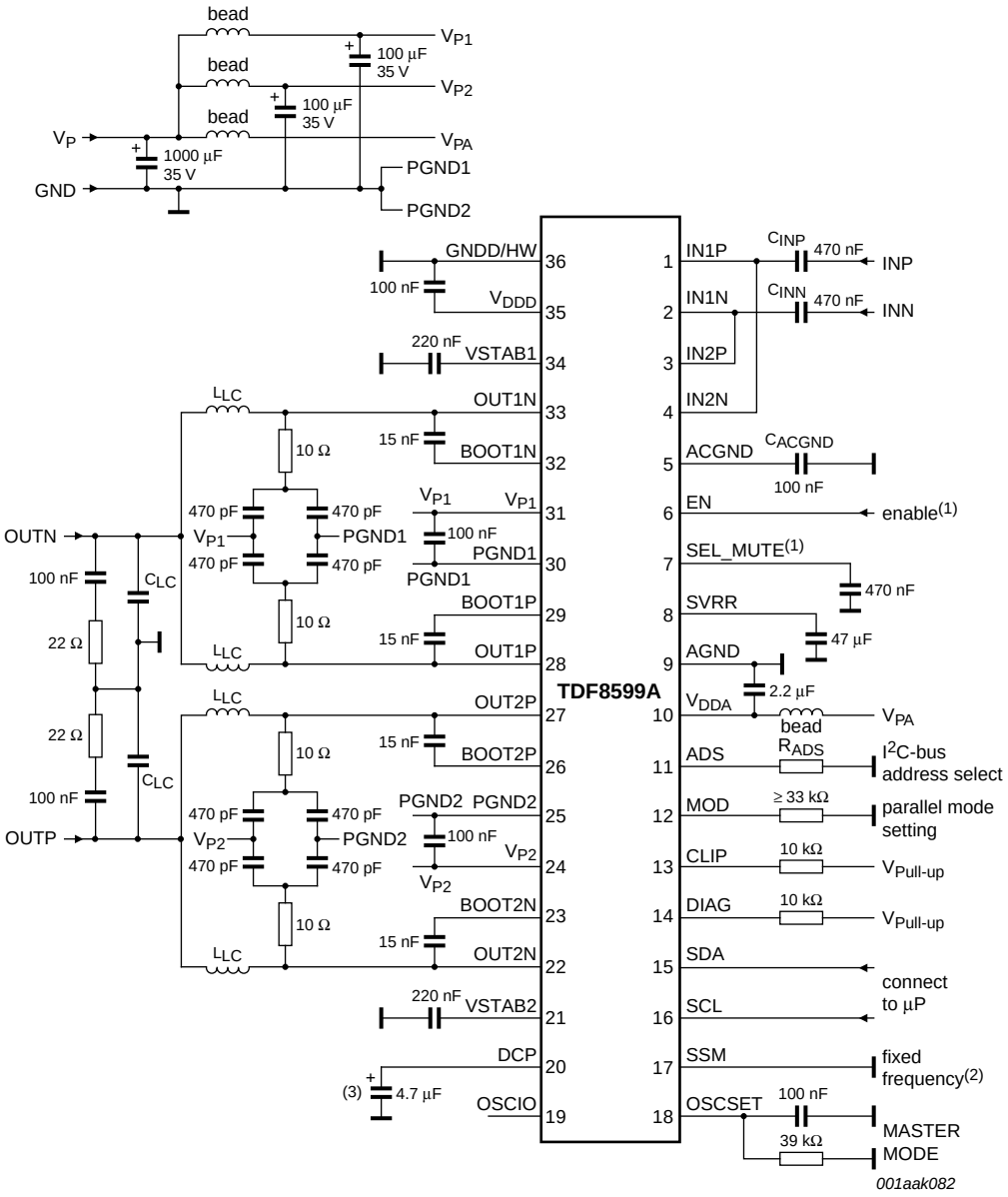

Single BTL mode (parallel) in I²C-bus mode with DC offset protection enabled, Spread spectrum mode disabled.

(1) See Figure 3 on page 6 for a diagram of the connection for pins EN and SEL_MUTE.

(2) See Section 8.3.2 on page 8 for detailed information.

(3) See Section 8.5.5 on page 16 for detailed information on DC offset protection.

Fig 49. Example application diagram: single BTL in I²C-bus mode

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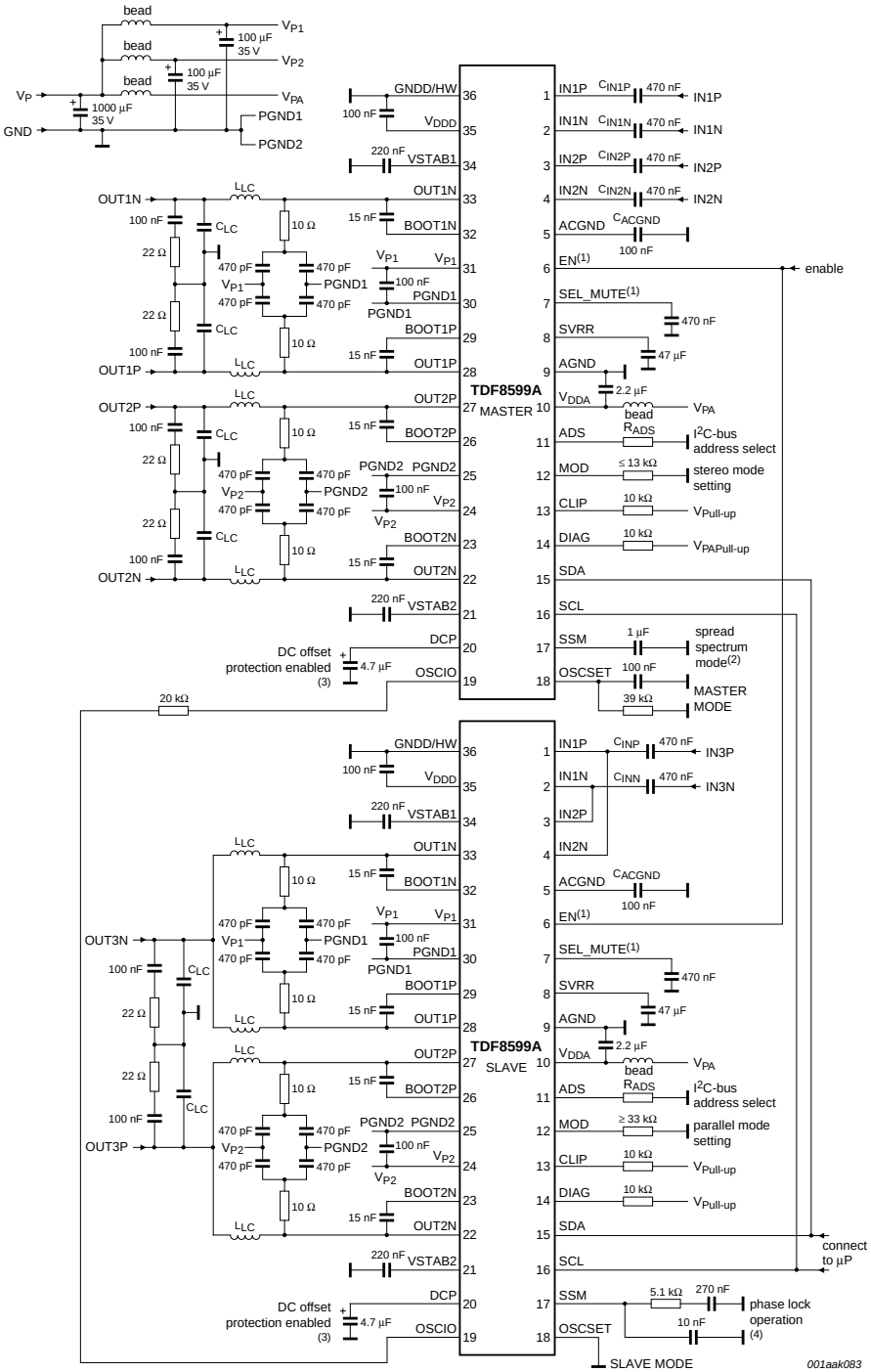

I²C-bus mode: dual BTL in Master mode, one BTL in Slave mode; DC offset protection enabled.

(1) See Figure 3 on page 6 for a diagram of the connection for pins EN and SEL_MUTE.

(2) See Section 8.3.2 on page 8 for detailed information.

(3) See Section 8.5.5 on page 16 for detailed information on disabling DC offset protection.

(4) See Section 8.3.4 on page 10 for detailed information on PLL operation.

Fig 50. Example application diagram: dual BTL master, single BTL slave in I²C-bus mode

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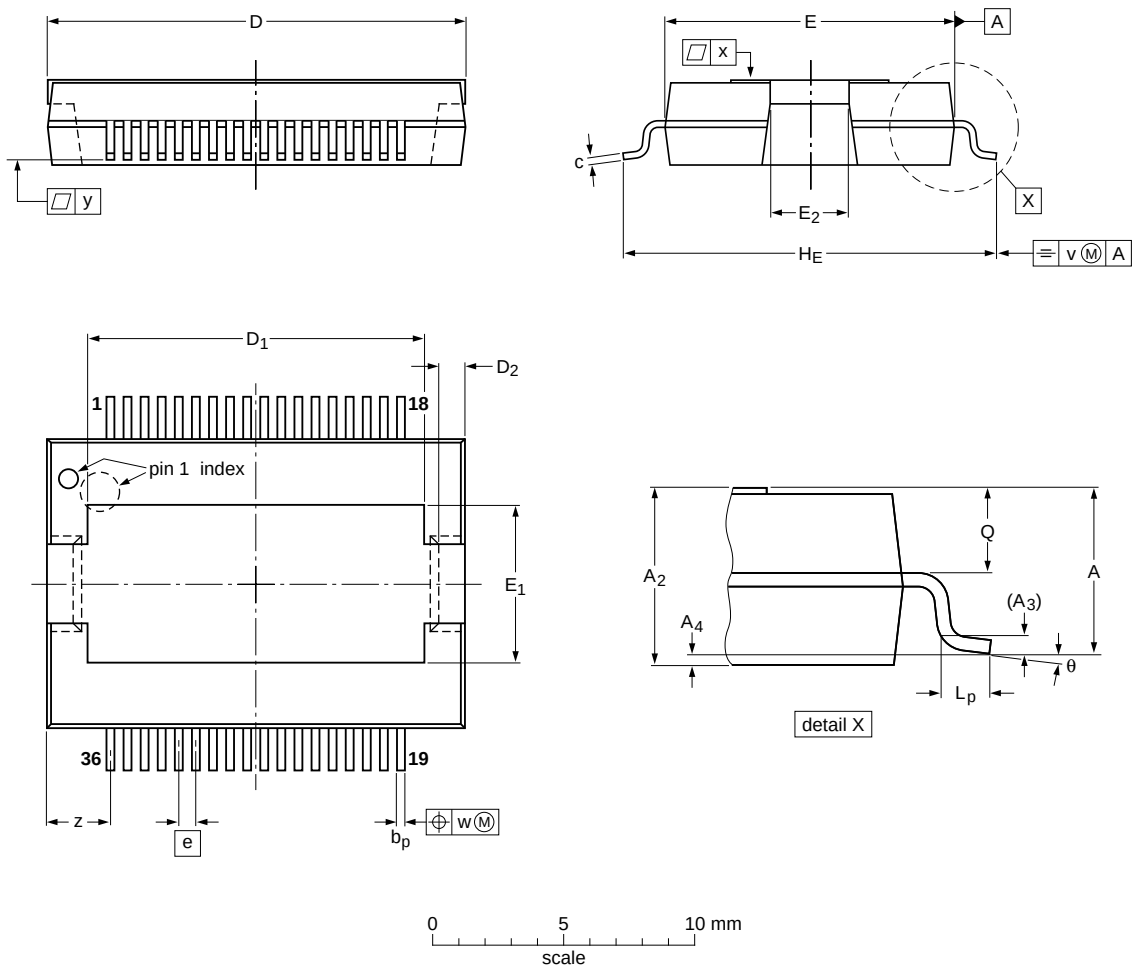
15. Package outline

HSOP36: plastic, heatsink small outline package; 36 leads; low stand-off height **SOT851-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4[1]	b_p	c	D[2]	D_1	D_2	E[2]	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 −0.04	0.38 0.25	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	0.65	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.12	0.03	0.07	2.55 2.20	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT851-2						04-05-04

Fig 51. Package outline SOT851-2 (HSOP36)

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16. Handling information

In accordance with SNW-FQ-611-D. The number of the quality specification can be found in the Quality Reference Handbook. The handbook can be ordered using the code 9398 510 63011.

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

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- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 52) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 23 and 24

Table 23. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 24. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 52.

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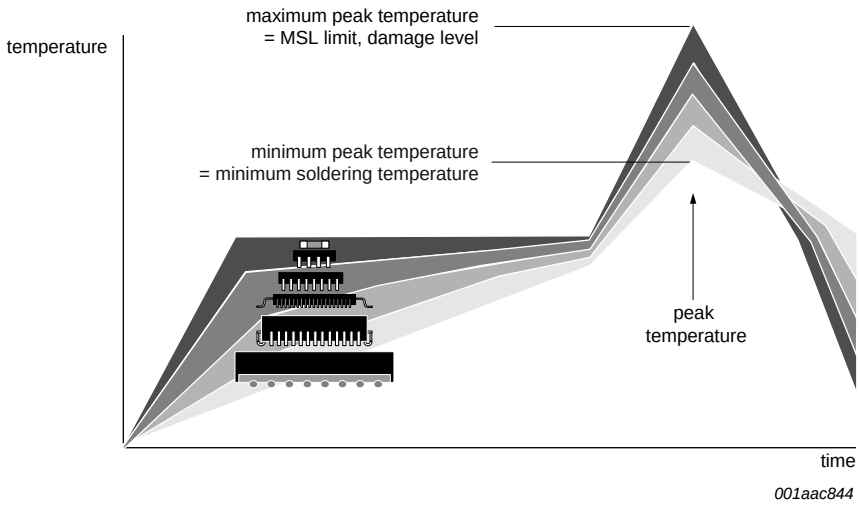

MSL: Moisture Sensitivity Level

Fig 52. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Abbreviations

Table 25. Abbreviations

Abbreviation	Description
BCDMOS	Bipolar Complementary and double Diffused Metal-Oxide Semiconductor
BTL	Bridge-Tied Load
DCP	DC offset Protection
DMOST	double Diffused Metal-Oxide Semiconductor Transistor
EMI	ElectroMagnetic Interference
I^2C	Inter-Integrated Circuit
LSB	Least Significant Bit
Mμp	Master microprocessor
MSB	Most Significant Bit
NDMOST	N-type double Diffused Metal-Oxide Semiconductor Transistor
OCP	OverCurrent Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse-Width Modulation
SOI	Silicon On Insulator

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Table 25. Abbreviations *...continued*

Abbreviation	Description
TFP	Thermal Foldback Protection
UVP	UnderVoltage Protection
WP	Window Protection

19. Revision history

Table 26. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDF8599A v.3	20130502	Product data sheet	-	TDF8599A v.2
Modifications:	• Changed title Figure 45.			
TDF8599A v.2	20090630	Product data sheet	-	TDF8599A v.1
Modifications:	• Data sheet status changed from Objective data sheet to Product data sheet. • Various minor textual inconsistencies in the data sheet corrected. • Changed Section 8.2: Figure 3 on page 6. • Changed Section 8.2: Table 4 on page 7. • Changed Section 8.2: Table 5 on page 7. • Changed Section 8.6.3: Figure 20 on page 22. • Changed Section 8.6.3: Figure 21 on page 23. • Changed Section 14.7: Figure 47 on page 42, Figure 48 on page 43, Figure 49 on page 44 and Figure 50 on page 45.			
TDF8599A v.1	20090602	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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