

# NCN5150NGEVB

## NCN5150 Evaluation Board User's Manual



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### Introduction

The NCN5150SOICGEVB and NCN5150QFNGEVB evaluation boards demonstrate the NCN5150 M-BUS transceiver in SOIC and QFN package respectively. These evaluation boards include all external components needed for operating NCN5150 and demonstrate the small PCB surface area such an implementation requires.

### Overview

The NCN5150 is a single-chip integrated slave transceiver for use in two-wire Meter Bus (M-BUS) slave devices and repeaters. The transceiver provides all of the functions needed to satisfy the European Standards EN 13757-2 and EN 1434-3 describing the physical layer requirements for M-BUS. It includes a programmable power level of up to 2 (SOIC version) or 6 (NQFP version) unit loads, which are available for use in external circuits through a 3.3 V LDO regulator. The NCN5150 can provide communication up to the maximum M-BUS communication speed of 38,400 baud (half-duplex).

### Applications

Multi-energy Utility Meters

- Water
- Gas
- Electricity
- Heating Systems

### Features

- Single-chip MBUS Transceiver
- UART Communication Speeds Up to 38,400 baud

## EVAL BOARD USER'S MANUAL

- Integrated 3.3 V VDD LDO Regulator with Extended Peak Current
- Capability of 15 mA
- Supports Powering Slave Device from the Bus or from External Power Supply
- Adjustable I/O Levels
- Adjustable Constant Current Sink up to 2 or 6 Unit Loads Depending on the Package
- Low Bus Voltage Operation
- Extended Current Budget for External Circuits: minimum 0.8 mA
- Polarity Independent
- Power-Fail Function
- Fast Startup – No External Transistor Required on STC Pin
- Industrial Ambient Temperature Range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Available in:
  - ♦ 16-pin SOIC (Pin-to-Pin Compatible with TSS721A)
  - ♦ 20-pin QFN
- These are Pb-free Devices

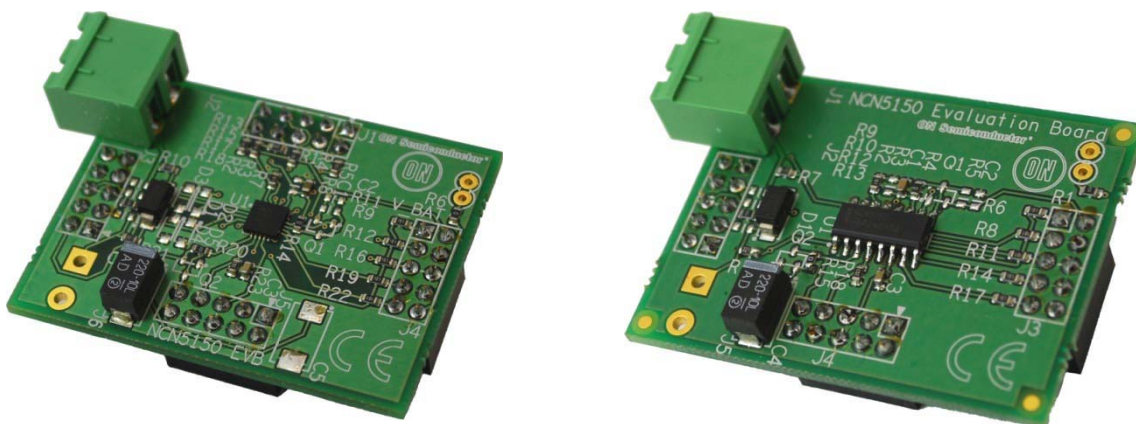


Figure 1. The NCN5150NGEVB Evaluation Boards

# NCN5150NGEVB

## ELECTRICAL CHARACTERISTICS

**Table 1. ELECTRICAL CHARACTERISTICS OF THE NCN5150SOICGEVB AND NCN5150QFNGEVB BOARD**

| Symbol                     | Parameter / Condition | Value |     |     | Unit |
|----------------------------|-----------------------|-------|-----|-----|------|
|                            |                       | Min   | Typ | Max |      |
| Bus Voltage                |                       |       |     |     |      |
| V <sub>BUS</sub>           | Bus Voltage           | 12    | 36  | 42  | V    |
| Current Drawn from the Bus |                       |       |     |     |      |
| I <sub>BUS</sub>           | 1 UL                  |       | 1.3 | 1.5 | mA   |
| Output Voltage             |                       |       |     |     |      |
| V <sub>DD</sub>            | LDO output            | 3.1   | 3.3 | 3.6 | V    |

## NCN5150 DESCRIPTION

The NCN5150 provide a complete transceiver for the Metering Bus (M-BUS). It consists of a transmit block which will translate the logic level uart input to current level signaling on the bus, and a receive block which will translate the voltage-level signaling on the bus to a logic-level uart output. The device includes an echo function which will echo the uart input on the uart output, provided the device is powered. This can be used by the software stack to monitor if the message was transmitted. The high voltage level of the microcontroller interface can be changed by connecting the desired voltage to the VIO pin. By default, this pin is

connected through a 0R resistor to 3.3 V on the evaluation boards.

A constant current regulator that will draw a fixed current from the bus, expressed in unit loads (UL). This current is made available to the application through a low-dropout 3.3 V regulator. The NCN5150 will detect when the bus is disconnected and provide an early warning to the microcontroller that the 3.3 V supply is about to collapse through the PFb pin.

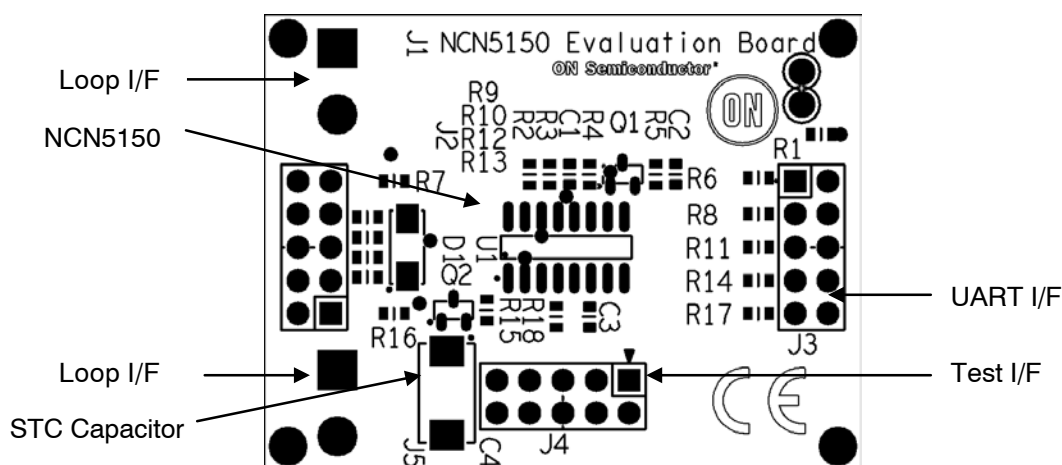
A thermal shutdown protects the device against high junction temperatures.

## NCN5150SOICGEVB DESCRIPTION

### General Overview

The NCN5192NGEVB evaluation board demonstrates the external components required for the operation of the IC.

We will cover the different sections below as well as possible alternatives. A drawing of the board where the different sections are indicated is shown below.



**Figure 2. Board Drawing with Indication of Different Sections**

## NCN5150NGEVB

### BOM List

Table 2. NCN5150SOICGEVB BILL OF MATERIALS

| Quantity | Reference                 | Part        | Footprint | Comments | Manufacturer     | Product Code         |
|----------|---------------------------|-------------|-----------|----------|------------------|----------------------|
| 1        | C1                        | 1u          | C0603     | 6V3      | Multicomp        | MCCA000515           |
| 1        | C2                        | DNP         | C0603     | DNP      | –                | –                    |
| 5        | R3, R5, R9, R12, R13      | DNP         | R0603     | DNP      | –                | –                    |
| 1        | C3                        | 100n        | C0603     | 50 V     | Multicomp        | MCCA000256           |
| 1        | C4                        | 220u        | Case E    | 10 V     | AVX              | TAJD227K010RNJ       |
| 1        | D1                        | 1SMA40CAT3G | SMA       |          | ON Semiconductor | 1SMA40CAT3G          |
| 2        | J1,J5                     | CON2        |           | DNP      | IMO Precision    | 21.95MH/2            |
| 3        | J2,J3,J4                  | CON10A      |           | DNP      | Multicomp        | 2214S–10SG–85        |
| 2        | Q1,Q2                     | DNP         | SOT–23    | DNP      | –                | –                    |
| 4        | R1, R4, R10, R15          | 0R          | R0603     | 62.5 mW  | Multicomp        | MC0603WG00000T5E–TR  |
| 6        | R2, R6, R8, R11, R14, R17 | 100R        | R0603     | 62.5 mW  | Multicomp        | MC0.063W06031%100RFR |
| 2        | R7, R16                   | 220R        | R0603     | 62.5 mW  | Multicomp        | MC0.063W06031%220RFR |
| 1        | R18                       | 30K         | R0603     | 62.5 mW  | Multicomp        | MC0.063W06031%30KFR  |
| 1        | TP1                       | GND         |           | DNP      | –                | –                    |
| 1        | TP2                       | 3V3         |           | DNP      | –                | –                    |
| 1        | U1                        | NCN5150     | SOIC16    | DNP      | ON Semiconductor | NCN5150DR2G          |

### Schematic Diagram



# NCN5150NGEVB

## NCN5150QFNGEVB DESCRIPTION

### General Overview

The NCN5150QFNGEVB evaluation board demonstrates the external components required for the operation of the IC. We will cover the different sections

below as well as possible alternatives. A drawing of the board where the different sections are indicated is shown below.

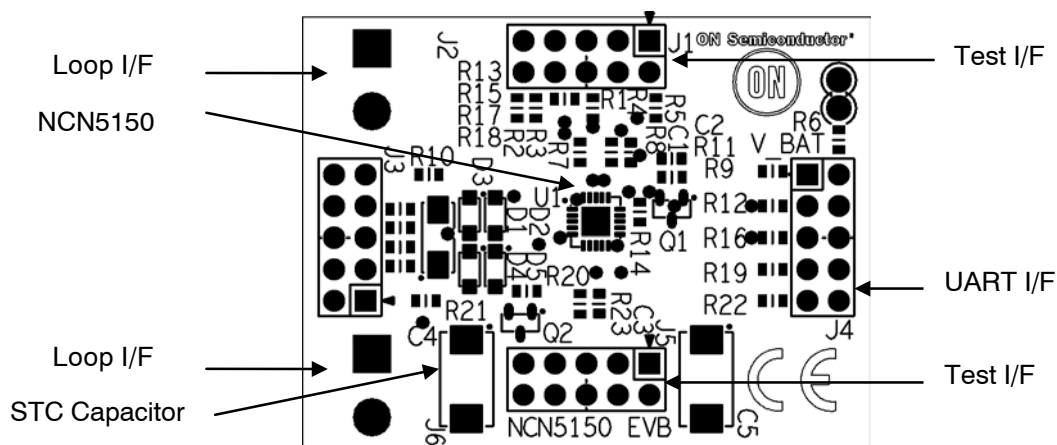


Figure 4. Board Drawing with Indication of Different Sections

### BOM List

Table 3. NCN5150QFNGEVB BILL OF MATERIALS

| Quantity | Reference                                 | Part        | Footprint | Comments  | Manufacturer     | Product Code         |
|----------|-------------------------------------------|-------------|-----------|-----------|------------------|----------------------|
| 1        | C1                                        | 1u          | C0603     | 6.3 V     | Multicomp        | MCCA000515           |
| 1        | C2                                        | DNP         | C0603     | DNP       | -                | -                    |
| 1        | C3                                        | 100n        | C0603     | 50 V      | Multicomp        | MCCA000256           |
| 1        | C4                                        | 220u        | Case E    | 10 V      | AVX              | TAJD227K010RNJ       |
| 1        | C5                                        | DNP         | Case E    | DNP       | -                | -                    |
| 4        | D1, D2, D4, D5                            | DNP         | SOD-123   | DNP       | -                | -                    |
| 1        | D3                                        | 1SMA40CAT3G | SMA       |           | ON Semiconductor | 1SMA40CAT3G          |
| 4        | J1, J3, J4, J5                            | CON10A      |           | DNP       | IMO Precision    | 21.95MH/2            |
| 2        | J2, J6                                    | CON2        |           | DNP       | Multicomp        | 2214S-10SG-85        |
| 2        | Q1, Q2                                    | DNP         | SOT-23    | DNP       | -                | -                    |
| 10       | R1,R2,R3,R4,R5,<br>R8,R11,R13,R15,<br>R18 | DNP         |           | DNP       | -                | -                    |
| 6        | R7,R9,R12,R16,<br>R19,R22                 | 100R        | R0603     | 62.5 mW   | Multicomp        | MC0.063W06031%100RFR |
| 4        | R6,R14,R17,R20                            | 0R          | R0603     | 62.5 mW   | Multicomp        | MC0603WG00000T5E-TR  |
| 2        | R10, R21                                  | 220R        | R0603     | 62.5 mW   | Multicomp        | MC0.063W06031%220RFR |
| 1        | R23                                       | 30K         | R0603     | 62.5 mW   | Multicomp        | MC0.063W06031%30KFR  |
| 1        | TP1                                       | GND         |           | DNP       | -                | -                    |
| 1        | TP2                                       | 3V3         |           | DNP       | -                | -                    |
| 1        | U1                                        | NCN5150     | QFN20     | ON Sample | ON Semiconductor | NCN5150MNTWG         |

# NCN5150NGEVB

## Schematic Diagram

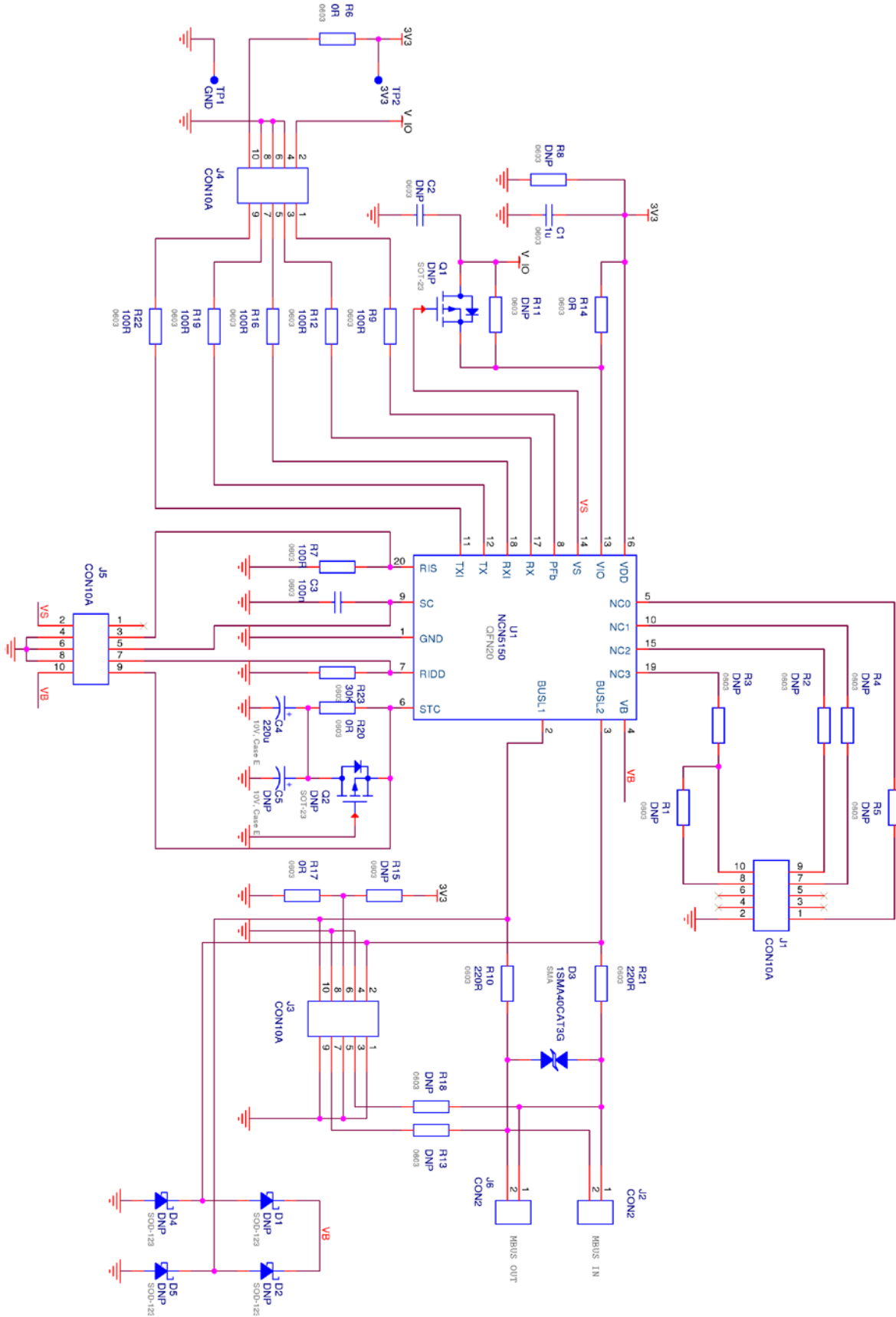


Figure 5. Schematic of NCN5150QFNGEVB

## FUNCTIONAL DESCRIPTION

### Power Supply

The NCN5150 provides power to be used in the application. To do this, the NCN5150 draws a fixed current from the bus. The amount of current drawn is fixed at a number of unit loads (intervals of 1.5 mA) and can be set by changing the value of the RIDD resistor. The SOIC version can support up to 2 UL, while the QFN version can support up to 6 UL. The required resistors for are shown in table xx.

Also shown in table xx is the maximum amount of capacitance allowed on the STC pin. This limit will ensure that the transceiver will start up in less than 3 s as required by the M-BUS standard. Using a smaller capacitor on STC is allowed, and will result in faster start-up, but also in a faster shutdown, reducing the time between the early warning PFb toggling (when the bus is removed) and the point where the 3.3V VDD voltage can no longer be maintained. The minimum allowed capacitance on STC is 10 times the capacitance on the VDD pin. The minimum required capacitance on the VDD pin is 1  $\mu$ F.

**Table 4. UL, RIDD VALUES, STC CAPACITANCE**

| Number of Unit Loads | RIDD Value      | Maximum STC Capacitor Value | Min. Available Current |
|----------------------|-----------------|-----------------------------|------------------------|
| 1                    | 30 k $\Omega$   | 330 $\mu$ F                 | 0.88 mA                |
| 2                    | 13 k $\Omega$   | 820 $\mu$ F                 | 2.10 mA                |
| 3                    | 8.45 k $\Omega$ | 1200 $\mu$ F                | 3.10 mA                |
| 4                    | 6.19 k $\Omega$ | 1500 $\mu$ F                | 4.20 mA                |
| 5                    | 4.87 k $\Omega$ | 2200 $\mu$ F                | 5.30 mA                |
| 6                    | 4.02 k $\Omega$ | 2700 $\mu$ F                | 6.50 mA                |

Shown in Figure 6 is the startup sequence of the device. Note that the NCN5150 does not require any external (PMOS) transistor on the STC pin for proper startup. The yellow waveform is the bus voltage, the purple waveform the STC voltage, the green waveform the VDD output, and the blue waveform the TX output.



**Figure 6. NCN5150 Startup Sequence**

Shown in Figure 7 is the shutdown sequence of the device. The green waveform is the bus voltage, the blue waveform

is the VDD output, the purple waveform is the PFb output, and the yellow waveform is the TX output.



Figure 7. NCN5150 Shutdown Sequence

#### UART Interface IDC1

The interface between the transceiver and an external microcontroller is a standard uart interface consisting of the TX and RX. Alternatively, inverted signals, TXI and RXI, which are active high, are also available. Only one signal from TX and TXI, or from RX and RXI can be used at the same time. The uart pins can handle communication up to 38400 baud. The M-BUS standard requires communication with 1 start bit, 8 data-bits, 1 even parity bit and 1 stop bit.

Also available on the same connector is the VIO connection, PFb indication and 3V3 VDD output.

Table 5. MICROCONTROLLER INTERFACE

| Pin number | Signal | Type   | Description            |
|------------|--------|--------|------------------------|
| 1          | PFb    | Output | Bus failure indication |
| 2          | VIO    | Power  | IO voltage level       |
| 3          | RX     | Input  | UART input             |
| 5          | RXI    | Input  | UART input, inverted   |
| 7          | TX     | Output | UART output            |
| 9          | TXI    | Output | UART output, Inverted  |
| 4, 6, 8    | GND    | Power  | Ground                 |
| 10         | VDD    | Power  | 3V3 Output             |

#### Transmitter

The M-Bus transmitter translated the RX or RXI voltage levels to current levels on the bus. Typically, 15 mA is added when transmitting a space.

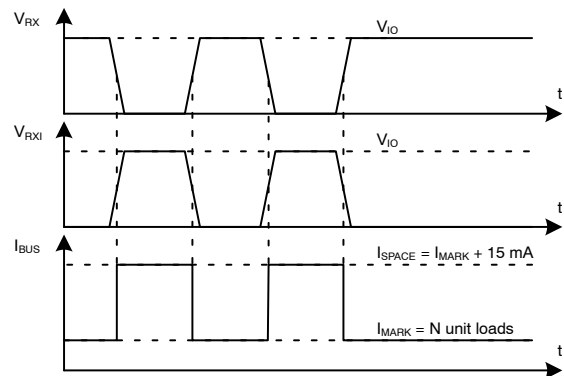


Figure 8. Output Waveforms

#### Receiver

The receiver will compare the bus voltage level with the mark level stored on the SC capacitor minus the threshold level (typically 6 V). It will translate these voltage levels to low voltage communication on the TX and TXI pins. The high voltage of these pins is determined by the VIO voltage.

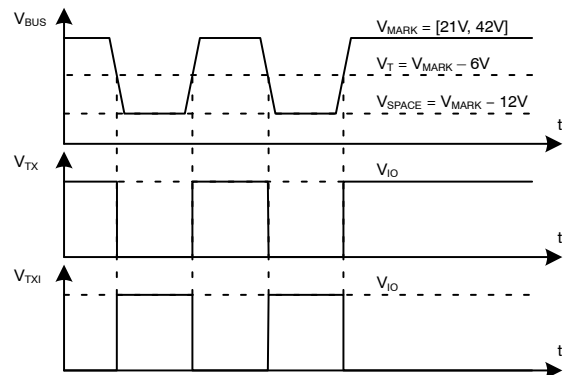


Figure 9. Receive Waveforms



## APPENDIX

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# NCN5150NGEVB

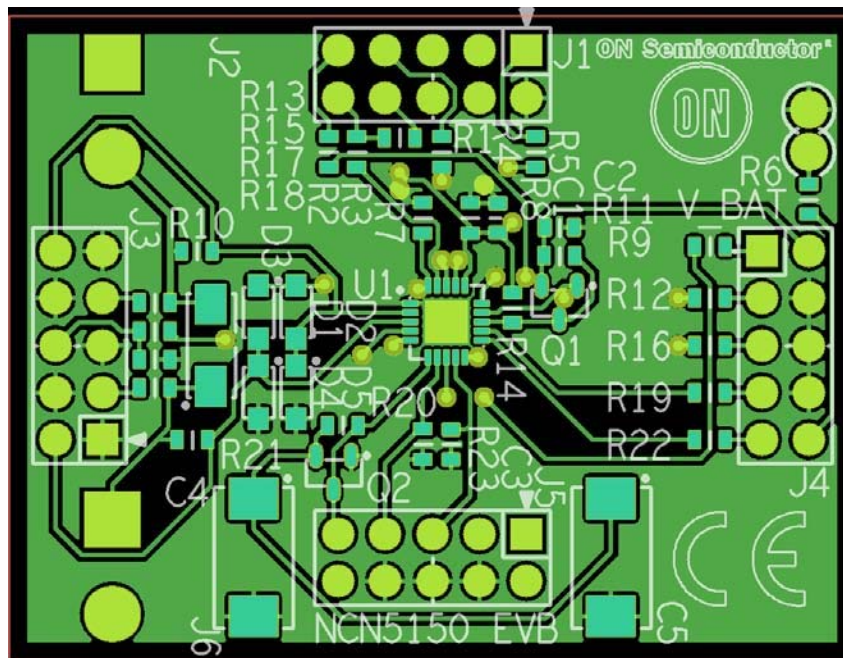


Figure 12. Top Layer Layout (QFN)

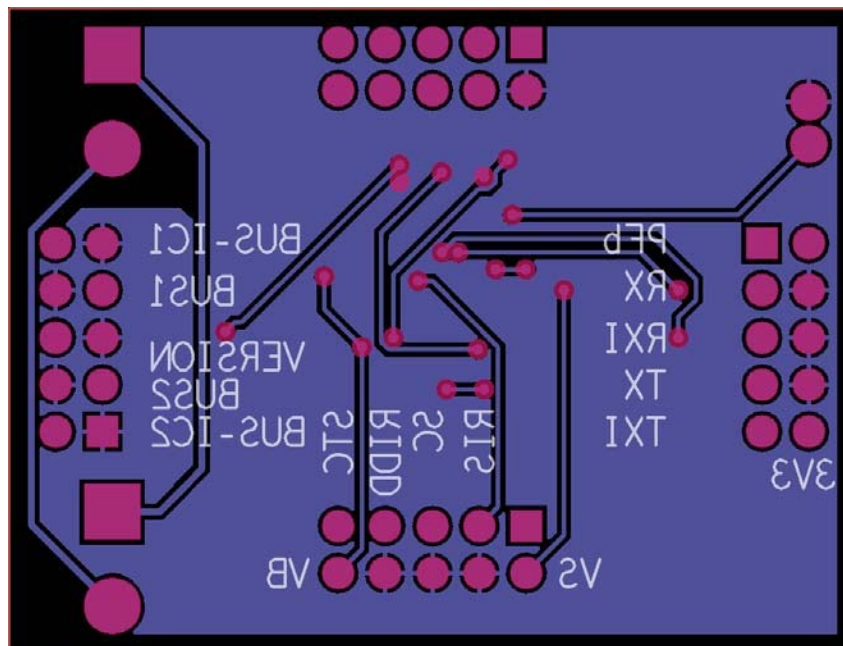


Figure 13. Bottom Layer Layout (QFN)

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