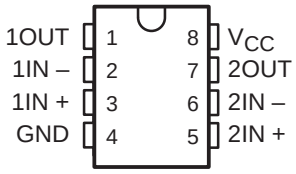
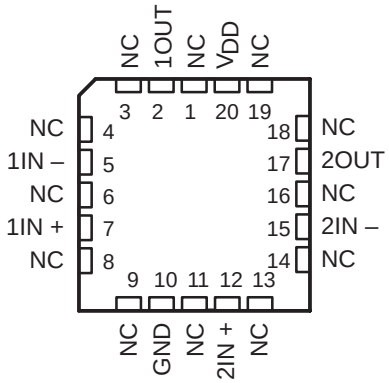
Jameco Part Number 1088702

- **Trimmed Offset Voltage:**
  **TLC27M7 . . . 500 μV Max at 25°C,**
  **$V_{DD}$ = 5 V**
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Ranges:**
  **0°C to 70°C . . . 3 V to 16 V**
  **–40°C to 85°C . . . 4 V to 16 V**
  **–55°C to 125°C . . . 4 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Low Noise . . . Typically 32 nV/$\sqrt{Hz}$ at f = 1 kHz**
- **Low Power . . . Typically 2.1 mW at 25°C, $V_{DD}$ = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input impedance . . . $10^{12}$ Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

**D, JG, P OR PW PACKAGE**
**(TOP VIEW)**

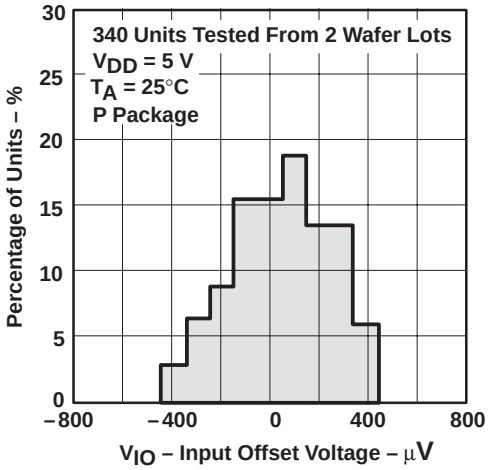



**FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

**DISTRIBUTION OF TLC27M7**
**INPUT OFFSET VOLTAGE**




**AVAILABLE OPTIONS**

| $T_A$ | $V_{IO}$max AT 25°C | PACKAGE | | | | |
|---|---|---|---|---|---|---|
| | | SMALL OUTLINE (D) | CHIP CARRIER (FK) | CERAMIC DIP (JG) | PLASTIC DIP (P) | TSSOP (PW) |
| 0°C to 70°C | 500 μV | TLC27M7CD | — | — | TLC27M7CP | — |
| | 2 mV | TLC27M2BCD | — | — | TLC27M2BCP | — |
| | 5 mV | TLC27M2ACD | — | — | TLC27M2ACP | — |
| | 10 mV | TLC27M2CD | — | — | TLC27M2CP | TLC27M2CPW |
| –40°C to 85°C | 500 μV | TLC27M7ID | — | — | TLC27M7IP | — |
| | 2 mV | TLC27M2BID | — | — | TLC27M2BIP | — |
| | 5 mV | TLC27M2AID | — | — | TLC27M2AIP | — |
| | 10 mV | TLC27M2ID | — | — | TLC27M2IP | TLC27M2IPW |
| –55°C to 125°C | 500 μV | TLC27M7MD | TLC27M7MFK | TLC27M7MJG | TLC27M7MP | — |
| | 10 mV | TLC27M2MD | TLC27M2MFK | TLC27M2MJG | TLC27M2MP | — |

The D and PW package is available taped and reeled. Add R suffix to the device type (e.g.,TLC27M7CDR).

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## description

The TLC27M2 and TLC27M7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose bipolar devices.These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for general-purpose bipolar products,but with only a fraction of the power consumption. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M2 (10 mV) to the high-precision TLC27M7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M2 and TLC27M7. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

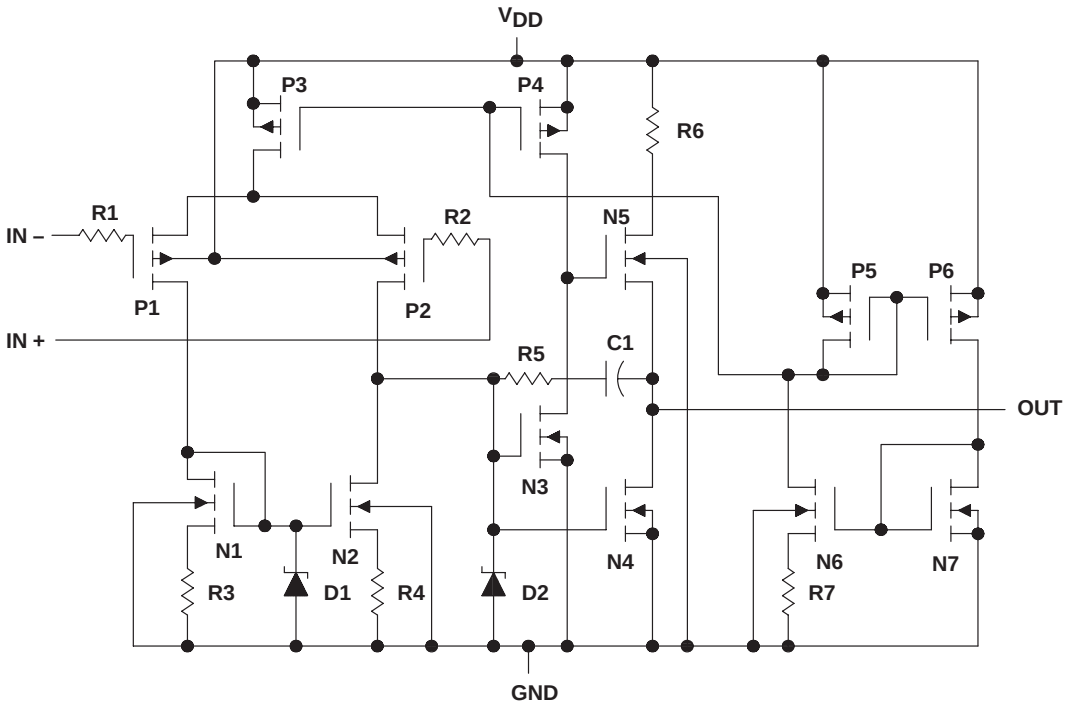
A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC27M2 and TLC27M7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

## equivalent schematic (each amplifier)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1) . . . . . 18 V
Differential input voltage, $V_{ID}$ (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, $V_I$ (any input) . . . . . – 0.3 V to $V_{DD}$
Input current, $I_I$ . . . . . ±5 mA
Output current, $I_O$ (each output) . . . . . ±30 mA
Total current into $V_{DD}$ . . . . . 45 mA
Total current out of GND . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, $T_A$: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
M suffix . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW | |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |
| JG | 1050 mW | 8.4 mW/°C | 672 mW | 546 mW | 210 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW | 520 mW | |

### recommended operating conditions

| | | C SUFFIX | | I SUFFIX | | M SUFFIX | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Supply voltage, $V_{DD}$ | | 3 | 16 | 4 | 16 | 4 | 16 | V |
| Common-mode input voltage, $V_{IC}$ | $V_{DD}$ = 5 V | –0.2 | 3.5 | –0.2 | 3.5 | 0 | 3.5 | V |
| | $V_{DD}$ = 10 V | –0.2 | 8.5 | –0.2 | 8.5 | 0 | 8.5 | |
| Operating free-air temperature, $T_A$ | | 0 | 70 | –40 | 85 | –55 | 125 | °C |

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | $T_A$† | TLC27M2C, TLC27M2AC, TLC27M2BC, TLC27M7C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | TLC27M2C | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_I$ = 100 kΩ | 25°C | | 1.1 | 10 | mV |
| | | | | | Full range | | | 12 | |
| | | TLC27M2AC | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_I$ = 100 kΩ | 25°C | | 0.9 | 5 | |
| | | | | | Full range | | | 6.5 | |
| | | TLC27M2BC | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_I$ = 100 kΩ | 25°C | | 220 | 2000 | μV |
| | | | | | Full range | | | 3000 | |
| | | TLC27M7C | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_I$ = 100 kΩ | 25°C | | 185 | 500 | |
| | | | | | Full range | | | 1500 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | | | 25°C to 70°C | | 1.7 | | μV/°C |
| $I_{IO}$ | Input offset current (see Note 4) | | $V_O$ = 2.5 V, | $V_{IC}$ = 2.5 V | 25°C | | 0.1 | | pA |
| | | | | | 70°C | | 7 | 300 | |
| $I_{IB}$ | Input bias current (see Note 4) | | $V_O$ = 2.5 V, | $V_{IC}$ = 2.5 V | 25°C | | 0.6 | | pA |
| | | | | | 70°C | | 40 | 600 | |
| $V_{ICR}$ | Common-mode input voltage range (see Note 5) | | | | 25°C | −0.2 to 4 | −0.3 to 4.2 | | V |
| | | | | | Full range | −0.2 to 3.5 | | | V |
| $V_{OH}$ | High-level output voltage | | $V_{ID}$ = 100 mV, | $R_L$ = 100 kΩ | 25°C | 3.2 | 3.9 | | V |
| | | | | | 0°C | 3 | 3.9 | | |
| | | | | | 70°C | 3 | 4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = −100 mV, | $I_{OL}$ = 0 | 25°C | | 0 | 50 | mV |
| | | | | | 0°C | | 0 | 50 | |
| | | | | | 70°C | | 0 | 50 | |
| $A_{VD}$ | Large-signal differential voltage amplification | | $V_O$ = 0.25 V to 2 V, | $R_L$ = 100 kΩ | 25°C | 25 | 170 | | V/mV |
| | | | | | 0°C | 15 | 200 | | |
| | | | | | 70°C | 15 | 140 | | |
| CMRR | Common-mode rejection ratio | | $V_{IC}$ = $V_{ICR}$min | | 25°C | 65 | 91 | | dB |
| | | | | | 0°C | 60 | 91 | | |
| | | | | | 70°C | 60 | 92 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | | $V_{DD}$ = 5 V to 10 V, | $V_O$ = 1.4 V | 25°C | 70 | 93 | | dB |
| | | | | | 0°C | 60 | 92 | | |
| | | | | | 70°C | 60 | 94 | | |
| $I_{DD}$ | Supply current (two amplifiers) | | $V_O$ = 2.5 V, No load | $V_{IC}$ = 2.5 V, | 25°C | | 210 | 560 | μA |
| | | | | | 0°C | | 250 | 640 | |
| | | | | | 70°C | | 170 | 440 | |

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 10 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | $T_A$† | TLC27M2C TLC27M2AC TLC27M2BC TLC27M7C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | TLC27M2C | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 1.1 | 10 | mV |
| | | | | | Full range | | | 12 | |
| | | TLC27M2AC | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 0.9 | 5 | |
| | | | | | Full range | | | 6.5 | |
| | | TLC27M2BC | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 224 | 2000 | μV |
| | | | | | Full range | | | 3000 | |
| | | TLC27M7C | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 190 | 800 | |
| | | | | | Full range | | | 1900 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | | | 25°C to 70°C | | 2.1 | | μV/°C |
| $I_{IO}$ | Input offset current (see Note 4) | | $V_O$ = 5 V, | $V_{IC}$ = 5 V | 25°C | | 0.1 | | pA |
| | | | | | 70°C | | 7 | 300 | |
| $I_{IB}$ | Input bias current (see Note 4) | | $V_O$ = 5 V, | $V_{IC}$ = 5 V | 25°C | | 0.7 | | pA |
| | | | | | 70°C | | 50 | 600 | |
| $V_{ICR}$ | Common-mode input voltage range (see Note 5) | | | | 25°C | −0.2 to 9 | −0.3 to 9.2 | | V |
| | | | | | Full range | −0.2 to 8.5 | | | V |
| $V_{OH}$ | High-level output voltage | | $V_{ID}$ = 100 mV, | $R_L$ = 100 kΩ | 25°C | 8 | 8.7 | | V |
| | | | | | 0°C | 7.8 | 8.7 | | |
| | | | | | 70°C | 7.8 | 8.7 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = –100 mV, | $I_{OL}$ = 0 | 25°C | | 0 | 50 | mV |
| | | | | | 0°C | | 0 | 50 | |
| | | | | | 70°C | | 0 | 50 | |
| $A_{VD}$ | Large-signal differential voltage amplification | | $V_O$ = 1 V to 6 V, | $R_L$ = 100 kΩ | 25°C | 25 | 275 | | V/mV |
| | | | | | 0°C | 15 | 320 | | |
| | | | | | 70°C | 15 | 230 | | |
| CMRR | Common-mode rejection ratio | | $V_{IC}$ = $V_{ICR}$min | | 25°C | 65 | 94 | | dB |
| | | | | | 0°C | 60 | 94 | | |
| | | | | | 70°C | 60 | 94 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | | $V_{DD}$ = 5 V to 10 V, | $V_O$ = 1.4 V | 25°C | 70 | 93 | | dB |
| | | | | | 0°C | 60 | 92 | | |
| | | | | | 70°C | 60 | 94 | | |
| $I_{DD}$ | Supply current (two amplifiers) | | $V_O$ = 5 V, No load | $V_{IC}$ = 5 V, | 25°C | | 285 | 600 | μA |
| | | | | | 0°C | | 345 | 800 | |
| | | | | | 70°C | | 220 | 560 | |

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | $T_A$† | TLC27M2I TLC27M2AI TLC27M2BI TLC27M7I | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | TLC27M2I | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 1.1 | 10 | mV |
| | | | | | Full range | | | 13 | |
| | | TLC27M2AI | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 0.9 | 5 | |
| | | | | | Full range | | | 7 | |
| | | TLC27M2BI | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 220 | 2000 | μV |
| | | | | | Full range | | | 3500 | |
| | | TLC27M7I | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 185 | 500 | |
| | | | | | Full range | | | 2000 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | | | 25°C to 85°C | | 1.7 | | μV/°C |
| $I_{IO}$ | Input offset current (see Note 4) | | $V_O$ = 2.5 V, | $V_{IC}$ = 2.5 V | 25°C | | 0.1 | | pA |
| | | | | | 85°C | | 24 | 1000 | |
| $I_{IB}$ | Input bias current (see Note 4) | | $V_O$ = 2.5 V, | $V_{IC}$ = 2.5 V | 25°C | | 0.6 | | pA |
| | | | | | 85°C | | 200 | 2000 | |
| $V_{ICR}$ | Common-mode input voltage range (see Note 5) | | | | 25°C | −0.2 to 4 | −0.3 to 4.2 | | V |
| | | | | | Full range | −0.2 to 3.5 | | | V |
| $V_{OH}$ | High-level output voltage | | $V_{ID}$ = 100 mV, | $R_L$ = 100 kΩ | 25°C | 3.2 | 3.9 | | V |
| | | | | | −40°C | 3 | 3.9 | | |
| | | | | | 85°C | 3 | 4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = –100 mV, | $I_{OL}$ = 0 | 25°C | | 0 | 50 | mV |
| | | | | | −40°C | | 0 | 50 | |
| | | | | | 85°C | | 0 | 50 | |
| $A_{VD}$ | Large-signal differential voltage amplification | | $V_O$ = 0.25 V to 2 V, | $R_L$ = 100 kΩ | 25°C | 25 | 170 | | V/mV |
| | | | | | −40°C | 15 | 270 | | |
| | | | | | 85°C | 15 | 130 | | |
| CMRR | Common-mode rejection ratio | | $V_{IC}$ = $V_{ICR}$min | | 25°C | 65 | 91 | | dB |
| | | | | | −40°C | 60 | 90 | | |
| | | | | | 85°C | 60 | 90 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | | $V_{DD}$ = 5 V to 10 V, | $V_O$ = 1.4 V | 25°C | 70 | 93 | | dB |
| | | | | | −40°C | 60 | 91 | | |
| | | | | | 85°C | 60 | 94 | | |
| $I_{DD}$ | Supply current (two amplifiers) | | $V_O$ = 2.5 V, No load | $V_{IC}$ = 2.5 V, | 25°C | | 210 | 560 | μA |
| | | | | | −40°C | | 315 | 800 | |
| | | | | | 85°C | | 160 | 400 | |

† Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 10 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | $T_A$† | TLC27M2I TLC27M2AI TLC27M2BI TLC27M7I | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | TLC27M2I | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 1.1 | 10 | mV |
| | | | | | Full range | | | 13 | |
| | | TLC27M2AI | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 0.9 | 5 | |
| | | | | | Full range | | | 7 | |
| | | TLC27M2BI | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 224 | 2000 | μV |
| | | | | | Full range | | | 3500 | |
| | | TLC27M7I | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 190 | 800 | |
| | | | | | Full range | | | 2900 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | | | 25°C to 85°C | | 2.1 | | μV/°C |
| $I_{IO}$ | Input offset current (see Note 4) | | $V_O$ = 5 V, | $V_{IC}$ = 5 V | 25°C | | 0.1 | | pA |
| | | | | | 85°C | | 26 | 1000 | |
| $I_{IB}$ | Input bias current (see Note 4) | | $V_O$ = 5 V, | $V_{IC}$ = 5 V | 25°C | | 0.7 | | pA |
| | | | | | 85°C | | 220 | 2000 | |
| $V_{ICR}$ | Common-mode input voltage range (see Note 5) | | | | 25°C | −0.2 to 9 | −0.3 to 9.2 | | V |
| | | | | | Full range | −0.2 to 8.5 | | | V |
| $V_{OH}$ | High-level output voltage | | $V_{ID}$ = 100 mV, | $R_L$ = 100 kΩ | 25°C | 8 | 8.7 | | V |
| | | | | | −40°C | 7.8 | 8.7 | | |
| | | | | | 85°C | 7.8 | 8.7 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = −100 mV, | $I_{OL}$ = 0 | 25°C | | 0 | 50 | mV |
| | | | | | −40°C | | 0 | 50 | |
| | | | | | 85°C | | 0 | 50 | |
| $A_{VD}$ | Large-signal differential voltage amplification | | $V_O$ = 1 V to 6 V, | $R_L$ = 100 kΩ | 25°C | 25 | 275 | | V/mV |
| | | | | | −40°C | 15 | 390 | | |
| | | | | | 85°C | 15 | 220 | | |
| CMRR | Common-mode rejection ratio | | $V_{IC}$ = $V_{ICR}$min | | 25°C | 65 | 94 | | dB |
| | | | | | −40°C | 60 | 93 | | |
| | | | | | 85°C | 60 | 94 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | | $V_{DD}$ = 5 V to 10 V, | $V_O$ = 1.4 V | 25°C | 70 | 93 | | dB |
| | | | | | −40°C | 60 | 91 | | |
| | | | | | 85°C | 60 | 94 | | |
| $I_{DD}$ | Supply current | | $V_O$ = 5 V, No load | $V_{IC}$ = 5 V, | 25°C | | 285 | 600 | μA |
| | | | | | −40°C | | 450 | 900 | |
| | | | | | 85°C | | 205 | 520 | |

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | $T_A$† | TLC27M2M TLC27M7M | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | TLC27M2M | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 1.1 | 10 | mV |
| | | | | | Full range | | | 12 | |
| | | TLC27M7M | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 185 | 500 | |
| | | | | | Full range | | | 3750 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | | | 25°C to 125°C | | 1.7 | | µV/°C |
| $I_{IO}$ | Input offset current (see Note 4) | | $V_O$ = 2.5 V, | $V_{IC}$ = 2.5 V | 25°C | | 0.1 | | pA |
| | | | | | 125°C | | 1.4 | 15 | nA |
| $I_{IB}$ | Input bias current (see Note 4) | | $V_O$ = 2.5 V, | $V_{IC}$ = 2.5 V | 25°C | | 0.6 | | pA |
| | | | | | 125°C | | 9 | 35 | nA |
| $V_{ICR}$ | Common-mode input voltage range (see Note 5) | | | | 25°C | 0 to 4 | −0.3 to 4.2 | | V |
| | | | | | Full range | 0 to 3.5 | | | V |
| $V_{OH}$ | High-level output voltage | | $V_{ID}$ = 100 mV, | $R_L$ = 100 kΩ | 25°C | 3.2 | 3.9 | | V |
| | | | | | −55°C | 3 | 3.9 | | |
| | | | | | 125°C | 3 | 4 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = −100 mV, | $I_{OL}$ = 0 | 25°C | | 0 | 50 | mV |
| | | | | | −55°C | | 0 | 50 | |
| | | | | | 125°C | | 0 | 50 | |
| $A_{VD}$ | Large-signal differential voltage amplification | | $V_O$ = 0.25 V to 2 V, | $R_L$ = 100 kΩ | 25°C | 25 | 170 | | V/mV |
| | | | | | −55°C | 15 | 290 | | |
| | | | | | 125°C | 15 | 120 | | |
| CMRR | Common-mode rejection ratio | | $V_{IC}$ = $V_{ICR}$min | | 25°C | 65 | 91 | | dB |
| | | | | | −55°C | 60 | 89 | | |
| | | | | | 125°C | 60 | 91 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | | $V_{DD}$ = 5 V to 10 V, | $V_O$ = 1.4 V | 25°C | 70 | 93 | | dB |
| | | | | | −55°C | 60 | 91 | | |
| | | | | | 125°C | 60 | 94 | | |
| $I_{DD}$ | Supply current (two amplifiers) | | $V_O$ = 2.5 V, No load | $V_{IC}$ = 2.5 V, | 25°C | | 210 | 560 | µA |
| | | | | | −55°C | | 340 | 880 | |
| | | | | | 125°C | | 140 | 360 | |

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 10 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | $T_A$† | TLC27M2M TLC27M7M | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | TLC27M2M | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 1.1 | 10 | mV |
| | | | | | Full range | | | 12 | |
| | | TLC27M7M | $V_O$ = 1.4 V, $R_S$ = 50 Ω, | $V_{IC}$ = 0, $R_L$ = 100 kΩ | 25°C | | 190 | 800 | |
| | | | | | Full range | | | 4300 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | | | 25°C to 125°C | | 2.1 | | µV/°C |
| $I_{IO}$ | Input offset current (see Note 4) | | $V_O$ = 5 V, | $V_{IC}$ = 5 V | 25°C | | 0.1 | | pA |
| | | | | | 125°C | | 1.8 | 15 | |
| $I_{IB}$ | Input bias current (see Note 4) | | $V_O$ = 5 V, | $V_{IC}$ = 5 V | 25°C | | 0.7 | | pA |
| | | | | | 125°C | | 10 | 35 | |
| $V_{ICR}$ | Common-mode input voltage range (see Note 5) | | | | 25°C | 0 to 9 | −0.3 to 9.2 | | V |
| | | | | | Full range | 0 to 8.5 | | | V |
| $V_{OH}$ | High-level output voltage | | $V_{ID}$ = 100 mV, | $R_L$ = 100 kΩ | 25°C | 8 | 8.7 | | V |
| | | | | | −55°C | 7.8 | 8.6 | | |
| | | | | | 125°C | 7.8 | 8.8 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = −100 mV, | $I_{OL}$ = 0 | 25°C | | 0 | 50 | mV |
| | | | | | −55°C | | 0 | 50 | |
| | | | | | 125°C | | 0 | 50 | |
| $A_{VD}$ | Large-signal differential voltage amplification | | $V_O$ = 1 V to 6 V, | $R_L$ = 100 kΩ | 25°C | 25 | 275 | | V/mV |
| | | | | | −55°C | 15 | 420 | | |
| | | | | | 125°C | 15 | 190 | | |
| CMRR | Common-mode rejection ratio | | $V_{IC}$ = $V_{ICR}$min | | 25°C | 65 | 94 | | dB |
| | | | | | −55°C | 60 | 93 | | |
| | | | | | 125°C | 60 | 93 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | | $V_{DD}$ = 5 V to 10 V, | $V_O$ = 1.4 V | 25°C | 70 | 93 | | dB |
| | | | | | −55°C | 60 | 91 | | |
| | | | | | 125°C | 60 | 94 | | |
| $I_{DD}$ | Supply current (two amplifiers) | | $V_O$ = 5 V, No load | $V_{IC}$ = 5 V, | 25°C | | 285 | 600 | µA |
| | | | | | −55°C | | 490 | 1000 | |
| | | | | | 125°C | | 180 | 480 | |

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

## operating characteristics at specified free-air temperature, $V_{DD}$ = 5 V

| PARAMETER | | TEST CONDITIONS | | $T_A$ | TLC27M2C, TLC27M2AC, TLC27M2BC, TLC27M7C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| SR | Slew rate at unity gain | $R_L$ = 100 kΩ, $C_L$ = 20 pF, See Figure 1 | $V_{I(PP)}$ = 1 V | 25°C | | 0.43 | | V/μs |
| | | | | 0°C | | 0.46 | | |
| | | | | 70°C | | 0.36 | | |
| | | | $V_{I(PP)}$ = 2.5 V | 25°C | | 0.40 | | |
| | | | | 0°C | | 0.43 | | |
| | | | | 70°C | | 0.34 | | |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz, See Figure 2 | $R_S$ = 20 Ω, | 25°C | | 32 | | nV/√Hz |
| $B_{OM}$ | Maximum output-swing bandwidth | $V_O = V_{OH}$, $R_L$ = 100 kΩ, | $C_L$ = 20 pF, See Figure 1 | 25°C | | 55 | | kHz |
| | | | | 0°C | | 60 | | |
| | | | | 70°C | | 50 | | |
| $B_1$ | Unity-gain bandwidth | $V_I$ = 10 mV, See Figure 3 | $C_L$ = 20 pF, | 25°C | | 525 | | kHz |
| | | | | 0°C | | 600 | | |
| | | | | 70°C | | 400 | | |
| $\phi_m$ | Phase margin | $V_I$ = 10 mV, $C_L$ = 20 pF, | f = $B_1$, See Figure 3 | 25°C | | 40° | | |
| | | | | 0°C | | 41° | | |
| | | | | 70°C | | 39° | | |

## operating characteristics at specified free-air temperature, $V_{DD}$ = 10 V

| PARAMETER | | TEST CONDITIONS | | $T_A$ | TLC27M2C, TLC27M2AC, TLC27M2BC, TLC27M7C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| SR | Slew rate at unity gain | $R_L$ = 100 kΩ, $C_L$ = 20 pF, See Figure 1 | $V_{I(PP)}$ = 1 V | 25°C | | 0.62 | | V/μs |
| | | | | 0°C | | 0.67 | | |
| | | | | 70°C | | 0.51 | | |
| | | | $V_{I(PP)}$ = 5.5 V | 25°C | | 0.56 | | |
| | | | | 0°C | | 0.61 | | |
| | | | | 70°C | | 0.46 | | |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz, See Figure 2 | $R_S$ = 20 Ω, | 25°C | | 32 | | nV/√Hz |
| $B_{OM}$ | Maximum output-swing bandwidth | $V_O = V_{OH}$, $R_L$ = 100 kΩ, | $C_L$ = 20 pF, See Figure 1 | 25°C | | 35 | | kHz |
| | | | | 0°C | | 40 | | |
| | | | | 70°C | | 30 | | |
| $B_1$ | Unity-gain bandwidth | $V_I$ = 10 mV, See Figure 3 | $C_L$ = 20 pF, | 25°C | | 635 | | kHz |
| | | | | 0°C | | 710 | | |
| | | | | 70°C | | 510 | | |
| $\phi_m$ | Phase margin | $V_I$ = 10 mV, $C_L$ = 20 pF, | f = $B_1$, See Figure 3 | 25°C | | 43° | | |
| | | | | 0°C | | 44° | | |
| | | | | 70°C | | 42° | | |

## operating characteristics at specified free-air temperature, $V_{DD}$ = 5 V

| PARAMETER | | TEST CONDITIONS | | $T_A$ | TLC27M2I TLC27M2AI TLC27M2BI TLC27M7I | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| SR | Slew rate at unity gain | $R_L$ = 100 kΩ, $C_L$ = 20 pF, See Figure 1 | $V_{I(PP)}$ = 1 V | 25°C | | 0.43 | | V/µs |
| | | | | –40°C | | 0.51 | | |
| | | | | 85°C | | 0.35 | | |
| | | | $V_{I(PP)}$ = 2.5 V | 25°C | | 0.40 | | |
| | | | | –40°C | | 0.48 | | |
| | | | | 85°C | | 0.32 | | |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz, See Figure 2 | $R_S$ = 20 Ω, | 25°C | | 32 | | nV/√Hz |
| $B_{OM}$ | Maximum output-swing bandwidth | $V_O = V_{OH}$, $R_L$ = 100 kΩ, | $C_L$ = 20 pF, See Figure 1 | 25°C | | 55 | | kHz |
| | | | | –40°C | | 75 | | |
| | | | | 85°C | | 45 | | |
| $B_1$ | Unity-gain bandwidth | $V_I$ = 10 mV, See Figure 3 | $C_L$ = 20 pF, | 25°C | | 525 | | MHz |
| | | | | –40°C | | 770 | | |
| | | | | 85°C | | 370 | | |
| $\phi_m$ | Phase margin | $V_I$ = 10 mV, $C_L$ = 20 pF, | f = $B_1$, See Figure 3 | 25°C | | 40° | | |
| | | | | –40°C | | 43° | | |
| | | | | 85°C | | 38° | | |

## operating characteristics at specified free-air temperature, $V_{DD}$ = 10 V

| PARAMETER | | TEST CONDITIONS | | $T_A$ | TLC27M2I TLC27M2AI TLC27M2BI TLC27M7I | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| SR | Slew rate at unity gain | $R_L$ = 100 kΩ, $C_L$ = 20 pF, See Figure 1 | $V_{I(PP)}$ = 1 V | 25°C | | 0.62 | | V/µs |
| | | | | –40°C | | 0.77 | | |
| | | | | 85°C | | 0.47 | | |
| | | | $V_{I(PP)}$ = 5.5 V | 25°C | | 0.56 | | |
| | | | | –40°C | | 0.70 | | |
| | | | | 85°C | | 0.44 | | |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz, See Figure 2 | $R_S$ = 20 Ω, | 25°C | | 32 | | nV/√Hz |
| $B_{OM}$ | Maximum output-swing bandwidth | $V_O = V_{OH}$, $R_L$ = 100 kΩ, | $C_L$ = 20 pF, See Figure 1 | 25°C | | 35 | | kHz |
| | | | | –40°C | | 45 | | |
| | | | | 85°C | | 25 | | |
| $B_1$ | Unity-gain bandwidth | $V_I$ = 10 mV, See Figure 3 | $C_L$ = 20 pF, | 25°C | | 635 | | MHz |
| | | | | –40°C | | 880 | | |
| | | | | 85°C | | 480 | | |
| $\phi_m$ | Phase margin | $V_I$ = 10 mV, $C_L$ = 20 pF, | f = $B_1$, See Figure 3 | 25°C | | 43° | | |
| | | | | –40°C | | 46° | | |
| | | | | 85°C | | 41° | | |

## operating characteristics at specified free-air temperature, $V_{DD}$ = 5 V

| PARAMETER | | TEST CONDITIONS | | $T_A$ | TLC27M2M TLC27M7M | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| SR | Slew rate at unity gain | $R_L$ = 100 kΩ, $C_L$ = 20 pF, See Figure 1 | $V_{I(PP)}$ = 1 V | 25°C | | 0.43 | | V/μs |
| | | | | –55°C | | 0.54 | | |
| | | | | 125°C | | 0.29 | | |
| | | | $V_{I(PP)}$ = 2.5 V | 25°C | | 0.40 | | |
| | | | | –55°C | | 0.49 | | |
| | | | | 125°C | | 0.28 | | |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz, See Figure 2 | $R_S$ = 20 Ω, | 25°C | | 32 | | nV/√Hz |
| $B_{OM}$ | Maximum output-swing bandwidth | $V_O = V_{OH}$, $R_L$ = 100 kΩ, | $C_L$ = 20 pF, See Figure 1 | 25°C | | 55 | | kHz |
| | | | | –55°C | | 80 | | |
| | | | | 125°C | | 40 | | |
| $B_1$ | Unity-gain bandwidth | $V_I$ = 10 mV, See Figure 3 | $C_L$ = 20 pF, | 25°C | | 525 | | kHz |
| | | | | –55°C | | 850 | | |
| | | | | 125°C | | 330 | | |
| $\phi_m$ | Phase margin | $V_I$ = 10 mV, $C_L$ = 20 pF, | f = $B_1$, See Figure 3 | 25°C | | 40° | | |
| | | | | –55°C | | 44° | | |
| | | | | 125°C | | 36° | | |

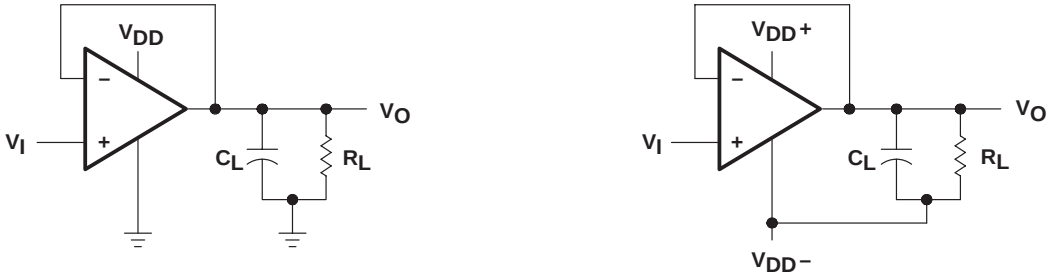
## operating characteristics at specified free-air temperature, $V_{DD}$ = 10 V

| PARAMETER | | TEST CONDITIONS | | $T_A$ | TLC27M2M TLC27M7M | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| SR | Slew rate at unity gain | $R_L$ = 100 kΩ, $C_L$ = 20 pF, See Figure 1 | $V_{I(PP)}$ = 1 V | 25°C | | 0.62 | | V/μs |
| | | | | –55°C | | 0.81 | | |
| | | | | 125°C | | 0.38 | | |
| | | | $V_{I(PP)}$ = 5.5 V | 25°C | | 0.56 | | |
| | | | | –55°C | | 0.73 | | |
| | | | | 125°C | | 0.35 | | |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz, See Figure 2 | $R_S$ = 20 Ω, | 25°C | | 32 | | nV/√Hz |
| $B_{OM}$ | Maximum output-swing bandwidth | $V_O = V_{OH}$, $R_L$ = 100 kΩ, | $C_L$ = 20 pF, See Figure 1 | 25°C | | 35 | | kHz |
| | | | | –55°C | | 50 | | |
| | | | | 125°C | | 20 | | |
| $B_1$ | Unity gain bandwidth | $V_I$ = 10 mV, See Figure 3 | $C_L$ = 20 pF, | 25°C | | 635 | | kHz |
| | | | | –55°C | | 960 | | |
| | | | | 125°C | | 440 | | |
| $\phi_m$ | Phase margin | $V_I$ = 10 mV, $C_L$ = 20 pF, | f = $B_1$, See Figure 3 | 25°C | | 43° | | |
| | | | | –55°C | | 47° | | |
| | | | | 125°C | | 39° | | |

## PARAMETER MEASUREMENT INFORMATION

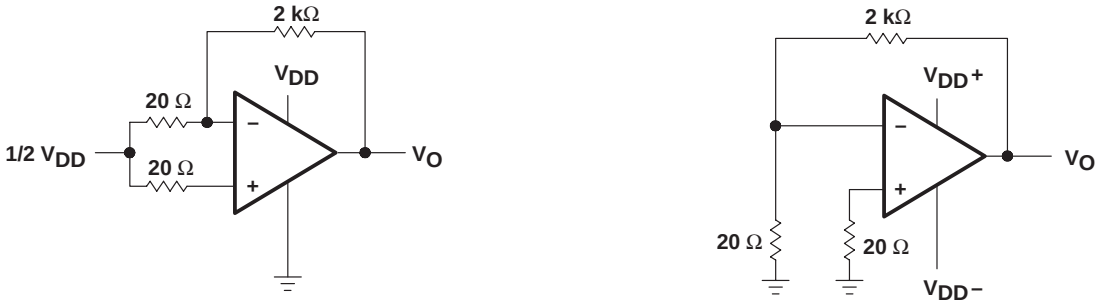
### single-supply versus split-supply test circuits

Because the TLC27M2 and TLC27M7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



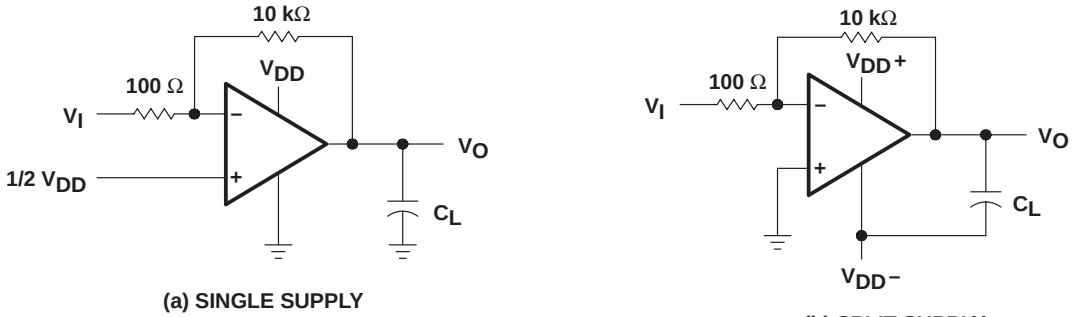

(a) SINGLE SUPPLY (b) SPLIT SUPPLY

**Figure 1. Unity-Gain Amplifier**




(a) SINGLE SUPPLY (b) SPLIT SUPPLY

**Figure 2. Noise-Test Circuit**




(a) SINGLE SUPPLY (b) SPLIT SUPPLY

**Figure 3. Gain-of-100 Inverting Amplifier**

## PARAMETER MEASUREMENT INFORMATION

### input bias current

Because of the high input impedance of the TLC27M2 and TLC27M7 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

   One word of caution—many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

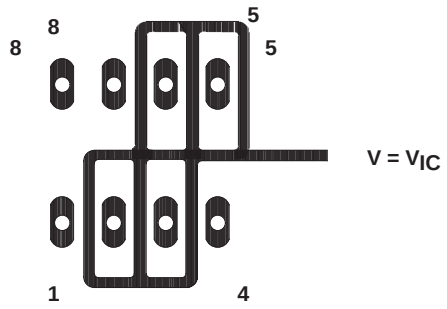



**Figure 4. Isolation Metal Around Device Inputs (JG and P packages)**

### low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

## PARAMETER MEASUREMENT INFORMATION

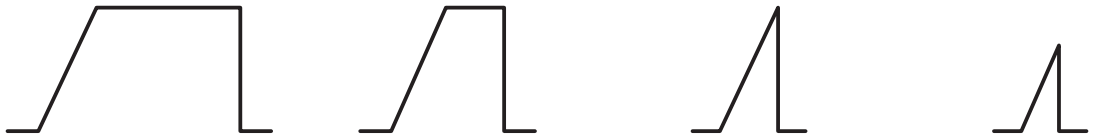
### input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage, since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

### full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



**(a) f = 1 kHz** **(b) $B_{OM}$ > f > 1 kHz** **(c) f = $B_{OM}$** **(d) f > $B_{OM}$**

**Figure 5. Full-Power-Response Output Signal**

### test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | Distribution | 6, 7 |
| $\alpha_{VIO}$ | Temperature coefficient | Distribution | 8, 9 |
| $V_{OH}$ | High-level output voltage | vs High-level output current<br>vs Supply voltage<br>vs Free-air temperature | 10, 11<br>12<br>13 |
| $V_{OL}$ | Low-level output voltage | vs Common-mode input voltage<br>vs Differential input voltage<br>vs Free-air temperature<br>vs Low-level output current | 14, 15<br>16<br>17<br>18, 19 |
| $A_{VD}$ | Differential voltage amplification | vs Supply voltage<br>vs Free-air temperature<br>vs Frequency | 20<br>21<br>32, 33 |
| $I_{IB}/I_{IO}$ | Input bias and input offset current | vs Free-air temperature | 22 |
| $V_{IC}$ | Common-mode input voltage | vs Supply voltage | 23 |
| $I_{DD}$ | Supply current | vs Supply voltage<br>vs Free-air temperature | 24<br>25 |
| SR | Slew rate | vs Supply voltage<br>vs Free-air temperature | 26<br>27 |
| | Normalized slew rate | vs Free-air temperature | 28 |
| $V_{O(PP)}$ | Maximum peak-to-peak output voltage | vs Frequency | 29 |
| $B_1$ | Unity-gain bandwidth | vs Free-air temperature<br>vs Supply voltage | 30<br>31 |
| $\phi_m$ | Phase margin | vs Supply voltage<br>vs Free-air temperature<br>vs Capacitive loads | 34<br>35<br>36 |
| $V_n$ | Equivalent input noise voltage | vs Frequency | 37 |
| $\phi$ | Phase shift | vs Frequency | 32, 33 |

## TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE**

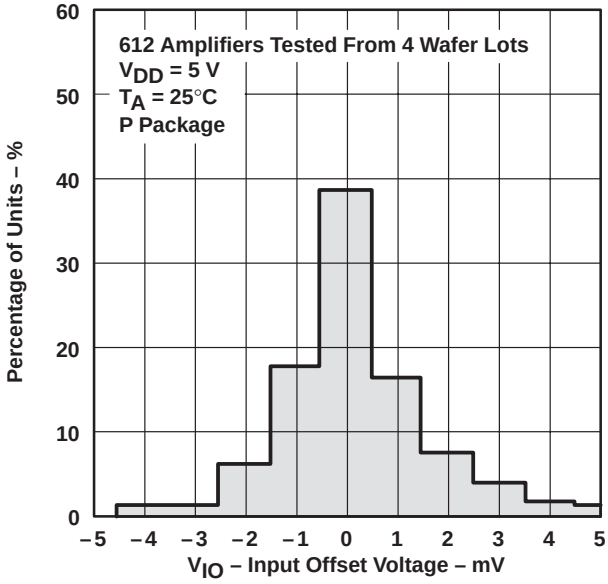



Figure 6

**DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE**

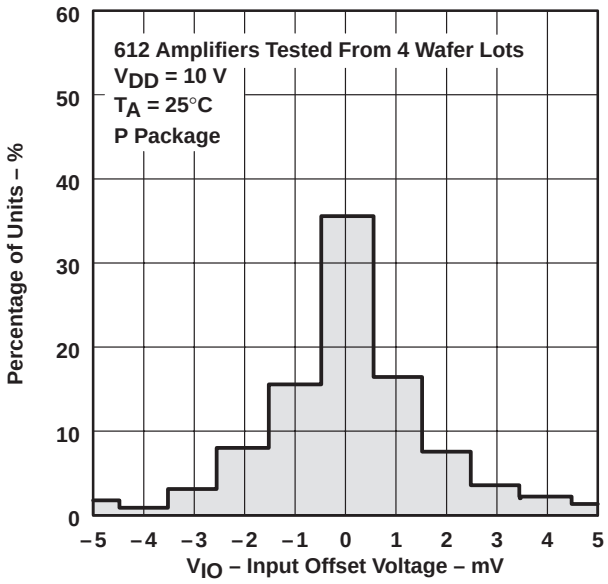



Figure 7

**DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

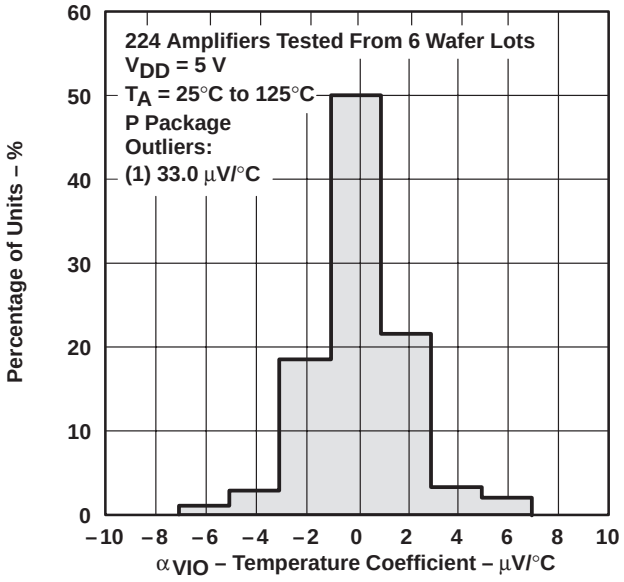



Figure 8

**DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

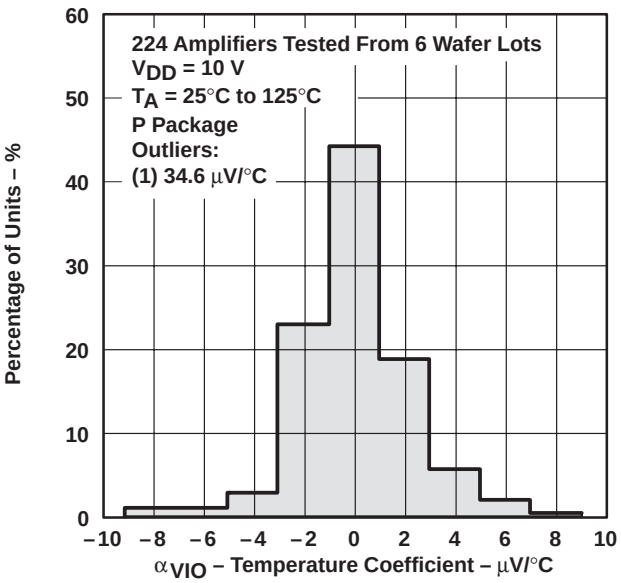



Figure 9

## TYPICAL CHARACTERISTICS†

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

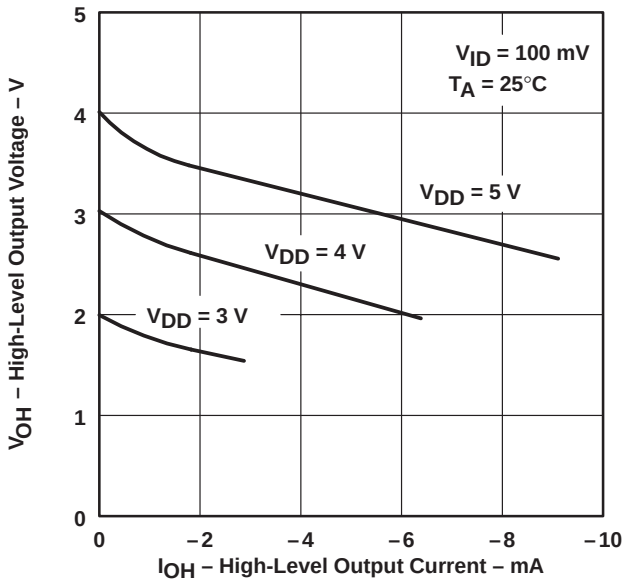



Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

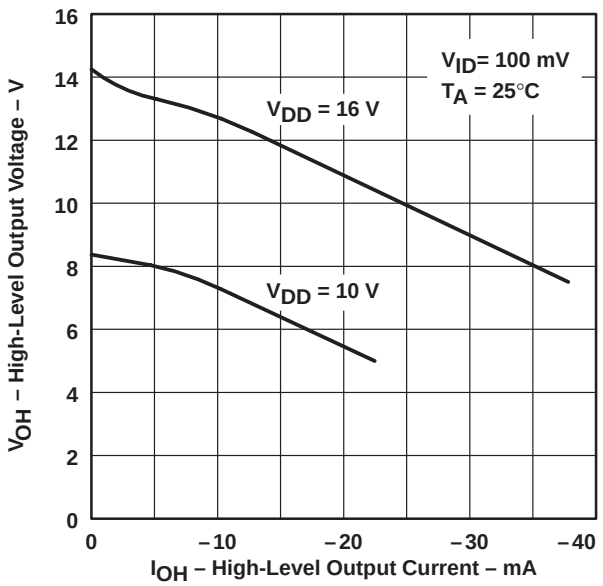



Figure 11

**HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE**

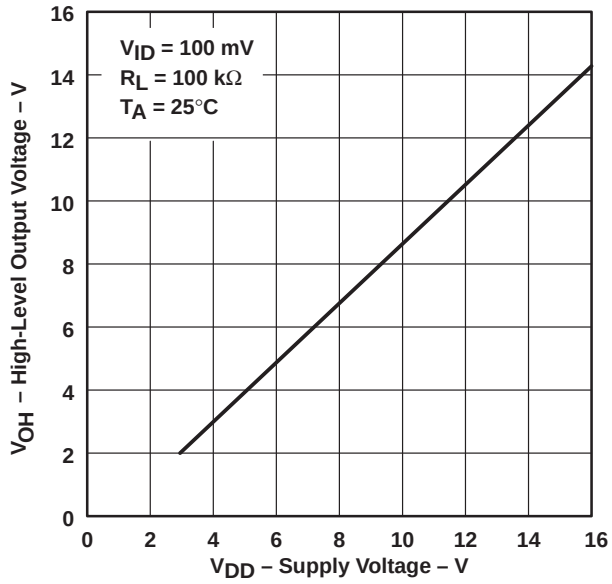



Figure 12

**HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

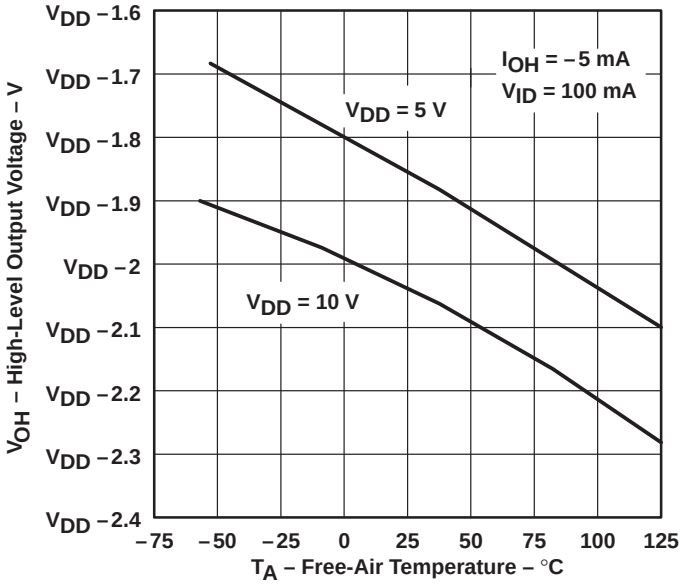



Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS†

**LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

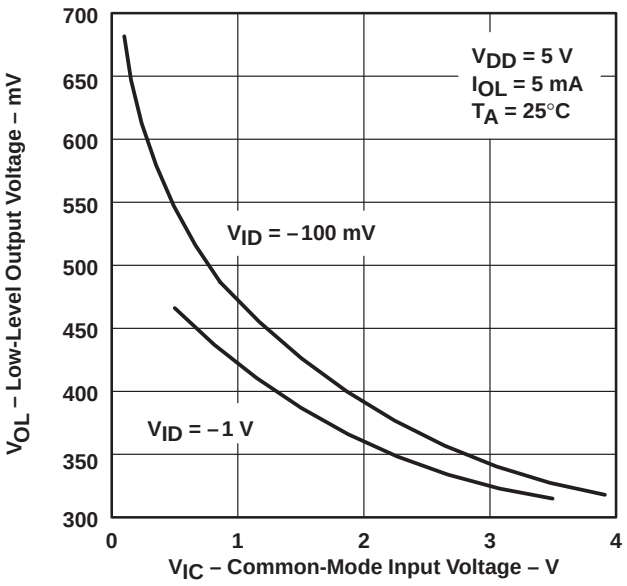



Figure 14

**LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

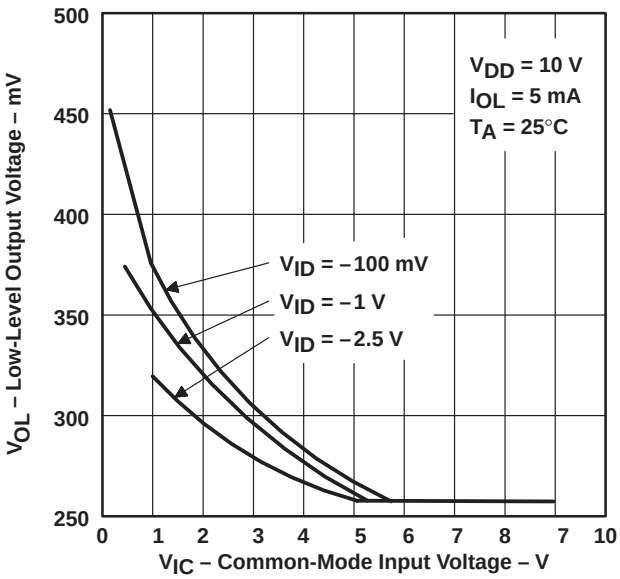



Figure 15

**LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE**

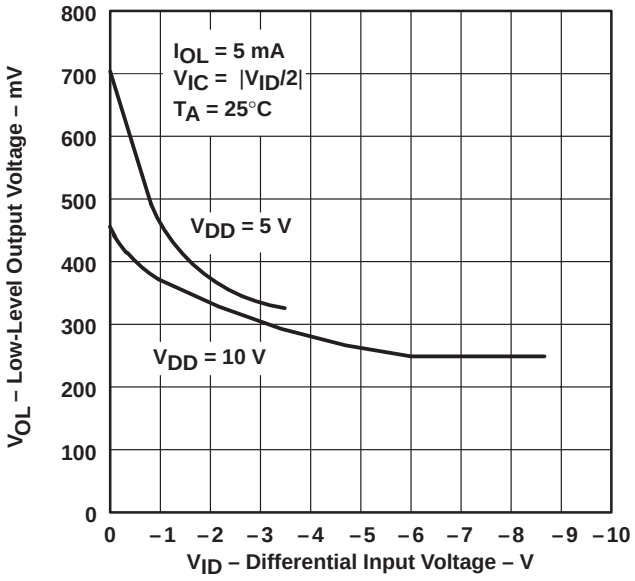



Figure 16

**LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

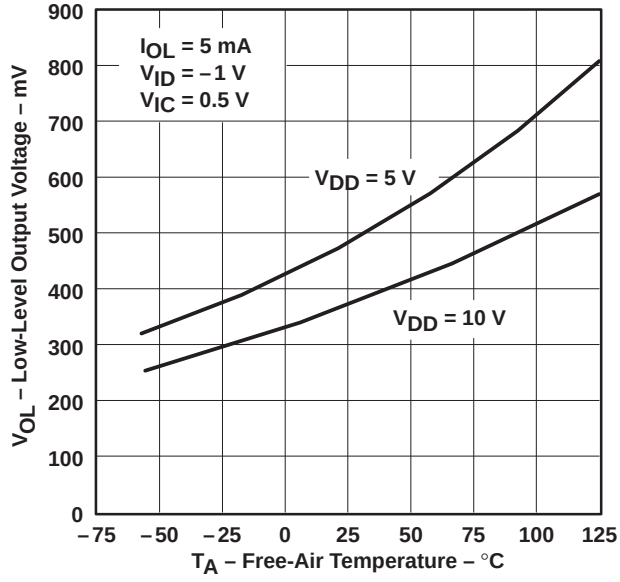



Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS†

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

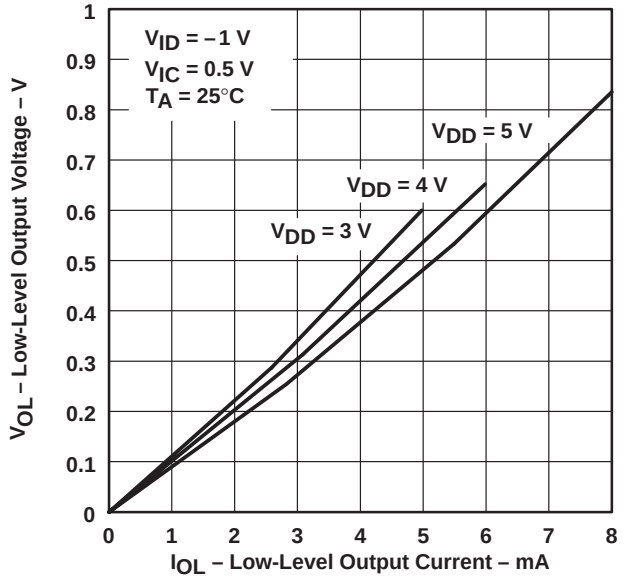



Figure 18

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

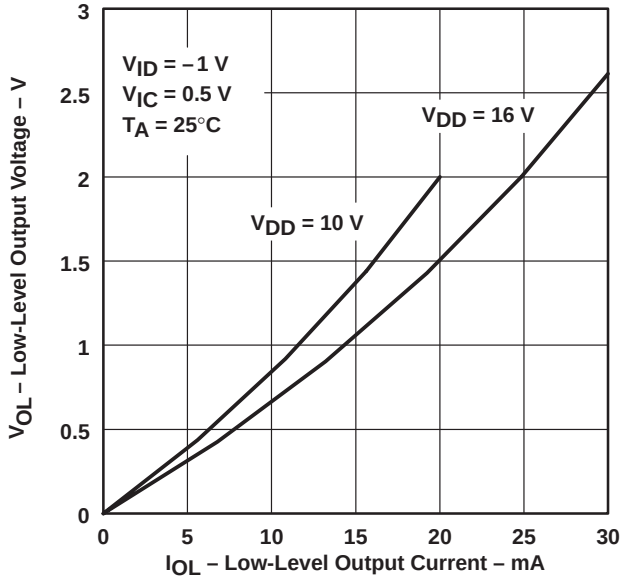



Figure 19

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE**

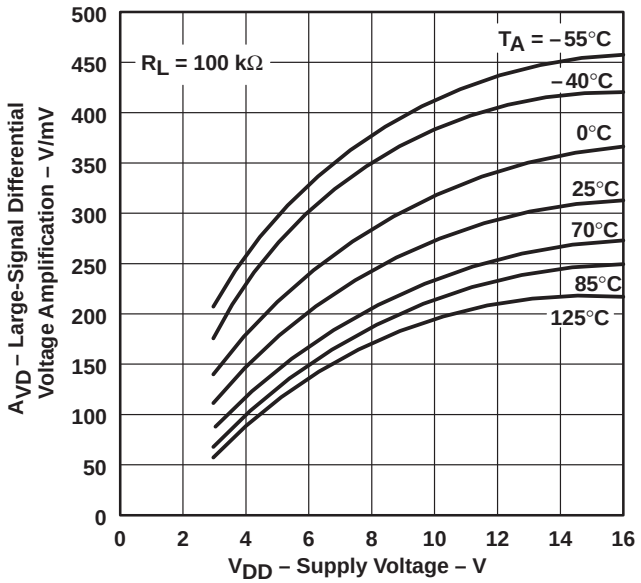



Figure 20

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE**

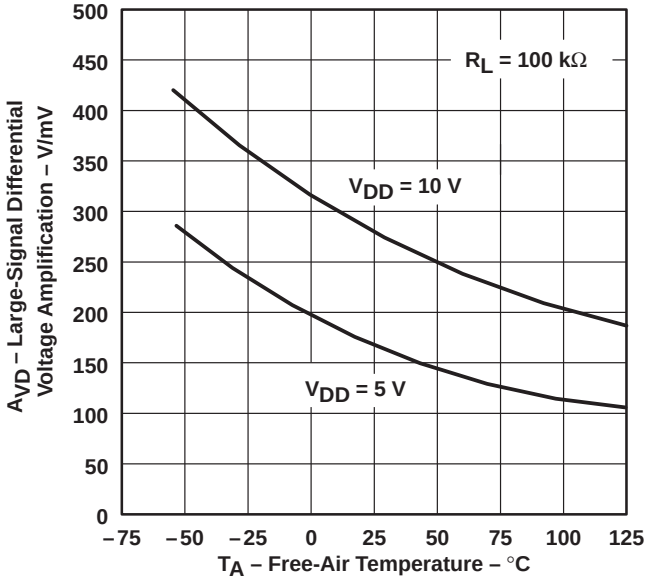
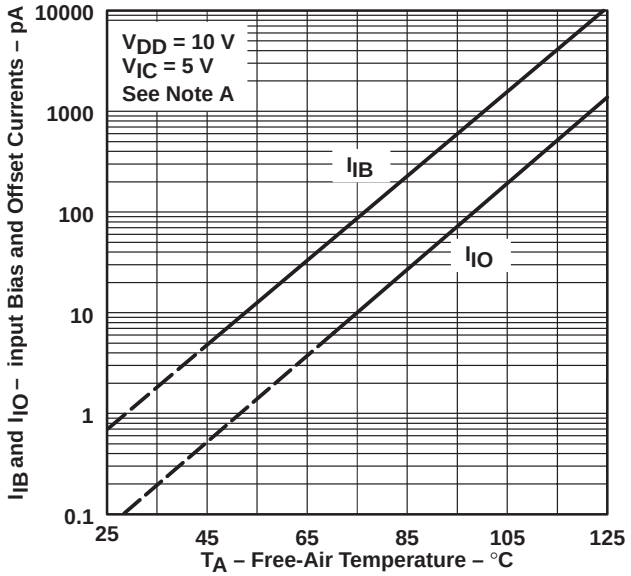



Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS†

**INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE**




NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

**Figure 22**

**COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE**

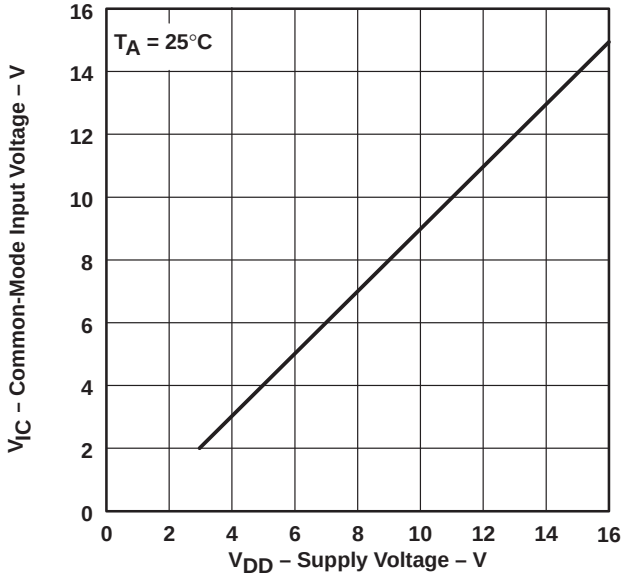



**Figure 23**

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

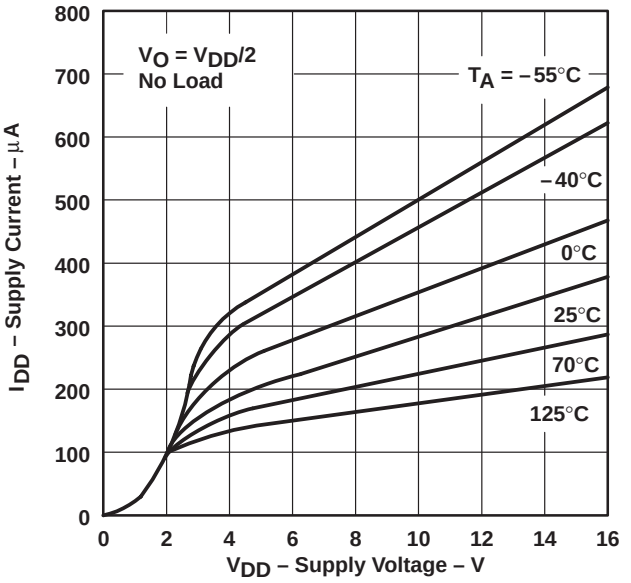



**Figure 24**

**SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

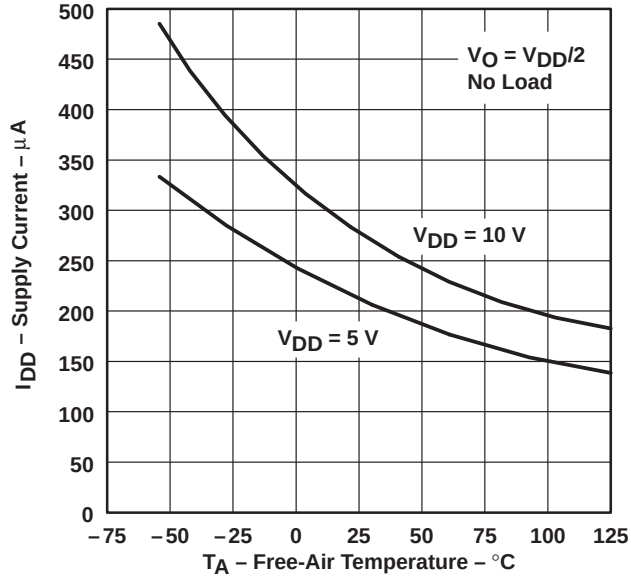



**Figure 25**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS†

**SLEW RATE vs SUPPLY VOLTAGE**

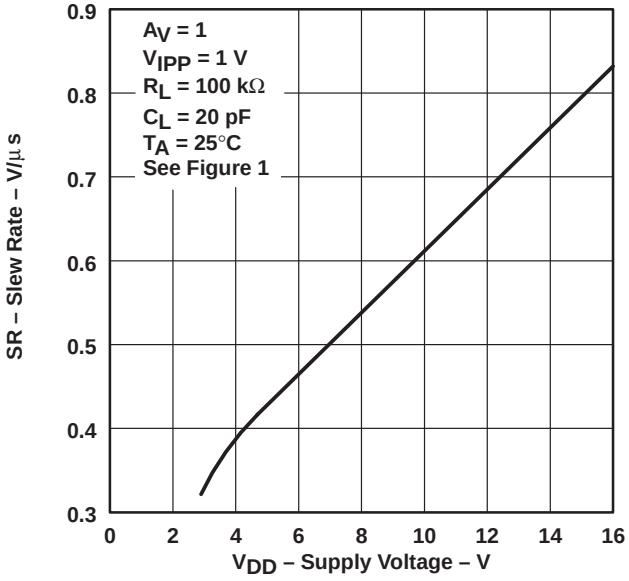



Figure 26

**SLEW RATE vs FREE-AIR TEMPERATURE**

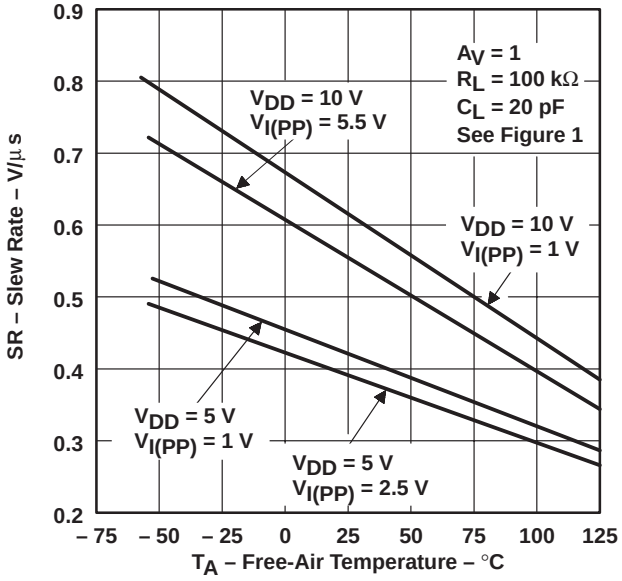



Figure 27

**NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE**

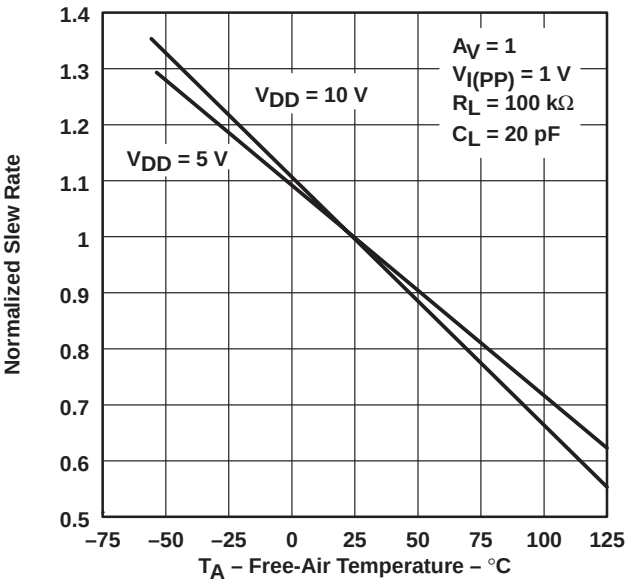



Figure 28

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY**

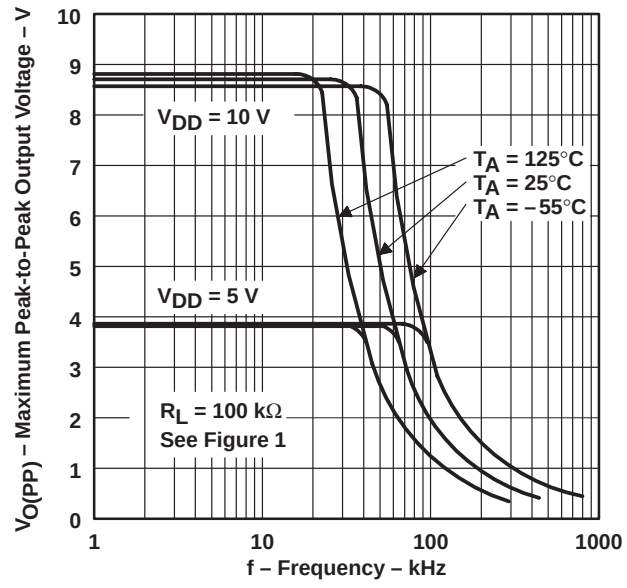



Figure 29

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS†

**UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE**

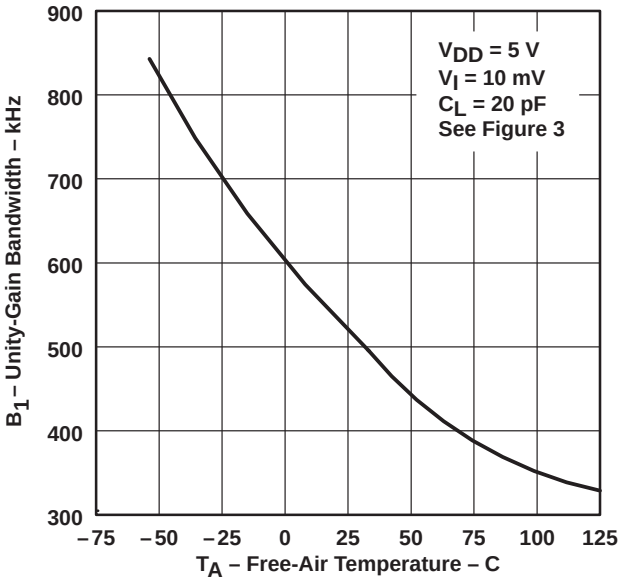



Figure 30

**UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE**

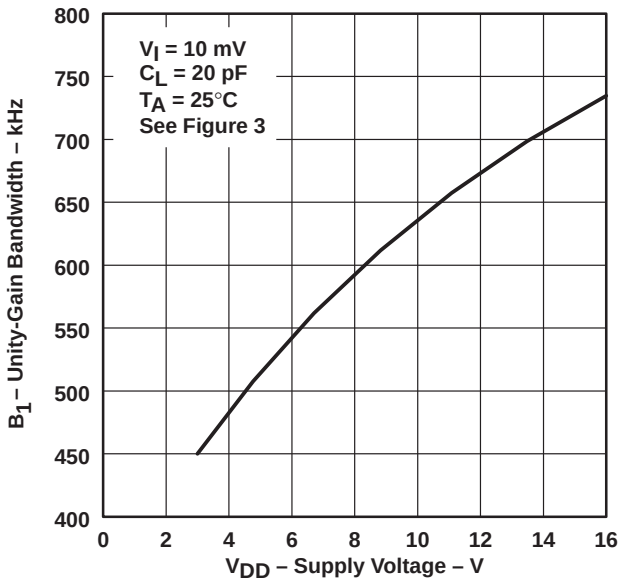



Figure 31

**LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY**

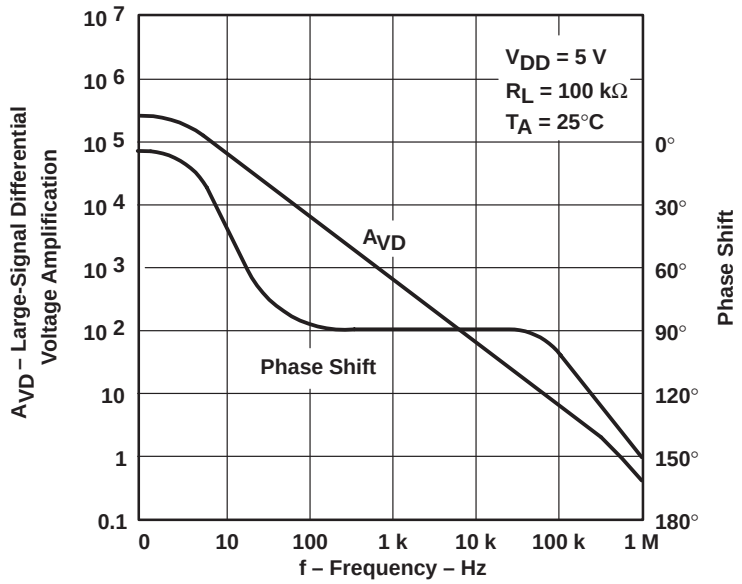



Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS†

**LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY**

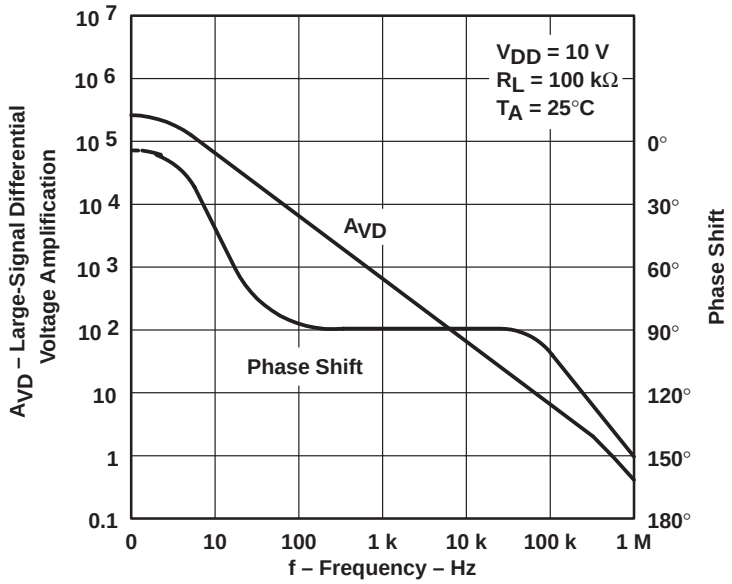



**Figure 33**

**PHASE MARGIN vs SUPPLY VOLTAGE**

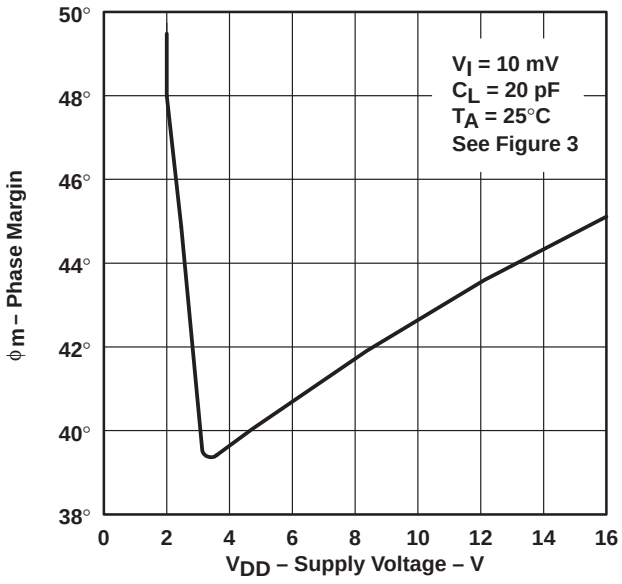



**Figure 34**

**PHASE MARGIN vs FREE-AIR TEMPERATURE**

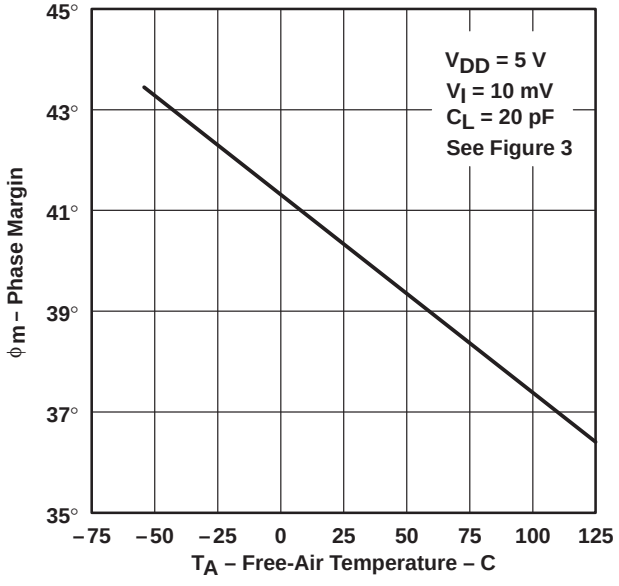



**Figure 35**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS

**PHASE MARGIN
vs
CAPACITIVE LOAD**

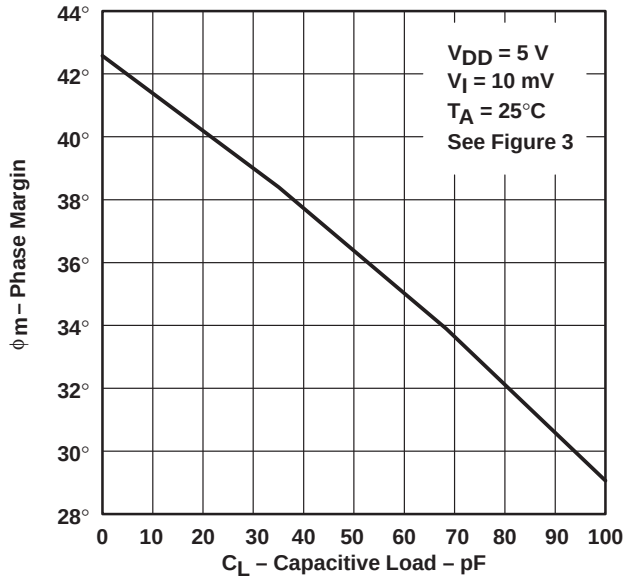



**Figure 36**

**EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY**

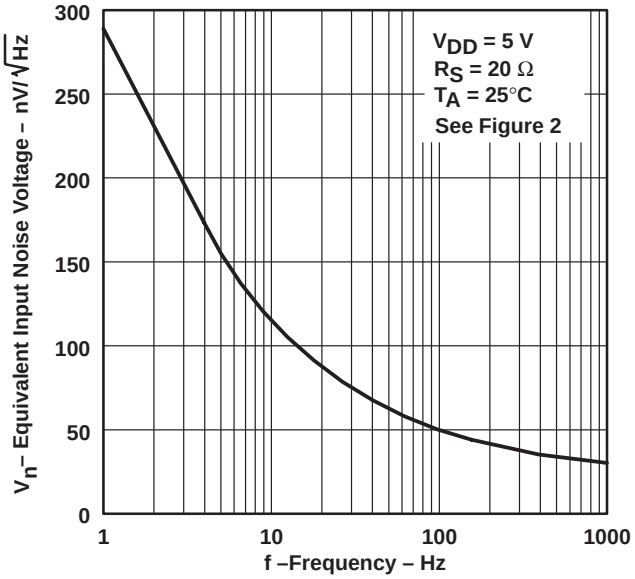



**Figure 37**

## APPLICATION INFORMATION

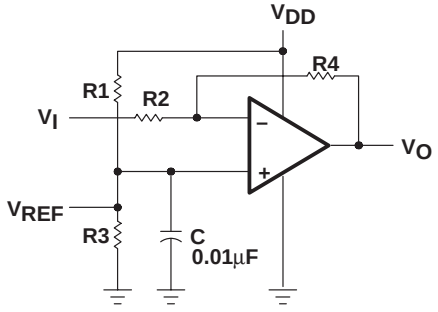
### single-supply operation

While the TLC27M2 and TLC27M7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M2 and TLC27M7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M2 and TLC27M7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.




$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

**Figure 38. Inverting Amplifier With Voltage Reference**

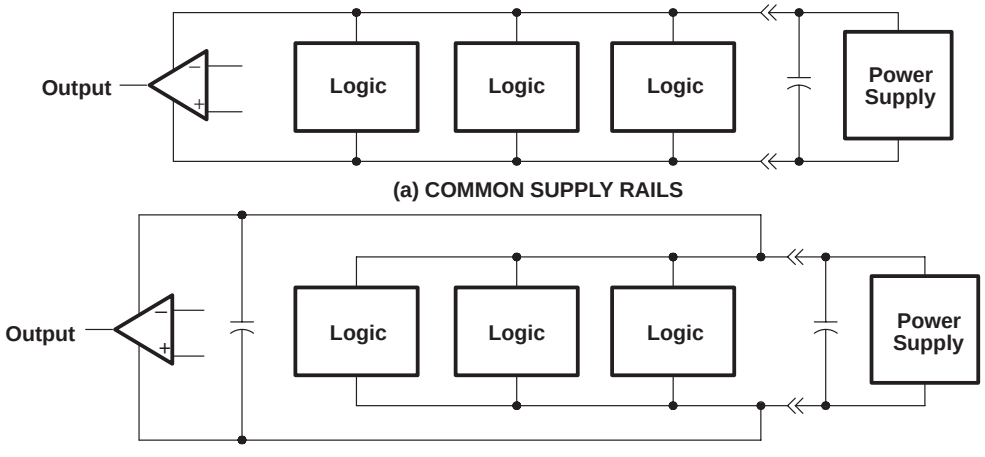



**Figure 39. Common Versus Separate Supply Rails**

## APPLICATION INFORMATION

### input characteristics

The TLC27M2 and TLC27M7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD}$ –1 V at $T_A$ = 25°C and at $V_{DD}$ –1.5 V at all other temperatures.

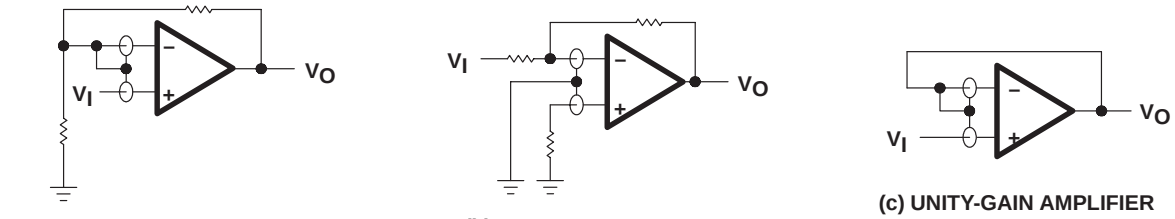
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M2 and TLC27M7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M2 and TLC27M7 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

### noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M2 and TLC27M7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.




(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

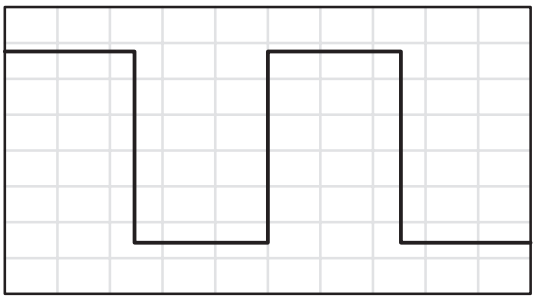
**Figure 40. Guard-Ring Schemes**

### output characteristics

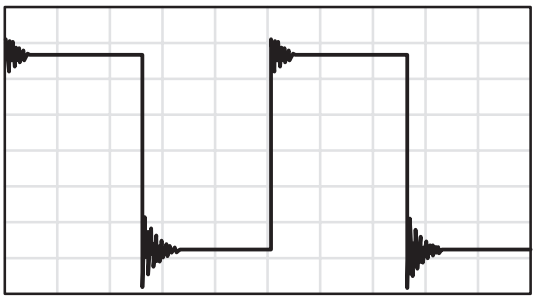
The output stage of the TLC27M2 and TLC27M7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M2 and TLC27M7 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

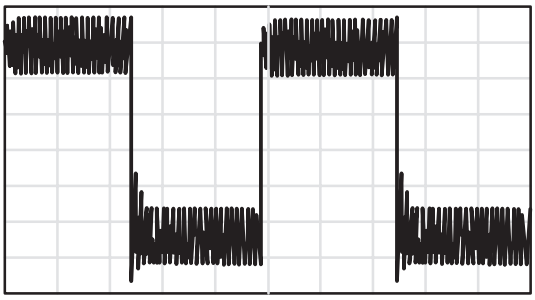
## APPLICATION INFORMATION



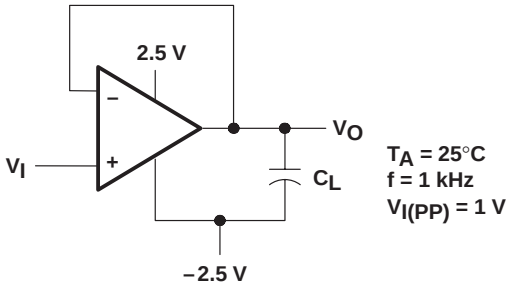
(a) $C_L$ = 20 pF, $R_L$ = NO LOAD



(b) $C_L$ = 170 pF, $R_L$ = NO LOAD



(c) $C_L$ = 190 pF, $R_L$ = NO LOAD




(d) TEST CIRCUIT

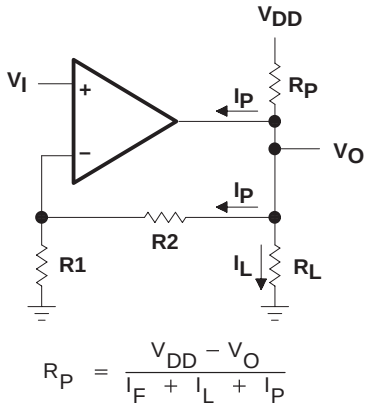
**Figure 41. Effect of Capacitive Loads and Test Circuit**

### output characteristics (continued)

Although the TLC27M2 and TLC27M7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor ($R_P$) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of $R_P$, a voltage offset from 0 V at the output occurs. Second, pullup resistor $R_P$ acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

## APPLICATION INFORMATION

### output characteristics (continued)




$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

**$I_P$ = Pullup current required by the operational amplifier (typically 500 μA)**

**Figure 42. Resistive Pullup to Increase $V_{OH}$**

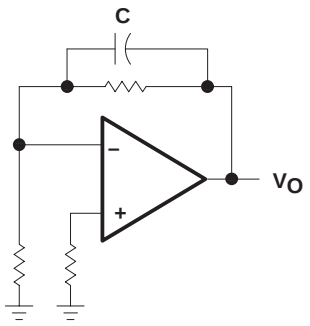



**Figure 43. Compensation for Input Capacitance**

### feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

### electrostatic-discharge protection

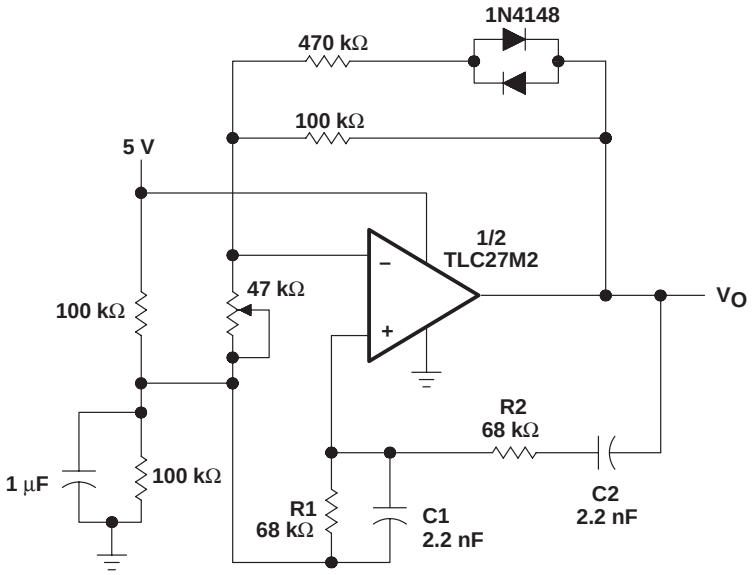
The TLC27M2 and TLC27M7 incorporate an internal electrostatic-discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

### latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27M2 and TLC27M7 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

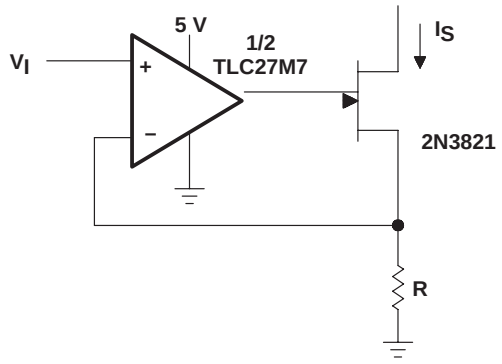
## APPLICATION INFORMATION




NOTES: $V_{O(PP)} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

**Figure 44. Wien Oscillator**

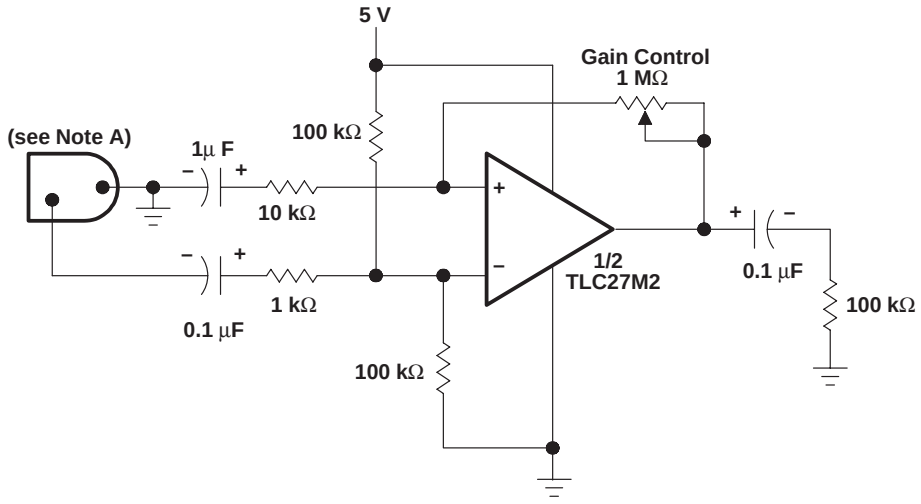



NOTES: $V_I = 0$ V to 3 V

$$I_S = \frac{V_I}{R}$$

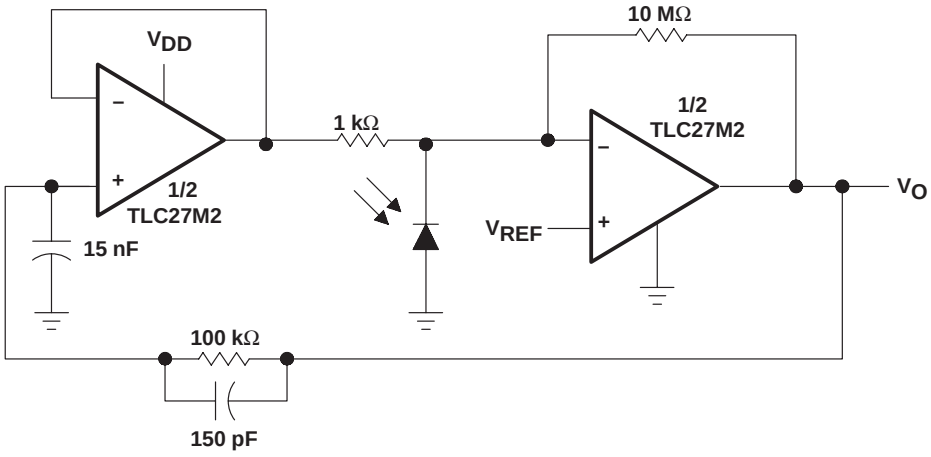
**Figure 45. Precision Low-Current Sink**

## APPLICATION INFORMATION




NOTE A: Low to medium impedance dynamic mike

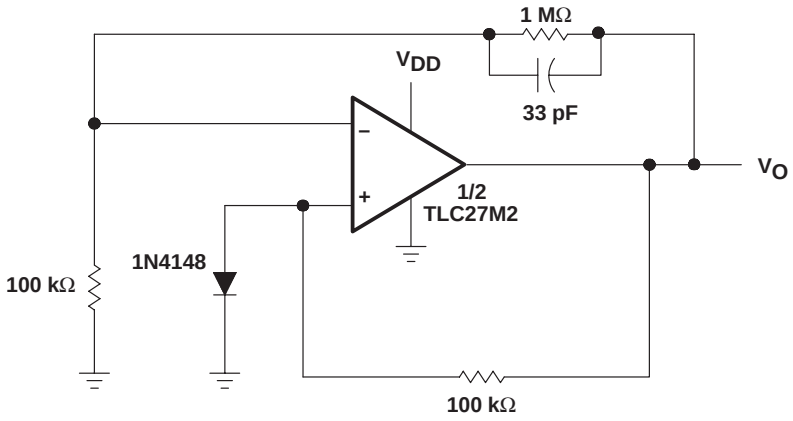
**Figure 46. Microphone Preamplifier**




NOTES: $V_{DD}$ = 4 V to 15 V
$V_{ref}$ = 0 V to $V_{DD}$ – 2 V

**Figure 47. Photo-Diode Amplifier With Ambient Light Rejection**

## APPLICATION INFORMATION




NOTES: $V_{DD}$ = 8 V to 16 V
$V_O$ = 5 V, 10 mA

**Figure 48. 5-V Low-Power Voltage Regulator**

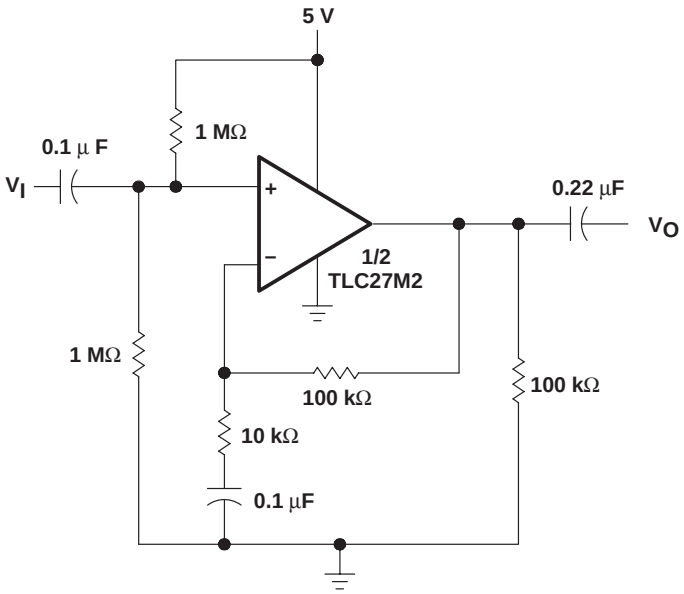



**Figure 49. Single-Rail AC Amplifiers**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TLC27M2ACD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2ACDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2ACDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2ACDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2ACP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2ACPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2AIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2AIDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2AIP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2AIPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2BCD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2BCDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2BCDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2BCDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2BCP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2BCPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2BID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2BIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2BIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2BIDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2BIP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2BIPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TLC27M2CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2CPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2CPSLE | OBSOLETE | SO | PS | 8 | | TBD | Call TI | Call TI |
| TLC27M2CPSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2CPSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2CPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2CPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2CPWLE | OBSOLETE | TSSOP | PW | 8 | | TBD | Call TI | Call TI |
| TLC27M2CPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2CPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2IPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M2IPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2IPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2IPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2MD | ACTIVE | SOIC | D | 8 | 75 | TBD | CU NIPDAU | Level-1-220C-UNLIM |
| TLC27M2MDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M2MDR | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI |
| TLC27M2MFKB | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| TLC27M2MJG | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| TLC27M2MJGB | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |
| TLC27M7CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M7CPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M7CPSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7CPSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TLC27M7IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M7IPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| TLC27M7MFKB | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| TLC27M7MJG | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |
| TLC27M7MJGB | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |
| TLC27M7MUB | OBSOLETE | CFP | U | 10 | | TBD | Call TI | Call TI |

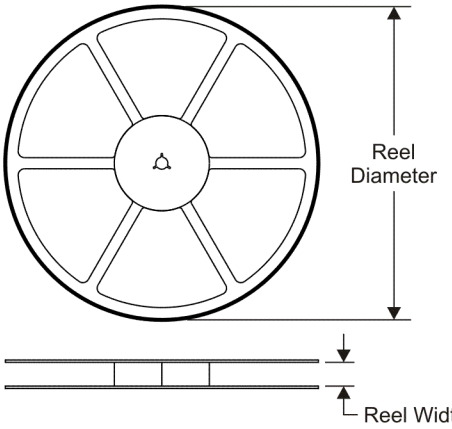
[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

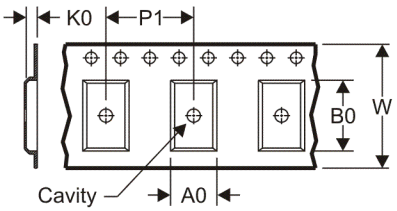
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

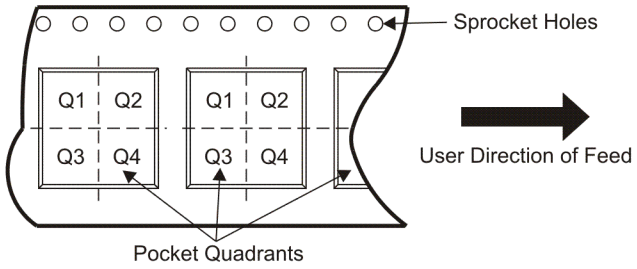



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

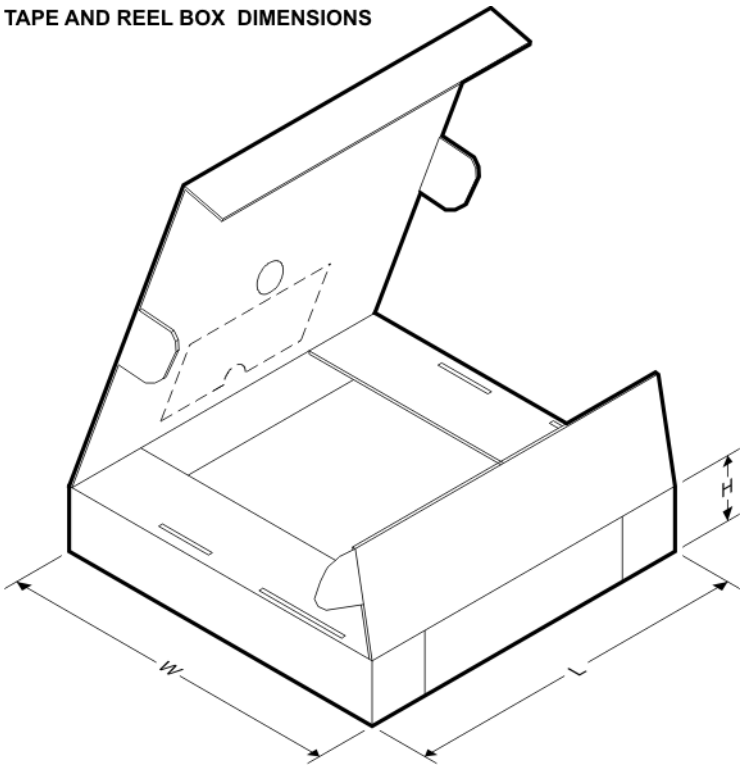
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLC27M2ACDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC27M2AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC27M2BCDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC27M2BIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC27M2CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC27M2CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| TLC27M2CPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC27M2IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC27M2IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC27M7CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC27M7CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| TLC27M7IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

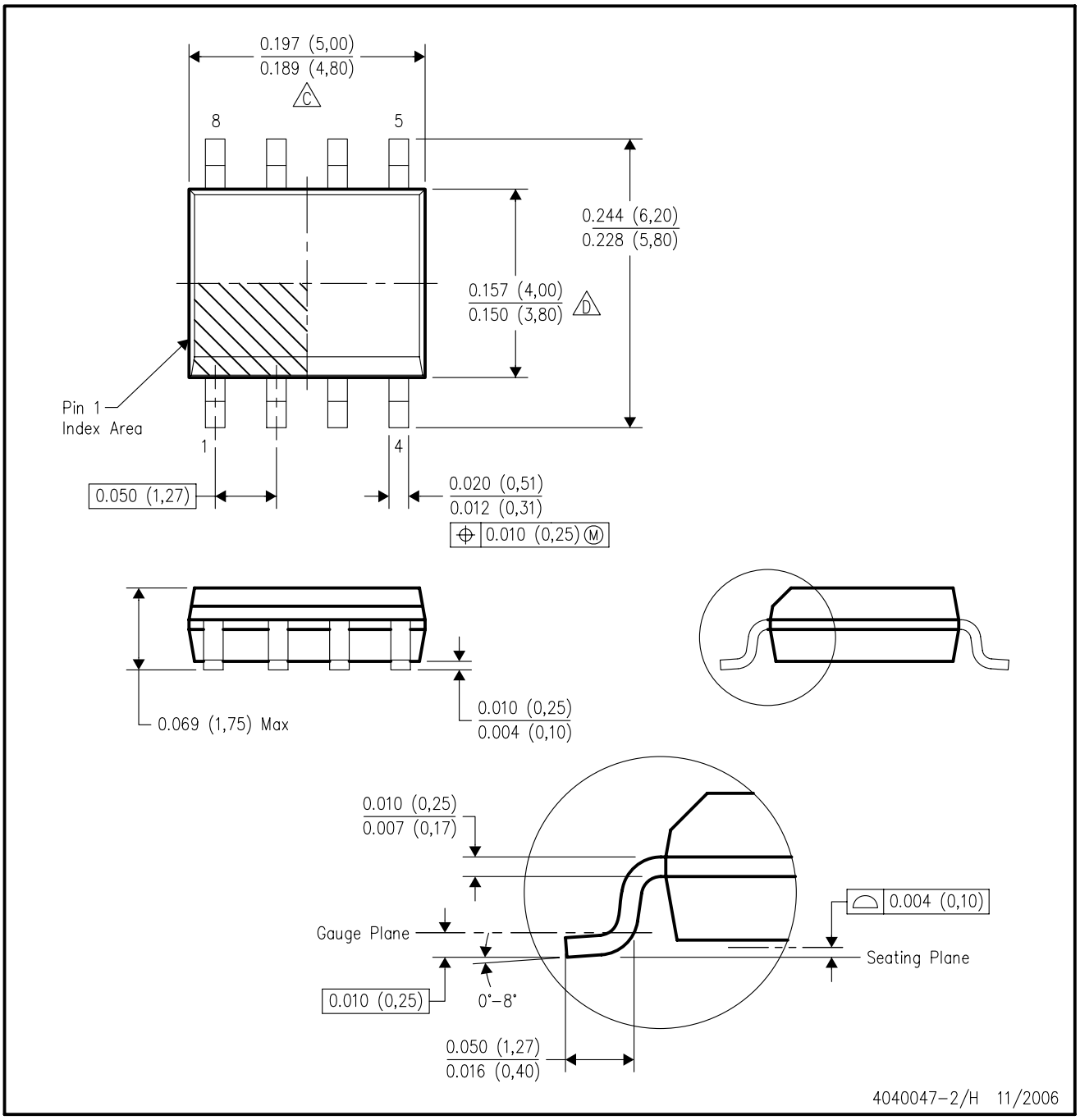
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLC27M2ACDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC27M2AIDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC27M2BCDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| TLC27M2BIDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| TLC27M2CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC27M2CPSR | SO | PS | 8 | 2000 | 346.0 | 346.0 | 33.0 |
| TLC27M2CPWR | TSSOP | PW | 8 | 2000 | 346.0 | 346.0 | 29.0 |
| TLC27M2IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLC27M2IPWR | TSSOP | PW | 8 | 2000 | 346.0 | 346.0 | 29.0 |
| TLC27M7CDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| TLC27M7CPSR | SO | PS | 8 | 2000 | 346.0 | 346.0 | 33.0 |
| TLC27M7IDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

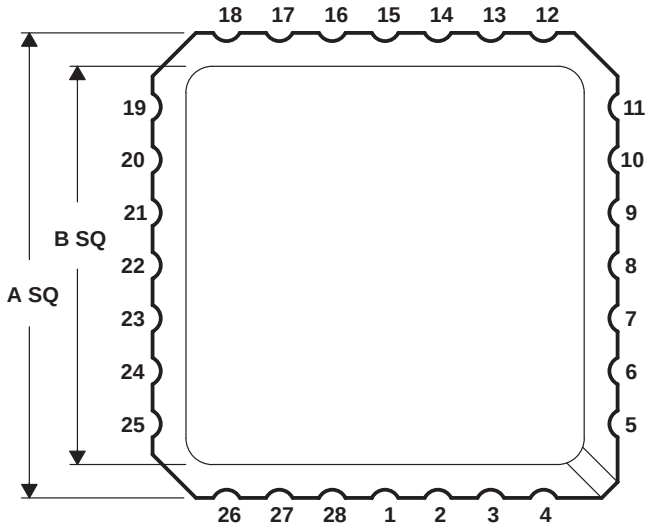
## D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



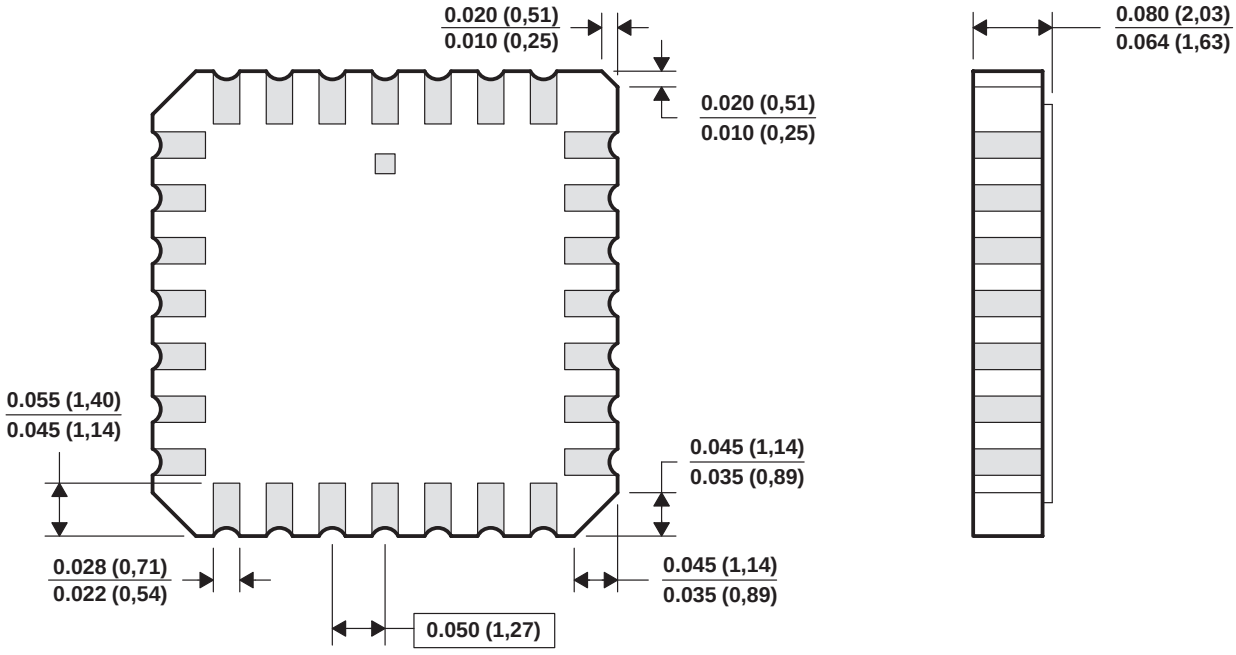

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

**FK (S-CQCC-N**)** **LEADLESS CERAMIC CHIP CARRIER**

**28 TERMINAL SHOWN**




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.739 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

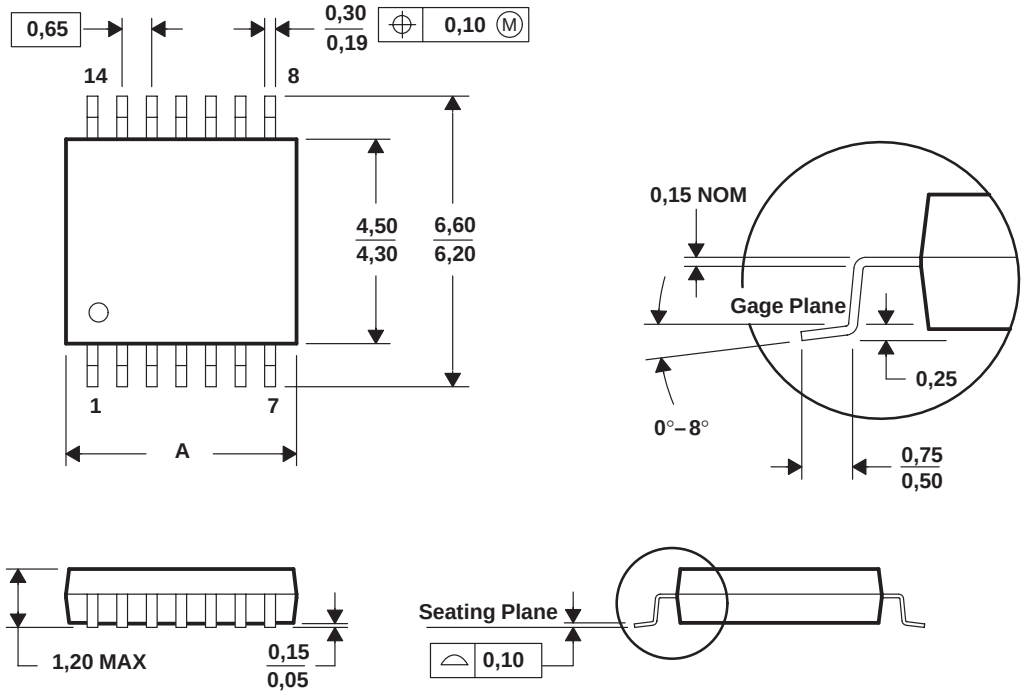



**4040140/D 10/96**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**



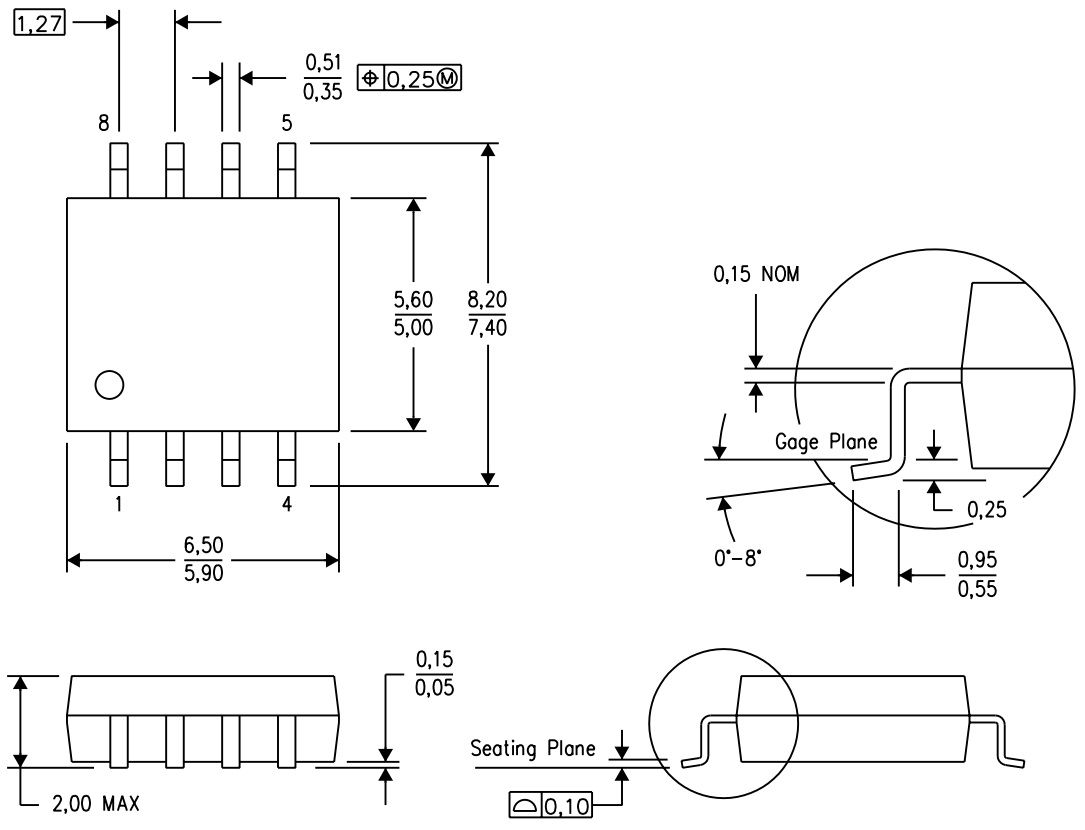

| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

## MECHANICAL DATA

**PS (R-PDSO-G8)** **PLASTIC SMALL-OUTLINE PACKAGE**

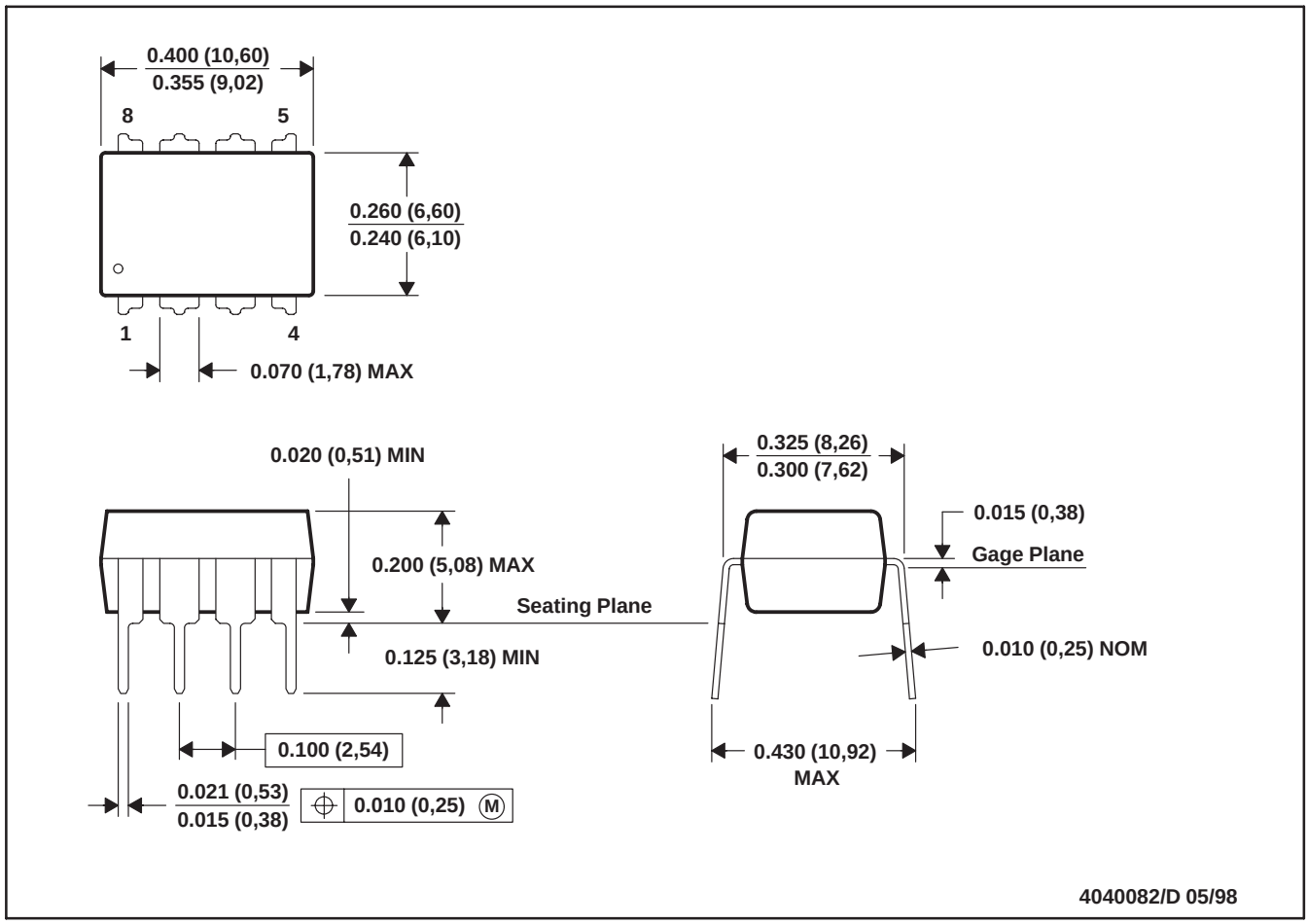



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

**P (R-PDIP-T8)** **PLASTIC DUAL-IN-LINE**

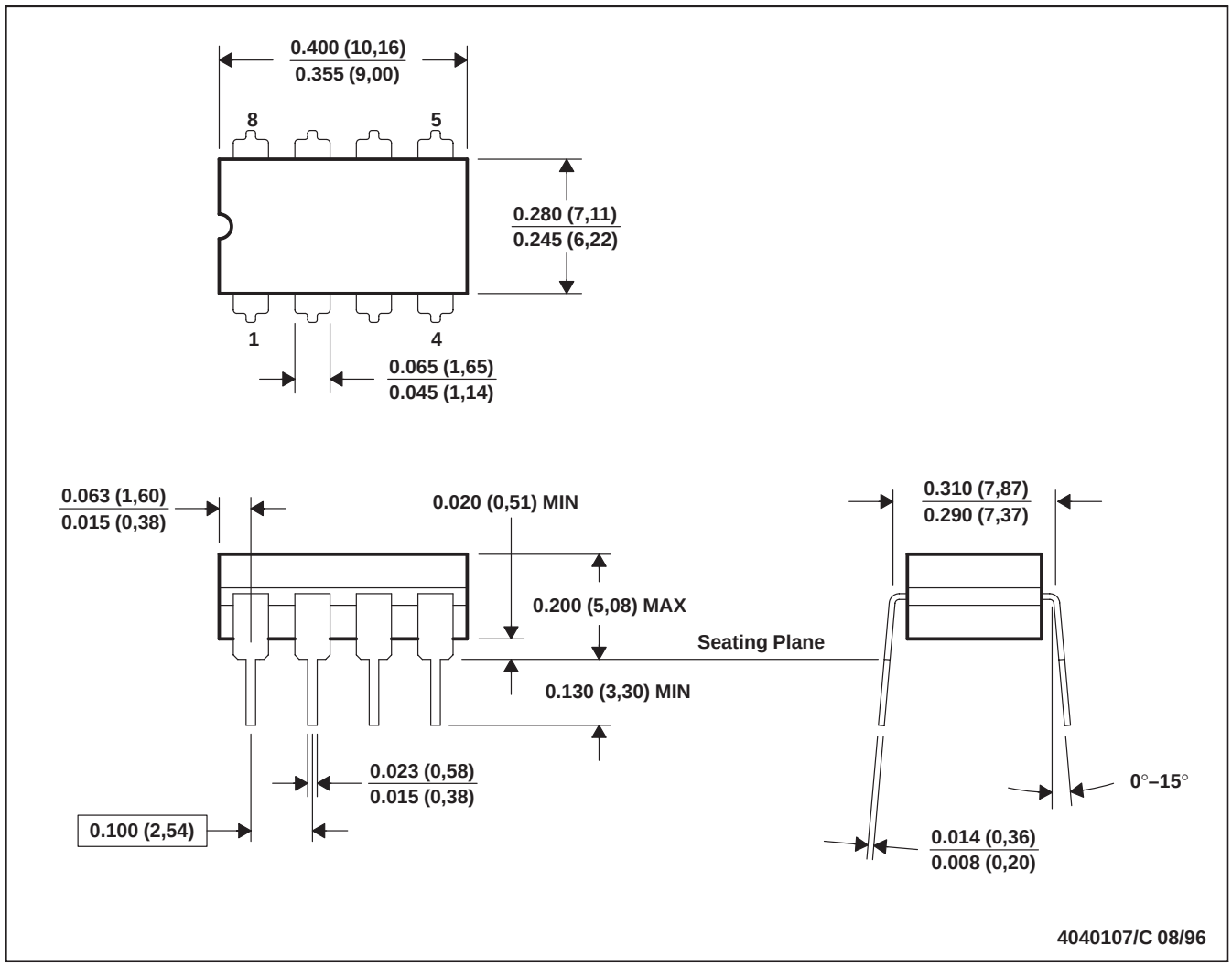



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

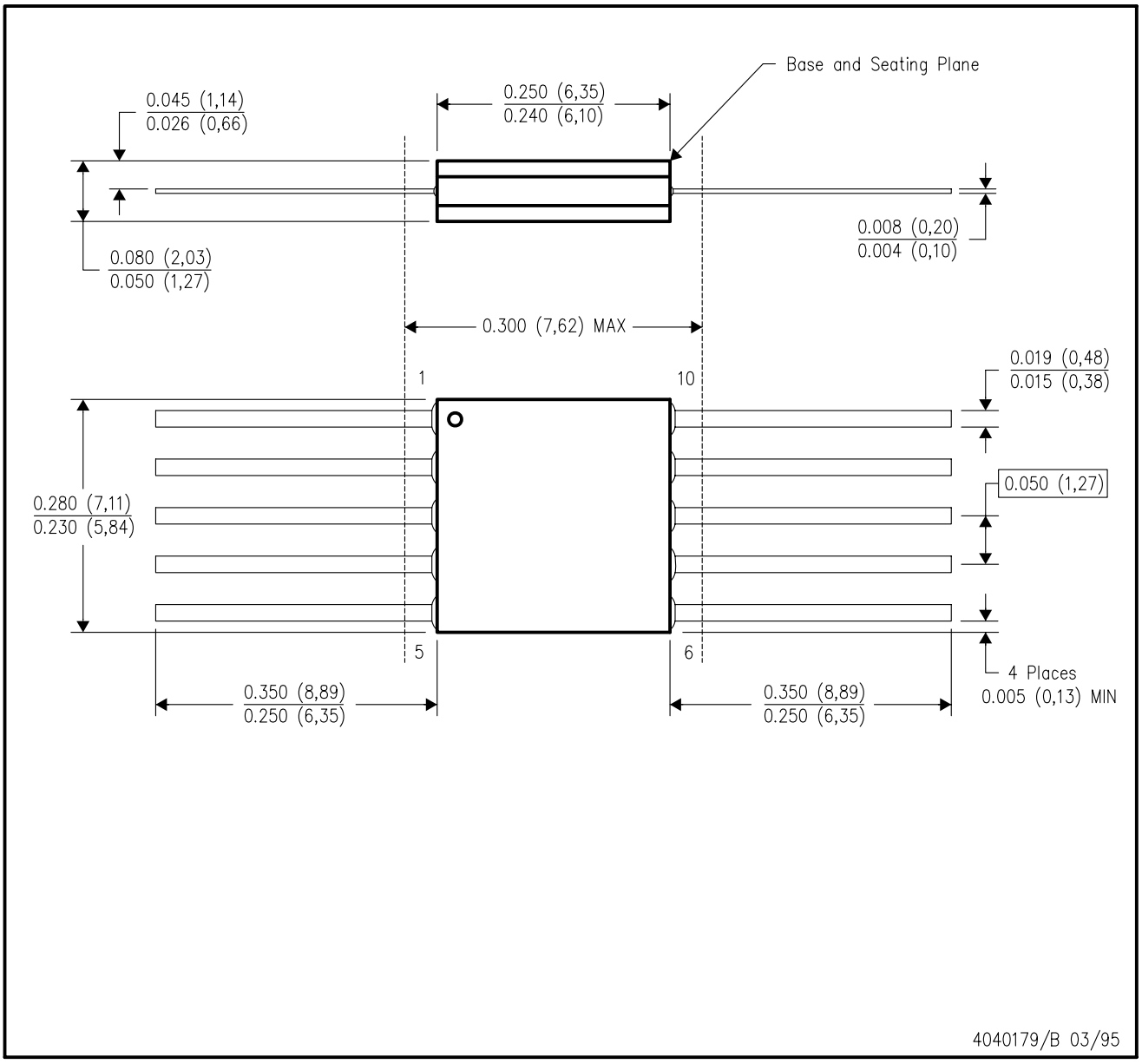
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

**JG (R-GDIP-T8)** **CERAMIC DUAL-IN-LINE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

## U (S–GDFP–F10) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

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