

TL431, A, B Series, NCV431A

Programmable Precision References

The TL431, A, B integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22 Ω . The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431, A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

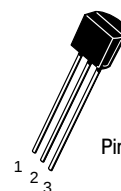
Features

- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance: $\pm 0.4\%$, Typ @ 25°C (TL431B)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- Pb-Free Packages are Available



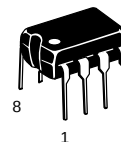
ON Semiconductor®

<http://onsemi.com>



Pin 1. Reference
2. Anode
3. Cathode

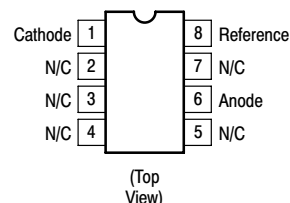
**TO-92 (TO-226)
LP SUFFIX
CASE 29**



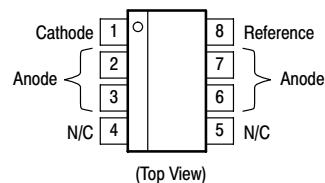
**PDIP-8
P SUFFIX
CASE 626**



**Micro8™
DM SUFFIX
CASE 846A**



**SOIC-8
D SUFFIX
CASE 751**



This is an internally modified SOIC-8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification increases power dissipation capability when appropriately mounted on a printed circuit board. This modified package conforms to all external dimensions of the standard SOIC-8 package.

ORDERING INFORMATION

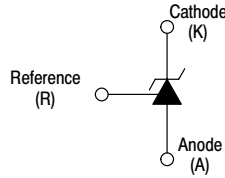
See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 15 of this data sheet.

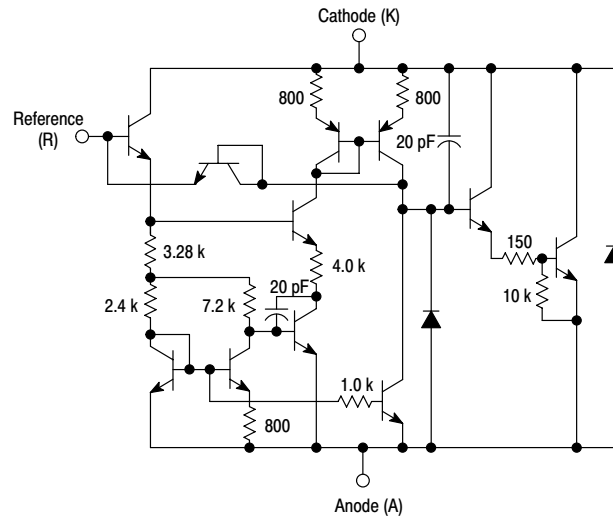
TL431, A, B Series, NCV431A

Symbol

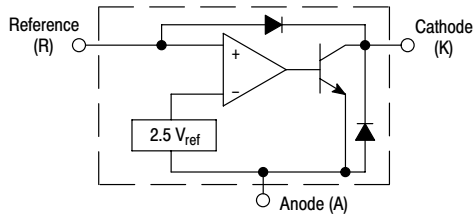


Representative Schematic Diagram

Component values are nominal



Representative Block Diagram



This device contains 12 active transistors.

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	-100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	-0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431I, TL431AI, TL431BI TL431C, TL431AC, TL431BC NCV431AI, TL431BV	T_A	-40 to +85 0 to +70 -40 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package DM Suffix Plastic Package	P_D	0.70 1.10 0.52	W
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package	P_D	1.5 3.0	W

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

THERMAL CHARACTERISTICS

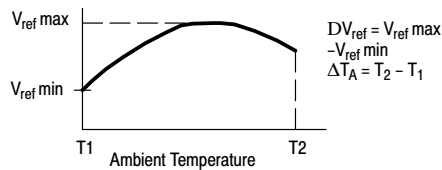
Characteristic	Symbol	D, LP Suffix Package	P Suffix Package	DM Suffix Package	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	178	114	240	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	83	41	-	°C/W

TL431, A, B Series, NCV431A

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) V _{KA} = V _{ref} , I _K = 10 mA T _A = 25°C T _A = T _{low} to T _{high} (Note 1)	V _{ref}	2.44 2.41	2.495 –	2.55 2.58	2.44 2.423	2.495 –	2.55 2.567	V
High Logic Level Supply Current from V _{CC}	I _{CCH}	60	–	45	60	mA	mA	mA
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2) V _{KA} = V _{ref} , I _K = 10 mA	ΔV _{ref}	–	7.0	30	–	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I _K = 10 mA (Figure 2), ΔV _{KA} = 10 V to V _{ref} ΔV _{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	– –	–1.4 –1.0	–2.7 –2.0	– –	–1.4 –1.0	–2.7 –2.0	mV/V
Reference Input Current (Figure 2) I _K = 10 mA, R1 = 10 k, R2 = ∞ T _A = 25°C T _A = T _{low} to T _{high} (Note 1)	I _{ref}	– –	1.8 –	4.0 6.5	– –	1.8 –	4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) I _K = 10 mA, R1 = 10 k, R2 = ∞	ΔI _{ref}	–	0.8	2.5	–	0.4	1.2	μA
Minimum Cathode Current For Regulation V _{KA} = V _{ref} (Figure 1)	I _{min}	–	0.5	1.0	–	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V _{KA} = 36 V, V _{ref} = 0 V	I _{off}	–	20	1000	–	20	1000	nA
Dynamic Impedance (Figure 1, Note 3) V _{KA} = V _{ref} , ΔI _K = 1.0 mA to 100 mA f ≤ 1.0 kHz	Z _{KA}	–	0.22	0.5	–	0.22	0.5	Ω

1. T_{low} = –40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM;
= 0°C for TL431ACP, TL431ACL, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
= +70°C for TL431ACP, TL431ACL, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
2. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25^{\circ}\text{C}} \right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25^{\circ}\text{C})}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 2.495 \text{ V}, \Delta T_A = 70^{\circ}\text{C} \quad \alpha V_{ref} = \frac{0.008 \times 10^6}{70 (2.495)} = 45.8 \text{ ppm}/^{\circ}\text{C}$$

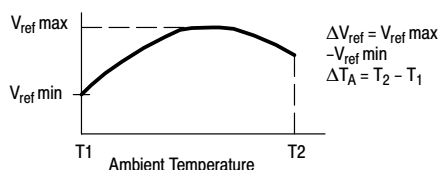
3. The dynamic impedance Z_{KA} is defined as: $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$. When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as: $|Z_{KA}'| \approx |Z_{KA}| \left(1 + \frac{R1}{R2} \right)$

TL431, A, B Series, NCV431A

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431AI / NCV431AI			TL431AC			TL431BI / TL431BV			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) V _{KA} = V _{ref} , I _K = 10 mA T _A = 25°C T _A = T _{low} to T _{high}	V _{ref}	2.47 2.44	2.495 –	2.52 2.55	2.47 2.453	2.495 –	2.52 2.537	2.483 2.475	2.495 2.495	2.507 2.515	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 4, 5) V _{KA} = V _{ref} , I _K = 10 mA	ΔV _{ref}	–	7.0	30	–	3.0	17	–	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I _K = 10 mA (Figure 2), ΔV _{KA} = 10 V to V _{ref} ΔV _{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	– –	–1.4 –1.0	–2.7 –2.0	– –	–1.4 –1.0	–2.7 –2.0	– –	–1.4 –1.0	–2.7 –2.0	mV/V
Reference Input Current (Figure 2) I _K = 10 mA, R ₁ = 10 k, R ₂ = ∞ T _A = 25°C T _A = T _{low} to T _{high} (Note 4)	I _{ref}	– –	1.8 –	4.0 6.5	– –	1.8 –	4.0 5.2	– –	1.1 –	2.0 4.0	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 4) I _K = 10 mA, R ₁ = 10 k, R ₂ = ∞	ΔI _{ref}	–	0.8	2.5	–	0.4	1.2	–	0.8	2.5	μA
Minimum Cathode Current For Regulation V _{KA} = V _{ref} (Figure 1)	I _{min}	–	0.5	1.0	–	0.5	1.0	–	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V _{KA} = 36 V, V _{ref} = 0 V	I _{off}	–	20	1000	–	20	1000	–	0.23	500	nA
Dynamic Impedance (Figure 1, Note 6) V _{KA} = V _{ref} , ΔI _K = 1.0 mA to 100 mA f ≤ 1.0 kHz	Z _{KA}	–	0.22	0.5	–	0.22	0.5	–	0.14	0.3	Ω

4. T_{low} = –40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431BV, TL431AIDM, TL431IDM, TL431BIDM, NCV431AIDMR2, NCV431AIDR2
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
= +125°C TL431BV, NCV431AIDMR2, NCV431AIDR2
5. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$\alpha V_{ref} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25^{\circ}\text{C}} \right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25^{\circ}\text{C})}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 2.495 \text{ V}, \Delta T_A = 70^{\circ}\text{C}$$

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70 (2.495)} = 45.8 \text{ ppm}/^{\circ}\text{C}$$

6. The dynamic impedance Z_{KA} is defined as $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$ When the device is programmed with two external resistors, R₁ and R₂, (refer to Figure 2) the total dynamic impedance of the circuit is defined as: $|Z_{KA}'| \approx |Z_{KA}| \left(1 + \frac{R_1}{R_2} \right)$
7. NCV431AIDMR2, NCV431AIDR2 T_{low} = –40°C, T_{high} = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

TL431, A, B Series, NCV431A

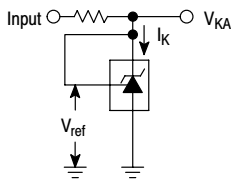


Figure 1. Test Circuit for $V_{KA} = V_{ref}$

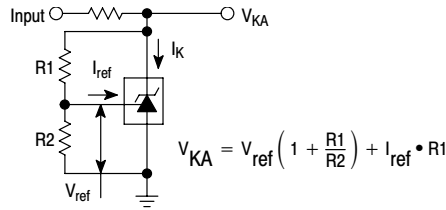


Figure 2. Test Circuit for $V_{KA} > V_{ref}$

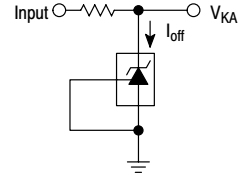


Figure 3. Test Circuit for I_{off}

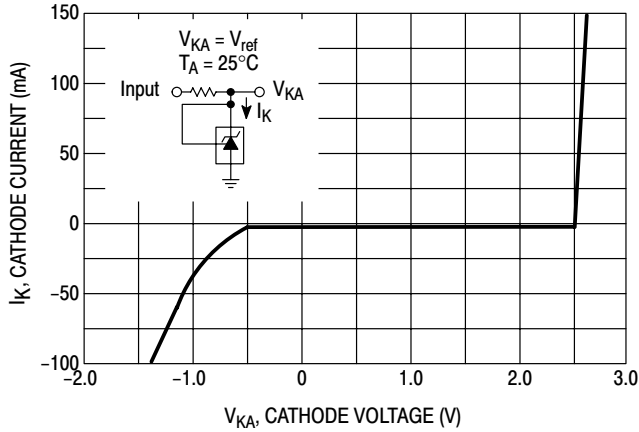


Figure 4. Cathode Current versus Cathode Voltage

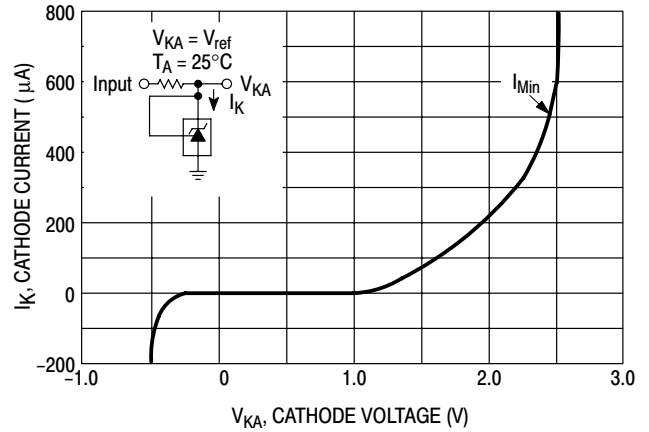


Figure 5. Cathode Current versus Cathode Voltage

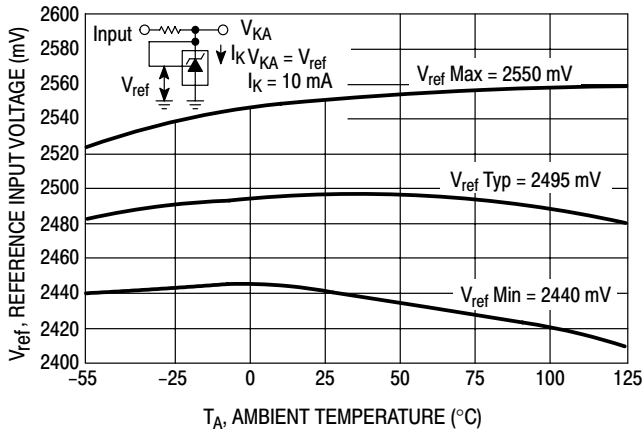


Figure 6. Reference Input Voltage versus Ambient Temperature

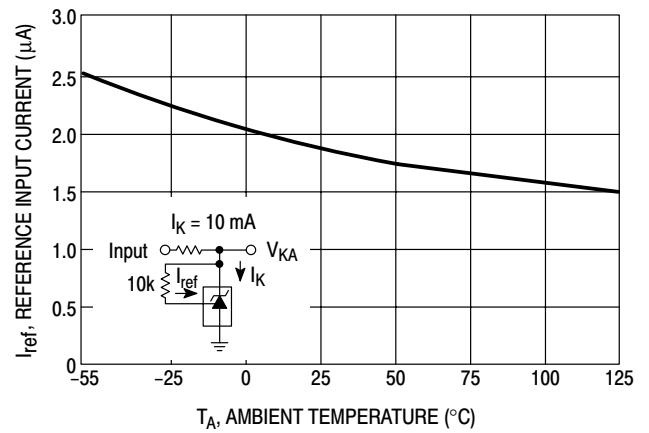


Figure 7. Reference Input Current versus Ambient Temperature

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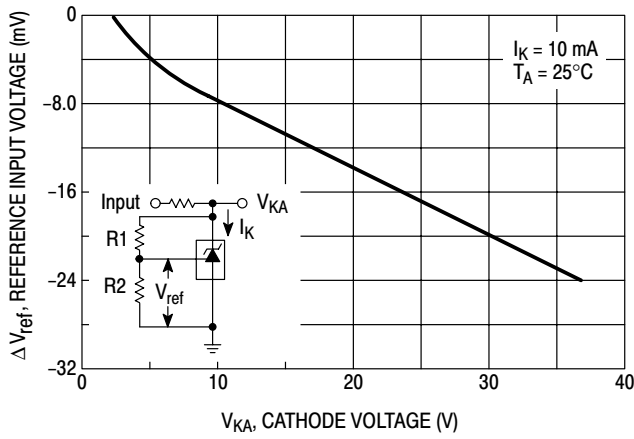


Figure 8. Change in Reference Input Voltage versus Cathode Voltage

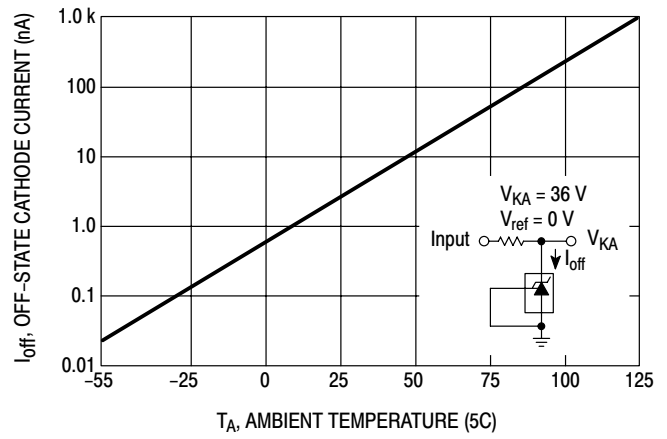


Figure 9. Off-State Cathode Current versus Ambient Temperature

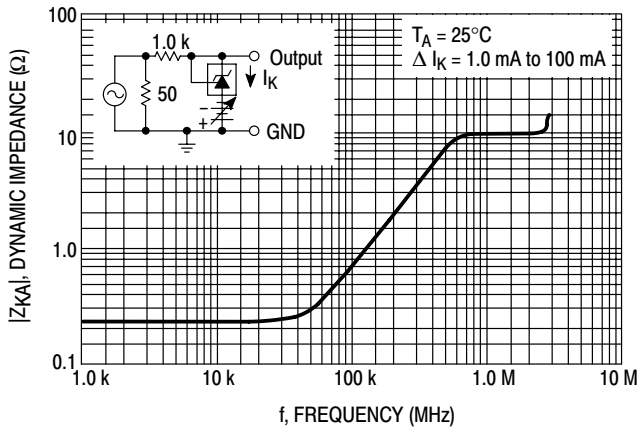


Figure 10. Dynamic Impedance versus Frequency

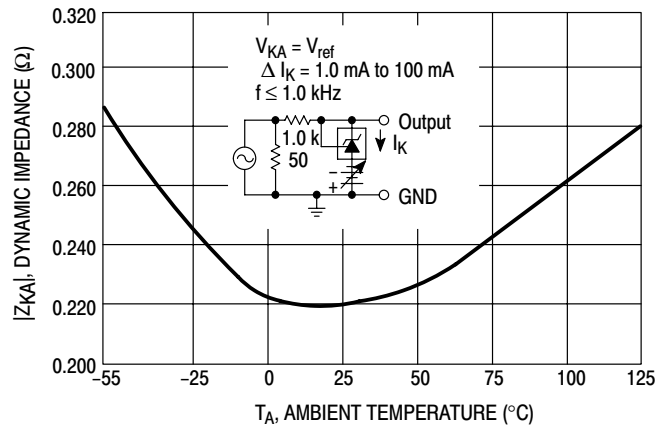


Figure 11. Dynamic Impedance versus Ambient Temperature

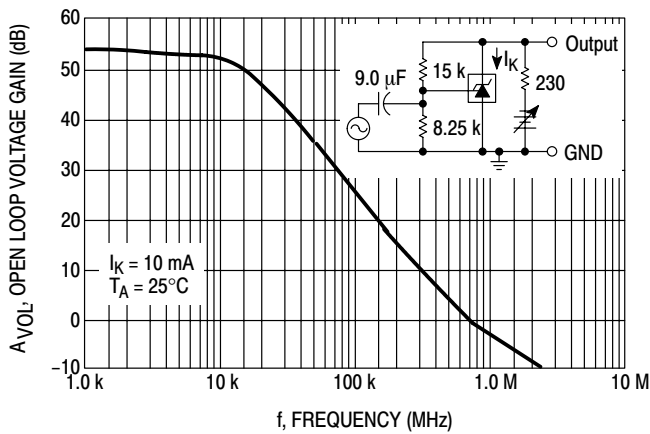


Figure 12. Open-Loop Voltage Gain versus Frequency

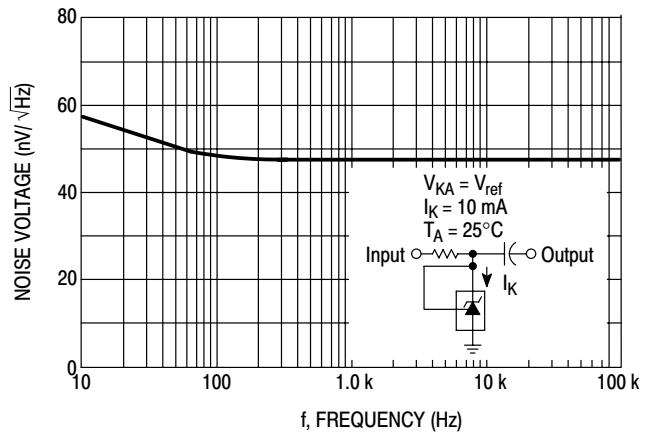


Figure 13. Spectral Noise Density

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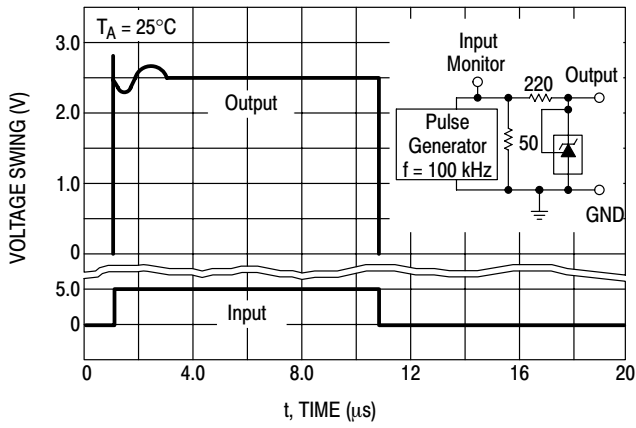


Figure 14. Pulse Response

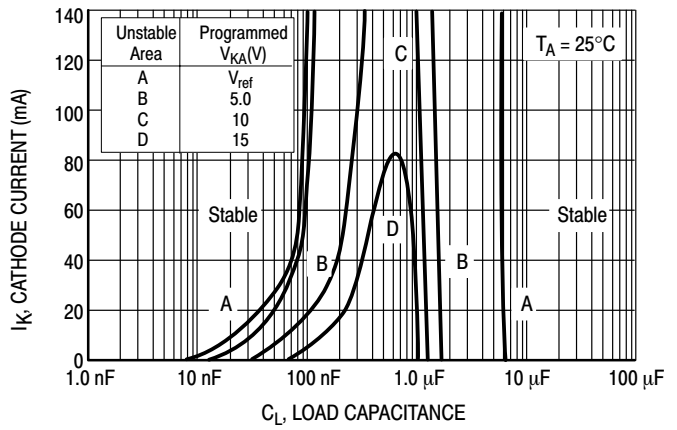


Figure 15. Stability Boundary Conditions

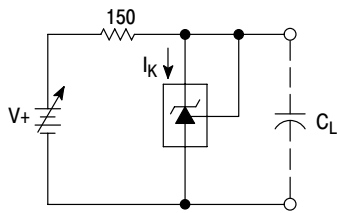


Figure 16. Test Circuit For Curve A of Stability Boundary Conditions

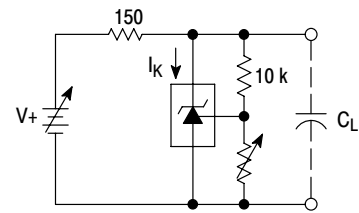


Figure 17. Test Circuit For Curves B, C, and D of Stability Boundary Conditions

TYPICAL APPLICATIONS

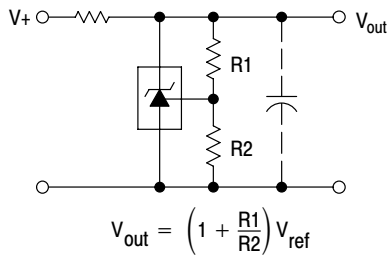


Figure 18. Shunt Regulator

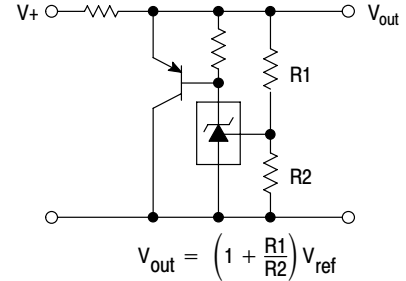


Figure 19. High Current Shunt Regulator

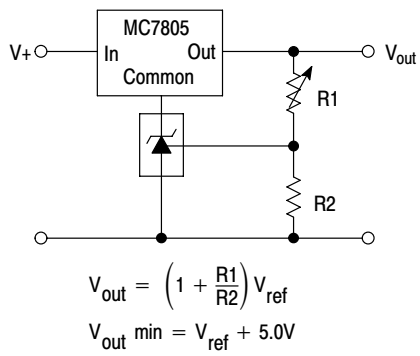


Figure 20. Output Control for a Three-Terminal Fixed Regulator

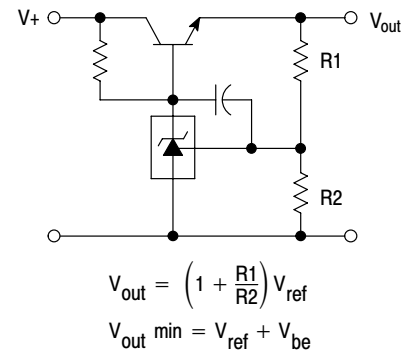


Figure 21. Series Pass Regulator

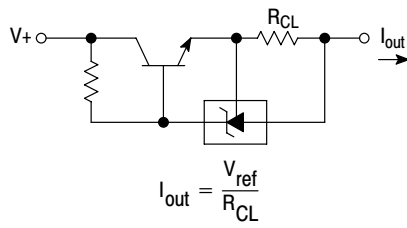


Figure 22. Constant Current Source

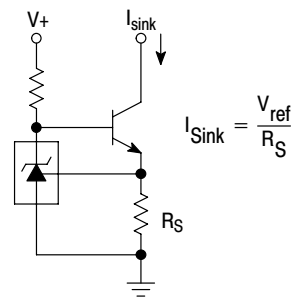


Figure 23. Constant Current Sink

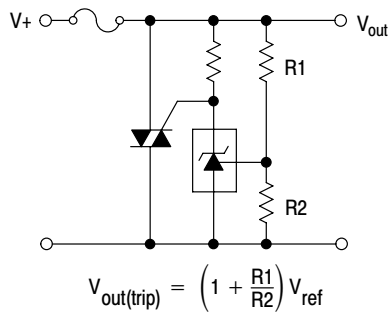


Figure 24. TRIAC Crowbar

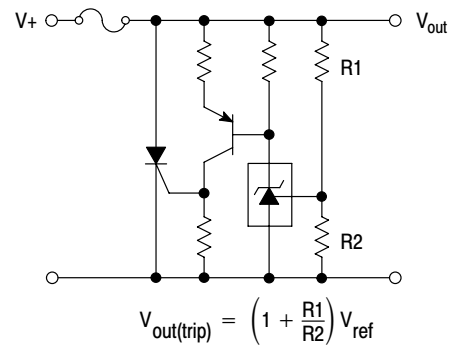
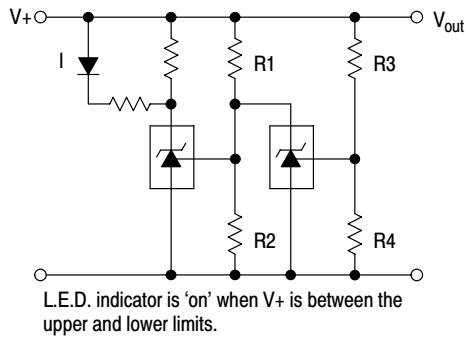


Figure 25. SRC Crowbar

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$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right) V_{\text{ref}}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right) V_{\text{ref}}$$

Figure 26. Voltage Monitor

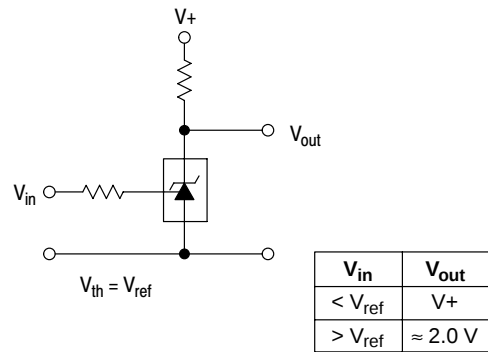


Figure 27. Single-Supply Comparator with Temperature-Compensated Threshold

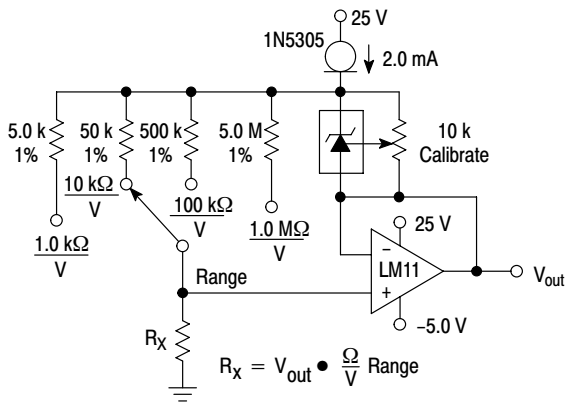


Figure 28. Linear Ohmmeter

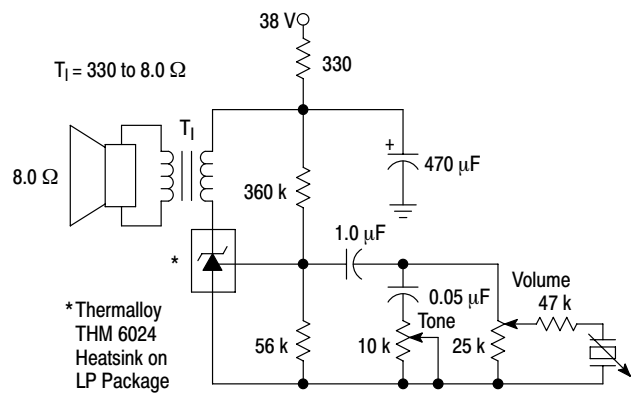


Figure 29. Simple 400 mW Phono Amplifier

TL431, A, B Series, NCV431A

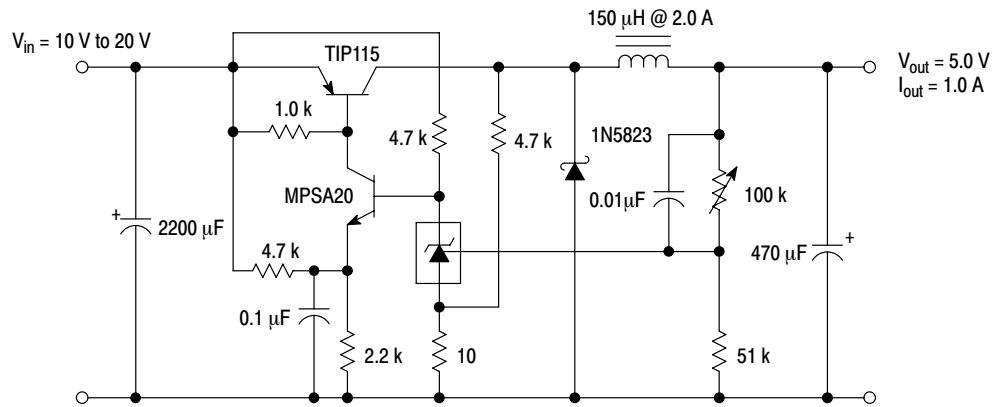


Figure 30. High Efficiency Step-Down Switching Converter

Test	Conditions	Results
Line Regulation	$V_{in} = 10 \text{ V to } 20 \text{ V}$, $I_o = 1.0 \text{ A}$	53 mV (1.1%)
Load Regulation	$V_{in} = 15 \text{ V}$, $I_o = 0 \text{ A to } 1.0 \text{ A}$	25 mV (0.5%)
Output Ripple	$V_{in} = 10 \text{ V}$, $I_o = 1.0 \text{ A}$	50 mVpp P.A.R.D.
Output Ripple	$V_{in} = 20 \text{ V}$, $I_o = 1.0 \text{ A}$	100 mVpp P.A.R.D.
Efficiency	$V_{in} = 15 \text{ V}$, $I_o = 1.0 \text{ A}$	82%

APPLICATIONS INFORMATION

The TL431 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non-standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 15. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition. Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation.

A simplified model of the TL431 is shown in Figure 31. When tested for stability boundaries, the load resistance is 150 Ω . The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, G_m , develops a current whose amplitude is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of G_m flows through compensation capacitance, C_{P2} . The voltage across C_{P2} drives the output dependent current source, G_o , which is connected across the device cathode and anode.

Model component values are:

$$V_{ref} = 1.78 \text{ V}$$

$$G_m = 0.3 + 2.7 \exp(-I_C/26 \text{ mA})$$

where I_C is the device cathode current and G_m is in mhos

$$G_o = 1.25 (V_{CP2}) \mu\text{mhos}.$$

Resistor and capacitor typical values are shown on the model. Process tolerances are $\pm 20\%$ for resistors, $\pm 10\%$ for capacitors, and $\pm 40\%$ for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$P1 = \frac{1}{2\pi R_{GM} C_{P1}} = \frac{1}{2\pi * 1.0 \text{ M} * 20 \text{ pF}} = 7.96 \text{ kHz}$$

$$P2 = \frac{1}{2\pi R_{P2} C_{P2}} = \frac{1}{2\pi * 10 \text{ M} * 0.265 \text{ pF}} = 60 \text{ kHz}$$

$$Z1 = \frac{1}{2\pi R_{Z1} C_{P1}} = \frac{1}{2\pi * 15.9 \text{ k} * 20 \text{ pF}} = 500 \text{ kHz}$$

In addition, there is an external circuit pole defined by the load:

$$P_L = \frac{1}{2\pi R_L C_L}$$

Also, the transfer dc voltage gain of the TL431 is:

$$G = G_M R_{GM} G_o R_L$$

Example 1:

$I_C = 10 \text{ mA}$, $R_L = 230 \Omega$, $C_L = 0$. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} G_o R_L = (2.138)(1.0 \text{ M})(1.25 \mu)(230) = 615 = 56 \text{ dB}$$

$$\text{Loop gain} = G \frac{8.25 \text{ k}}{8.25 \text{ k} + 15 \text{ k}} = 218 = 47 \text{ dB}$$

The resulting transfer function Bode plot is shown in Figure 32. The asymptotic plot may be expressed as the following equation:

$$A_v = 615 \frac{\left(1 + \frac{jf}{500 \text{ kHz}}\right)}{\left(1 + \frac{jf}{8.0 \text{ kHz}}\right)\left(1 + \frac{jf}{60 \text{ kHz}}\right)}$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9 degrees. This model matches the Open-Loop Bode Plot of Figure 12. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44 degrees.

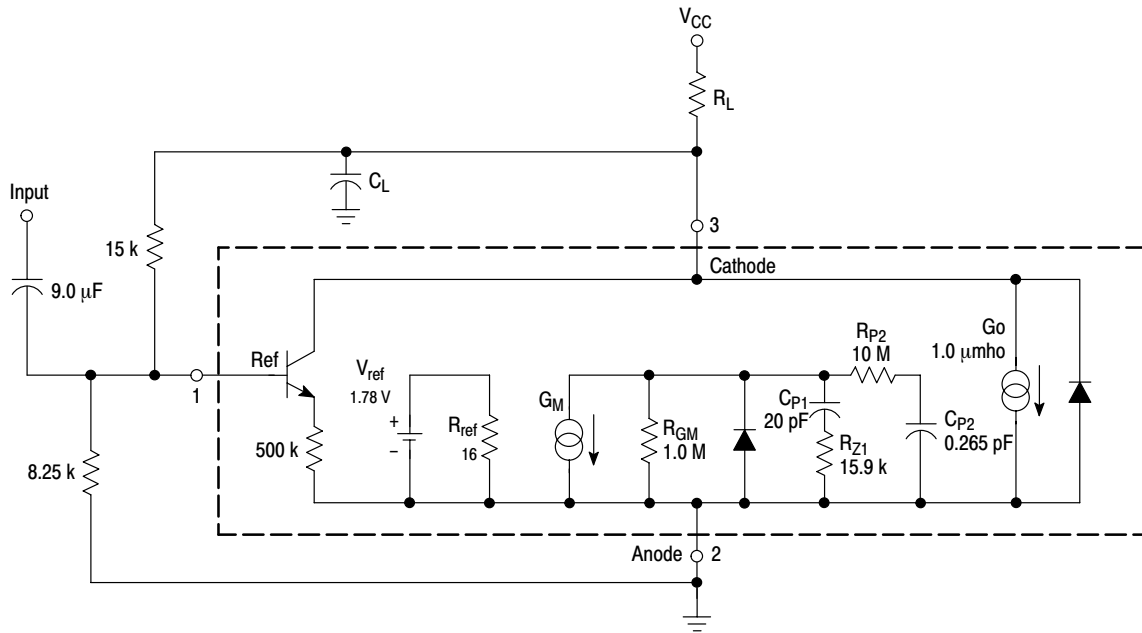


Figure 31. Simplified TL431 Device Model

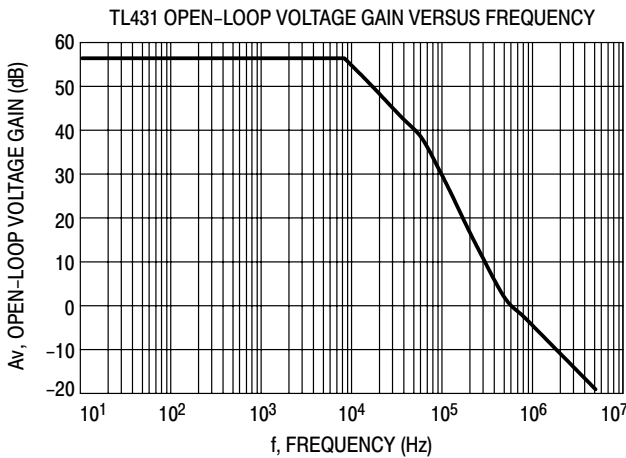


Figure 32. Example 1 Circuit Open Loop Gain Plot

Example 2.

$I_C = 7.5 \text{ mA}$, $R_L = 2.2 \text{ k}\Omega$, $C_L = 0.01 \text{ }\mu\text{F}$. Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} G_O R_L =$$

$$(2.323)(1.0 \text{ M})(1.25 \text{ }\mu)(2200) = 6389 = 76 \text{ dB}$$

The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

$$A_v = 615 \frac{\left(1 + \frac{jf}{500 \text{ kHz}}\right)}{\left(1 + \frac{jf}{8.0 \text{ kHz}}\right)\left(1 + \frac{jf}{60 \text{ kHz}}\right)\left(1 + \frac{jf}{7.2 \text{ kHz}}\right)}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about -46 degrees. Therefore, instability of this circuit is likely.

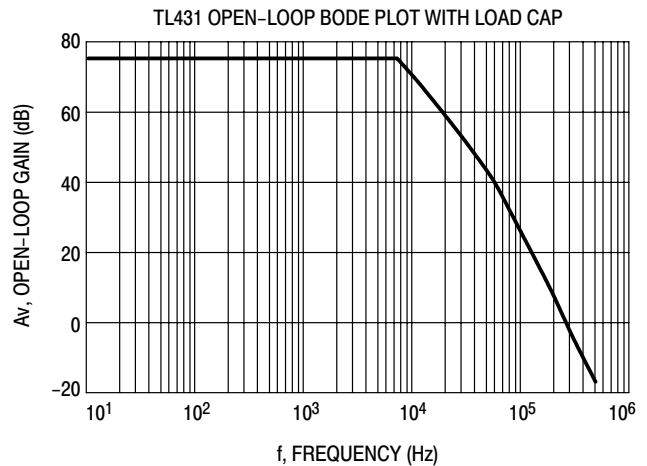


Figure 33. Example 2 Circuit Open Loop Gain Plot

With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

TL431, A, B Series, NCV431A

ORDERING INFORMATION

Device	Operating Temperature Range	Package Code	Shipping Information [†]	Tolerance	
TL431ACD	0°C to 70°C	SOIC-8	98 Units / Rail	1.0%	
TL431ACDG		SOIC-8 (Pb-Free)		1.0%	
TL431BCD		SOIC-8		0.4%	
TL431BCDG		SOIC-8 (Pb-Free)		0.4%	
TL431CD		SOIC-8		2.2%	
TL431ACDR2		SOIC-8 (Pb-Free)	2500 Units / Tape & Reel	1.0%	
TL431ACDR2G				1.0%	
TL431BCDR2				0.4%	
TL431BCDR2G				0.4%	
TL431CDR2				2.2%	
TL431CDR2G				2.2%	
TL431ACDMR2				Micro8	4000 Units / Tape & Reel
TL431BCDMR2		0.4%			
TL431BCDMR2G		Micro8 (Pb-Free)	0.4%		
TL431CDMR2		Micro8	2.2%		
TL431CDMR2G		Micro8 (Pb-Free)	2.2%		
TL431ACP		PDIP-8	50 Units / Rail	1.0%	
TL431BCP				0.4%	
TL431CP				2.2%	
TL431CPG				PDIP-8 (Pb-Free)	2.2%
TL431ACLP		TO-92 (TO-226)	2000 Units / Bag	1.0%	
TL431ACLPG		TO-92 (TO-226) (Pb-Free)		1.0%	
TL431BCLP		TO-92 (TO-226)		0.4%	
TL431BCLPG		TO-92 (TO-226) (Pb-Free)		0.4%	
TL431CLP		TO-92 (TO-226)		2.2%	
TL431CLPG		TO-92 (TO-226) (Pb-Free)		2.2%	
TL431ACLPRA		TO-92 (TO-226)	2000 Units / Tape & Reel	1.0%	
TL431ACLPRAG		TO-92 (TO-226) (Pb-Free)		1.0%	
TL431BCLPRA		TO-92 (TO-226)		0.4%	
TL431BCLPRAG		TO-92 (TO-226) (Pb-Free)		0.4%	
TL431CLPRA		TO-92 (TO-226)		2.2%	
TL431CLPRAG		TO-92 (TO-226) (Pb-Free)		2.2%	
TL431ACLPRE		TO-92 (TO-226)		1.0%	
TL431ACLPREG		TO-92 (TO-226) (Pb-Free)		1.0%	
TL431BCLPRE		TO-92 (TO-226)		0.4%	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TL431, A, B Series, NCV431A

ORDERING INFORMATION

Device	Operating Temperature Range	Package Code	Shipping Information [†]	Tolerance
TL431BCLPREG	0°C to 70°C	TO-92 (TO-226) (Pb-Free)	2000 Units / Tape & Reel	0.4%
TL431ACLPRP		TO-92 (TO-226)	2000 Units / Fan-Fold	1.0%
TL431ACLPRPG		TO-92 (TO-226) (Pb-Free)		1.0%
TL431BCLPRM		TO-92 (TO-226)		0.4%
TL431BCLPRMG		TO-92 (TO-226) (Pb-Free)		0.4%
TL431CLPRP		TO-92 (TO-226)		2.2%
TL431CLPRPG		TO-92 (TO-226) (Pb-Free)		2.2%
TL431AID	-40°C to 85°C	SOIC-8	98 Units / Rail	1.0%
TL431AIDG		SOIC-8 (Pb-Free)		1.0%
TL431BID		SOIC-8		0.4%
TL431BIDG		SOIC-8 (Pb-Free)		0.4%
TL431ID		SOIC-8		2.2%
TL431IDG		SOIC-8 (Pb-Free)		2.2%
TL431AIDR2		SOIC-8	2500 Units / Tape & Reel	1.0%
TL431AIDR2G		SOIC-8 (Pb-Free)		1.0%
TL431BIDR2		SOIC-8		0.4%
TL431BIDR2G		SOIC-8 (Pb-Free)		0.4%
TL431IDR2		SOIC-8		2.2%
TL431IDR2G		SOIC-8 (Pb-Free)		2.2%
TL431AIDMR2		Micro8	4000 Units / Tape & Reel	1.0%
TL431BIDMR2		Micro8 (Pb-Free)		0.4%
TL431BIDMR2G		Micro8		2.2%
TL431IDMR2		Micro8 (Pb-Free)		2.2%
TL431IDMR2G		PDIP-8	50 Units / Rail	1.0%
TL431AIP		PDIP-8 (Pb-Free)		1.0%
TL431AIPG		PDIP-8		0.4%
TL431BIP		PDIP-8		2.2%
TL431IP		TO-92 (TO-226)	2000 Units / Box	1.0%
TL431AILP		TO-92 (TO-226) (Pb-Free)		0.4%
TL431BILP		TO-92 (TO-226) (Pb-Free)		0.4%
TL431BILPG		TO-92 (TO-226)		2.2%
TL431ILP		TO-92 (TO-226) (Pb-Free)	2000 Units / Tape & Reel	2.2%
TL431ILPG		TO-92 (TO-226)		2.2%
TL431AILPRA		TO-92 (TO-226)	2000 Units / Tape & Reel	1.0%
TL431AILPRAG		TO-92 (TO-226) (Pb-Free)		1.0%

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TL431, A, B Series, NCV431A

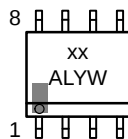
ORDERING INFORMATION

Device	Operating Temperature Range	Package Code	Shipping Information [†]	Tolerance
TL431BILPRA	-40°C to 85°C	TO-92 (TO-226)	2000 Units / Tape & Reel	0.4%
TL431BILPRAG		TO-92 (TO-226) (Pb-Free)		0.4%
TL431ILPRA		TO-92 (TO-226)		2.2%
TL431ILPRAG		TO-92 (TO-226) (Pb-Free)		2.2%
TL431AILPRM		TO-92 (TO-226)	2000 Units / Ammo Pack	1.0%
TL431AILPRP				1.0%
TL431ILPRP				2.2%
TL431BVD	-40°C to 125°C	SOIC-8	98 Units / Rail	0.4%
TL431BVDR2		SOIC-8		0.4%
TL431BVDMR2		Micro8	4000 Units / Tape & Reel	0.4%
TL431BVLP		TO-92 (TO-226)	2000 Units / Box	0.4%
TL431BVP		PDIP-8	50 Units / Rail	0.4%
NCV431AIDMR2		Micro8	4000 Units / Tape & Reel	1%
NCV431AIDR2		SOIC-8	2500 Units / Tape & Reel	1%

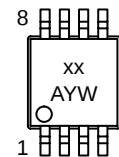
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

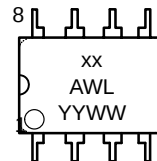
**SOIC-8
D SUFFIX
CASE 751**



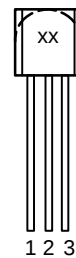
**Micro8
CASE 846A**



**PDIP-8
CASE 626**



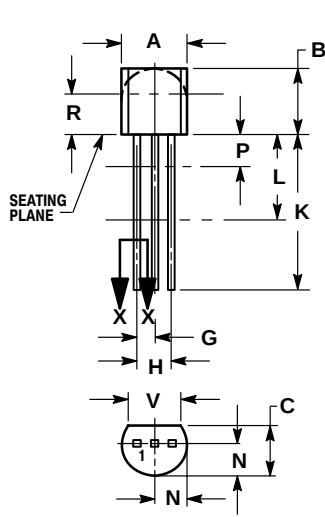
**TO-92 (TO-226)
CASE 29**



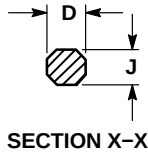
xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

TL431, A, B Series, NCV431A

PACKAGE DIMENSIONS



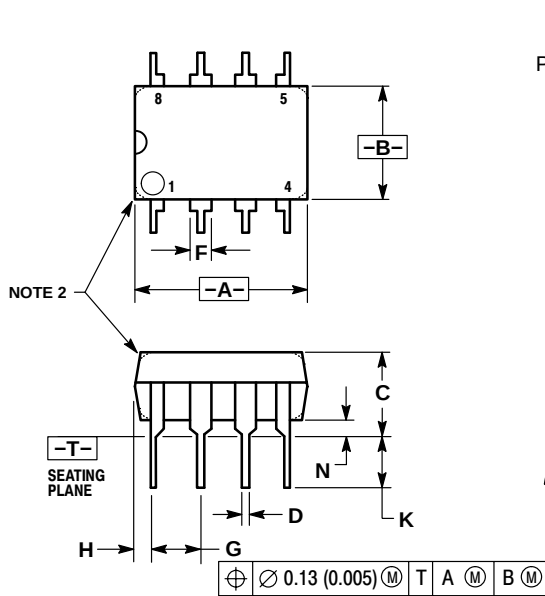
TO-92 (TO-226)
LP SUFFIX
PLASTIC PACKAGE
CASE 29-11
ISSUE AL



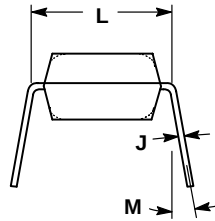
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



PDIP-8
P SUFFIX
PLASTIC PACKAGE
CASE 626-05
ISSUE L



NOTES:

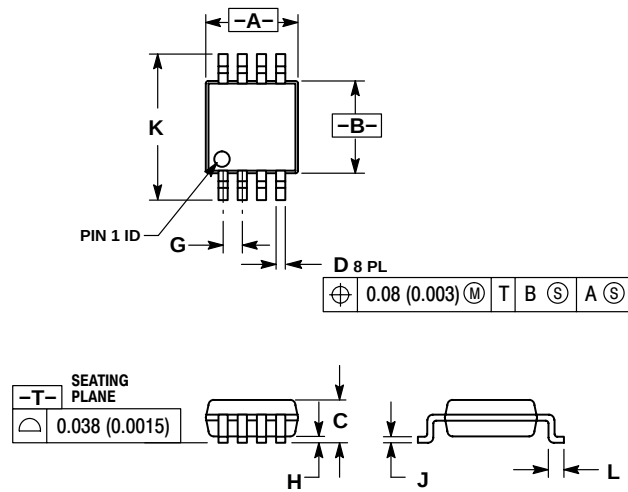
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC	---	0.100 BSC	---
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC	---	0.300 BSC	---
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

TL431, A, B Series, NCV431A

PACKAGE DIMENSIONS

Micro8
DM SUFFIX
PLASTIC PACKAGE
CASE 846A-02
ISSUE F

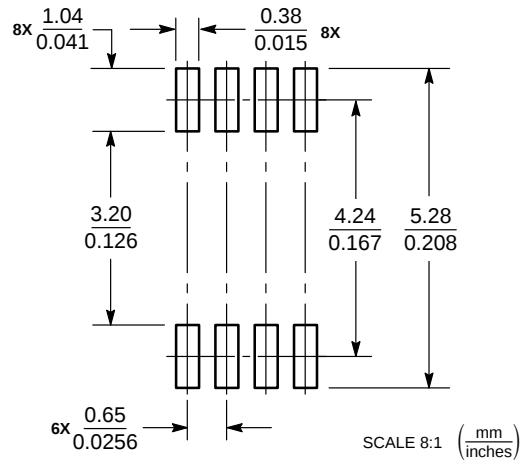


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC-8
D SUFFIX
PLASTIC PACKAGE
CASE 751-07
ISSUE AE



1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

Figure 1: Plan view of a four-lane highway cross-section. The diagram shows a four-lane highway with a centerline and two shoulders. Dimensions are given in feet and inches. The total width is 7.0 feet (0.275 inches). The lane width is 1.52 feet (0.060 inches). The shoulder width is 4.0 feet (0.155 inches). The distance from the centerline to the edge of the shoulder is 0.6 feet (0.024 inches). The distance from the centerline to the edge of the lane is 1.270 feet (0.050 inches). The scale is 6:1 (mm/inches).

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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