

TSL2584TSV

Light-to-Digital Device

General Description

The TSL2584TSV is a very-high sensitivity light-to-digital converter that transforms light intensity into a digital signal output capable of direct I²C interface. The device combines one broadband photodiode (visible plus infrared), one infrared-responding photodiode, and a photopic infrared-blocking filter on a single CMOS integrated circuit. Two integrating ADCs convert the photodiode currents into a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response. The TSL2584TSV supports a traditional level style interrupt that remains asserted until the firmware clears it.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2584TSV, Light-to-Digital Device are listed below:

Figure 1:
Added Value of Using TSL2584TSV

Benefits	Features
• Approximates Human Eye Response	• Dual Diode with Photopic Filter
• Flexible Operation	• Programmable Analog Gain and Integration Time
• Suited for Operation Behind Dark Glass	• 1,000,000: 1 Dynamic Range
• Low Operating Overhead	• Programmable Upper and Lower Thresholds • Programmable Persistence Filter
• Low Power	• 3.0 μ A Sleep State
• Industry Standard Two-Wire Interface	• I ² C Fast Mode Compatible Interface • Data Rates up to 400 kbit/s • Input Voltage Levels Compatible with 1.8–V Bus
• Ultra-Small Foot-Print	• 1.145 mm x 1.660 mm TSV (Through Silicon Via) • 0.218 mm Height w/o Solder Balls
• Unlimited Manufacturing Floor Life	• MSL1 Rated

Applications

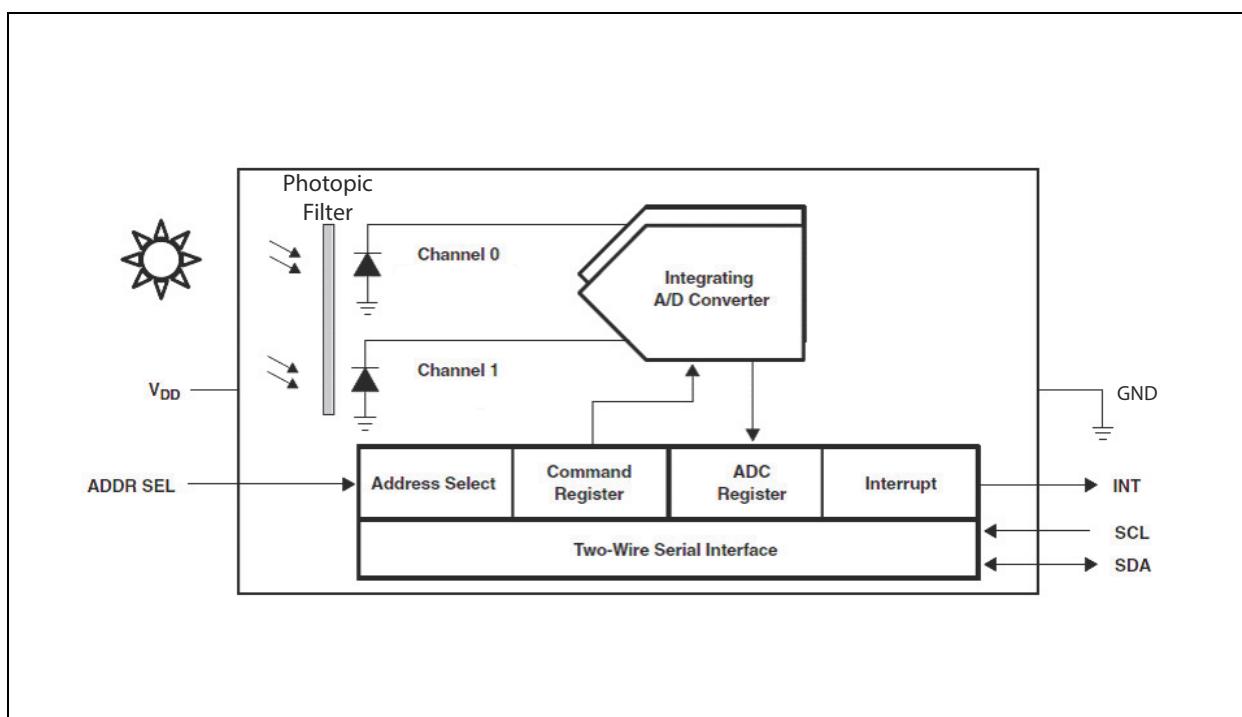
The TSL2584TSV applications include:

- Display Backlight Control
- Keyboard Illumination Control
- Printer Paper Detection
- Medical Diagnostics

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL2584TSV Block Diagram



Detailed Description

The TSL2584TSV contains two integrating analog-to-digital converters (ADC) that integrate currents from two photodiodes. Integration of both channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the Channel 0 and Channel 1 data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained. After the transfer, the device automatically begins the next integration cycle.

Communication with the device is accomplished through a standard, two-wire I²C serial bus. Consequently, the TSL2584TSV can be easily connected to a microcontroller or embedded controller. No external circuitry is required for signal conditioning. Because the output of the device is digital, the output is effectively immune to noise when compared to an analog signal.

The TSL2584TSV also supports an interrupt feature that simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. The primary purpose of the interrupt function is to detect a meaningful change in light intensity. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The device has the ability to define thresholds above and below the current light level. An interrupt is generated when the value of a conversion exceeds either of these limits.

Pin Assignment

The TSL2584TSV pin assignments are described below.

Figure 3:
Pin Diagram

Package TSV - 6 Lead Through - Silicon VIA (Top View): Package drawing is not to scale.

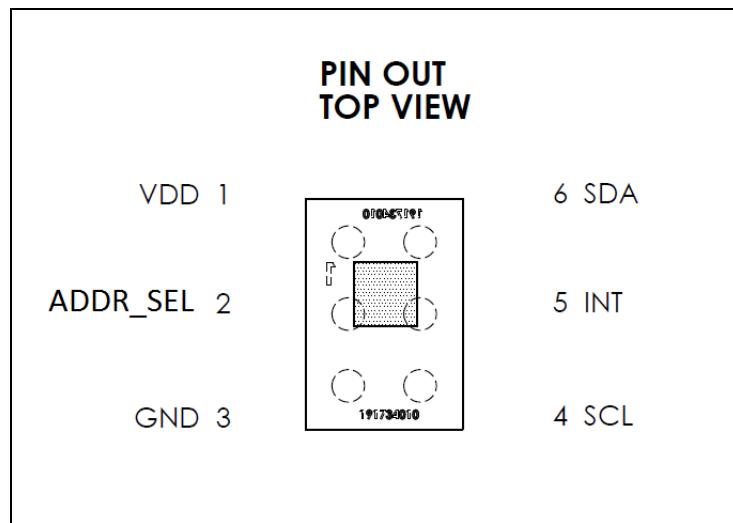


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	V _{DD}	Supply voltage
2	ADDR_SEL	Address select – three-state.
3	GND	Power supply ground. All voltages are referenced to GND.
4	SCL	I ² C serial clock input terminal
5	INT	Interrupt — open drain output (active low).
6	SDA	I ² C serial data I/O terminal

Absolute Maximum Ratings

Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions** is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Supply voltage, V_{DD}		3.8	V	All voltages are with respect to GND
Output terminal voltage V_O	-0.5	3.8	V	
Output terminal current I_O	-1	20	mA	
Storage temperature range, T_{STRG}	-40	85	°C	
ESD tolerance, human body model	± 2000		V	

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	2.7	3	3.6	V
T_A	Operating free-air temperature	-40		85	°C

Figure 7:
Operating Characteristics, $V_{DD}=3V$, $T_A=25^{\circ}C$ (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Supply Current	Active		175	250	μA
		Sleep state - no I ² C activity		3	10	
V_{OL}	INT, SDA output low voltage	3mA sink current	0		0.4	V
		6mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		-5		5	μA
V_{IH}	SCL, SDA input high voltage		1.25			V
V_{IL}	SCL, SDA input low voltage				0.54	V

Figure 8:

ALS Characteristics, $V_{DD}=3V$, $T_A=25^{\circ}C$, GAIN=16x, AEN=1(unless otherwise noted) ⁽¹⁾

Parameter	Conditions	Channel	Min	Typ	Max	Units
Dark ADC count value	$E_e = 0$, GAIN = 111x, ATIME=0xB6 (200ms)	CH0 CH1	0 0	1 1	3 3	counts
ADC integration time step size	ATIME = 0xFF		2.58	2.73	2.90	ms
ADC integration time steps ⁽⁴⁾			1		256	steps
Full scale ADC count value	ATIME = 0xDB (100ms) ATIME = 0x6C (400ms)				37887 65535	counts
ADC count value	White light $E_e = 218 \mu W/cm^2$ ATIME = 0xF6 (27ms) ⁽²⁾	CH0 CH1	2480	3100 223	3720	counts
	$\lambda_p = 850 \text{ nm}$ $E_e = 220 \mu W/cm^2$, ATIME = 0xF6 (27ms) ⁽³⁾	CH0			400	counts
ADC count value ratio: CH1/CH0	White light ⁽²⁾		0.036	0.072	0.108	
R_e Irradiance responsivity	White light, ATIME = 0xF6 (27 ms) ⁽²⁾	CH0 CH1	11.4	14.2 1.0	17.1	counts/ ($\mu W/cm^2$)
Gain scaling, relative to 1x gain setting	GAIN = 8x	CH0 CH1	7 7	8 8	9 9	x
	GAIN = 16x	CH0 CH1	15 15	16 16	17 17	
	GAIN = 111x Decoupling capacitor 25 mm from VDD pin ⁽⁵⁾	CH0 CH1	97 100	107 115	115 125	

Note(s) and/or Footnote(s):

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible white LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
2. The white LED irradiance is supplied by a white light-emitting diode with a nominal color temperature of 4000 K.
3. The 850 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength $\lambda_p = 850 \text{ nm}$ and spectral halfwidth $\Delta\lambda_{1/2} = 42 \text{ nm}$.
4. The integration time T_{int} is dependent on the internal oscillator frequency (f_{osc}) and on the number of integration cycles (ATIME) in the Timing Register as described in the register section. For nominal $f_{osc} = 750 \text{ kHz}$, nominal $T_{int} = 2.7 \text{ ms} \times \text{ATIME}$.
5. 111x gain is affected by the line inductance between the VDD pin and the decoupling capacitor.

Timing Characteristics

The timing characteristics of TSL2584TSV are given below.

Figure 9:

AC Electrical Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Parameter ⁽¹⁾	Description	Min	Max	Units
$t_{(CONV)}$	Conversion time	2.7	688	ms
$f_{(SCL)}$	Clock frequency	0	400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition	1.3		μs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6		μs
$t_{(SUSTA)}$	Repeated start condition setup time	0.6		μs
$t_{(SUSTO)}$	Stop condition setup time	0.6		μs
$t_{(HDDAT)}$	Data hold time	0.043	0.9	μs
$t_{(SUDAT)}$	Data setup time	100		ns
$t_{(LOW)}$	SCL clock low period	1.3		μs
$t_{(HIGH)}$	SCL clock high period	0.6		μs
t_F	Clock/data fall time		300	ns
t_R	Clock/data rise time		300	ns
C_i	Input pin capacitance		10	pF

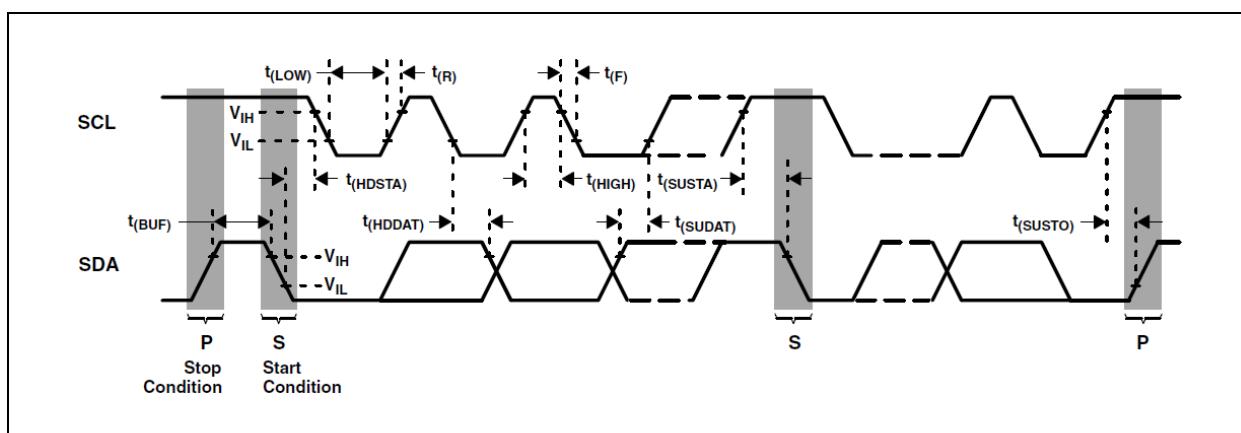
Note(s) and/or Footnote(s):

1. Specified by design and characterization; not production tested.

Timing Diagrams

Figure 10:

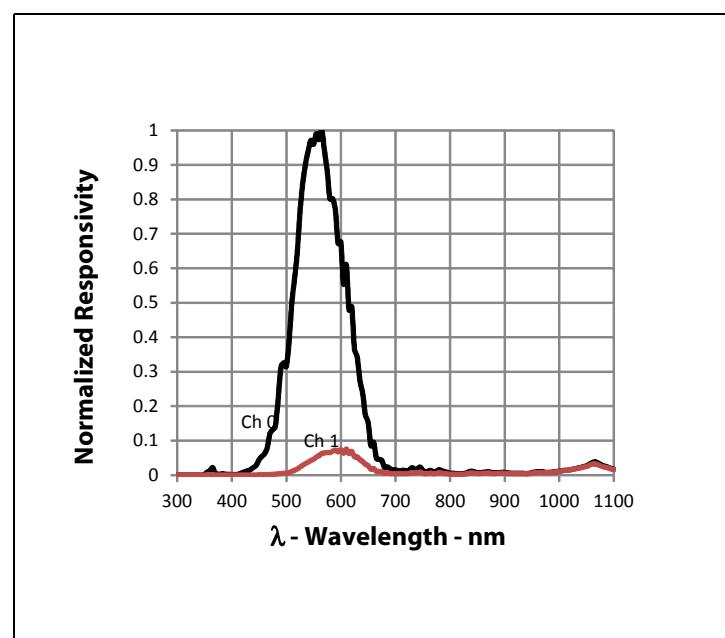
Parameter Measurement Information



Typical Operating Characteristics

Spectral Responsivity: Two channel response allows for tunable illuminance (lux) calculation regardless of transmissivity of glass.

Figure 11:
Spectral Responsivity



111x Gain Scale vs. Line Inductance:
High gain mode (111x) dependency on the line inductance between the VDD pin and the decoupling capacitor.

Figure 12:
111x Gain Scale vs. Line Inductance

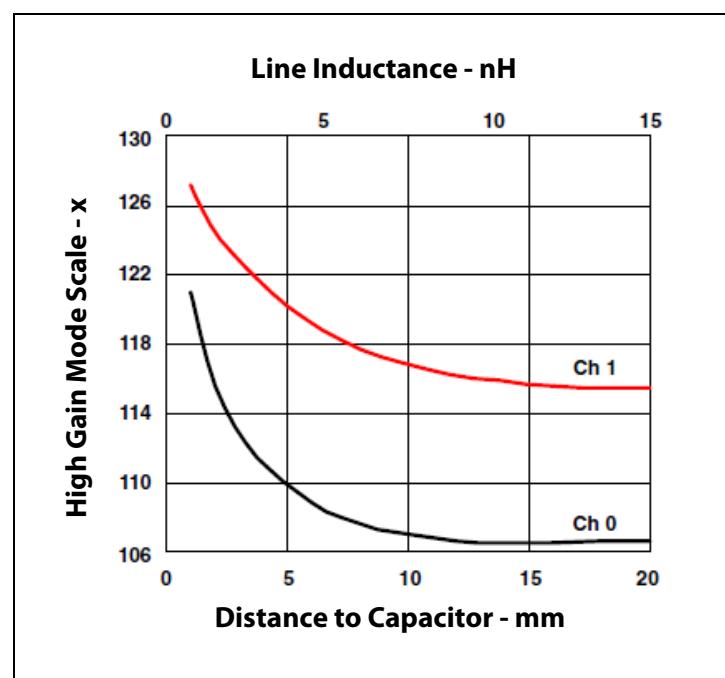


Figure 13:
Ch0 Response to White LED (CCT = 4000K) vs. Incident Angle



Digital Interface

Interface and control of the device is accomplished through a two-wire serial interface to a set of registers that provide access to device control functions and output data. The serial interface is compatible with the I²C bus, Fast-Mode. The device offers three slave addresses that are selectable via an external pin (ADDR SEL). The slave address options are shown in [Figure 14](#).

Figure 14:
Slave Address Selection

ADDR SEL Terminal Level	7-BIT Slave Address	
GND	0101001	0x29
Float	0111001	0x39
V _{DD}	1001001	0x49

Note(s) and/or Footnote(s):

1. The slave addresses are 7 bits. A read/write bit should be appended to the slave address by the master device to properly communicate with the slave device.

Register Description

The device is controlled and monitored by sixteen registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in [Figure 15](#).

Figure 15:
Register Map

Address	Register Name	R/W	Register Function
--	COMMAND	W	Specifies register address
00h	CONTROL	R/W	Control of basic functions
01h	TIMING		Integration time/gain control
02h	INTERRUPT		Interrupt control
03h	THLLOW		Low byte of low interrupt threshold
04h	THLHIGH		High byte of low interrupt threshold
05h	THHLOW		Low byte of high interrupt threshold
06h	THHHIGH		High byte of high interrupt threshold
07h	ANALOG		Analog control register
12h	ID	R	Part number / Rev ID
14h	DATA0LOW		ADC Channel 0 - LOW data register
15h	DATA0HIGH		ADC Channel 0 - HIGH data register
16h	DATA1LOW		ADC Channel 1 - LOW data register
17h	DATA1HIGH		ADC Channel 1 - HIGH data register
18h	TIMERLOW		Manual integration timer LOW register
19h	TIMERHIGH		Manual integration timer HIGH register
1Eh	ID2	R/W	Supplemental identification

The mechanics of accessing a specific register depends on the specific I²C protocol used. See the section on I²C protocols, above. In general, the Command Register is written first to specify the specific control/status register for following read/write operations.

Command Register

The Command Register specifies the address of the target register for subsequent read and write operations and contains eight bits as described in [Figure 16](#). The command register defaults to 00h at power on.

Figure 16:
Command Register

	7	6	5	4	3	2	1	0
CMD	TRANSACTION			ADDRESS				
Fields								
CMD	7	Select command register. Must write as 1 when addressing COMMAND register.						
TRANSACTION	6:5	Select type of transaction to follow in subsequent data transfers:						
		FIELD VALUE		DESCRIPTION				
		00		Repeated byte protocol transaction				
		01		Auto - increment protocol transaction				
		10		Reserved - Do not use				
		11		Special function - See description below				
		Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.						

Fields	Bits	Description (Reset - 00h)		
ADDRESS	4:0	Register Address/Special Function. This field selects the specific control or status register for following write and read commands according to Figure 15 . When the TRANSACTION field is set to 11b, this field specifies a special command function as outlined below.		
		FIELD VALUE	SPECIAL FUNCTION	DESCRIPTION
		00000	Reserved	Reserved
		00001	Interrupt clear	Clear any pending interrupt and is a write-once-to-clear bit
		00010	Stop manual integration	When the Timing Register is set to 00h, a Byte command with the ADDRESS field set to 0010b will stop a manual integration. The actual length of the integration cycle may be read in the MANUAL INTEGRATION TIMER Register.
		00011	Start manual integration	When the Timing Register is set to 00h, a Byte command with the ADDRESS field set to 0011b will start a manual integration. The actual length of the integration cycle may be read in the MANUAL INTEGRATION TIMER Register.
		x11xx	Reserved	Reserved

Control Register (00h)

The Control Register is used primarily to power the device up and down as shown in [Figure 17](#).

Figure 17:
Control Register.

7	6	5	4	3	2	1	0
Reserved		ADC_INTR	ADC_VALID	Reserved		ADC_EN	POWER

Field	Bits	Description (Reset - 00h)
Reserved	7:6	Reserved. Write as 0.
ADC_INTR	5	ADC Interrupt. Read only. Indicates that the device is asserting an interrupt.
ADC_VALID	4	ADC Valid. Read only. Indicates that the ADC Channel has completed an integration cycle.
Reserved	3:2	Reserved. Write as 0.
ADC_EN	1	ADC Enable. This field enables the two ADC Channels to begin integration. Writing a 1 activates the ADC Channels, and writing a 0 disables the ADCs.
POWER	0	Power On. Writing a 1 powers on the device, and writing a 0 turns it off.

Note(s) and/or Footnote(s):

1. ADC_EN and POWER must be asserted before the ADC changes will operate correctly. After POWER is asserted, a 2-ms delay is required before asserting ADC_EN.
2. The device registers should be configured before ADC_EN is asserted.

Timing Register (01h)

The Timing Register controls the internal integration time of the ADC Channels in 2.7 ms increments. The TIMING register defaults to 00h at power on.

Figure 18:
Timing Register

7	6	5	4	3	2	1	0
ATIME							
Field	Bits	Description (Reset = 00h)					
ATIME	7:0	Integration Cycles. Specifies the integration time in 2.7-ms intervals. Time is expressed as a 2's complement number. So, to quickly work out the correct value to write: <ul style="list-style-type: none">• (Step 1) Determine the number of 2.7-ms intervals required• (Step 2) Take the 2's complement. Example: For a 1 × 2.7-ms interval, 0xFF should be written. For 2 × 2.7-ms intervals, 0xFE should be written. The maximum integration time is 688.5 ms (00000001b). Writing a 0x00 to this register is a special case and indicates manual timing mode. See CONTROL and MANUAL INTEGRATION TIMER Registers for other device options related to manual integration.					
		INTEG_CYCLES	TIME	VALUE			
		–	Manual integration	00000000			
		1	2.7 ms	11111111			
		2	5.4 ms	11111110			
		19	51.3 ms	11101101			
		37	99.9 ms	11011011			
		74	199.8 ms	10110110			
		148	399.6 ms	01101100			
		255	688.5 ms	00000001			

Note(s) and/or Footnote(s):

1. The Byte protocol cannot be used when ATIME is greater than 127 (for example ATIME[7] = 1) since the upper bit is set aside for write transactions in the COMMAND register.

Interrupt Register (02h)

The Interrupt Register controls the extensive interrupt capabilities of the device. The open-drain interrupt pin is active low and requires a pull-up resistor to V_{DD} in order to pull high in the inactive state. The Interrupt Register provides control over when a meaningful interrupt will occur. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence of that change in intensity. The value must cross the threshold (as configured in the Threshold Registers 03h through 06h) and persist for some period of time as outlined in [Figure 19](#).

When a level Interrupt is selected, an interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window. The interrupt is active-low and remains asserted until cleared by writing an 11 in the TRANSACTION field in the COMMAND register.

Figure 19:
Interrupt Control Register

7	6	5	4	3	2	1	0
Reserved	INTR_STOP		INTR			PERSIST	

Field	Bits	Description (Reset = 00h)
Reserved	7	Reserved. Write as 0.
INTR_STOP ⁽²⁾	6	Stop ADC Integration on Interrupt. When high, ADC integration will stop once an interrupt is asserted. To resume operation (1) de-assert ADC_EN using CONTROL register, (2) clear interrupt using COMMAND register, and (3) re-assert ADC_EN using CONTROL register.
INTR	5:4	INTR Control Select. This field determines mode of interrupt logic according to Figure 20 , below.
PERSIST	3:0	Interrupt Persistence. Controls rate of interrupts to the host processor as shown in Figure 21 , below.

Note(s) and/or Footnote(s):

1. Interrupts are based on the value of Channel 0 only.
2. Use this bit to isolate a particular condition when the sensor is continuously integrating.

Figure 20:
Interrupt Control Select

INTR Field Value	Read Value
00	Interrupt output disabled
01	Level Interrupt
10	Reserved
11	Reserved

Note(s) and/or Footnote(s):

1. Field value of 11 may be used to test interrupt connectivity in a system or to assist in debugging interrupt service routine software.

Figure 21:
Interrupt Persistence Select

Persist Field Value	Interrupt Persist Function
0000	Every ADC cycle generates interrupt
0001	Any value outside of threshold range
0010	2 integration time periods out of range
0011	3 integration time periods out of range
0100	4 integration time periods out of range
0101	5 integration time periods out of range
0110	6 integration time periods out of range
0111	7 integration time periods out of range
1000	8 integration time periods out of range
1001	9 integration time periods out of range
1010	10 integration time periods out of range
1011	11 integration time periods out of range
1100	12 integration time periods out of range
1101	13 integration time periods out of range
1110	14 integration time periods out of range
1111	15 integration time periods out of range

Interrupt Threshold Registers (03h-06h)

The Interrupt Threshold Registers store the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by Channel 0 crosses below or is equal to the low threshold specified, an interrupt is asserted on the interrupt pin. If the value generated by Channel 0 crosses above the high threshold specified, an interrupt is asserted on the interrupt pin. Registers THLLOW and THLHIGH provide the low byte and high byte, respectively, of the lower interrupt threshold. Registers THHLOW and THHHIGH provide the low and high bytes, respectively, of the upper interrupt threshold. The high and low bytes from each set of registers are combined to form a 16-bit threshold value. The interrupt threshold registers default to 00h on power up.

Figure 22:
Interrupt Threshold Registers

Register	Address	Bits	Description
THLLOW	3h	7:0	ADC Channel 0 lower byte of the low threshold
THLHIGH	4h	7:0	ADC Channel 0 upper byte of the low threshold
THHLOW	5h	7:0	ADC Channel 0 lower byte of the high threshold
THHHIGH	6h	7:0	ADC Channel 0 upper byte of the high threshold

Note(s) and/or Footnote(s):

1. Since two 8-bit values are combined for a single 16-bit value for each of the high and low interrupt thresholds, the Byte protocol should not be used to write to these registers. Any values transferred by the Byte protocol with the MSB set would be interpreted as the COMMAND field and stored as an address for subsequent read/write operations and not as the interrupt threshold information as desired. The Write Word protocol should be used to write byte-paired registers. For example, the THLLOW and THLHIGH registers (as well as the THHLOW and THHHIGH registers) can be written together to set the 16-bit ADC value in a single transaction.

Analog Register (07h)

The Analog Register provides eight bits of control to the analog block. These bits control the analog gain settings of the device.

Figure 23:
Analog Register

7	6	5	4	3	2	1	0
Reserved						GAIN	

Field	Bits	Description (Reset = 00h)	
Reserved	7:2	Reserved. Write as 0.	
GAIN	1:0	Gain Control. Sets the analog gain of the device according to the following Figure 24 .	
		FIELD VALUE	GAIN VALUE
		00	1×
		01	8×
		10	16×
		11	111×

ID Register (12h)

The ID Register provides the value for both the part number and silicon revision number for that part number. It is a read-only register whose value never changes.

Figure 24:
ID Register

7	6	5	4	3	2	1	0
PARTNO				REVNO			

Field	Bits	Description
PARTNO	7:4	Part Number Identification: field value 1001b
REVNO	3:0	Revision number identification

ADC Channel Data Registers (14h-17h)

The ADC Channel data are expressed as 16-bit values spread across two registers. The ADC Channel 0 data registers, DATA0LOW and DATA0HIGH provide the lower and upper bytes, respectively, of the ADC value of Channel 0. Registers DATA1LOW and DATA1HIGH provide the lower and upper bytes, respectively, of the ADC value of Channel 1. All Channel data registers are read-only and default to 00h on power up.

Figure 25:
ADC Channel Data Registers

Register	Address	Bits	Description
DATA0LOW	14h	7:0	ADC Channel 0 lower byte
DATA0HIGH	15h	7:0	ADC Channel 0 upper byte
DATA1LOW	16h	7:0	ADC Channel 1 lower byte
DATA1HIGH	17h	7:0	ADC Channel 1 upper byte

Note(s) and/or Footnote(s):

1. The Read Word protocol can be used to read byte-paired registers. For example, the DATA0LOW and DATA0HIGH registers (as well as the DATA1LOW and DATA1HIGH registers) may be read together to obtain the 16-bit ADC value in a single transaction.

The upper byte data registers can only be read following a read to the corresponding lower byte register. When the lower byte register is read, the upper eight bits are strobed into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Manual Integration Timer Registers (18h-19h)

The Manual Integration Timer Registers provide the number of cycles in 10.9 μ s increments that occurred during a manual start/stop integration period. The timer is expressed as a 16-bit value across two registers. See CONTROL and TIMING Registers for further instructions in configuring a manual integration. The maximum time that can be derived without an overflow is 714.3ms.

Figure 26:
Manual Integration Timer Registers

7	6	5	4	3	2	1	0
TIMER							
Register	Address	Bits	Description (Reset = 00h)				
TIMERLOW	18h	7:0	Manual Integration Timer lower byte				
TIMERHIGH	19h	7:0	Manual Integration Timer upper byte				

ID2 Register (1Eh)

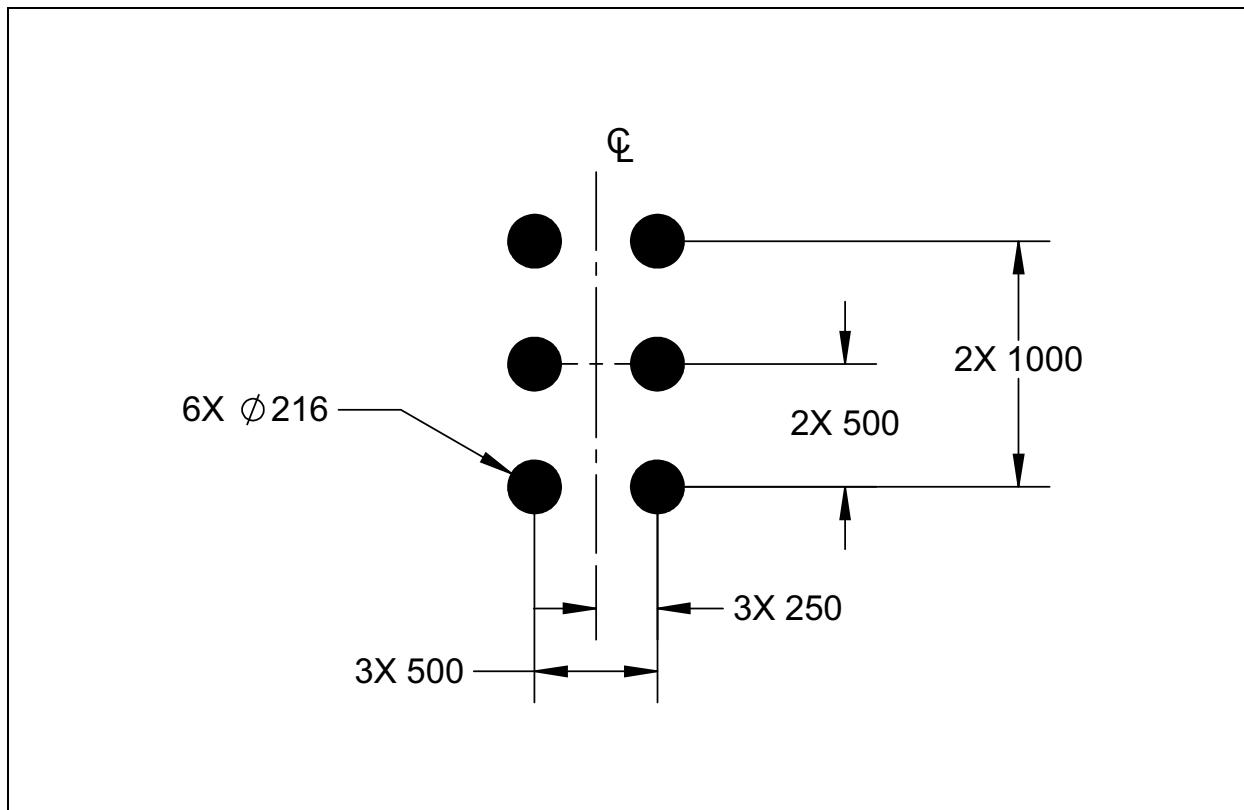
The ID2 Register provides the means to identify the device as TSL2584TSV. Although this is a W/R register, it is strongly advised that this register not be written to. Any value written to this register could adversely affect the performance of the device.

Figure 27:
ID2 Register

7	6	5	4	3	2	1	0
ID2	Reserved						
Field	Bits	Description					
ID2	7	This bit will be set (1) for all TSL2584TSV devices					
Reserved	6:0	Reserved					

PCB Pad Layout

Figure 28:
Suggested TSV Package PCB Layout

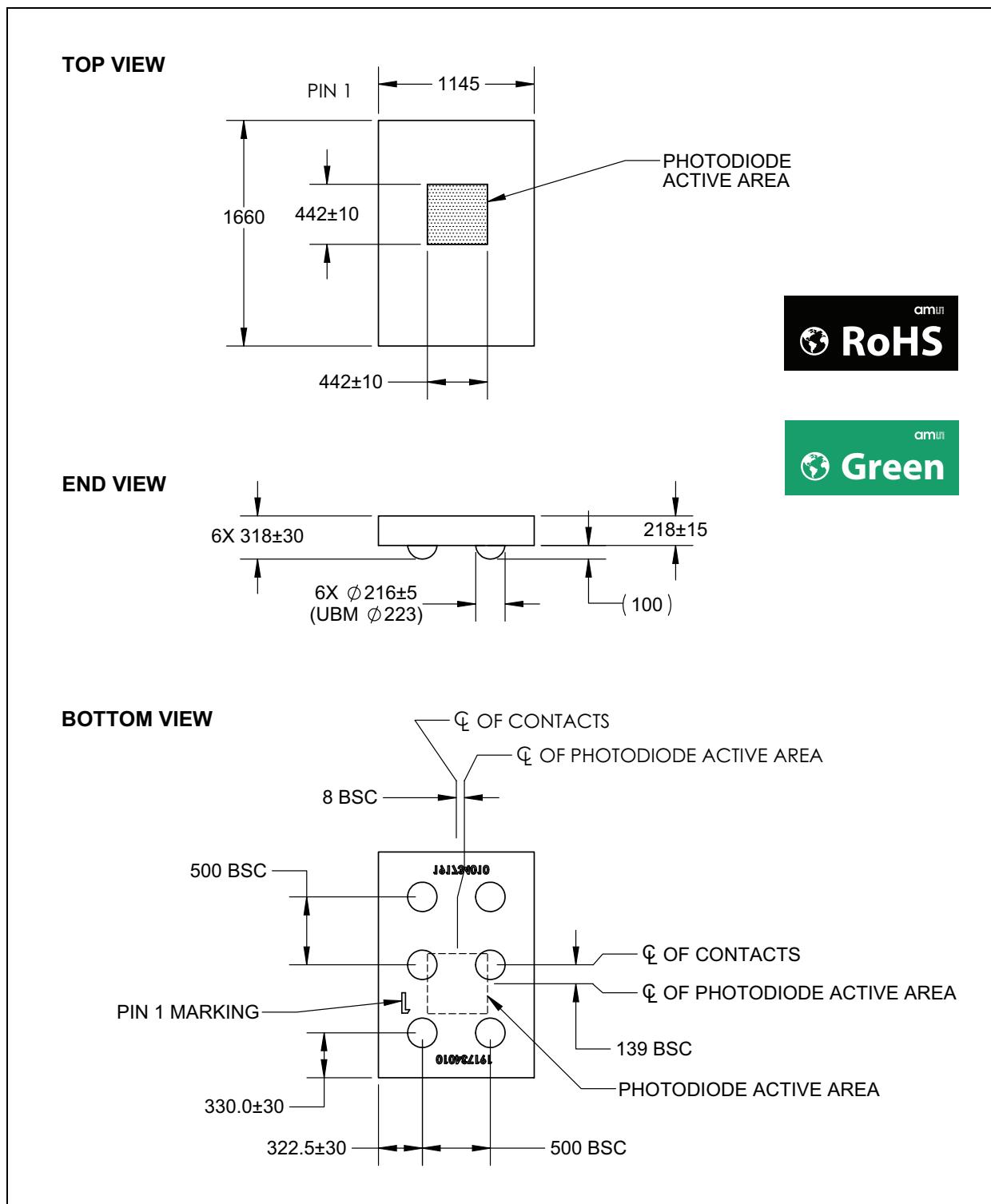


Note(s) and/or Footnote(s):

1. All linear dimensions are in microns.
2. This drawing is subject to change without notice.

Package Drawings & Markings

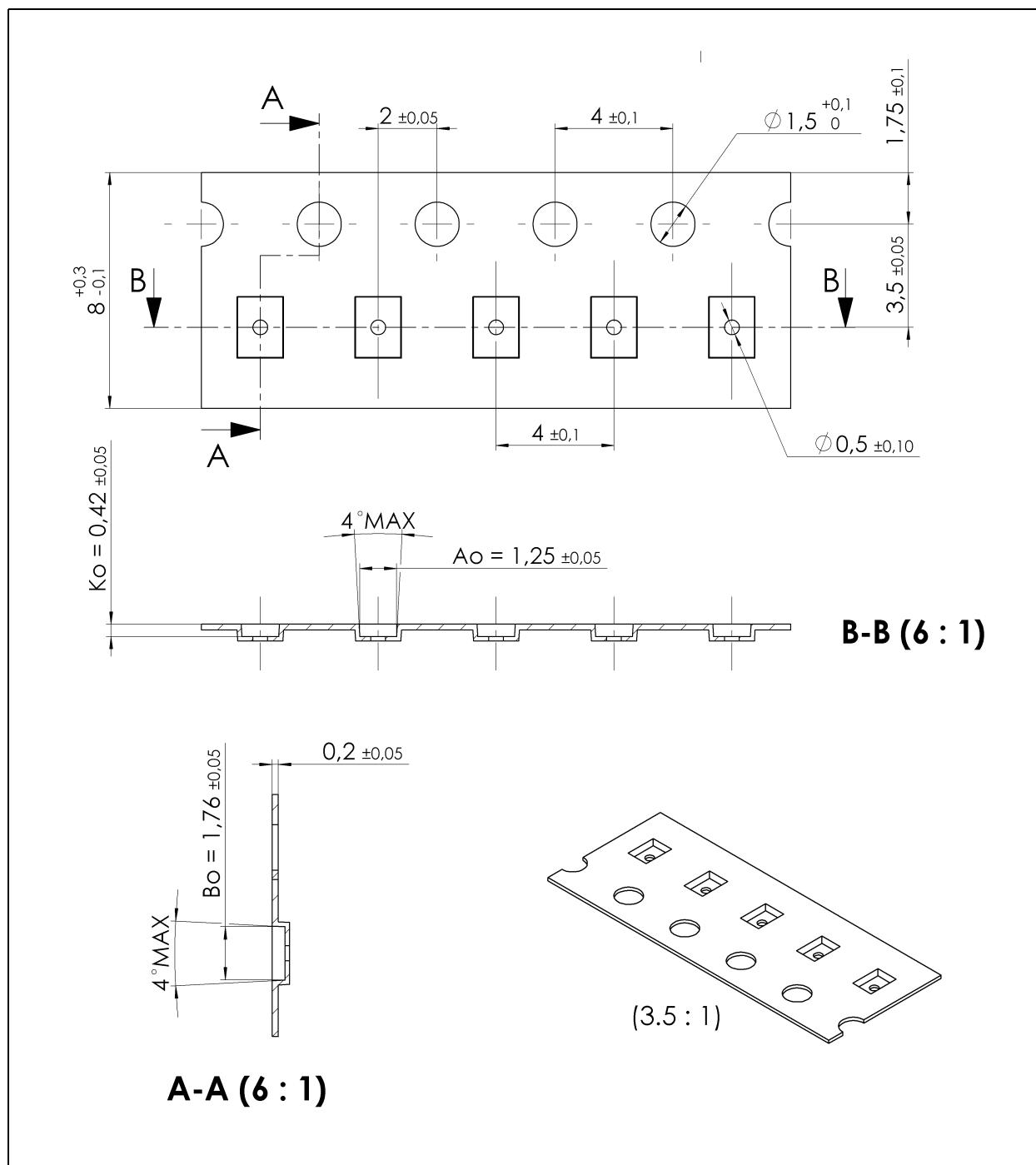
Figure 29:
Package TSV - Six-Lead Chipscale Packing Configuration

**Note(s) and/or Footnote(s):**

1. Dimensions are in microns.
2. Dimension tolerance is $\pm 25\mu\text{m}$ unless otherwise noted.
3. This drawing is subject to change without notice.
4. UBM (under ball metalization) is $\phi 223\mu\text{m}$.

Tape & Reel Information

Figure 30:
TSL2584TSV – Carrier Tape & Reel Information



Soldering & Storage Information

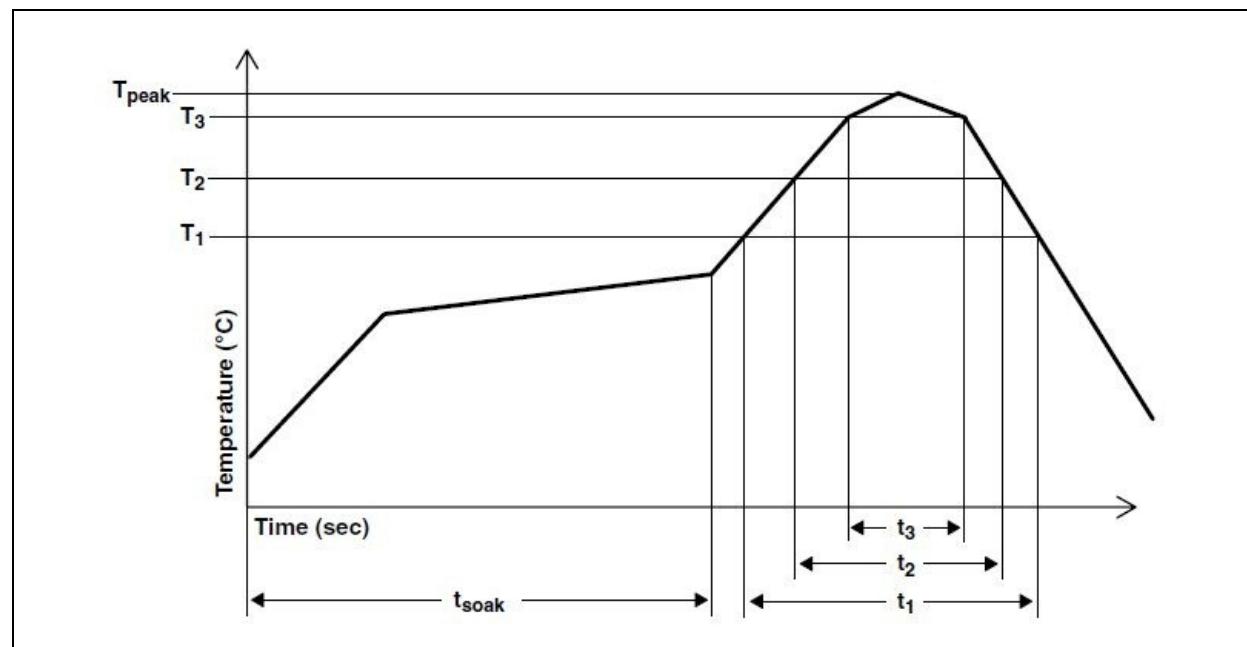
Soldering Information

The reflow profile specified here describes expected maximum heat exposure of devices during the solder reflow process of the device on a PCB. Temperature is measured at the top of the device. Devices should be limited to one pass through solder reflow profile. It is recommended after solder reflow that underfill is used for increased robustness.

Figure 31:
Solder Reflow Profile

Symbol	Parameter	Device
	Average temperature gradient in preheating	2.5 °C/sec
t_{soak}	Soak time	2 to 3 minutes
t_1	Time above 217 °C (T_1)	Max 60 sec
t_2	Time above 230 °C (T_2)	Max 50 sec
t_3	Time above $T_{peak} - 10$ °C (T_3)	Max 10 sec
T_{peak}	Peak temperature in reflow	260 °C (-0 °C/+5 °C)
	Temperature gradient in cooling	Max -5 °C/sec

Figure 32:
Solder Reflow Profile Graph



Note(s) and/or Footnote(s):

1. Not to scale – for reference only.

Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Floor Life

This package has been assigned a moisture sensitivity level of MSL 1. As a result, the floor life of the devices removed from the moisture barrier bag is unlimited from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: Unlimited
- Ambient Temperature: < 30°C
- Relative Humidity: < 85%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 33:
Ordering Information

Ordering Code	Interface	Delivery Form	Delivery Quantity
TSL2584TSV	I ² C $V_{bus} = 1.8$ V Interface	Tape & Reel	3500 pcs/reel

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 1-03 (2015-Jun-10) to current revision 1-05 (2015-Sep-01)	Page
1-03 (2015-Jun-10) to 1-04 (2015-Aug-31)	
Added Figure 13	10
Updated Figure 28	23
Updated Figure 29	24
1-04 (2015-Aug-31) to 1-05 (2015-Sep-01)	
Updated Figure 13	10

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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