

N-Channel Power MOSFET

40V, 91A, 7mΩ

FEATURES

- Low $R_{DS(on)}$ to minimize conductive losses
- Logic level
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

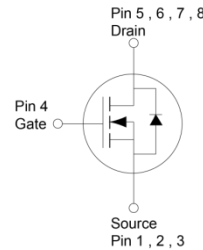
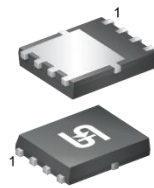
PARAMETER		VALUE	UNIT
V_{DS}		40	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	7	mΩ
	$V_{GS} = 4.5V$	8.9	
Q_g		11.5	nC

APPLICATIONS

- Motor Control for BLDC
- Battery Power Management
- DC-DC converter
- 2nd Synchronous Rectifier



PDFN56



Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	91	A
	$T_A = 25^\circ\text{C}$		14	
Pulsed Drain Current (Note 1)		I_{DM}	364	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	33	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	163	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	113	W
	$T_C = 125^\circ\text{C}$		22	
Total Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2.6	W
	$T_A = 125^\circ\text{C}$		0.5	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.1	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	48	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 3)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	40	--	--	V
Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250μA	V _{GS(TH)}	1.2	1.6	2.5	V
Gate-Source Leakage Current	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V _{GS} = 0V, V _{DS} = 40V	I _{DSS}	--	--	1	μA
	V _{GS} = 0V, V _{DS} = 40V T _J = 125°C		--	--	100	
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 14A	R _{DS(on)}	--	4.5	7	mΩ
	V _{GS} = 4.5V, I _D = 14A		--	5.7	8.9	
Forward Transconductance	V _{DS} = 5V, I _D = 14A	g _{fs}	--	41	--	S
Dynamic ^(Note 4)						
Total Gate Charge	V _{GS} = 10V, V _{DS} = 20V, I _D = 14A	Q _g	--	23.5	--	nC
Total Gate Charge	V _{GS} = 4.5V, V _{DS} = 20V, I _D = 14A	Q _g	--	11.5	--	
Gate-Source Charge		Q _{gs}	--	4.3	--	
Gate-Drain Charge		Q _{gd}	--	3.8	--	
Input Capacitance	V _{GS} = 0V, V _{DS} = 20V f = 1.0MHz	C _{iss}	--	1469	--	pF
Output Capacitance		C _{oss}	--	317	--	
Reverse Transfer Capacitance		C _{rss}	--	80	--	
Gate Resistance	f = 1.0MHz, open drain	R _g	0.8	2.8	5.6	Ω
Switching ^(Note 4)						
Turn-On Delay Time	V _{GS} = 10V, V _{DS} = 20V, I _D = 9A, R _G = 10Ω,	t _{d(on)}	--	14.1	--	ns
Turn-On Rise Time		t _r	--	8.9	--	
Turn-Off Delay Time		t _{d(off)}	--	48	--	
Turn-Off Fall Time		t _f	--	8.4	--	
Source-Drain Diode ^(Note 3)						
Forward Voltage	V _{GS} = 0V, I _S = 14A	V _{SD}	--	--	1.2	V
Reverse Recovery Time	I _S = 14A , dI/dt = 100A/μs	t _{rr}	--	19	--	ns
Reverse Recovery Charge		Q _{rr}	--	12	--	nC

Notes:

- Current limited by package.
- $L = 0.3\text{mH}$, $V_{GS} = 10V$, $V_{DS} = 30V$, $R_G = 25\Omega$, $I_{AS} = 33A$, Starting $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

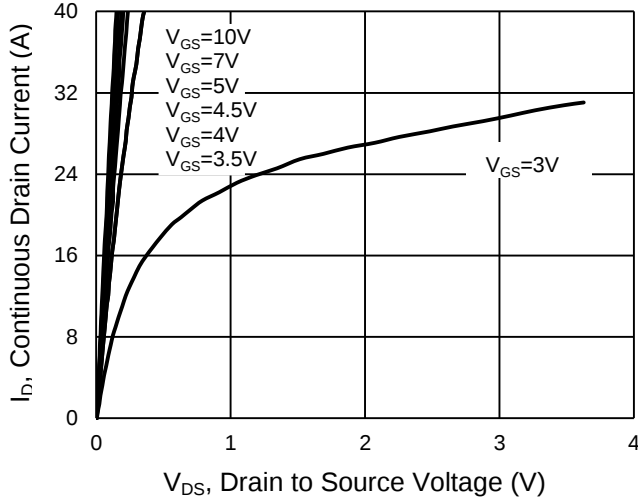
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM070NA04LCR RLG	PDFN56	2,500pcs / 13" Reel

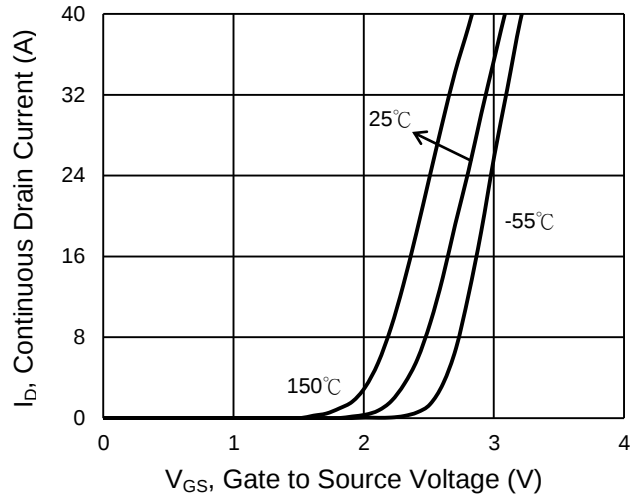
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

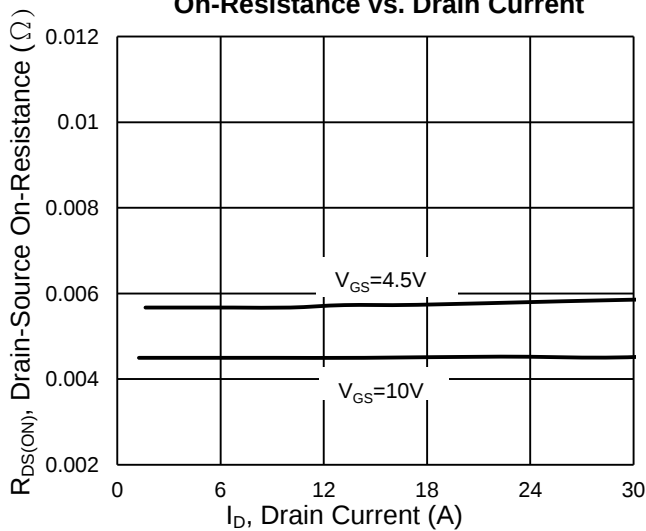
Output Characteristics



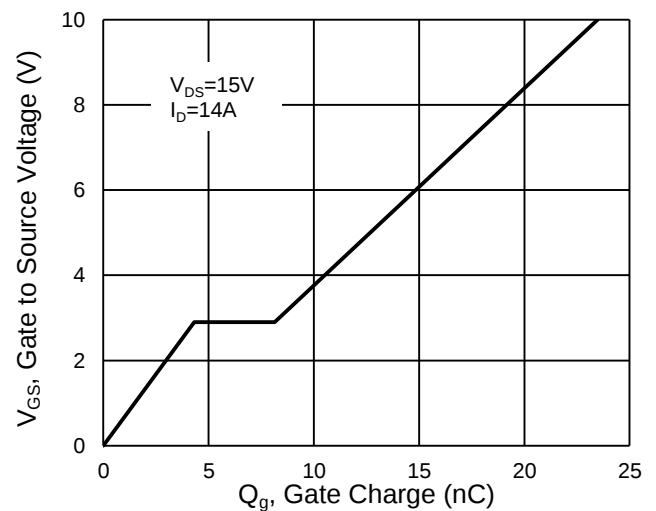
Transfer Characteristics



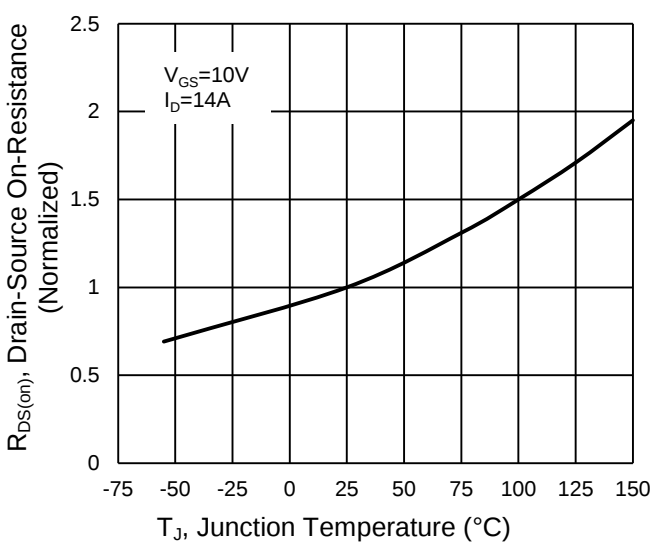
On-Resistance vs. Drain Current



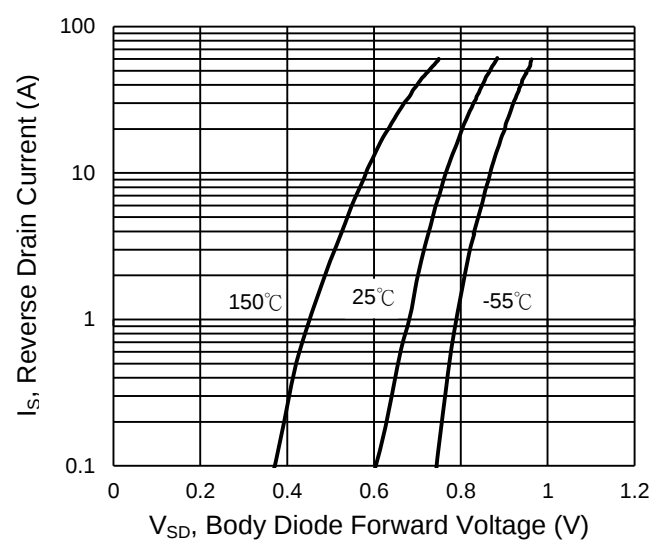
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



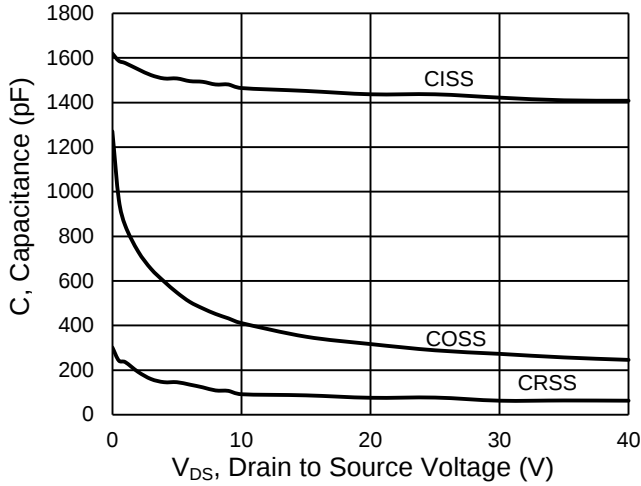
Source-Drain Diode Forward Current vs. Voltage



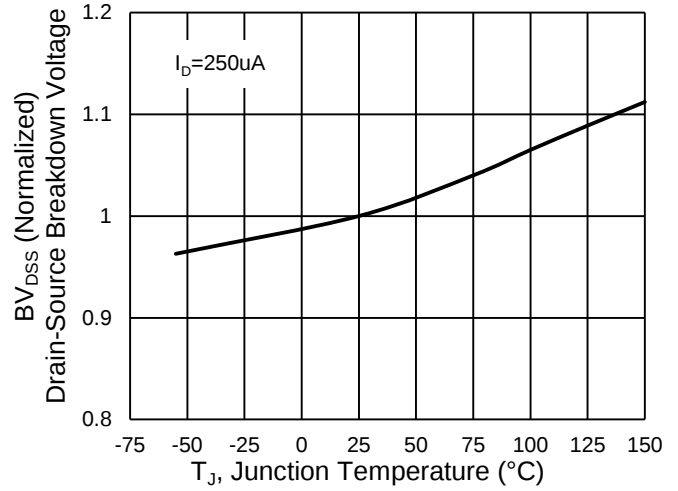
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

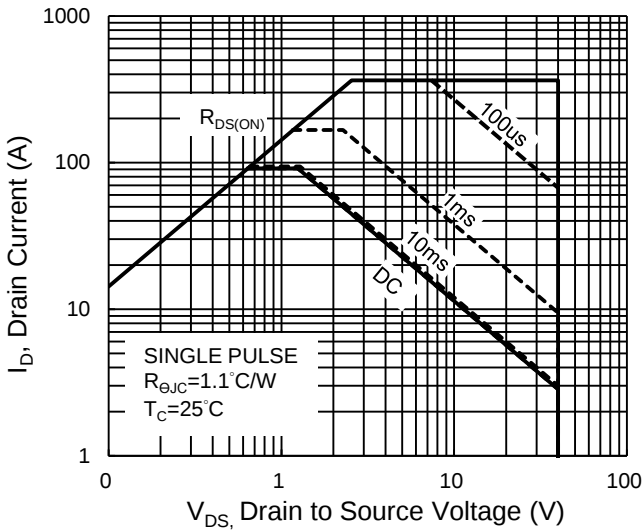
Capacitance vs. Drain-Source Voltage



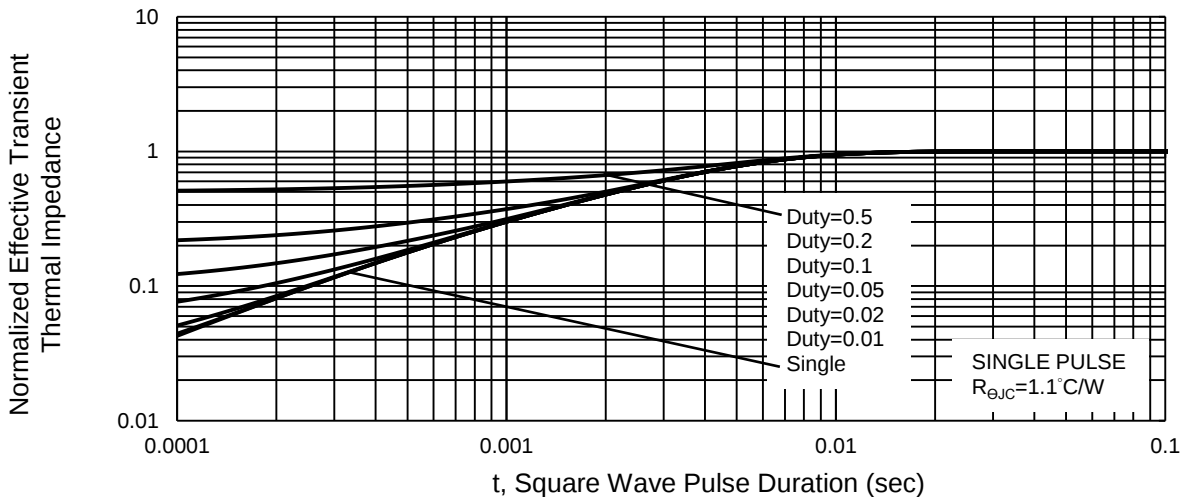
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area, Junction-to-Case

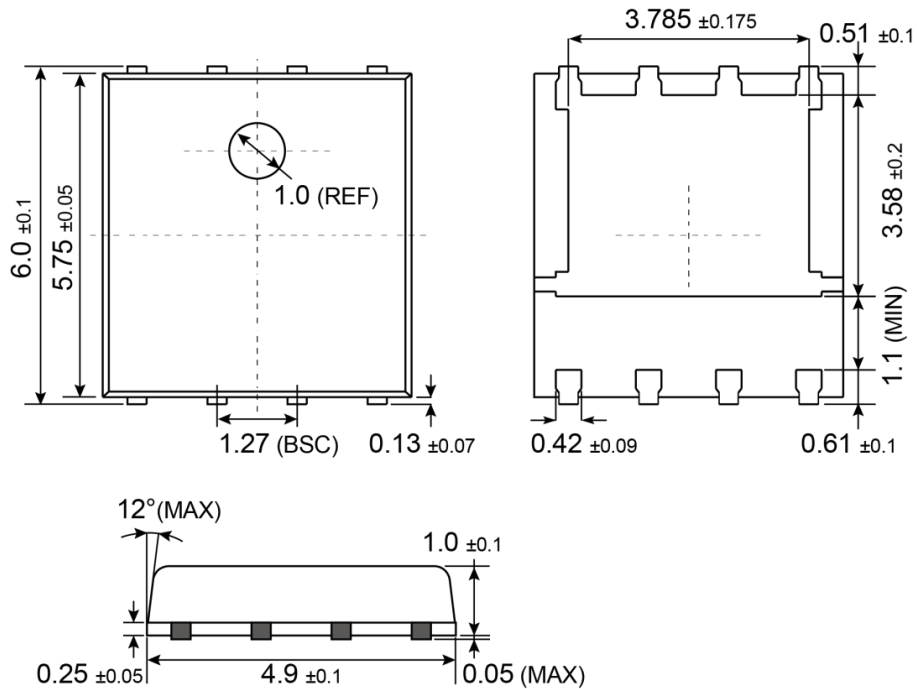


Normalized Thermal Transient Impedance, Junction-to-Case

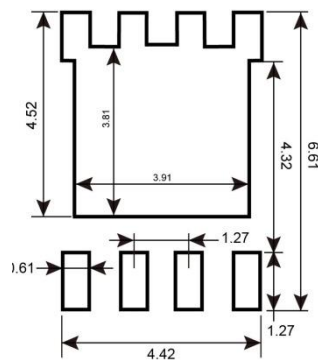


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

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