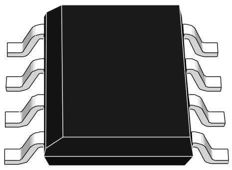
TSV912H

High temperature, rail-to-rail input/output, 8 MHz operational amplifier

Datasheet - production data



SO8

Features

- Rail-to-rail input and output
- Wide bandwidth
- Low power consumption: 820 µA typ
- Unity gain stability
- High output current: 35 mA
- Operating range from 2.5 to 5.5 V
- Low input bias current, 1 pA typ
- ESD internal protection ≥ 5 kV
- Latch-up immunity

Applications

- Automotive products

Description

The TSV912H operational amplifier offers low voltage operation and rail-to-rail input and output.

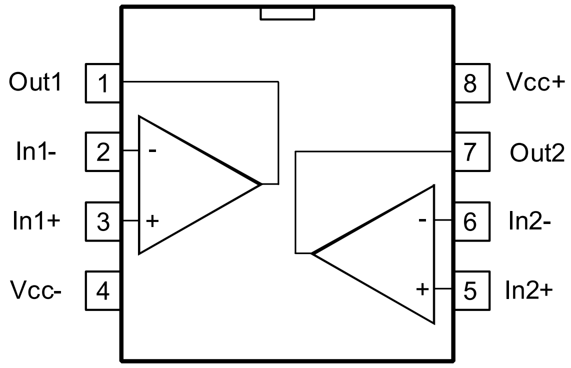
The device features an excellent speed/power consumption ratio, offering an 8 MHz gain-bandwidth product while consuming only 1.1 mA maximum at 5 V. It is unity gain stable and features an ultra-low input bias current.

The TSV912H is a high temperature version of the TSV912, and can operate from -40 °C to 150 °C with unique characteristics. Its main target applications are automotive, but the device is also ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

Contents

1 Package pin connections

Figure 1: Pin connection (top view)



2 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage, $(V_{CC}^+) - (V_{CC}^-)$ (1)	6	V
V_{id}	Differential input voltage (2)	$\pm V_{CC}$	
V_{in}	Input voltage (3)	$(V_{CC}^-) - 0.2$ to $(V_{CC}^+) + 0.2$	
I_{in}	Input current (4)	10	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Maximum junction temperature	160	
R_{thja}	Thermal resistance junction to ambient (5)(6)	125	°C/W
R_{thjc}	Thermal resistance junction to case (5)(6)	40	
ESD	HBM: human body model (7)	5	kV
	MM: machine model (8)	400	V
	CDM: charged device model (9)	1500	
	Latch-up immunity	200	mA

Notes:

(1)All voltage values, except the differential voltage, are with respect to the network ground terminal.

(2)Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

(3)$V_{CC} - V_{in}$ must not exceed 6 V.

(4)Input current must be limited by a resistor in series with the inputs.

(5)R_{th} are typical values.

(6)Short-circuits can cause excessive heating and destructive dissipation.

(7)Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

(8)Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

(9)Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage $(V_{CC}^+) - (V_{CC}^-)$	2.5 to 5.5	V
V_{icm}	Common mode input voltage range	$(V_{CC}^-) - 0.1$ to $(V_{CC}^+) + 0.1$	
T_{oper}	Operating free-air temperature range	-40 to 150	°C

3 Electrical characteristics

Table 3: Electrical characteristics at VCC+ = 2.5 V with VCC- = 0 V, Vicm = VCC/2, RL connected to VCC/2, T = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		0.1	4.5	mV
		$T_{min} < T < T_{max}$			7.5	
DV_{io}/DT	Input offset voltage drift	-40 °C < T < 125 °C		2		μV/°C
		125 °C < T < 150 °C		20		
I_{io}	Input offset current	$V_{out} = V_{CC}/2$, T = 25 °C		1	10 (1)	pA
		$V_{out} = V_{CC}/2$, $T_{min} < T < T_{max}$			5	nA
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$, T = 25 °C		1	10 (1)	pA
		$V_{out} = V_{CC}/2$, $T_{min} < T < T_{max}$			5	nA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 2.5 V, V_{out} = 1.25 V, T = 25 °C	58	75		dB
		0 V to 2.5 V, V_{out} = 1.25 V, $T_{min} < T < T_{max}$	53			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 2 V, T = 25 °C	80	89		
		R_L = 10 kΩ, V_{out} = 0.5 V to 2 V, $T_{min} < T < T_{max}$	70			
V_{CC} - V_{OH}	High-level output voltage	R_L = 10 kΩ, T = 25 °C		15	40	mV
		R_L = 10 kΩ, $T_{min} < T < T_{max}$			60	
		R_L = 600 Ω, T = 25 °C		45	150	
		R_L = 600 Ω, $T_{min} < T < T_{max}$			250	
V_{OL}	Low-level output voltage	R_L = 10 kΩ, T = 25 °C		15	40	
		R_L = 10 kΩ, $T_{min} < T < T_{max}$			60	
		R_L = 600 Ω, T = 25 °C		45	150	
		R_L = 600 Ω, $T_{min} < T < T_{max}$			250	
I_{out}	I_{sink}	V_{out} = 2.5 V, T = 25 °C	18	32		mA
		V_{out} = 2.5 V, $T_{min} < T < T_{max}$	14			
	I_{source}	V_{out} = 0 V, T = 25 °C	18	35		
		V_{out} = 0 V, $T_{min} < T < T_{max}$	14			
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$, T = 25 °C		0.78	1.1	
		No load, $V_{out} = V_{CC}/2$, $T_{min} < T < T_{max}$			1.1	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T = 25 °C		8		MHz
		R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, $T_{min} < T < T_{max}$		4		
F_u	Unity gain frequency	R_L = 2 kΩ, C_L = 100 pF		7.2		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		45		Degrees
G_m	Gain margin			8		dB
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_v = 1, T = 25 °C		4.5		V/μs
		R_L = 2 kΩ, C_L = 100 pF, A_v = 1, $T_{min} < T < T_{max}$		3.5		
e_n	Equivalent input noise voltage	f = 10 kHz		21		nV/√Hz
THD+e_n	Total harmonic distortion	G =1, f =1 kHz, R_L = 2 kΩ, Bw = 22 kHz, $V_{icm} = (V_{CC} + 1)/2$, V_{out} = 1.1 V_{pp}		0.001		%

Notes:

(1)Guaranteed by design.

Table 4: Electrical characteristics at VCC+ = 3.3 V with VCC- = 0 V, Vicm = VCC/2, RL connected to VCC/2, T = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		0.1	4.5	mV
		$T_{min} < T < T_{max}$			7.5	
DV_{io}	Input offset voltage drift	-40 °C < T < 125 °C		2		μV/°C
		125 °C < T < 150 °C		20		
I_{io}	Input offset current	$V_{out} = V_{CC}/2$, T = 25 °C		1	10 [(1)]	pA
		$V_{out} = V_{CC}/2$, $T_{min} < T < T_{max}$			5	nA
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$, T = 25 °C		1	10 [(1)]	pA
		$V_{out} = V_{CC}/2$, $T_{min} < T < T_{max}$			5	nA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 3.3 V, V_{out} = 1.65 V, T = 25 °C	60	78		dB
		0 V to 3.3 V, V_{out} = 1.65 V, $T_{min} < T < T_{max}$	55			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 2.8 V, T = 25 °C	80	90		
		R_L = 10 kΩ, V_{out} = 0.5 V to 2.8 V, $T_{min} < T < T_{max}$	70			
V_{CC} - V_{OH}	High-level output voltage	R_L = 10 kΩ, T = 25 °C		15	40	mV
		R_L = 10 kΩ, $T_{min} < T < T_{max}$			60	
		R_L = 600 Ω, T = 25 °C		45	150	
		R_L = 600 Ω, $T_{min} < T < T_{max}$			250	
V_{OL}	Low-level output voltage	R_L = 10 kΩ, T = 25 °C		15	40	
		R_L = 10 kΩ, $T_{min} < T < T_{max}$			60	
		R_L = 600 Ω, T = 25 °C		45	150	
		R_L = 600 Ω, $T_{min} < T < T_{max}$			250	
I_{out}	I_{sink}	V_{out} = 3.3 V, T = 25 °C	18	32		mA
		V_{out} = 3.3 V, $T_{min} < T < T_{max}$	14			
	I_{source}	V_{out} = 0 V, T = 25 °C	18	35		
		V_{out} = 0 V, $T_{min} < T < T_{max}$	14			
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$, T = 25 °C		0.8	1.1	
		No load, $V_{out} = V_{CC}/2$, $T_{min} < T < T_{max}$			1.1	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T = 25 °C		8		MHz
		R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, $T_{min} < T < T_{max}$		4.2		
F_u	Unity gain frequency	R_L = 2 kΩ, C_L = 100 pF		7.2		
ϕm	Phase margin			45		Degrees
G_m	Gain margin			8		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_v = 1, T = 25 °C		4.5		V/μs
		R_L = 2 kΩ, C_L = 100 pF, A_v = 1, T_{min} < T < T_{max}		3.5		
e_n	Equivalent input noise voltage	f = 10 kHz		21		nV/√Hz
THD+e_n	Total harmonic distortion	G =1, f =1 kHz, R_L = 2 kΩ, Bw = 22 kHz, V_{icm} = (V_{CC} + 1)/2, V_{out} = 1.9 V_{pp}		0.0007		%

Notes:

(1)Guaranteed by design.

Table 5: Electrical characteristics at VCC+ = 5 V with VCC- = 0 V, Vicm = VCC/2, RL connected to VCC/2, full temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		0.1	4.5	mV
		$T_{min} < T < T_{max}$			7.5	
DV_{io}	Input offset voltage drift	-40 °C < T < 125 °C		2		μV/°C
		125 °C < T < 150 °C		20		
I_{io}	Input offset current	$V_{out} = V_{CC}/2$, T = 25 °C		1	10 (1)	pA
		$V_{out} = V_{CC}/2$, $T_{min} < T < T_{max}$			5	nA
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$, T = 25 °C		1	10 (1)	pA
		$V_{out} = V_{CC}/2$, $T_{min} < T < T_{max}$			5	nA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 5 V, V_{out} = 2.5 V, T = 25 °C	62	82		dB
		0 V to 5 V, V_{out} = 2.5 V, $T_{min} < T < T_{max}$	58			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 2.5 to 5 V, T = 25 °C	70	86		
		V_{CC} = 2.5 to 5 V, $T_{min} < T < T_{max}$	65			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 4.5 V, T = 25 °C	80	91		
		R_L = 10 kΩ, V_{out} = 0.5 V to 4.5 V, $T_{min} < T < T_{max}$	70			
V_{CC} - V_{OH}	High-level output voltage	R_L = 10 kΩ, T = 25 °C		15	40	mV
		R_L = 10 kΩ, $T_{min} < T < T_{max}$			60	
		R_L = 600 Ω, T = 25 °C		45	150	
		R_L = 600 Ω, $T_{min} < T < T_{max}$			250	
V_{OL}	Low-level output voltage	R_L = 10 kΩ, T = 25 °C		15	40	
		R_L = 10 kΩ, $T_{min} < T < T_{max}$			60	
		R_L = 600 Ω, T = 25 °C		45	150	
		R_L = 600 Ω, $T_{min} < T < T_{max}$			250	
I_{out}	I_{sink}	V_{out} = 5 V, T = 25 °C	18	32		mA
		V_{out} = 5 V, $T_{min} < T < T_{max}$	14			
	I_{source}	V_{out} = 0 V, T = 25 °C	18	35		
		V_{out} = 0 V, $T_{min} < T < T_{max}$	14			
I_{CC}	Supply current (per operator)	No load, V_{out} = 2.5 V, T = 25 °C		0.82	1.1	
		No load, V_{out} = 2.5 V, $T_{min} < T < T_{max}$			1.1	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T = 25 °C		8		MHz
		R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, $T_{min} < T < T_{max}$		4.5		
F_u	Unity gain frequency	R_L = 2 kΩ, C_L = 100 pF		7.5		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		45		Degrees
G_m	Gain margin			8		dB
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_v = 1, T = 25 °C		4.5		V/µs
		R_L = 2 kΩ, C_L = 100 pF, A_v = 1, $T_{min} < T < T_{max}$		3.5		
e_n	Equivalent input noise voltage	f = 1 kHz		27		nV/√Hz
		f = 10 kHz		21		
THD+e_n	Total harmonic distortion	G =1, f =1 kHz, R_L = 2 kΩ, Bw = 22 kHz, V_{icm} = (V_{CC} + 1)/2, V_{out} = 3.6 V_{pp}		0.0004		%

Notes:

(1)Guaranteed by design.

4 Electrical characteristic curves

Figure 2: Input offset voltage distribution at T = 25 °C

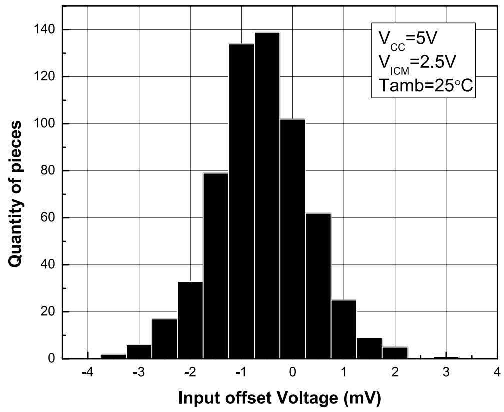


Figure 3: Input offset voltage distribution at T = 150 °C

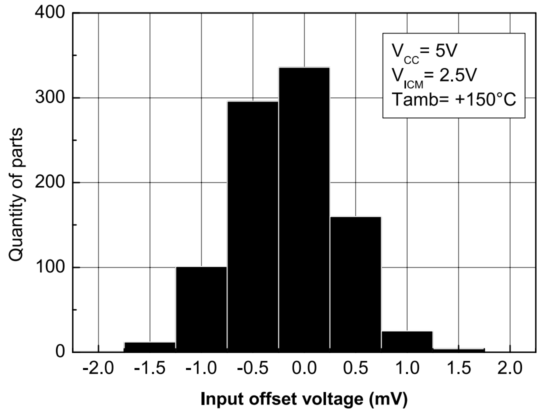


Figure 4: Supply current vs. input common-mode voltage at VCC = 2.5 V

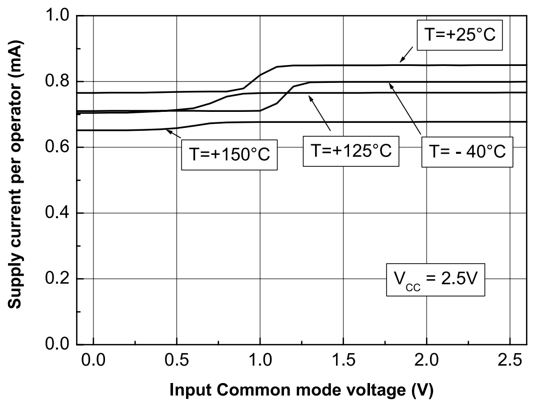


Figure 5: Supply current vs. input common-mode voltage at VCC = 5 V

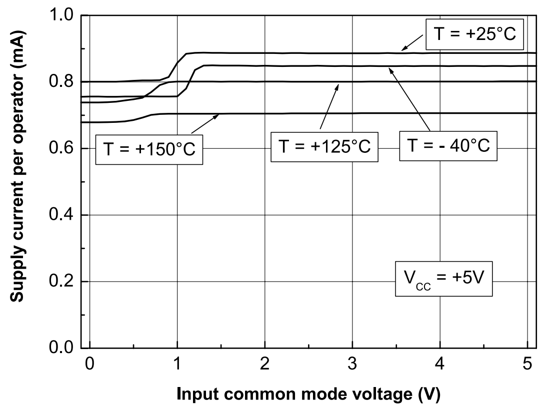


Figure 6: Output current vs. output voltage at VCC = 2.5 V

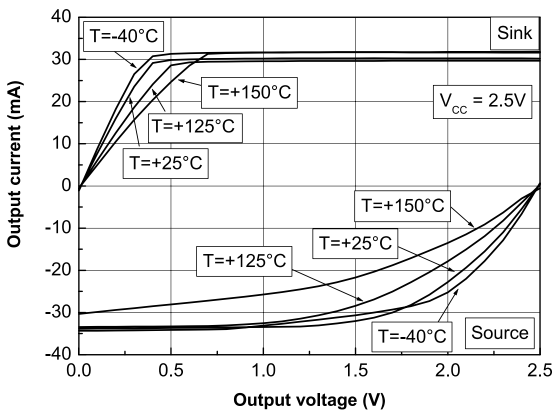


Figure 7: Output current vs. output voltage at VCC = 5 V

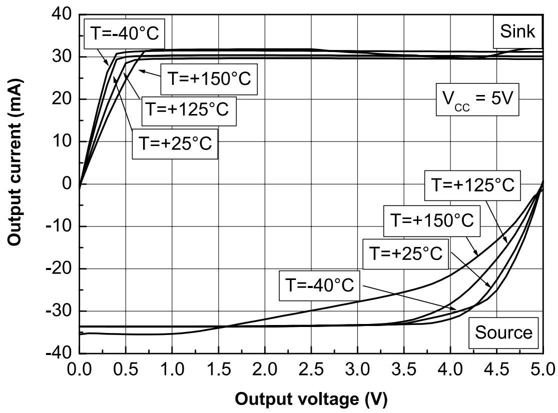


Figure 8: Voltage gain and phase vs frequency at VCC = 2.5 V and Vicm = 0.5 V

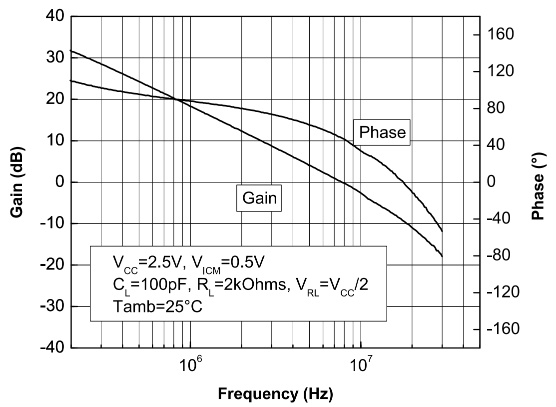


Figure 9: Voltage gain and phase vs frequency at VCC = 5.5 V and Vicm = 0.5 V

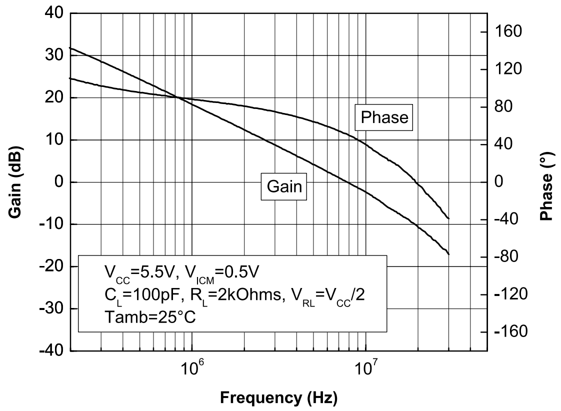


Figure 10: Phase margin vs. capacitive load

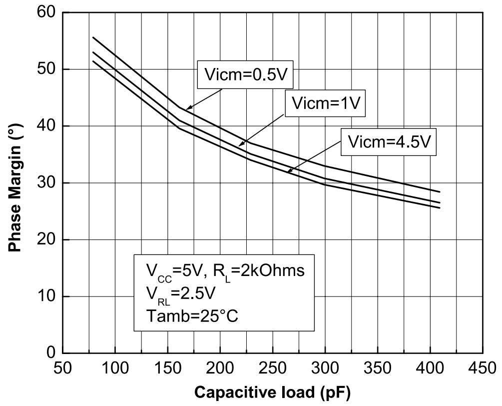


Figure 11: Phase margin vs. output current

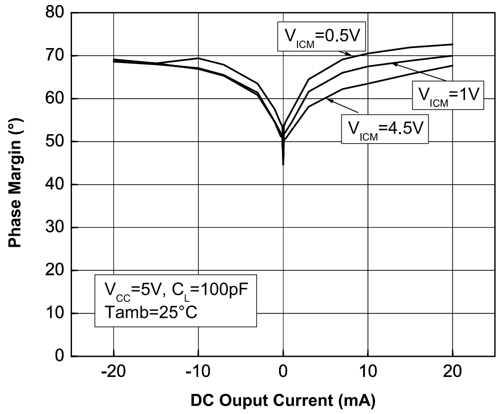


Figure 12: Positive slew rate

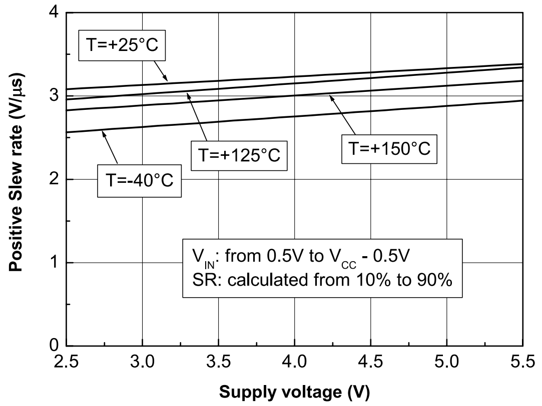


Figure 13: Negative slew rate

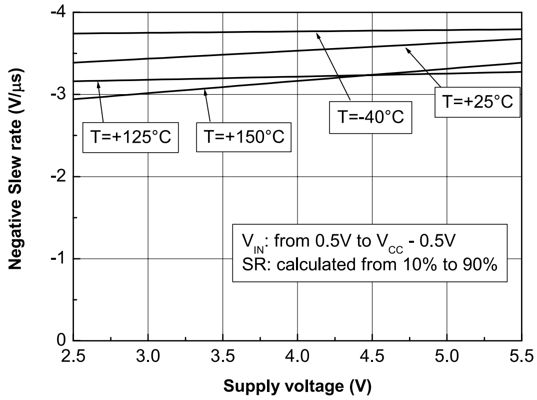


Figure 14: Distortion and noise vs. frequency

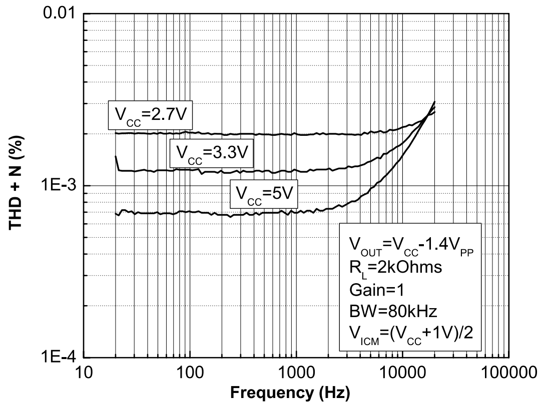


Figure 15: Distortion and noise vs. output voltage

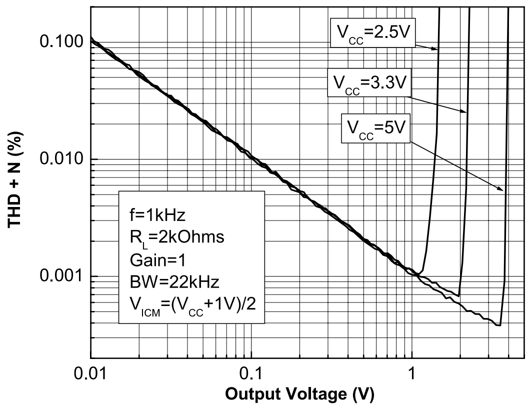


Figure 16: Noise vs. frequency

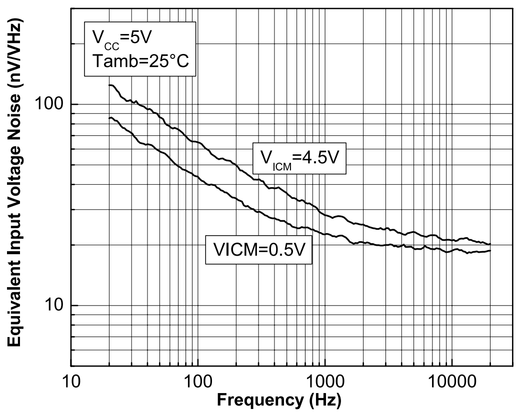


Figure 17: Phase margin vs. capacitive load and serial resistor

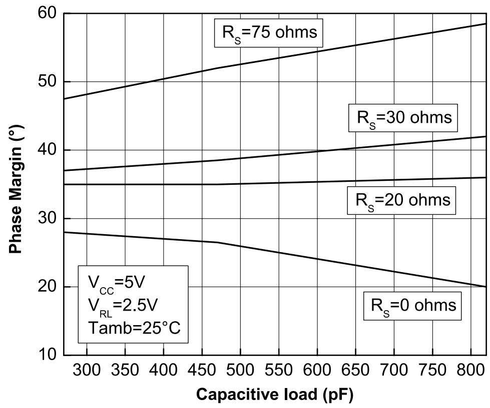
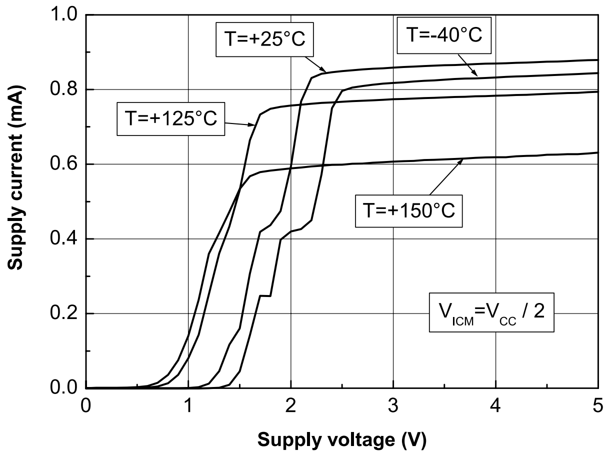


Figure 18: Supply current vs. supply voltage



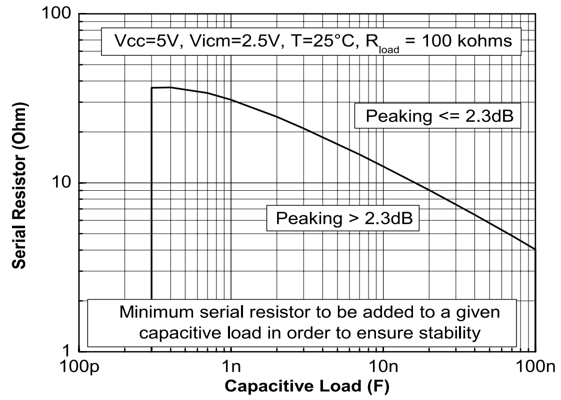
5 Application information

5.1 Driving resistive and capacitive loads

These products are low-voltage, low-power operational amplifiers optimized to drive rather large resistive loads above 2 kΩ.

In *follower* configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding a small in-series resistor at the output can improve the stability of the devices (see *Figure 19: "In-series resistor vs. capacitive load"* for recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on the bench and simulated with the simulation model.

Figure 19: In-series resistor vs. capacitive load



5.2 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 SO8 package information

Figure 20: SO8 package outline

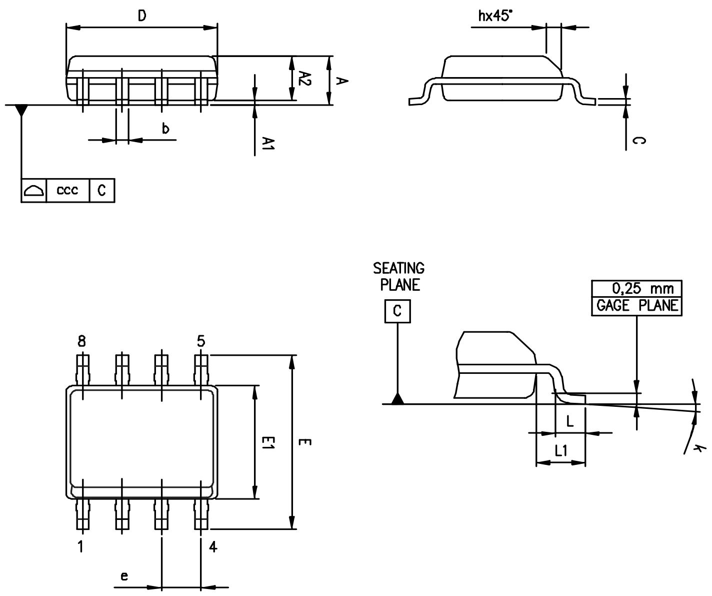


Table 6: SO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

7 Ordering information

Table 7: Order codes

Order code	Temperature range	Package	Packing	Marking
TSV912HYDT (1)	-40 °C to 150 °C	SO8 (2) (automotive grade level)	Tape and reel	V912HY

Notes:

(1)Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

(2)SO8 package is moisture sensitivity level 1 as per Jedec J-STD-020-C.

8 Revision history

Table 8: Document revision history

Date	Revision	Changes
08-Jul-2010	1	Initial release.
22-Feb-2016	2	Removed TSV912AH part number Updated layout *Table 3*, *Table 4*, and *Table 5*: removed all references to TSV912AH *Table 6*: updated min (mm) value for k parameter *Table 7: "Order codes"*: removed order code TSV912AHYDT