

IPAD™ EMI filter and line termination for USB upstream ports

Features

- Monolithic device with recommended line termination for USB upstream ports
- Integrated R_t series termination and C_t bypassing capacitors.
- Integrated ESD protection
- Small package size

Benefits

- EMI / RFI noise suppression
- Required line termination for USB upstream ports
- ESD protection exceeding IEC 61000-4-2 level 4
- High flexibility in the design of high density boards
- Tailored to meet USB 2.0 standard (low speed and full speed data transmission)

Complies with the following standards:

- IEC 61000-4-2 level4:
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883E-Method 3015-7:
 - Class 3, $C = 100$ pF, $R = 1500 \Omega$
 - 3 positive strikes, 3 negative strikes ($F = 1$ Hz)

Applications

EMI Filter and line termination for USB upstream ports on:

- USB Hubs
- PC peripherals

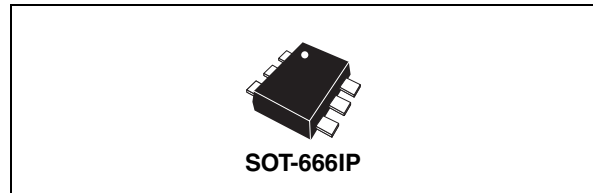
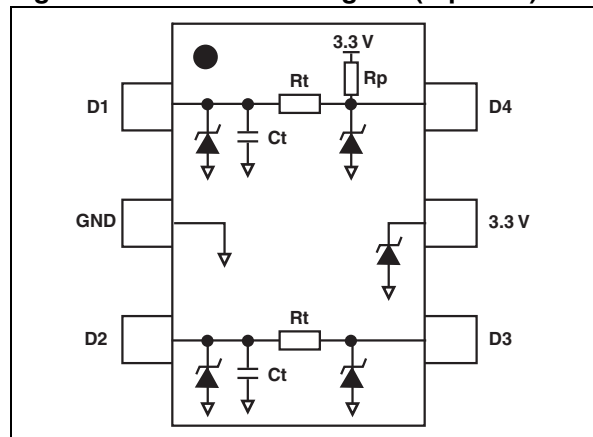


Figure 1. Functional diagram (top view)



Description

The USB specification requires upstream ports to be terminated with pull-up resistors from the D+ and D- lines to V_{bus} . For the implementation of USB systems, the radiated and conducted EMI should be kept within the required levels as stated by the FCC regulations. In addition to the requirements of termination and EMC compatibility, the computing devices are required to be tested for ESD susceptibility.

The USBUF01P6 provides the recommended line termination while implementing a low pass filter to limit EMI levels and providing ESD protection which exceeds IEC 61000-4-2 level 4 standard. The device is packaged in a SOT-666, which is the smallest available lead-frame package (45% smaller than the standard SOT323).

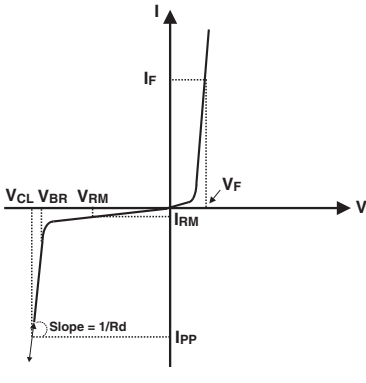
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1 Characteristics

Table 1. Absolute maximum rating ($T_{amb} = 25\text{ °C}$)

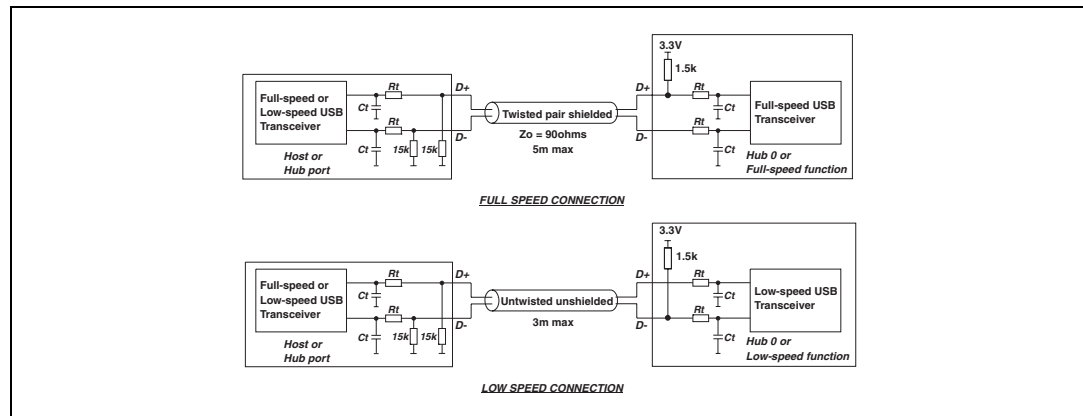
Symbol	Parameter		Value	Unit
V_{PP}	ESD discharge	IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge MIL STD 883E - Method 3015-7	± 16 ± 9 ± 25	kV
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s at 5 mm for case		260	°C
T_{op}	Operating temperature range		-40 to +85	°C

Table 2. Electrical characteristics ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter				
V_{RM}	Stand-off voltage				
V_{BR}	Breakdown voltage				
V_{CL}	Clamping voltage				
I_{RM}	Leakage current				
I_{PP}	Peak pulse current				
αT	Voltage temperature coefficient				
V_F	Forward voltage drop				
R_d	Dynamic resistance				
Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	6		10	V
I_{RM}	$V_{RM} = 3.3\text{ V per line}$			500	nA
R_t	Tolerance $\pm 10\%$		33		Ω
R_p	Tolerance $\pm 10\%$		1.5		k Ω
C_t	Tolerance $\pm 20\%$		47		pF

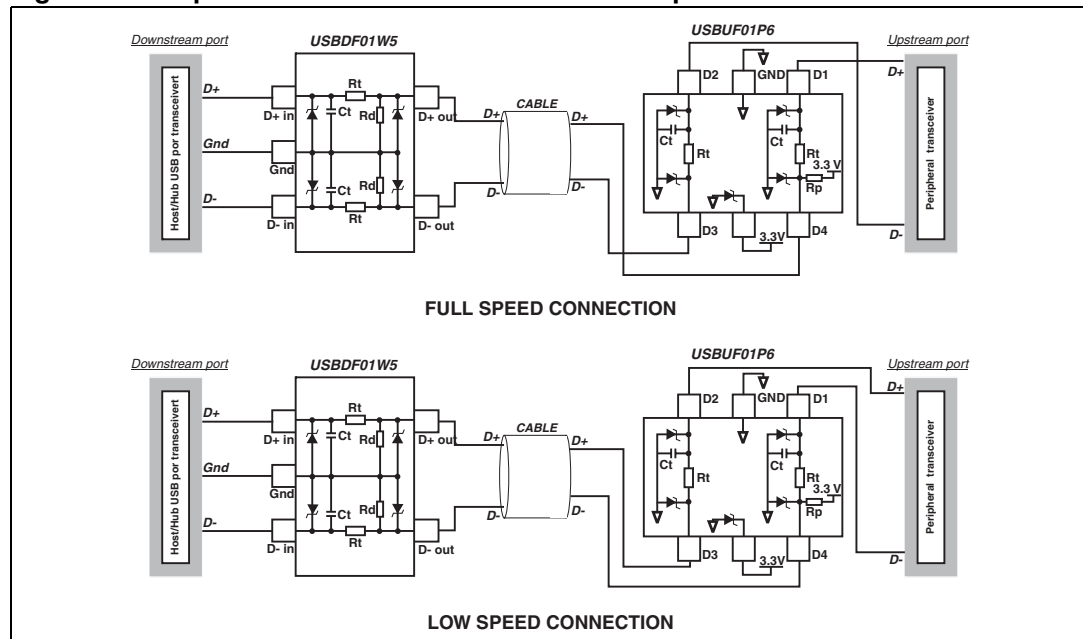
2 Technical information

Figure 2. USB standard requirements



2.1 Application example

Figure 3. Implementation of ST solutions for USB ports



2.1.1 EMI filtering

Current FCC regulations require that class B computing devices meet specified maximum levels for both radiated and conducted EMI.

- Radiated EMI covers the frequency range from 30 MHz to 1 GHz.
- Conducted EMI covers the 450 kHz to 30 MHz range.

For the types of device compliant with the USB standard, the most difficult test to pass is usually the radiated EMI test. For this reason the USBUF01P6 device aims to minimize radiated EMI.

The differential signal (D+ and D-) of USB devices does not contribute significantly to radiated or conducted EMI because the magnetic field of each conductor cancels out the other.

The inside of a PC product is very noisy and designers must minimize noise coupling from the different sources. D+ and D- must not be routed near high speed lines (clock spikes).

Induced common mode noise can be minimized by running pairs of USB signals parallel to each other and running grounded guard trace on each side of the signal pair from the USB controller to the USBUF device.

If possible, locate the USBUF device physically near the USB connectors. Distance between the USB controller and the USB connector must be minimized.

The 47 pF (C_t) capacitors are used to divert high frequency energy to ground and for edge control, and are placed between the driver chip and the series termination resistors (R_t). Both C_t and R_t should be placed as close to the driver chip as is practicable.

The USBUF01P6 ensures a filtering protection against electro-magnetic and radio frequency Interference thanks to its low-pass filter structure. This filter is characterized by the following parameters:

- Cut-off frequency
- Insertion loss
- High frequency rejection.

Figure 4. USBUF01P6 typical attenuation curve

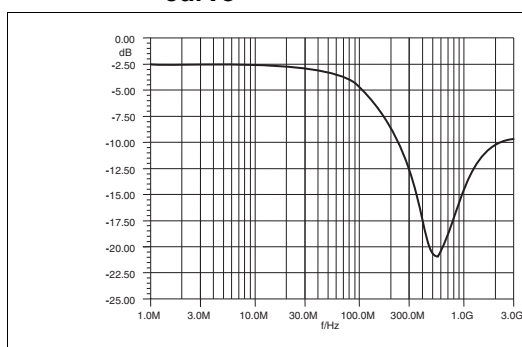
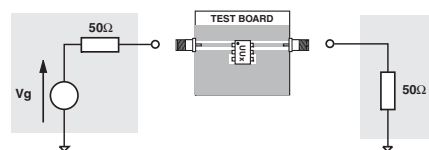


Figure 5. Measurement configuration



2.1.2 ESD protection

In addition to the requirements of termination and EMC compatibility, computing devices are required to be tested for ESD susceptibility. This test is described in IEC 61000-4-2 and is already in place in Europe. This test requires that a device tolerates ESD events and remains operational without user intervention.

The USB0F01P6 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at:

$$V_{CL} = V_{BR} + R_d \cdot I_{PP}$$

This protection function is split into 2 stages. As shown in [Figure 6](#). The ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R_t . Such a configuration makes the output voltage very low.

Figure 6. USB0F01P6 ESD clamping behavior

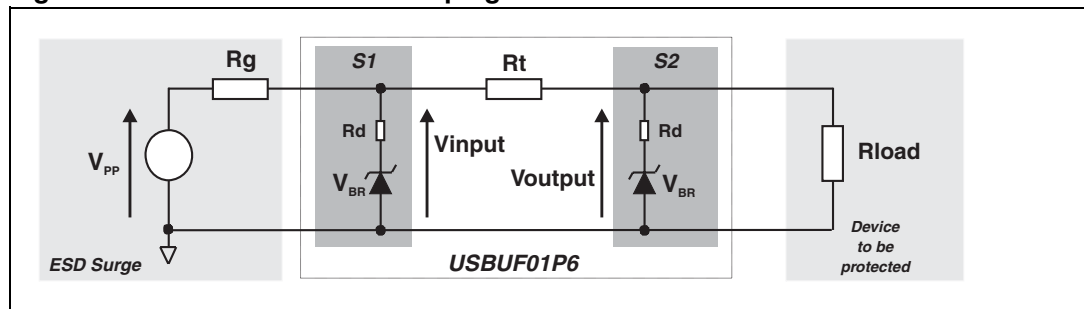
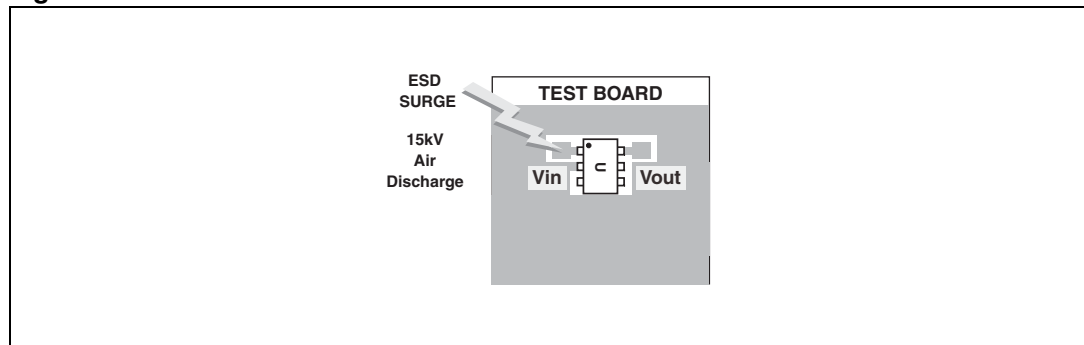


Figure 7. Measurement board



To have a good approximation of the remaining voltages at both V_{input} and V_{output} stages, we give the typical dynamical resistance value R_d . Taking into account the following hypothesis: $R_t > R_d$, $R_g > R_d$ and $R_{load} > R_d$, gives these formulas:

$$V_{input} = \frac{R_g \cdot V_{BR} + R_d \cdot V_g}{R_g}$$

$$V_{output} = \frac{R_t \cdot V_{BR} + R_d \cdot V_{input}}{R_t}$$

The calculation done for $V_g = 8 \text{ kV}$, $R_g = 330 \Omega$ (IEC 61000-4-2 standard), $V_{BR} = 7 \text{ V}$ (typ.) and $R_d = 2 \Omega$ (typ.) gives:

$$V_{input} = 55.48 \text{ V}$$

$$V_{output} = 10.36 \text{ V}$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be a few tenths of volts during a few ns at the V_{input} side. This parasitic effect is not present at the V_{output} side due the low current involved after the resistance R_t .

The measurements done hereafter show very clearly ([Figure 8](#) and [Figure 9](#)) the high efficiency of the ESD protection:

- No influence of the parasitic inductances on V_{output} stage
- V_{output} clamping voltage very close to V_{BR} (breakdown voltage) in the positive way and $-V_F$ (forward voltage) in the negative way

Figure 8. Remaining voltage at both stages S1 (V_{input}) and S2 (V_{output}) during positive ESD surge

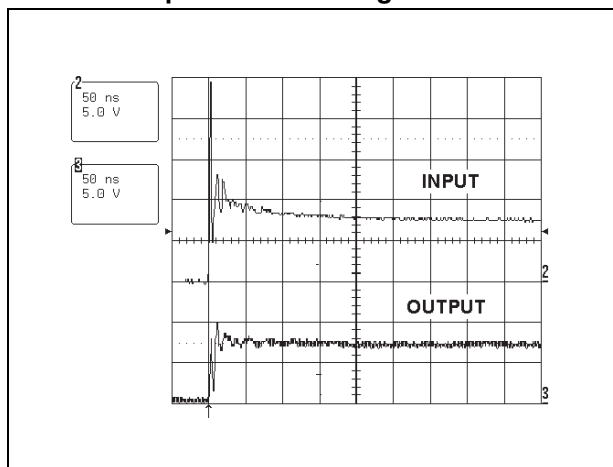
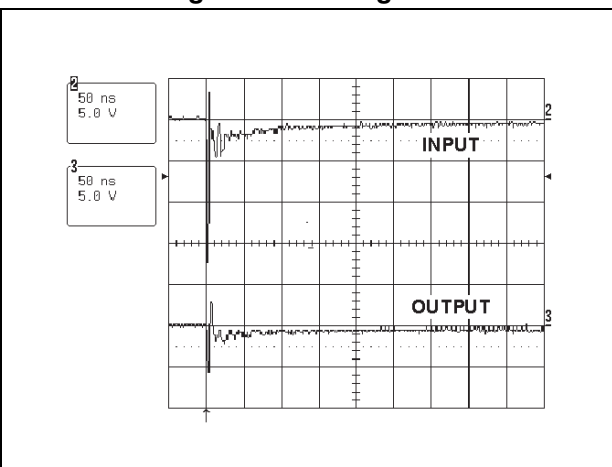


Figure 9. Remaining voltage at both stages S1 (V_{input}) and S2 (V_{output}) during negative ESD surge



Note: The USBUF01P6 acts not only for positive ESD surges but also for negative ones. For these kinds of disturbances it clamps close to ground voltage as shown in [Figure 9](#).

3 Package information

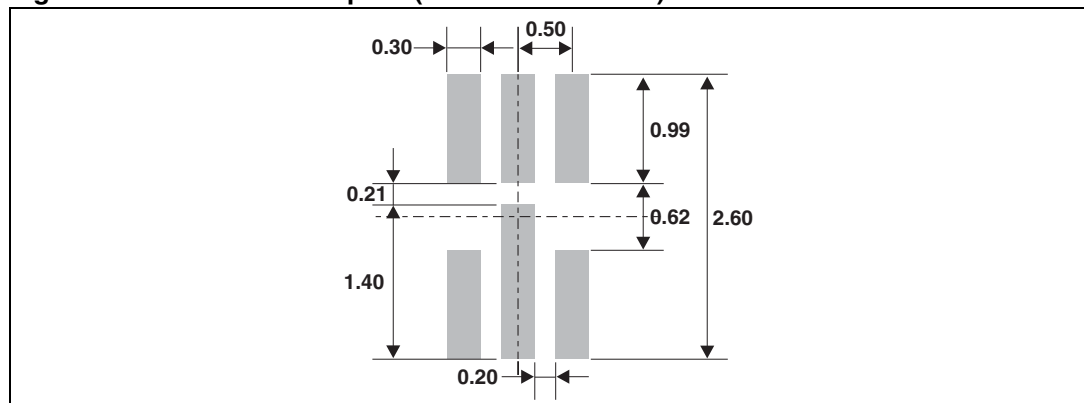
- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. SOT-666IP dimensions

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.53	0.57	0.60	0.021	0.22	0.024
A3	0.13	0.17	0.18	0.005	0.007	0.007
b	0.17		0.25	0.007		0.009
b1		0.27	0.34		0.011	0.013
D	1.50	1.66	1.70	0.059	0.065	0.067
E	1.50	1.65	1.70	0.059	0.065	0.067
E1	1.10	1.20	1.30	0.043	0.047	0.051
e		0.50			0.020	
L1	0.11	0.19	0.26	0.004	0.007	0.010
L2	0.10	0.23	0.30	0.004	0.009	0.012
L3	0.05	0.10		0.002	0.004	
L4		0.83			0.033	
angle°	8	10	12	8	10	12

Figure 10. SOT-666IP footprint (dimensions in mm)



3.1 Mechanical specifications

Lead plating	Mat tin
Lead plating thickness	7 µm min, 20 µm max
Lead coplanarity	10 µm max
Body material	Molded epoxy
Flammability	UL94, V0

4 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBUF01P6	U	SOT-666IP	2.9 mg	3000	Tape and reel

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
September-2003	1	First issue.
01-Jun-2004	2	SOT-666 Internal Pad version package change.
08-Jun-2005	3	Minor format changes; no content changed.
10-Mar-2006	4	Footprint and dimension graphic improved in packaging information. Ecopack statement added. Reformatted to current standard.
16-Aug-2006	5	Updated SOT-666IP package dimensions in Table 3.
29-Aug-2006	6	Typing error in table 2 on page 2: change W and kW unit to Ω and kΩ unit.
18-Feb-2010	7	Updated GND pin annotation in Figures 1 and 3. Added pin numbering indication to illustration and updated dimension values in Table 3. Updated mechanical specifications in Section 3.1.

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