

**Programmable Voltage Controlled Oscillator (VCXO)**

OUTPUT: LV-PECL

**VG7050ECN****NEW**

- Frequency range : 50 MHz to 800 MHz  
(Tuning resolution:  $2.2 \sim 2.8 \times 10^{-9}$ )
- Supply voltage : 2.5 V / 3.3 V
- External dimensions :  $7.0 \times 5.0 \times 1.5$  mm (10 pins)
- Absolute Pull Range :  $\pm 0$  to  $\pm 180 \times 10^{-6}$  (12 steps selectable)

**Features**

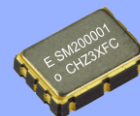
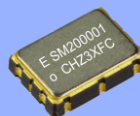
- User-specified four startup frequency, APR and 7-bit I<sup>2</sup>C address
- User Programming : I<sup>2</sup>C Interface
- Low jitter PLL technology

**Applications**

SONET/SDH, OTN, GbE, Fibre Channel



Product Number (please contact us)  
X1G004561xxxx00



Actual size

**Specifications (characteristics)**

| Item                         | Symbol                         | Specifications                                | Conditions / Remarks                                           |
|------------------------------|--------------------------------|-----------------------------------------------|----------------------------------------------------------------|
| Output frequency range       | f <sub>o</sub>                 | 50 MHz to 800 MHz                             | It can be changed by I <sup>2</sup> C                          |
| Supply voltage               | V <sub>CC</sub>                | D: 2.5 V $\pm$ 0.125 V, C: 3.3 V $\pm$ 0.33 V |                                                                |
| Storage temperature          | T <sub>stg</sub>               | -55 °C to +125 °C                             | Storage as single product                                      |
| Operating temperature        | T <sub>use</sub>               | -40 °C to +85 °C                              |                                                                |
| Frequency tolerance *1       | f <sub>tol</sub>               | $\pm 50 \times 10^{-6}$ Max.                  | Includes frequency aging (10 years)                            |
| Current consumption          | I <sub>CC</sub>                | 90 mA Max.                                    | OE Active, L <sub>ECL</sub> =50 $\Omega$                       |
| Disable current              | I <sub>dis</sub>               | 40 mA Max.                                    | OE Inactive, Output Standby: Hi-Z mode                         |
|                              |                                | 70 mA Max.                                    | OE Inactive, Output Standby: Fix mode                          |
|                              |                                |                                               |                                                                |
| Absolute pull range          | APR                            | $\pm 0$ to $\pm 180 \times 10^{-6}$           | V <sub>c</sub> = 1.65 V $\pm$ 1.35 V (V <sub>CC</sub> = 3.3 V) |
|                              |                                | $\pm 0$ to $\pm 180 \times 10^{-6}$           | V <sub>c</sub> = 1.25 V $\pm$ 1.00 V (V <sub>CC</sub> = 2.5 V) |
| Control voltage tuning range | V <sub>c</sub>                 | 0 to V <sub>CC</sub>                          |                                                                |
| Frequency change polarity    | -                              | Positive slope                                | 0 to V <sub>CC</sub>                                           |
| Symmetry                     | SYM                            | 45 % to 55 %                                  | At outputs crossing point                                      |
| Output voltage               | V <sub>OH</sub>                | V <sub>CC</sub> -1.025 V Min.                 | DC characteristics                                             |
|                              | V <sub>OL</sub>                | V <sub>CC</sub> -1.62 V Max.                  |                                                                |
| Output load condition        | L <sub>ECL</sub>               | 50 $\Omega$                                   | Termination to V <sub>CC</sub> - 2.0 V                         |
| Input voltage                | V <sub>IH</sub>                | 70% V <sub>CC</sub> Min.                      | OE, FSEL0, FSEL1, SDA and SCL                                  |
|                              | V <sub>IL</sub>                | 30% V <sub>CC</sub> Max.                      |                                                                |
| Rise time / Fall time        | t <sub>r</sub> /t <sub>f</sub> | 400 ps Max.                                   | Between 20% and 80% of (V <sub>OH</sub> -V <sub>OL</sub> )     |
| Start-up time                | t <sub>str</sub>               | 10 ms Max.                                    | Time at minimum supply voltage to be 0 s                       |

\*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift and 10 years aging at +25 °C.

Product name  
(Standard form)

VG7050 ECN SM20xxxx C J G H P Z  
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

①Model

②Output (E: LV-PECL)

③Parameter Designator (VG7050ECN: SM20xxxx)

④Supply voltage (C: 3.3 V Typ., D: 2.5 V Typ.)

⑤Frequency tolerance (J:  $\pm 50 \times 10^{-6}$ )

⑥Operating temperature (G: -40 ~ +85°C)

⑦OE Function (H: Active High, L: Active Low)

⑧Absolute Pull Range (P: Programmable)

⑨Output Standby Type (F: Fix (OUT="L", OUTN="H"), Z: High-Z)

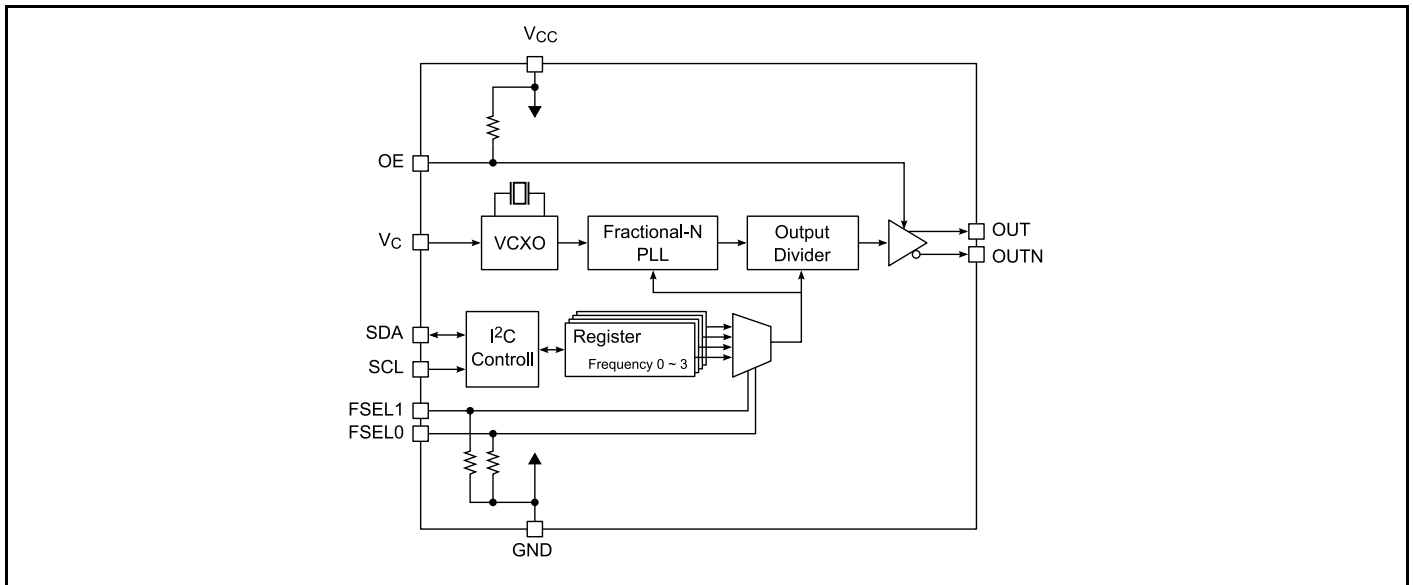
**Phase Jitter**

|                        | Offset Frequency | 125.00 MHz | 156.25 MHz | 250.00 MHz | 425.00 MHz | 622.08 MHz | 669.33 MHz | 794.73 MHz |
|------------------------|------------------|------------|------------|------------|------------|------------|------------|------------|
| Phase jitter*2<br>Typ. | 12 kHz to 20 MHz | 0.30 ps    | 0.26 ps    | 0.26 ps    | 0.25 ps    | 0.26 ps    | 0.26 ps    | 0.26 ps    |
|                        | 20 kHz to 50 MHz | 0.30 ps    | 0.27 ps    | 0.27 ps    | 0.26 ps    | 0.27 ps    | 0.27 ps    | 0.27 ps    |
|                        | 50 kHz to 80 MHz | 0.29 ps    | 0.27 ps    | 0.27 ps    | 0.26 ps    | 0.27 ps    | 0.27 ps    | 0.27 ps    |

\*2 In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1  $\mu$ F + 10  $\mu$ F) between V<sub>CC</sub> and GND pin should be placed as close to the V<sub>CC</sub> pin as possible.



## Block diagram

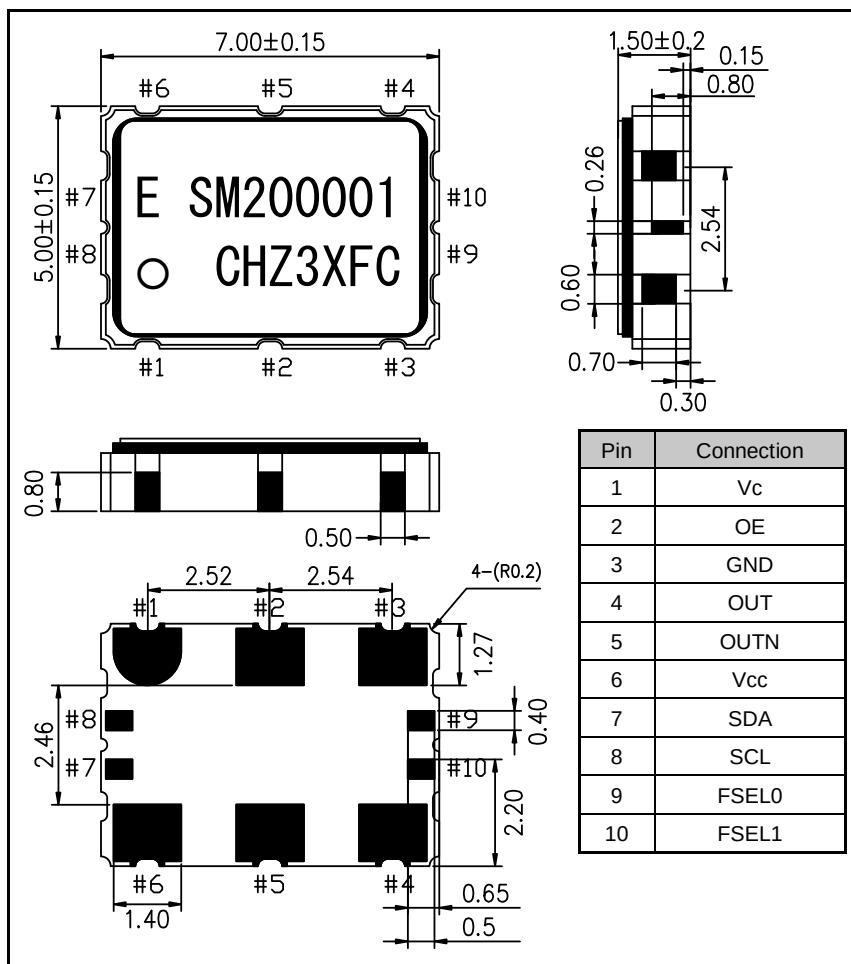


## OE Function / OE Standby Type

| OE Function    | OE Standby Type | Frequency output<br>OE pin | Oscillator Stop |                   |
|----------------|-----------------|----------------------------|-----------------|-------------------|
|                |                 |                            | OE pin          | OUT,OUTN state    |
| H: Active High | Z: High-Z       | "H" or "OPEN"              | "L"             | High Impedance    |
| L: Active Low  |                 | "L" or "OPEN"              | "H"             |                   |
| H: Active High | F: Fix          | "H" or "OPEN"              | "L"             | OUT="L", OUTN="H" |
| L: Active Low  |                 | "L" or "OPEN"              | "H"             |                   |

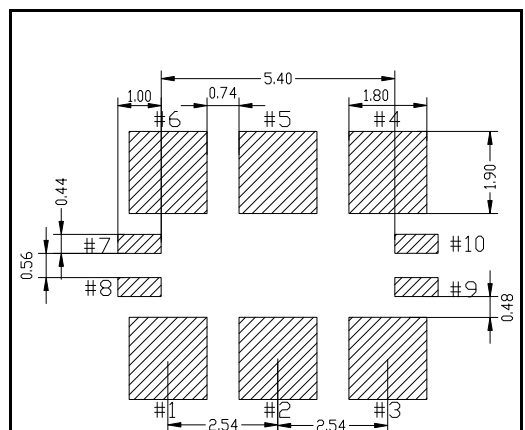
## External dimensions

(Unit: mm)



## Footprint (Recommended)

(Unit: mm)



In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1  $\mu$ F + 10  $\mu$ F) between VCC and GND pin should be placed as close to the VCC pin as possible.

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