

Off-line high voltage converters

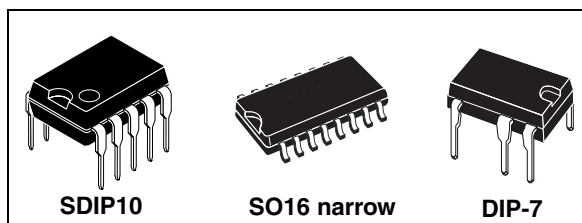
Datasheet — production data

Features

- 800 V avalanche rugged power section
- PWM operation with adjustable limiting current
- 30 mW stand-by power at 265 Vac
- Operating frequency:
 - 60 kHz for L type
 - 115 kHz for H type
- Frequency jittering for low EMC
- Output overvoltage protection
- High primary current protection (2nd OCP)
- Extra power timer for peak current management
- On-board soft-start
- Safe auto-restart after a fault condition
- Hysteretic thermal shutdown

Application

- Auxiliary power supply for consumer and home equipment
- ATX auxiliary power supply
- Low / medium power AC-DC adapters
- SMPS for set-top boxes, DVD players and recorders, white goods



Description

The device is an off-line converter with an 800 V rugged power section, a PWM control, two levels of over-current protection, over-voltage and overload protections, hysteretic thermal protection, soft-start and safe auto-restart after any fault condition removal. Burst mode operation and device very low consumption help to meet the standby energy saving regulations. Advance frequency jittering reduces EMI filter cost. The extra power timer allows the management of output peak power for a designed time window.

The high voltage start-up circuit is embedded in the device.

Figure 1. Typical application

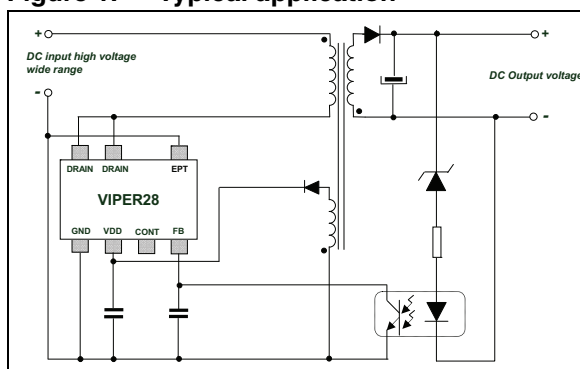


Table 1. Device summary

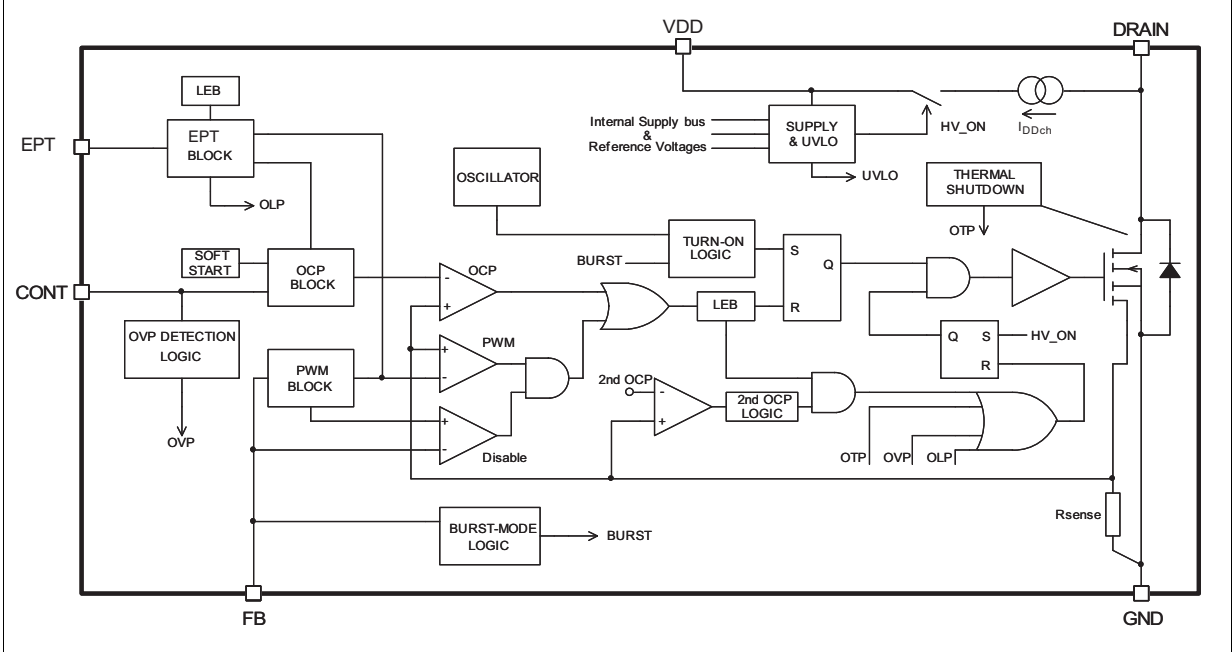
Order codes	Package	Packaging
VIPER28LN / VIPER28HN	DIP-7	Tube
VIPER28LE / VIPER28HE	SDIP10	
VIPER28HD / VIPER28LD	SO16 narrow	Tape and reel
VIPER28HDTR / VIPER28LDTR		

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1 **Block diagram**

Figure 2. **Block diagram**



2 **Typical power**

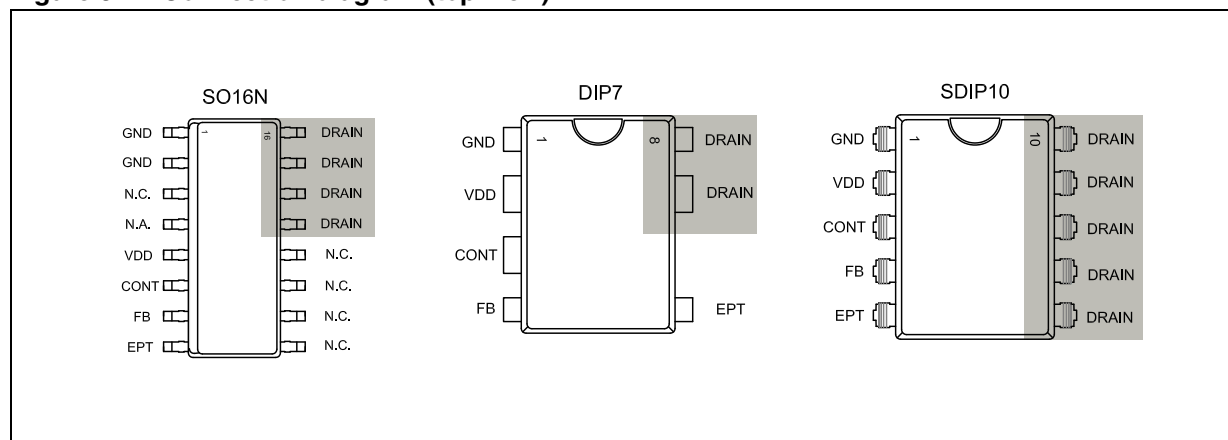
Table 2. **Typical power**

Part number	230 V _{AC}		85-265 V _{AC}	
	Adapter ⁽¹⁾	Open frame ⁽²⁾	Adapter ⁽¹⁾	Open frame ⁽²⁾
VIPER28	18 W	20 W	10 W	12 W

- 1. Typical continuous power in non ventilated enclosed adapter measured at 50 °C ambient.
- 2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.

3 Pin settings

Figure 3. Connection diagram (top view)



Note: The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 3. Pin description

Pin n.			Name	Function
SDIP10	DIP-7	SO16N		
1	1	1...2	GND	This pin represents the device ground and the source of the power section.
-	-	4	N.A.	Function: Not available for user. It can be connected to GND (pins 1-2) or left not connected.
2	2	5	VDD	Supply voltage of the control section. This pin also provides the charging current of the external capacitor during start-up time.
3	3	6	CONT	Control pin. The following functions can be selected: 1. current limit set point adjustment. The internal set default value of the cycle-by-cycle current limit can be reduced by connecting to ground an external resistor. 2. output voltage monitoring. A voltage exceeding V_{OVP} threshold (see Table 8 on page 7) shuts the IC down reducing the device consumption. This function is strobed and digitally filtered for high noise immunity.
4	4	7	FB	Control input for duty cycle control. Internal current generator provides bias current for loop regulation. A voltage below the threshold V_{FBbm} activates the burst-mode operation. A level close to the threshold V_{FBlin} means that we are approaching the cycle-by-cycle over-current set point.
5	5	8	EPT	This pin allows the connection of an external capacitor for the extra power management. If the function is not used, the pin has to be connected to GND.
6...10	7,8	13...16	DRAIN	High voltage drain pin. The built-in high voltage switched start-up bias current is drawn from this pin too. Pins connected to the metal frame to facilitate heat dissipation.

4 Electrical data

4.1 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
V_{DRAIN}	Drain-to-source (ground) voltage		800	V
E_{AV}	Repetitive avalanche energy (limited by $T_J = 150\text{ °C}$)		3.5	mJ
I_{AR}	Repetitive avalanche current (limited by $T_J = 150\text{ °C}$)		1	A
I_{DRAIN}	Pulse drain current (limited by $T_J = 150\text{ °C}$)		3	A
V_{CONT}	Control input pin voltage	-0.3	6	V
V_{FB}	Feed-back voltage	-0.3	5.5	V
V_{EPT}	EPT input pin voltage	-0.3	5	V
V_{DD}	Supply voltage ($I_{\text{DD}} = 25\text{ mA}$)	-0.3	Self limited	V
I_{DD}	Input current		25	mA
P_{TOT}	Power dissipation at $T_A < 40\text{ °C}$ (DIP-7)		1	W
	Power dissipation at $T_A < 60\text{ °C}$ (SO16N, SDIP-10)		1.5	
T_J	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature	-55	150	°C

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max value			Unit
		SO16N	DIP7	SDIP10	
R_{thJP}	Thermal resistance junction pin (Dissipated power = 1 W)	25	35	35	°C/W
R_{thJA}	Thermal resistance junction ambient (Dissipated power = 1 W)	60	100	80	°C/W
R_{thJA}	Thermal resistance junction ambient ⁽¹⁾ (Dissipated power = 1 W)	50	80	65	°C/W

1. When mounted on a standard single side FR4 board with 100 mm² (0.155 sq in) of Cu (35 µm thick)

4.3 Electrical characteristics

($T_J = -25$ to $125\text{ }^{\circ}\text{C}$, $V_{DD} = 14\text{ V}$ ^(a); unless otherwise specified)

Table 6. Power section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{BVDSS}	Break-down voltage	$I_{DRAIN} = 1\text{ mA}$, $V_{FB} = \text{GND}$, $T_J = 25\text{ }^{\circ}\text{C}$	800			V
I_{OFF}	OFF state drain current	$V_{DRAIN} = \text{max rating}$, $V_{FB} = \text{GND}$, $T_J = 25\text{ }^{\circ}\text{C}$			60	μA
$R_{DS(on)}$	Drain-source on state resistance	$I_{DRAIN} = 0.4\text{ A}$, $V_{FB} = 3\text{ V}$, $V_{EPT} = \text{GND}$, $T_J = 25\text{ }^{\circ}\text{C}$			7	Ω
		$I_{DRAIN} = 0.4\text{ A}$, $V_{FB} = 3\text{ V}$, $V_{EPT} = \text{GND}$, $T_J = 125\text{ }^{\circ}\text{C}$			14	Ω
C_{OSS}	Effective (energy related) output capacitance	$V_{DRAIN} = 0$ to 640 V , $T_J = 25\text{ }^{\circ}\text{C}$		40		pF

Table 7. Supply section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		60	80	100	V
I_{DDch}	Start up charging current	$V_{DRAIN} = 120\text{ V}$, $V_{EPT} = \text{GND}$, $V_{FB} = \text{GND}$, $V_{DD} = 4\text{ V}$	-2	-3	-4	mA
		$V_{DRAIN} = 120\text{ V}$, $V_{EPT} = \text{GND}$, $V_{FB} = \text{GND}$, $V_{DD} = 4\text{ V}$ after fault	-0.4	-0.6	-0.8	mA
V_{DD}	Operating voltage range	After turn-on	8.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	$I_{DD} = 20\text{ mA}$	23.5			V
V_{DDon}	V_{DD} start up threshold	$V_{DRAIN} = 120\text{ V}$, $V_{EPT} = \text{GND}$, $V_{FB} = \text{GND}$	13	14	15	V
V_{DDoff}	V_{DD} under voltage shutdown threshold		7.5	8	8.5	V
$V_{DD(RESTART)}$	V_{DD} restart voltage threshold	$V_{DRAIN} = 120\text{ V}$, $V_{EPT} = \text{GND}$, $V_{FB} = \text{GND}$	4	4.5	5	V
Current						
I_{DD0}	Operating supply current, not switching	$V_{FB} = \text{GND}$, $F_{SW} = 0\text{ kHz}$, $V_{EPT} = \text{GND}$, $V_{DD} = 10\text{ V}$			0.9	mA
I_{DD1}	Operating supply current, switching	$V_{DRAIN} = 120\text{ V}$, $F_{SW} = 60\text{ kHz}$			2.5	mA
		$V_{DRAIN} = 120\text{ V}$, $F_{SW} = 115\text{ kHz}$			3.5	mA
I_{DD_FAULT}	Operating supply current, with protection tripping	$V_{DD} = 10\text{ V}$			400	μA
I_{DD_OFF}	Operating supply current with $V_{DD} < V_{DD_OFF}$	$V_{DD} = 7\text{ V}$			270	μA

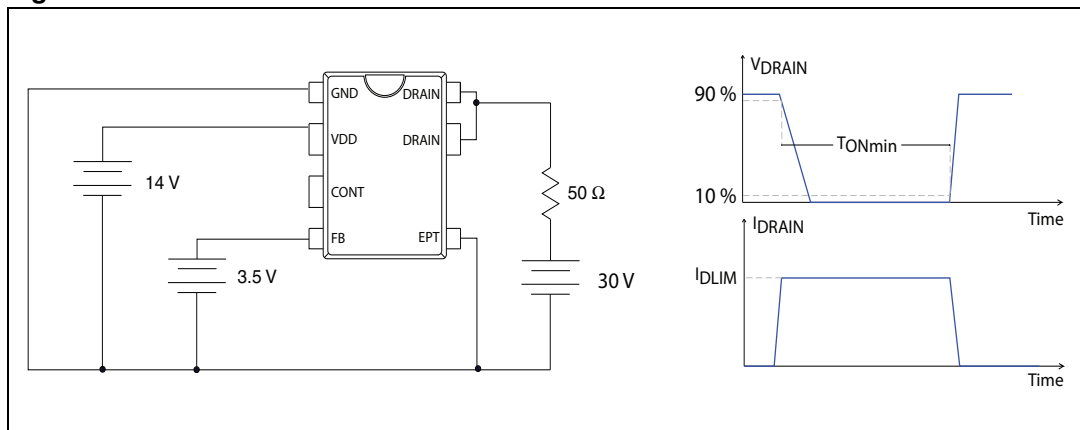
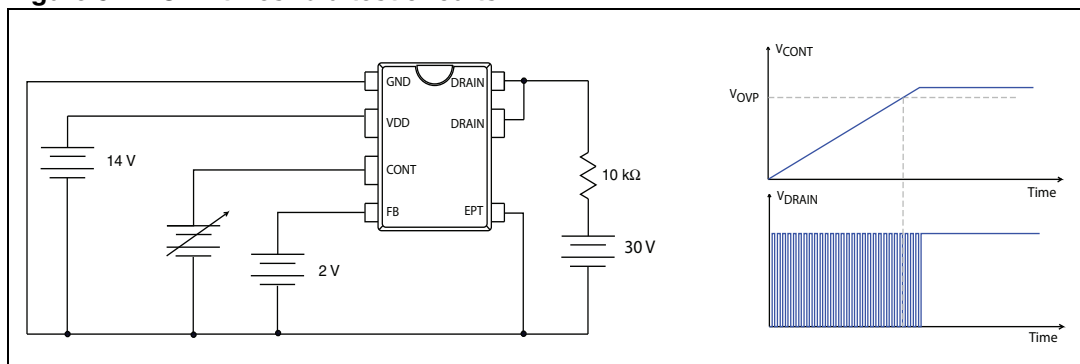
a. Adjust V_{DD} above V_{DDon} start-up threshold before setting to 14 V

Table 8. Controller section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Feed-back pin						
V_{FBolp}	Over-load shut down threshold		4.5	4.8	5.2	V
V_{FBlin}	Linear dynamics upper limit		3.2	3.5	3.7	V
V_{FBbm}	Burst mode threshold	Voltage falling		0.6		V
$V_{FBbmhys}$	Burst mode hysteresis	Voltage rising		100		mV
I_{FB}	Feed-back sourced current	$V_{FB} = 0.3 \text{ V}$	-150	-200	-280	uA
		$3.3 \text{ V} < V_{FB} < 4.8 \text{ V}$		-3		uA
$R_{FB(DYN)}$	Dynamic resistance	$V_{FB} < 3.3 \text{ V}$	14		20	k Ω
H_{FB}	$\Delta V_{FB} / \Delta I_D$		2		6	V/A
CONT pin						
V_{CONT_l}	Low level clamp voltage	$I_{CONT} = -100 \text{ }\mu\text{A}$		0.5		V
V_{CONT_h}	High level clamp voltage	$I_{CONT} = 1 \text{ mA}$	5	5.5	6	V
Current limitation						
I_{Dlim}	Max drain current limitation	$V_{FB} = 4 \text{ V}$, $I_{CONT} = -10 \text{ }\mu\text{A}$ $T_J = 25 \text{ }^\circ\text{C}$	0.75	0.80	0.85	A
t_{SS}	Soft-start time			8.5		ms
T_{ON_MIN}	Minimum turn ON time		220	400	480	ns
t_d	Propagation delay			100		ns
t_{LEB}	Leading edge blanking			300		ns
I_{D_BM}	Peak drain current during burst mode	$V_{FB} = 0.6 \text{ V}$		160		mA
Oscillator section						
F_{OSC}	VIPER28L	V_{DD} = operating voltage range, $V_{FB} = 1 \text{ V}$	54	60	66	kHz
	VIPER28H		103	115	127	kHz
FD	Modulation depth	VIPER28L		± 4		kHz
		VIPER28H		± 8		kHz
FM	Modulation frequency			250		Hz
D_{MAX}	Maximum duty cycle		70		80	%

Table 8. Controller section (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Over-current protection (2 nd OCP)						
I _{DMAX}	Second over-current threshold			1.2		A
Over-voltage protection						
V _{OVP}	Over-voltage protection threshold		2.7	3	3.3	V
T _{STROBE}	Over-voltage protection strobe time			2.2		us
Extra power management						
I _{DLIM_EPT}	Drain current limit with EPT function	I _{CONT} < -10 μA T _J = 25 °C		85% IDlim		A
V _{EPT(STOP)}	EPT shut down threshold	I _{CONT} < -10 μA		4		V
V _{EPT(RESTART)}	EPT restart threshold			0.6		V
I _{EPT}	Sourced EPT current			5		μA
Thermal shutdown						
T _{SD}	Thermal shutdown temperature		150	160		°C
T _{HYST}	Thermal shutdown hysteresis			30		°C

Figure 4. Minimum turn-on time test circuit**Figure 5. OVP threshold test circuits**

Note: Adjust V_{DD} above V_{DDon} start-up threshold before setting to 14 V

5 Typical electrical characteristics

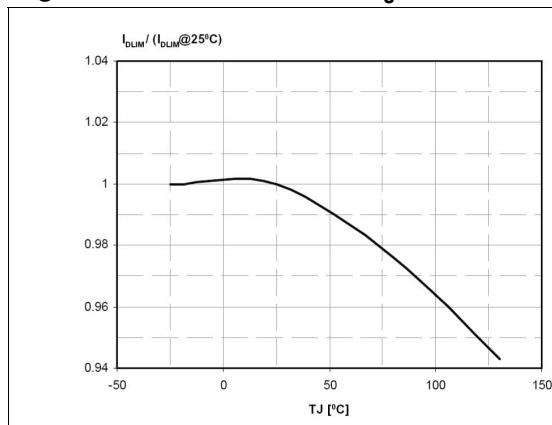
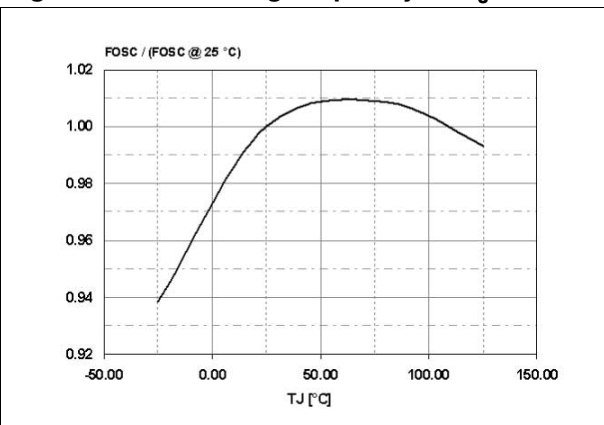
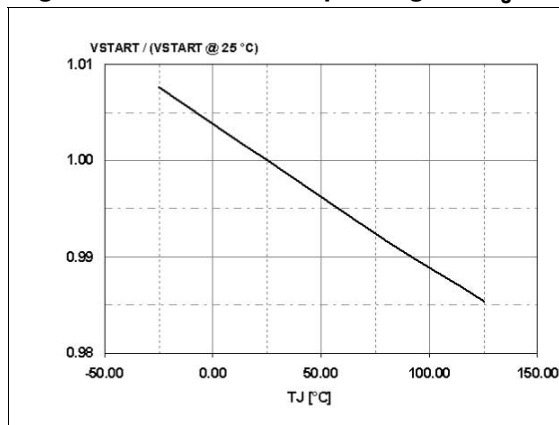
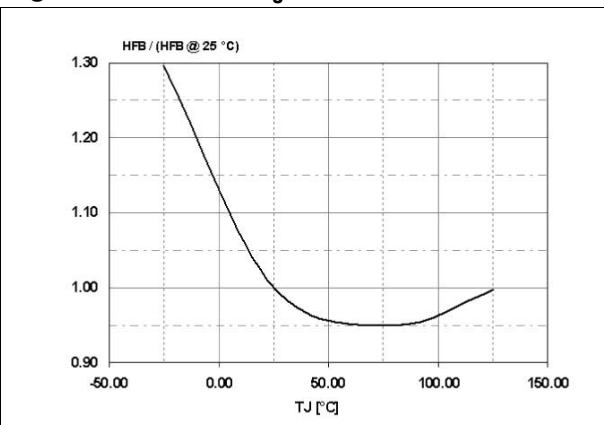
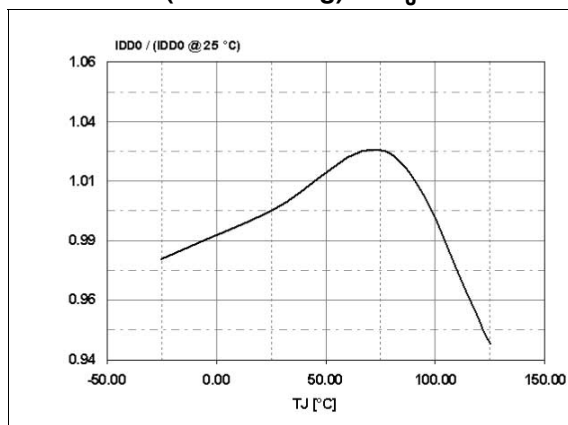
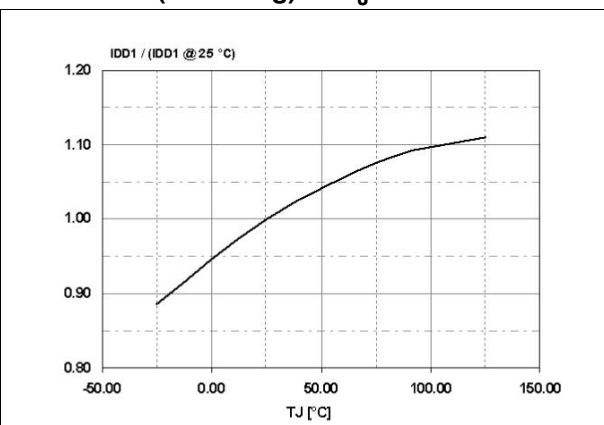
Figure 6. Current limit vs T_J Figure 7. Switching frequency vs T_J Figure 8. Drain start-up voltage vs T_J Figure 9. HFB vs T_J Figure 10. Operating supply current (no switching) vs T_J Figure 11. Operating supply current (switching) vs T_J 

Figure 12. Current limit vs R_{LIM}

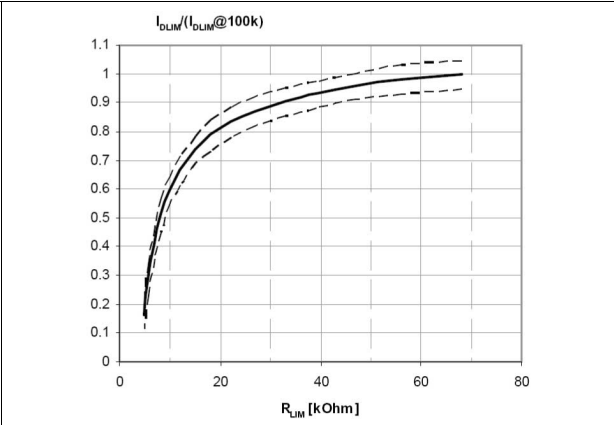


Figure 13. Power MOSFET on-resistance vs T_J

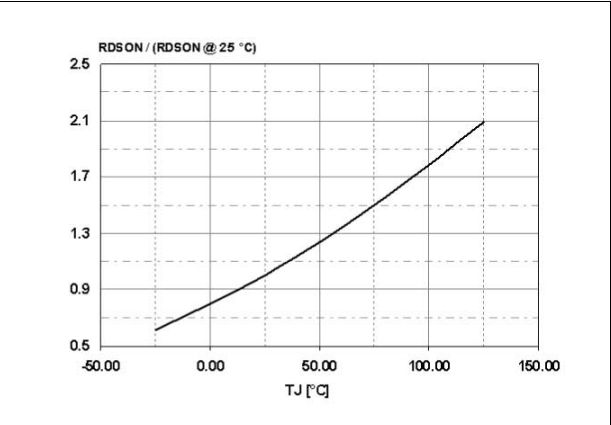


Figure 14. Power MOSFET break down voltage vs T_J

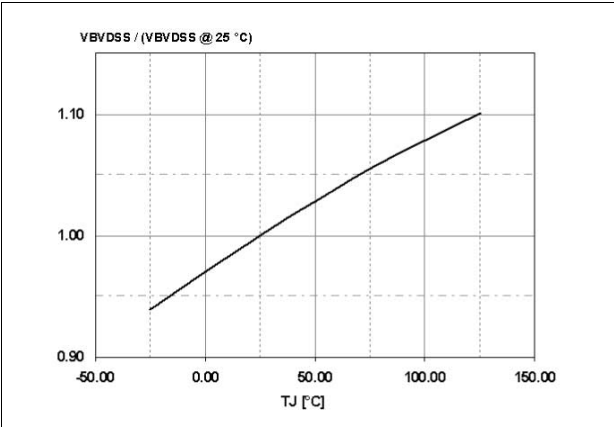
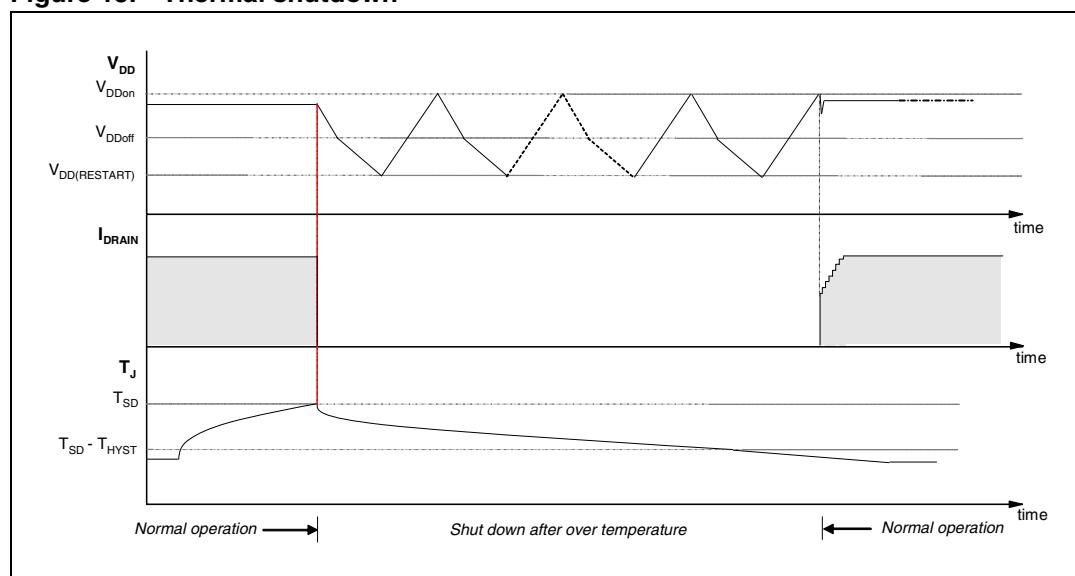


Figure 15. Thermal shutdown



7 Operation descriptions

The device is a high-performance low-voltage PWM controller chip with an 800 V, avalanche rugged Power section.

The controller includes: the oscillator with jittering feature, the start up circuits with soft-start feature, the PWM logic, the current limit circuit with adjustable set point, the second overcurrent circuit, the burst mode management, the brown-out circuit, the UVLO circuit, the auto-restart circuit and the thermal protection circuit.

The current limit set-point is set by the CONT pin. The burst mode operation guaranties high performance in the stand-by mode and helps in the energy saving norm accomplishment.

All the fault protections are built in auto restart mode with very low repetition rate to prevent IC's over heating.

7.1 Power section and gate driver

The power section is implemented with an avalanche ruggedness N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power section has a B_{VDSS} of 800 V min. and a typical $R_{DS(on)}$ of 7 Ω at 25 °C.

The integrated SenseFET structure allows a virtually loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power section cannot be turned on accidentally.

7.2 High voltage startup generator

The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than V_{DRAIN_START} threshold, 80 V_{DC} typically. When the HV current generator is ON, the I_{DDch} current (3 mA typical value) is delivered to the capacitor on the V_{DD} pin. In case of auto restart mode after a fault event, the I_{DDch} current is reduced to 0.6 mA, in order to have a slow duty cycle during the restart phase.

7.3 Power-up and soft-start up

If the input voltage rises up till the device start threshold, V_{DRAIN_START} , the V_{DD} voltage begins to grow due to the I_{DDch} current (see [Table 7 on page 6](#)) coming from the internal high voltage start up circuit. If the V_{DD} voltage reaches V_{DDon} threshold (see [Table 7 on page 6](#)) the power MOSFET starts switching and the HV current generator is turned OFF. See [Figure 18 on page 15](#).

The IC is powered by the energy stored in the capacitor on the VDD pin, C_{VDD} , until when the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation.

C_{VDD} capacitor must be sized enough to avoid fast discharge and keep the needed voltage value higher than V_{DDoff} threshold. In fact, a too low capacitance value could terminate the switching operation before the controller receives any energy from the auxiliary winding.

The following formula can be used for the V_{DD} capacitor calculation:

Equation 1

$$C_{VDD} = \frac{I_{DDch} \times t_{SSaux}}{V_{DDon} - V_{DDoff}}$$

The t_{SSaux} is the time needed for the steady state of the auxiliary voltage. This time is estimated by applicator according to the output stage configurations (transformer, output capacitances, etc.).

During the converter start up time, the drain current limitation is progressively increased to the maximum value. In this way the stress on the secondary diode is considerably reduced. It also helps to prevent transformer saturation. The soft-start time lasts 8.5 ms and the feature is implemented for every attempt of start up converter or after a fault.

Figure 18. I_{DD} current during start-up and burst mode

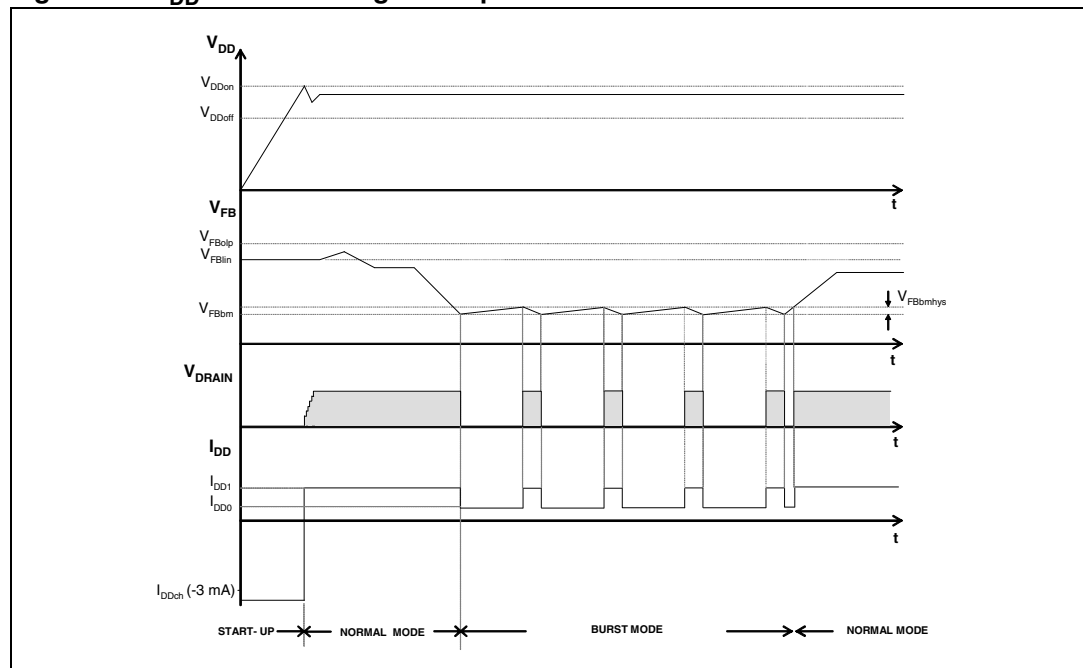


Figure 19. Timing diagram: normal power-up and power-down sequences

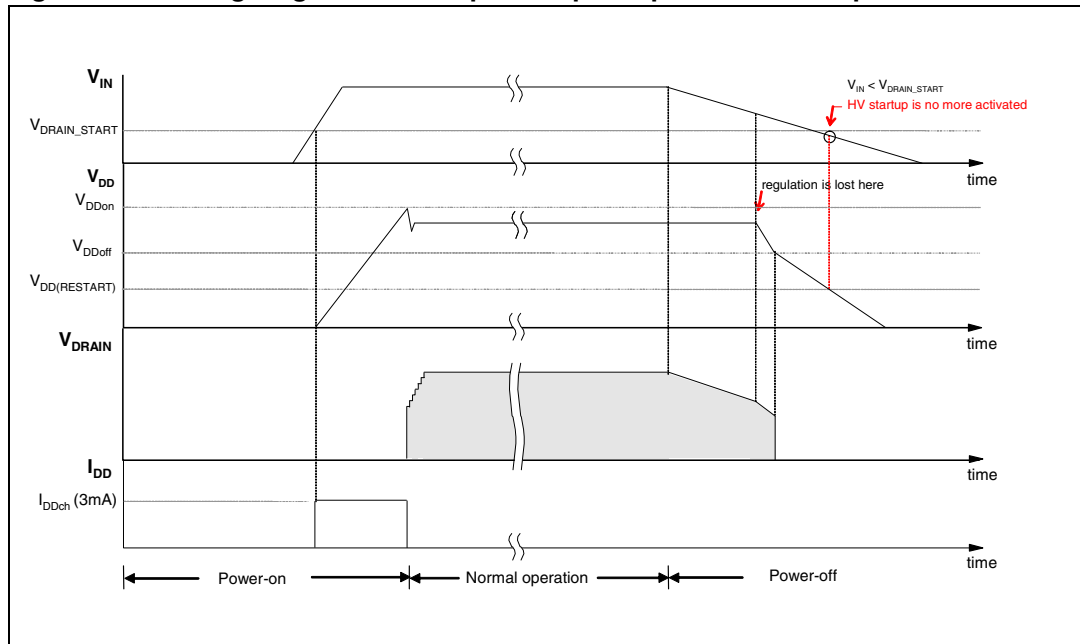
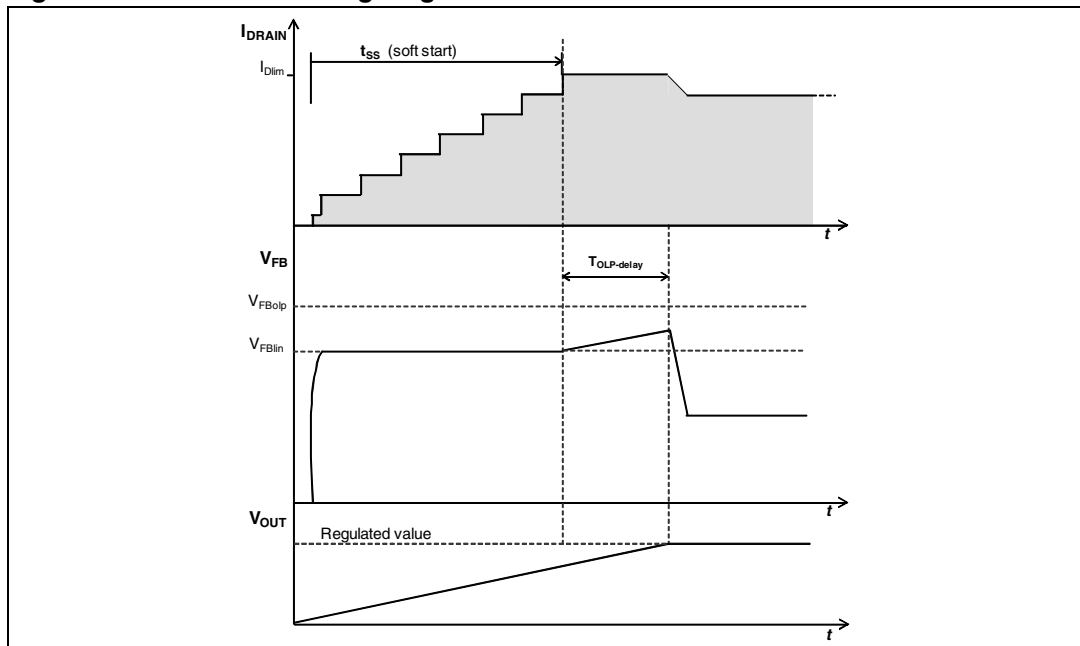


Figure 20. Soft-start: timing diagram



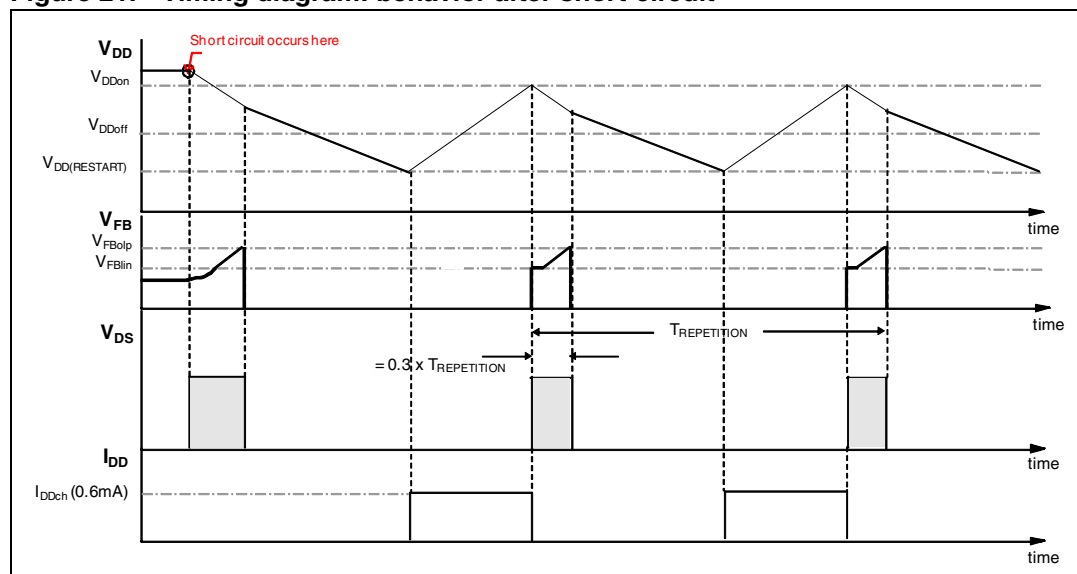
7.4 Power down operation

At converter power down, the system loses regulation as soon as the input voltage is so low that the peak current limitation is reached. The V_{DD} voltage drops and when it falls below the V_{DDoff} threshold (see [Table 7 on page 6](#)) the power MOSFET is switched OFF, the energy transfers to the IC interrupted and consequently the V_{DD} voltages decreases, [Figure 19 on page 16](#). Later, if the V_{IN} is lower than V_{DRAIN_START} (see [Table 7 on page 6](#)), the start up sequence is inhibited and the power down completed. This feature is useful to prevent converter's restart attempts and ensures monotonic output voltage decay during the system power down.

7.5 Auto restart operation

If after a converter power down, the V_{IN} is higher than V_{DRAIN_START} , the start up sequence is not inhibited and will be activated only when the V_{DD} voltage drops down the $V_{DD(RESTART)}$ threshold (see [Table 7 on page 6](#)). This means that the HV start up current generator restarts the V_{DD} capacitor charging only when the V_{DD} voltage drops below $V_{DD(RESTART)}$. The scenario above described is for instance a power down because of a fault condition. After a fault condition, the charging current, I_{DDch} , is 0.6 mA (typ.) instead of the 3 mA (typ.) of a normal start up converter phase. This feature together with the low $V_{DD(RESTART)}$ threshold ensures that, after a fault, the restart attempts of the IC has a very long repetition rate and the converter works safely with extremely low power throughput. The [Figure 21](#) shows the IC behavioral after a short-circuit event.

Figure 21. Timing diagram: behavior after short-circuit



7.6 Oscillator

The switching frequency is internally fixed to 60 kHz or 115 kHz. In both case the switching frequency is modulated by approximately ± 4 kHz (60 kHz version) or ± 8 kHz (115 kHz version) at 250 Hz (typical) rate, so that the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of side-band harmonics having the same energy on the whole but smaller amplitudes.

7.7 Current mode conversion with adjustable current limit set point

The device is a current mode converter: the drain current is sensed and converted in voltage that is applied to the non inverting pin of the PWM comparator. This voltage is compared with the one on the feed-back pin through a voltage divider on cycle by cycle basis.

The device has a default current limit value, I_{Dlim} , that the designer can adjust according the electrical specification, by the R_{LIM} resistor connected to the CONT, see [Figure 12 on page 11](#).

The CONT pin has a minimum current sunk needed to activate the I_{Dlim} adjustment: without R_{LIM} or with high R_{LIM} (i.e. 100 kΩ) the current limit is fixed to the default value (see I_{Dlim} , [Table 8 on page 7](#)).

7.8 Overvoltage protection (OVP)

The device has integrated the logic for the monitor of the output voltage using as input signal the voltage V_{CONT} during the OFF time of the power MOSFET. This is the time when the voltage from the auxiliary winding tracks the output voltage, through the turn ratio $\frac{N_{AUX}}{N_{SEC}}$

The CONT pin has to be connected to the auxiliary winding through the diode D_{OVP} and the resistors R_{OVP} and R_{LIM} as shows the [Figure 23 on page 20](#). When, during the OFF time, the voltage V_{CONT} exceeds, four consecutive times, the reference voltage V_{OVP} (see [Table 8 on page 7](#)) the overvoltage protection will stop the power MOSFET and the converter enters the auto-restart mode.

In order to bypass the noise immediately after the turn off of the power MOSFET, the voltage V_{CONT} is sampled inside a short window after the time T_{STROBE} , see [Table 8 on page 7](#) and the [Figure 22 on page 19](#). The sampled signal, if higher than V_{OVP} trigger the internal OVP digital signal and increments the internal counter. The same counter is reset every time the signal OVP is not triggered in one oscillator cycle.

Referring to the [Figure 23](#), the resistors divider ratio k_{OVP} will be given by:

Equation 2

$$k_{OVP} = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} \cdot (V_{OUTOVP} + V_{DSEC}) - V_{DAUX}}$$

Equation 3

$$k_{OVP} = \frac{R_{LIM}}{R_{LIM} + R_{OVP}}$$

Where:

- V_{OVP} is the OVP threshold (see [Table 8 on page 8](#))
- $V_{OUT\ OVP}$ is the converter output voltage value to activate the OVP set by designer
- N_{AUX} is the auxiliary winding turns
- N_{SEC} is the secondary winding turns
- V_{DSEC} is the secondary diode forward voltage
- V_{DAUX} is the auxiliary diode forward voltage
- R_{OVP} together R_{LIM} make the output voltage divider

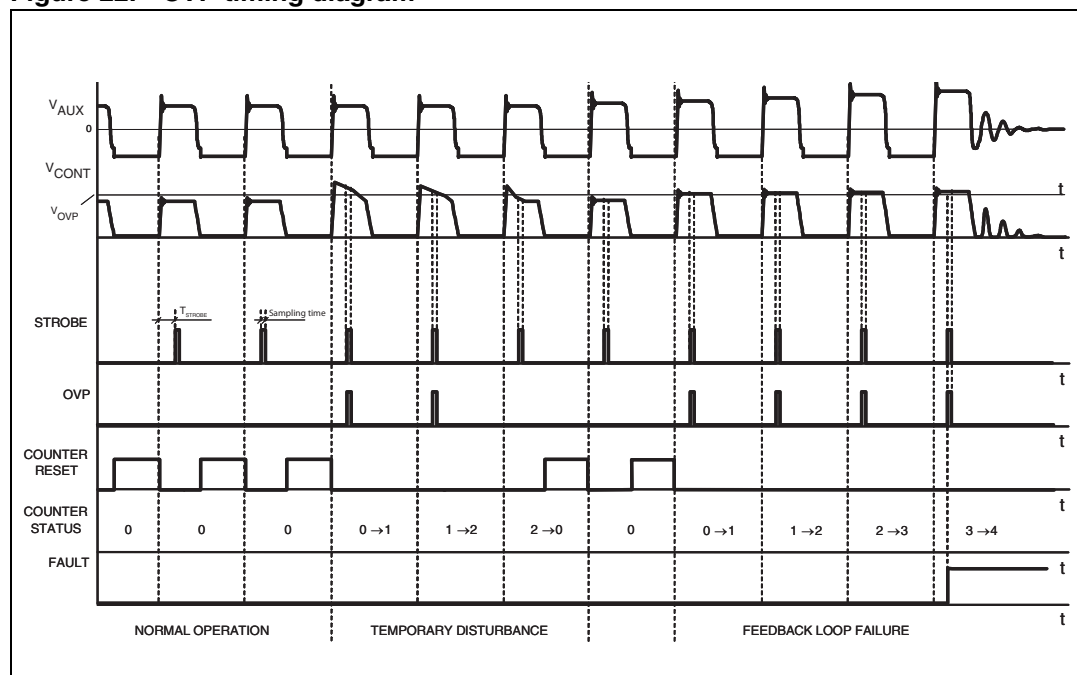
Then, fixed R_{LIM} , according to the desired I_{Dlim} , the R_{OVP} can be calculating by:

Equation 4

$$R_{OVP} = R_{LIM} \times \frac{1 - k_{OVP}}{k_{OVP}}$$

The resistor values will be such that the current sourced and sunk by the CONT pin be within the rated capability of the internal clamp.

Figure 22. OVP timing diagram



7.9 About CONT pin

Referring to the [Figure 23](#), through the CONT pin, the below features can be implemented:

1. Current limit set point
2. Overvoltage protection on the converter output voltage

The [Table 9 on page 20](#) referring to the [Figure 23](#), lists the external components needed to activate one or plus of the CONT pin functions.

Figure 23. CONT pin configuration

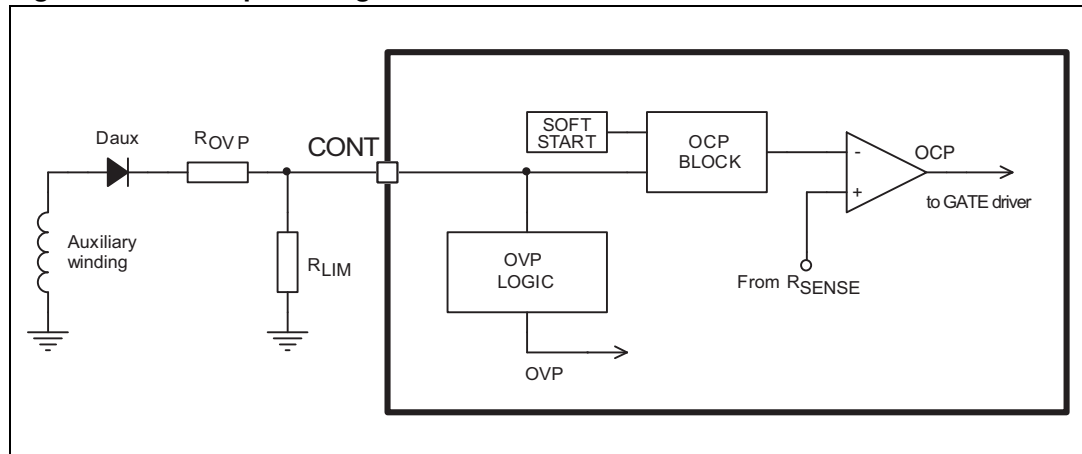


Table 9. CONT pin configurations

Function / component	$R_{LIM}^{(1)}$	R_{OVP}	D_{AUX}
I_{Dlim} reduction	See Figure 12	No	No
OVP	$\geq 80\text{ k}\Omega$	See Equation 4	Yes
I_{Dlim} reduction + OVP	See Figure 12	See Equation 4	Yes

1. R_{LIM} has to be fixed before of R_{OVP}

7.10 Feed-back and overload protection (OLP)

The device is a current mode converter: the feedback pin controls the PWM operation, controls the burst mode and activates the overload protection. [Figure 24 on page 22](#) and [Figure 25](#) show the internal current mode structure.

With the feedback pin voltage between V_{FBbm} and V_{FBlin} , (see [Table 8 on page 7](#)) the drain current is sensed and converted in voltage that is applied to the non inverting pin of the PWM comparator. See [Figure 2 on page 3](#).

This voltage is compared with the one on the feedback pin through a voltage divider on cycle by cycle basis. When these two voltages are equal, the PWM logic orders the switch off of the power MOSFET. The drain current is always limited to I_{Dlim} value.

In case of overload the feedback pin increases in reaction to this event and when it goes higher than V_{FBlin} , the PWM comparator is disabled and the drain current is limited to I_{Dlim} by the OCP comparator, see [Figure 2 on page 3](#).

When the feedback pin voltage reaches the threshold V_{FBlin} an internal current generator starts to charge the feedback capacitor (C_{FB}) and when the feedback voltage reaches the V_{FBolp} threshold, the converter is turned off and the start up phase is activated with reduced value of I_{DDch} to 0.6 mA, see [Table 7 on page 6](#).

During the first start up phase of the converter, after the soft-start up time, t_{SS} , the output voltage could force the feedback pin voltage to rise up to the V_{FBolp} threshold that switches off the converter itself.

To avoid this event, the appropriate feedback network has to be selected according to the output load. More the network feedback fixes the compensation loop stability. The [Figure 24 on page 22](#) and [Figure 25](#) show the two different feedback networks.

The time from the overload detection ($V_{FB} = V_{FBlin}$) to the device shutdown ($V_{FB} = V_{FBolp}$) can be set by C_{FB} value (see [Figure 24 on page 22](#) and [Figure 25](#)), using the formula:

Equation 5

$$T_{OLP-delay} = C_{FB} \times \frac{V_{FBolp} - V_{FBlin}}{3\mu A}$$

In the [Figure 24](#), the capacitor connected to FB pin (C_{FB}) is part of the compensation circuit as well as it needs to activate the overload protection (see equation 5).

After the start up time, t_{SS} , during which the feedback voltage is fixed at V_{FBlin} , the output capacitor could not be at its nominal value and the controller interprets this situation as an overload condition. In this case, the OLP delay helps to avoid an incorrect device shut down during the start up phase.

Owing to the above considerations, the OLP delay time must be long enough to by-pass the initial output voltage transient and check the overload condition only when the output voltage is in steady state. The output transient time depends from the value of the output capacitor and from the load.

When the value of the C_{FB} capacitor calculated for the loop stability is too low and cannot ensure enough OLP delay, an alternative compensation network can be used and it is showed in [Figure 25 on page 22](#).

Using this alternative compensation network, two poles (f_{PFB} , f_{PFB1}) and one zero (f_{ZFB}) are introduced by the capacitors C_{FB} and C_{FB1} and the resistor R_{FB1} .

The capacitor C_{FB} introduces a pole (f_{PFB}) at higher frequency than f_{ZB} and f_{PFB1} . This pole is usually used to compensate the high frequency zero due to the ESR (equivalent series resistor) of the output capacitance of the fly-back converter.

The mathematical expressions of these poles and zero frequency, considering the scheme in [Figure 25](#) are reported by the equations below:

Equation 6

$$f_{ZFB} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot R_{FB1}}$$

Equation 7

$$f_{PFB} = \frac{R_{FB(DYN)} + R_{FB1}}{2 \cdot \pi \cdot C_{FB} \cdot (R_{FB(DYN)} \cdot R_{FB1})}$$

Equation 8

$$f_{PFB} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot (R_{FB1} \cdot R_{FB(DYN)})}$$

The $R_{FB(DYN)}$ is the dynamic resistance seen by the FB pin.

The C_{FB1} capacitor fixes the OLP delay and usually C_{FB1} results much higher than C_{FB} . The [Equation 5](#) can be still used to calculate the OLP delay time but C_{FB1} has to be considered instead of C_{FB} . Using the alternative compensation network, the designer can satisfy, in all case, the loop stability and the enough OLP delay time alike.

Figure 24. FB pin configuration (option 1)

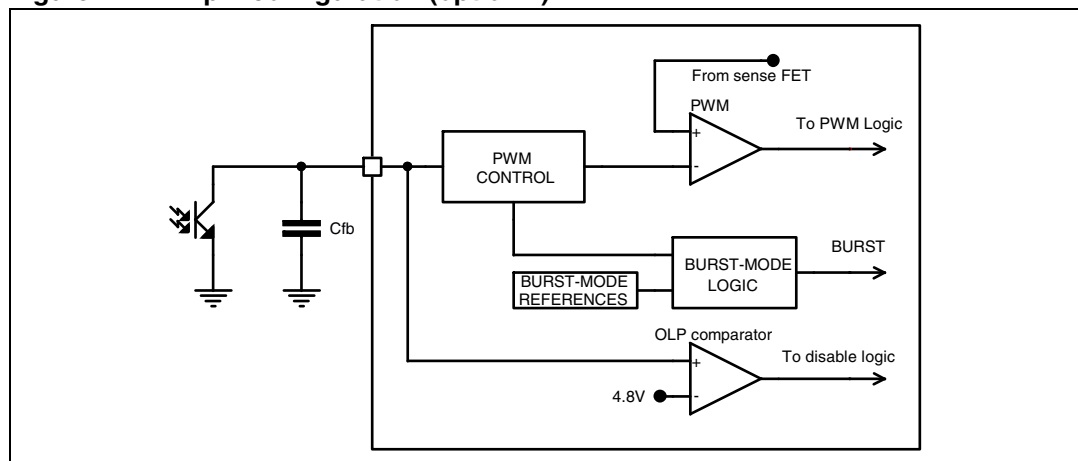
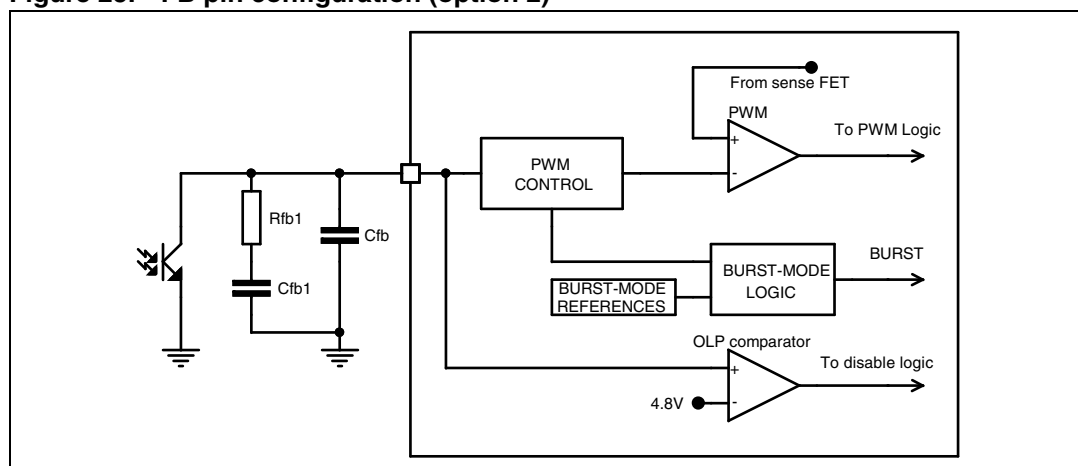


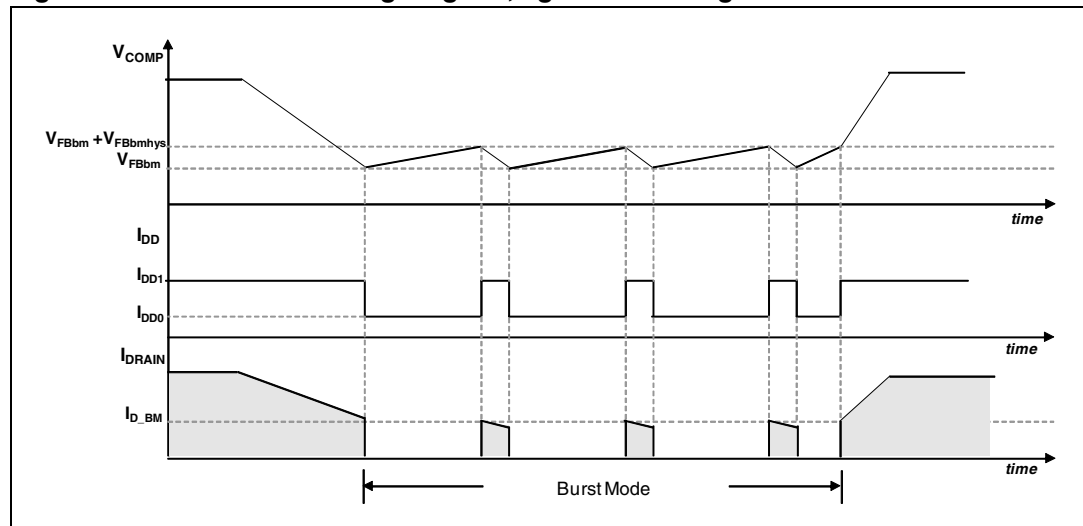
Figure 25. FB pin configuration (option 2)



7.11 Burst-mode operation at no load or very light load

When the load decrease the feedback loop reacts lowering the feedback pin voltage. If it falls down the burst mode threshold, V_{FBbm} , the power MOSFET is not more allowed to be switched on. After the MOSFET stops, as a result of the feedback reaction to the energy delivery stop, the feedback pin voltage increases and exceeding the level, $V_{FBbm} + V_{FBbmhys}$, the power MOSFET starts switching again. The burst mode thresholds are reported on [Table 8](#) and [Figure 26](#) shows this behavior. Systems alternates period of time where power MOSFET is switching to period of time where power MOSFET is not switching; this device working mode is the burst mode. The power delivered to output during switching periods exceeds the load power demands; the excess of power is balanced from not switching period where no power is processed. The advantage of burst mode operation is an average switching frequency much lower then the normal operation working frequency, up to some hundred of hertz, minimizing all frequency related losses. During the burst-mode the drain current peak is clamped to the level, I_{D_BM} , reported on [Table 8](#).

Figure 26. Burst mode timing diagram, light load management



7.12 Extra power management function (EPT)

Some applications need an extra power for a limited time window during which the converter regulation has to be guaranteed. The extra power management function allows to design a converter that can satisfy this request and is provided by the EPT pin, see [Table 8 on page 8](#).

This function requires the use of a capacitor on EPT pin (C_{EPT}) that is charged or discharged by means of a 5 μ A current cycle by cycle. When the drain current raises over 85% of I_{DLIM} value, see I_{DLIM_EPT} ([Table 8 on page 7](#)), the current generator charges C_{EPT} while when the drain current is below I_{DLIM_EPT} discharges the capacitor. If C_{EPT} 's voltage reaches the V_{EPT} threshold (typical, 4 V), the converter is shut down.

After the converter shut down, the V_{DD} voltage will drop below the $V_{DD(ON)}$ start up threshold (typ. 14.5 V) and according to the auto restart operation (see [Section 7.5 on page 17](#)) the V_{DD} pin voltage have to fall below the $V_{DD(RESTART)}$ threshold (typical, 4.5 V) in order to charge again the V_{DD} capacitor. Moreover the PWM operation is enabled again only when the voltage on EPT pin, drop below the $V_{EPT(RESTART)}$ (typical, 0.6 V). The low C_{EPT} discharge current in combination with its low restart threshold, ensures safe operations and avoids overheating in case of repeated overload events. The value of C_{EPT} has to be selected in order to prevent the device overheating. The EPT pin can be connected to GND if the function is not used.

7.13 2nd level overcurrent protection and hiccup mode

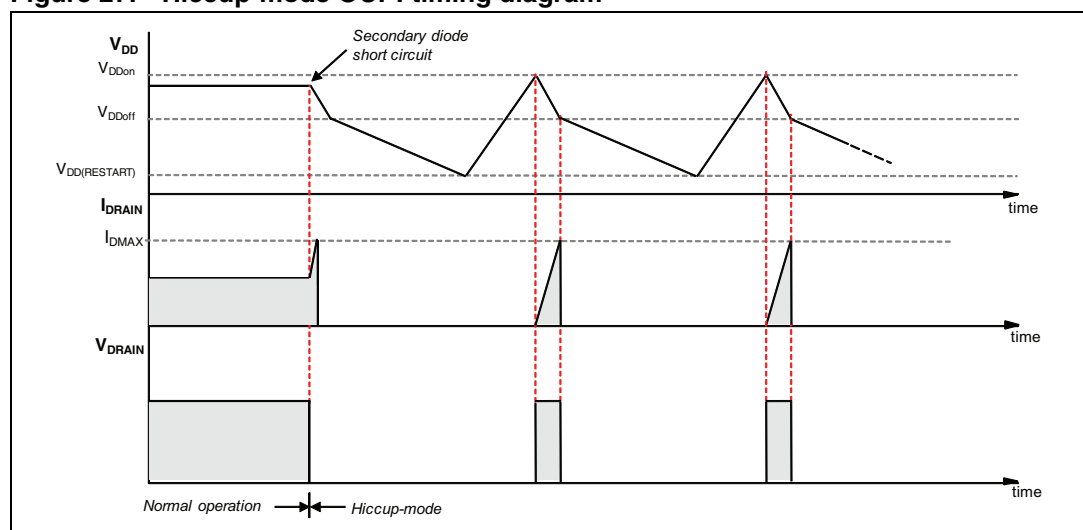
The device is protected against short-circuit of the secondary rectifier, short-circuit on the secondary winding or a hard-saturation of fly-back transformer. Such as anomalous condition is invoked when the drain current exceed the threshold $I_{D\text{MAX}}$, see [Table 8 on page 7](#).

To distinguish a real malfunction from a disturbance (e.g. induced during ESD tests) a “warning state” is entered after the first signal trip. If in the subsequent switching cycle the signal is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; otherwise if the $I_{D\text{MAX}}$ threshold is exceeded for two consecutive switching cycles a real malfunction is assumed and the power MOSFET is turned OFF.

The shutdown condition is latched as long as the device is supplied. While it is disabled, no energy is transferred from the auxiliary winding; hence the voltage on the V_{DD} capacitor decays till the V_{DD} under voltage threshold ($V_{DD\text{off}}$), which clears the latch.

The start up HV current generator is still off, until V_{DD} voltage goes below its restart voltage, $V_{DD(\text{RESTART})}$. After this condition the V_{DD} capacitor is charged again by 600 μA current, and the converter switching restarts if the $V_{DD\text{on}}$ occurs. If the fault condition is not removed the device enters in auto-restart mode. This behavioral results in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit. See the timing diagram of [Figure 27](#).

Figure 27. Hiccup-mode OCP: timing diagram



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 10. DIP-7 mechanical data

Dim.	mm		
	Typ	Min	Max
A			5,33
A1		0,38	
A2	3,30	2,92	4,95
b	0,46	0,36	0,56
b2	1,52	1,14	1,78
c	0,25	0,20	0,36
D	9,27	9,02	10,16
E	7,87	7,62	8,26
E1	6,35	6,10	7,11
e	2,54		
eA	7,62		
eB			10,92
L	3,30	2,92	3,81
M ⁽⁶⁾⁽⁸⁾	2,508		
N	0,50	0,40	0,60
N1			0,60
O ⁽⁷⁾⁽⁸⁾	0,548		

- 1- The leads size is comprehensive of the thickness of the leads finishing material.
- 2- Dimensions do not include mold protrusion, not to exceed 0,25 mm in total (both side).
- 3- Package outline exclusive of metal burrs dimensions.
- 4- Datum plane "H" coincident with the bottom of lead, where lead exits body.
- 5- Ref. POA MOTHER doc. 0037880
- 6- Creepage distance > 800 V
- 7- Creepage distance 250 V
- 8- Creepage distance as shown in the 664-1 CEI / IEC standard.

Figure 28. Package dimensions

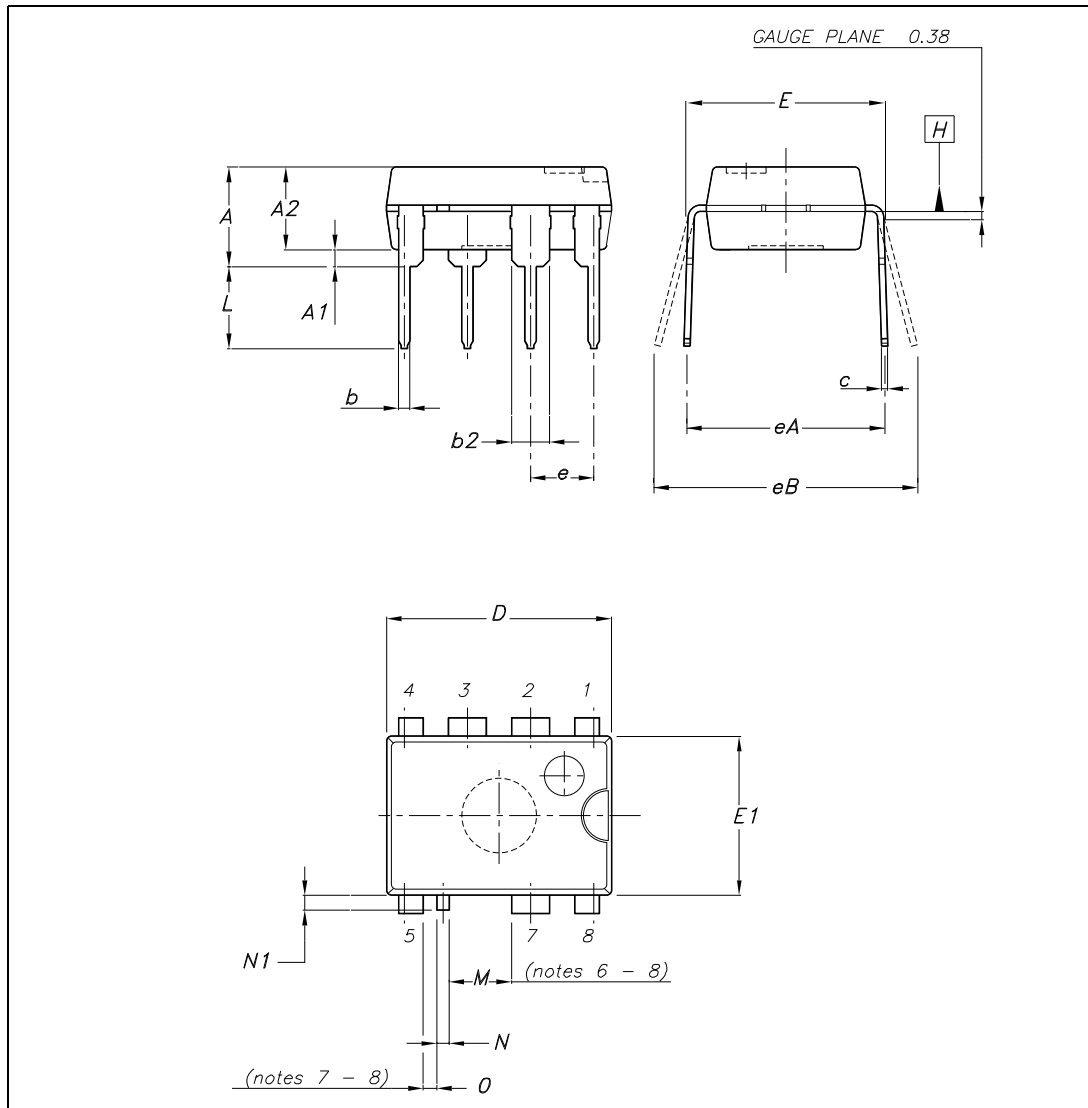


Table 11. SO16 narrow mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

Figure 29. SO16 narrow mechanical data

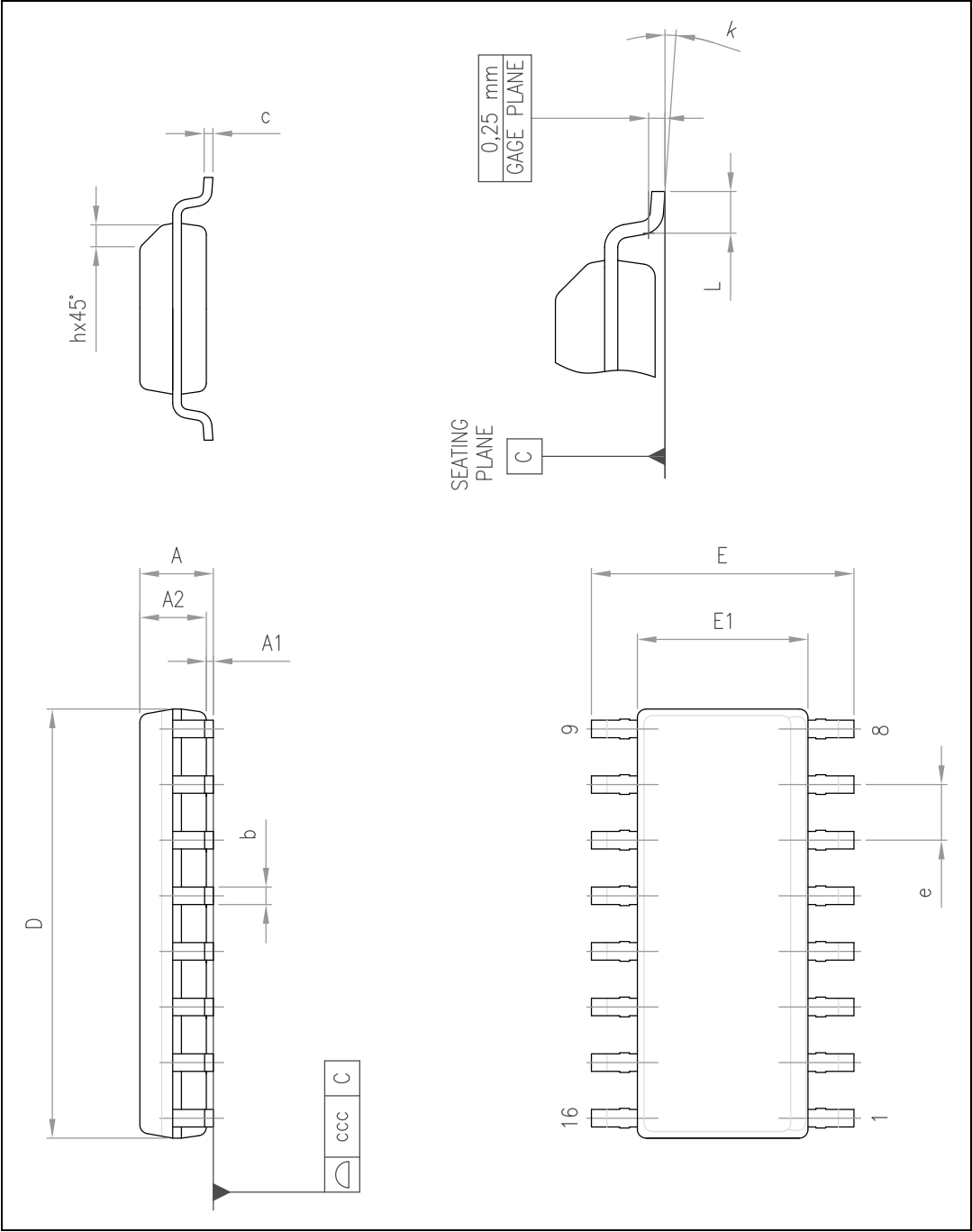
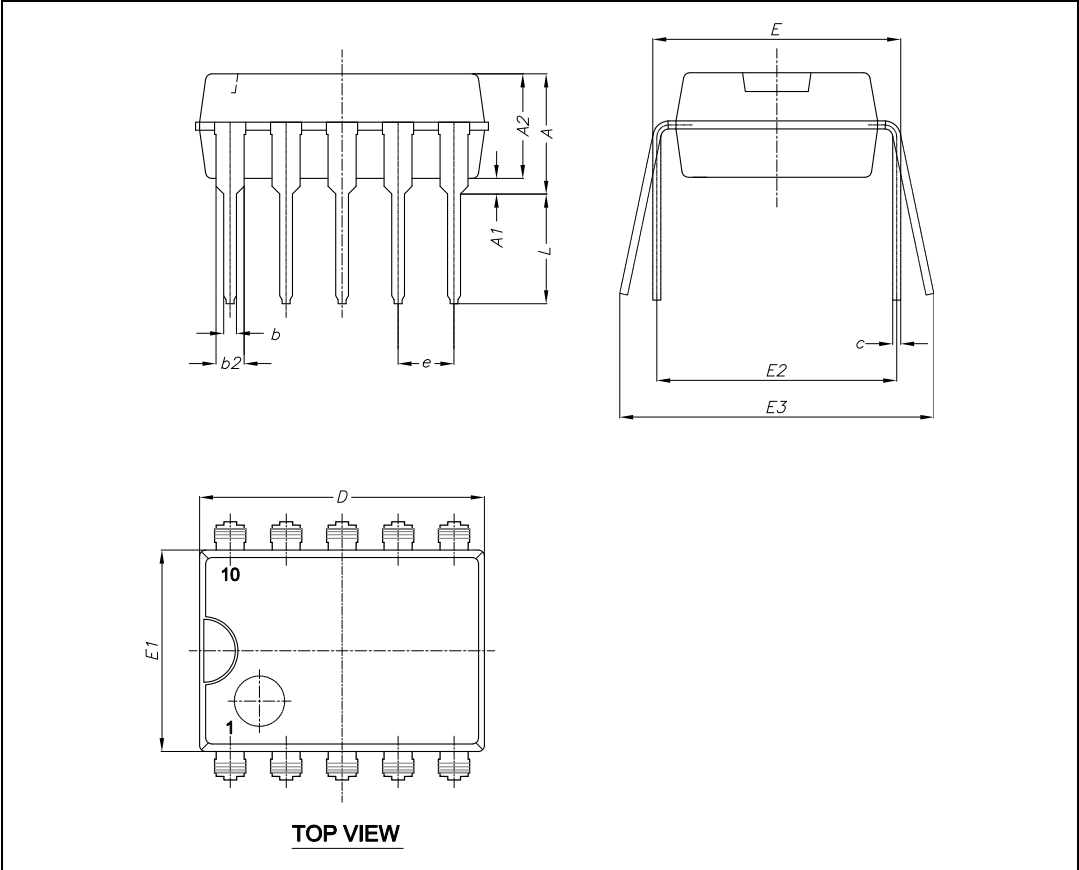


Table 12. SDIP10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			5.33
A1	0.38		
A2	2.92		4.95
b	0.36		0.56
b2	0.51		1.15
c	0.2		0.36
D	9.02		10.16
E	7.62		8.26
E1	6.1		7.11
E2		7.62	
E3			10.92
e		1.77	
L	2.92		3.81

Figure 30. SDIP10 mechanical drawing



9 Revision history

Table 13. Document revision history

Date	Revision	Changes
30-Sep-2008	1	Initial release
22-Jan-2009	2	Updated Figure 3 on page 4
21-Oct-2009	3	Added SO16N and SDIP10 packages
31-Aug-2010	4	Updated Figure 3 , Figure 4 , Figure 5 on page 9 and Table 3 on page 4
08-Jan-2013	5	Minor text changes to improve readability in Chapter 7.3 , Chapter 7.4 , Chapter 7.5 , Chapter 7.7 , Chapter 7.8 , Chapter 7.9 , Chapter 7.10 , Chapter 7.11 , Chapter 7.13 , in Table 7 on page 6 , Table 8 on page 7 and in Figure 22 on page 19

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