

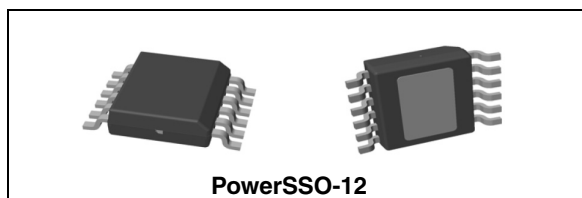
## Dual high side smart power solid state relay

### Features

Type	$V_{\text{demag}}^{(1)}$	$R_{\text{DSon}}^{(1)}$	$I_{\text{out}}^{(1)}$	$V_{\text{CC}}$
VNI2140J	$V_{\text{CC}}-45\text{ V}$	$0.08\ \Omega$	$1\text{ A}^{(2)}$	$45\text{ V}$

1. Per channel
2. Current limitation

- Nominal current: 0.5 A per channel
- Shorted load protections
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Thermal case shutdown restart not simultaneous for the various channels
- Protection against loss of ground
- Current limitation 1 A per channel
- Undervoltage shutdown
- Open load in off-state and short to  $V_{\text{CC}}$  detection
- Open-drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2



### Description

The VNI2140J is a monolithic device designed using STMicroelectronics' VIPower technology. The device drives two independent resistive or inductive loads with one side connected to ground. Active current limitation prevents a drop in system power supply in cases of shorted-load, and built-in thermal shutdown protects the chip from damage due to over-temperature and short-circuit. In overload conditions, channel turns OFF and ON automatically to maintain the junction temperature between TTSD and TR. If the case temperature reaches TCSD, the overloaded channel is turned OFF and restarts only when case temperature decreases down to TCR. In order to avoid high-peak current from the supply, when more than one channel is overloaded the TCSD restart is not simultaneous. Non overloaded channels continue to operate normally. The open-drain diagnostics output indicates over-temperature conditions and open-load in off state.

**Table 1. Device summary**

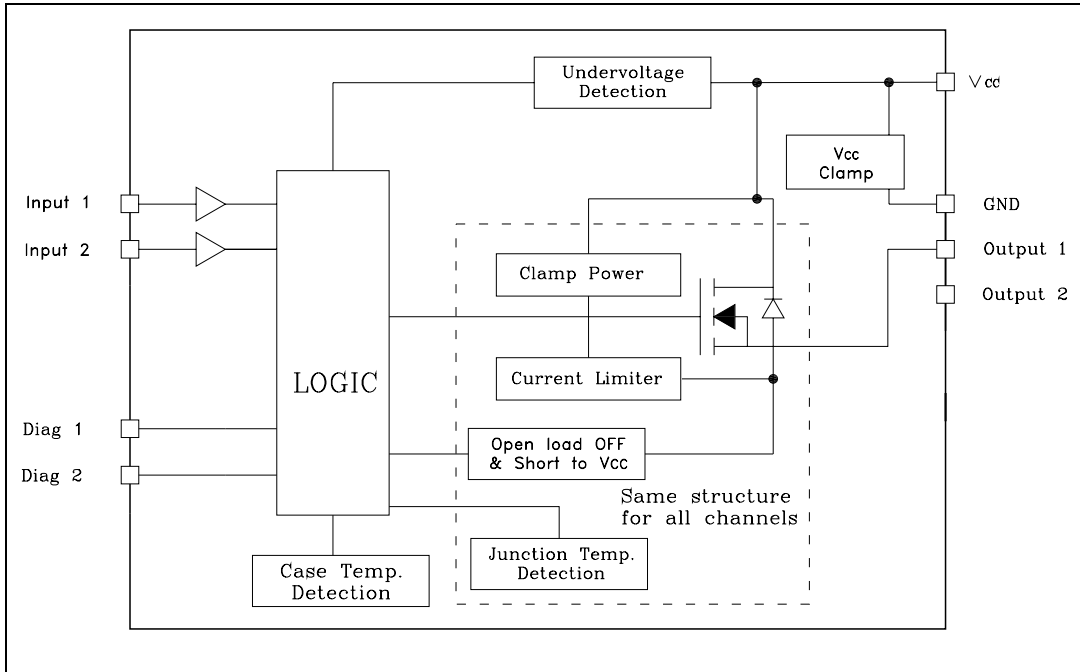
Order codes	Package	Packaging
VNI2140J	PowerSSO-12	Tube
VNI2140JTR		Tape and reel

# Contents

1	<b>Block diagram</b> .....	3
2	<b>Pin connections</b> .....	4
3	<b>Maximum ratings</b> .....	5
	3.1 Thermal data .....	5
4	<b>Electrical characteristics</b> .....	6
5	<b>Truth table</b> .....	9
6	<b>Switching waveforms</b> .....	10
7	<b>Open load</b> .....	13
8	<b>Package and PCB thermal data</b> .....	15
9	<b>Reverse polarity protection</b> .....	17
10	<b>Package mechanical data</b> .....	18
11	<b>Revision history</b> .....	22

# 1 Block diagram

Figure 1. Block diagram



## 2 Pin connections

Figure 2. Pin connections (top view)

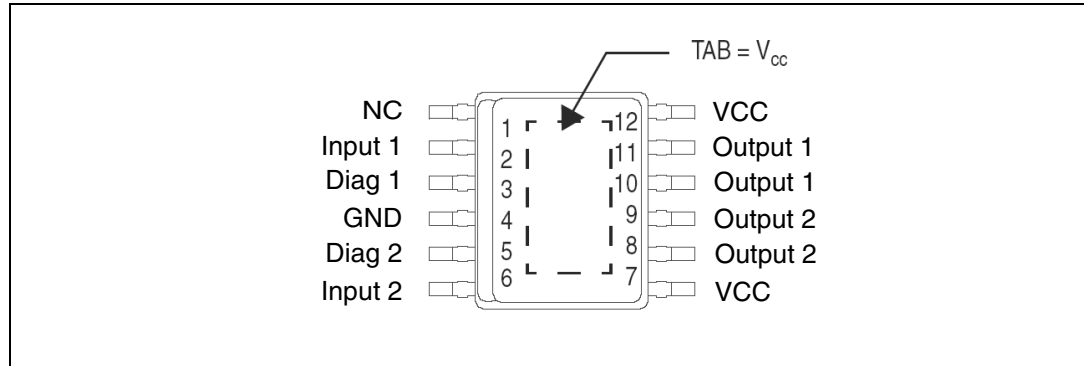


Table 2. Pin description

n°	Name	Description
1	NC	Not connected
2	Input 1	Channel 1 input 3.3 V CMOS/TTL compatible
3	Diag 1	Channel 1 diagnostic in open-drain configuration
4	GND	Device ground connection
5	Diag 2	Channel 2 diagnostic in open-drain configuration
6	Input 2	Channel 2 input 3.3 V CMOS/TTL compatible
7	VCC	Supply voltage
8	Output 2	Channel 2 power stage output, internally protected
9	Output 2	Channel 2 power stage output, internally protected
10	Output 1	Channel 1 power stage output, internally protected
11	Output 1	Channel 1 power stage output, internally protected
12	VCC	Supply voltage
TAB	TAB	Supply voltage

### 3 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
$I_{GND}$	DC ground reverse current	-250	mA
$I_{OUT}$	Output current (continuous)	Internally limited	A
$I_R$	Reverse output current (per channel)	-5	A
$I_{IN}$	Input current (per channel)	$\pm 10$	mA
$V_{IN}$	Input voltage	$+V_{CC}$	V
$V_{DIAG}$	Diag pin voltage	$+V_{CC}$	V
$I_{DIAG}$	Diag pin current	$\pm 10$	mA
$V_{ESD}$	Electrostatic discharge (R = 1.5 k $\Omega$ ; C = 100 pF)	2000	V
$E_{AS}$	Single pulse avalanche energy per channel not simultaneously	300	mJ
$P_{TOT}$	Power dissipation at $T_C = 25\text{ }^\circ\text{C}$	Internally limited	W
$T_J$	Junction operating temperature	Internally limited	$^\circ\text{C}$
$T_{STG}$	Storage temperature	-55 to 150	$^\circ\text{C}$

#### 3.1 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case <sup>(1)</sup>	Max 1	$^\circ\text{C}/\text{W}$
$R_{th(JA)}$	Thermal resistance junction-ambient <sup>(2)</sup>	Max See <a href="#">Figure 11 on page 15</a>	$^\circ\text{C}/\text{W}$

1. Per channel

2. When mounted using minimum recommended pad size on FR-4 board

## 4 Electrical characteristics

9 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>J</sub> < 125 °C; unless otherwise specified

**Table 5. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply voltage		9		45	V
R <sub>DS(ON)</sub>	On-state resistance	I <sub>OUT</sub> = 0.5 A at T <sub>J</sub> = 25 °C I <sub>OUT</sub> = 0.5 A		0.080	0.150	Ω Ω
V <sub>CLAMP</sub>	Clamp voltage	I <sub>S</sub> = 20 mA	45		52	V
I <sub>S</sub>	Supply current	All channel in off-state On-state with V <sub>IN</sub> = 5 V (T <sub>J</sub> = 125 °C)		300 1.9	4	μA mA
I <sub>LGND</sub>	Output current at turn-off	V <sub>CC</sub> = V <sub>DIAG</sub> = V <sub>IN</sub> = V <sub>GND</sub> = 24 V, V <sub>OUT</sub> = 0 V			1	mA
V <sub>OUT(OFF)</sub>	Off-state output voltage	V <sub>IN</sub> = 0 V and I <sub>OUT</sub> = 0 A			3	V
I <sub>OUT(OFF)</sub>	OFF-state output current	V <sub>IN</sub> = V <sub>OUT</sub> = 0 V	0		5	μA
I <sub>OUT(OFF1)</sub>		V <sub>IN</sub> = 0 V; V <sub>OUT</sub> = 4 V	-35		0	μA

V<sub>CC</sub> = 24

**Table 6. Switching**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(ON)</sub>	Turn-on delay time of output current	I <sub>OUT</sub> = 0.5 A, resistive load Input rise time < 0.1 μs, T <sub>J</sub> = 25 °C	-	20	-	μs
t <sub>r</sub>	Rise time of output current	I <sub>OUT</sub> = 0.5 A, resistive load Input rise time < 0.1 μs, T <sub>J</sub> = 25 °C	-	10	-	μs
t <sub>d(OFF)</sub>	Turn-off delay time of output current	I <sub>OUT</sub> = 0.5 A, resistive load Input rise time < 0.1 μs, T <sub>J</sub> = 25 °C	-	30	-	μs
t <sub>f</sub>	Fall time of output current	I <sub>OUT</sub> = 0.5 A, resistive load Input rise time < 0.1 μs, T <sub>J</sub> = 25 °C	-	8	-	μs
t <sub>DOL</sub>	Delay time for open load detection		-	500	-	μs
dV/dt(ON)	Turn ON voltage slope		-	3	-	V/μS
dV/dt(off)	Turn OFF voltage slope		-	4	-	V/μS

**Table 7. Logical input**

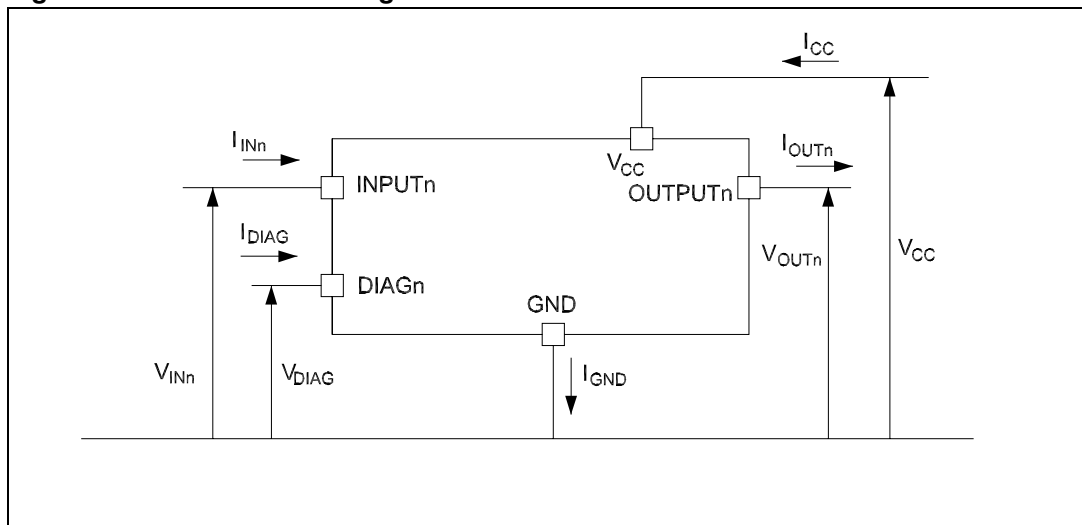
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				0.8	V
$V_{IH}$	Input high level voltage		2.20			V
$V_{I(HYST)}$	Input hysteresis voltage			0.15		V
$I_{IN}$	Input current	$V_{IN} = 15\text{ V}$			10	$\mu\text{A}$
		$V_{IN} = 36\text{ V}$			210	

**Table 8. Protection and diagnostic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DIAG}^{(1)}$	Diag voltage output low	$I_{DIAG} = 1.5\text{ mA}$ (fault condition)			0.6	V
$V_{USD}$	Undervoltage protection		7		9	V
$V_{USDHYS}$	Undervoltage hysteresis		0.4	0.5		V
$I_{LIM}$	DC short circuit current	$V_{CC} = 24\text{ V}; R_{LOAD} < 10\text{ m}\Omega$	1		2	A
$I_{LDIAG}$	Diag leakage current	$V_{CC} = 32\text{ V}$		30		$\mu\text{A}$
$V_{OL}$	Open-load off-state voltage detection threshold	$V_{IN} = 0\text{ V}$	2	3	4	V
$T_{TSD}$	Junction shutdown temperature		150	170		$^{\circ}\text{C}$
$T_R$	Junction reset temperature		135	155	200	$^{\circ}\text{C}$
$T_{HIST}$	Junction thermal hysteresis		7	15		$^{\circ}\text{C}$
$T_{CSD}$	Case shutdown temperature		125	130	135	$^{\circ}\text{C}$
$T_{CR}$	Case reset temperature		110			$^{\circ}\text{C}$
$T_{CHYST}$	Case thermal hysteresis		7	15		$^{\circ}\text{C}$
$V_{demag}$	Output voltage at turn-OFF	$I_{OUT} = 0.5\text{ A}; L_{LOAD} \geq 1\text{ mH}$	$V_{CC} - 45$	$V_{CC} - 50$	$V_{CC} - 52$	V

1. Diag determination > 100 ms after the switching edge.

Figure 3. Current and voltage conventions



## 5 Truth table

**Table 9. Truth table**

	INPUTn	OUTPUTn	DIAGn
Normal operation	L	L	H
	H	H	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Shorted load (Current limitation)	L	L	H
	H	X	H
Output voltage > V <sub>OL</sub>	L	Z <sup>(1)</sup>	L
	H	H	H
Short to V <sub>CC</sub>	L	H	L
	H	H	H

1. Z = Depending on the external circuit

# 6 Switching waveforms

Figure 4. Switching waveforms

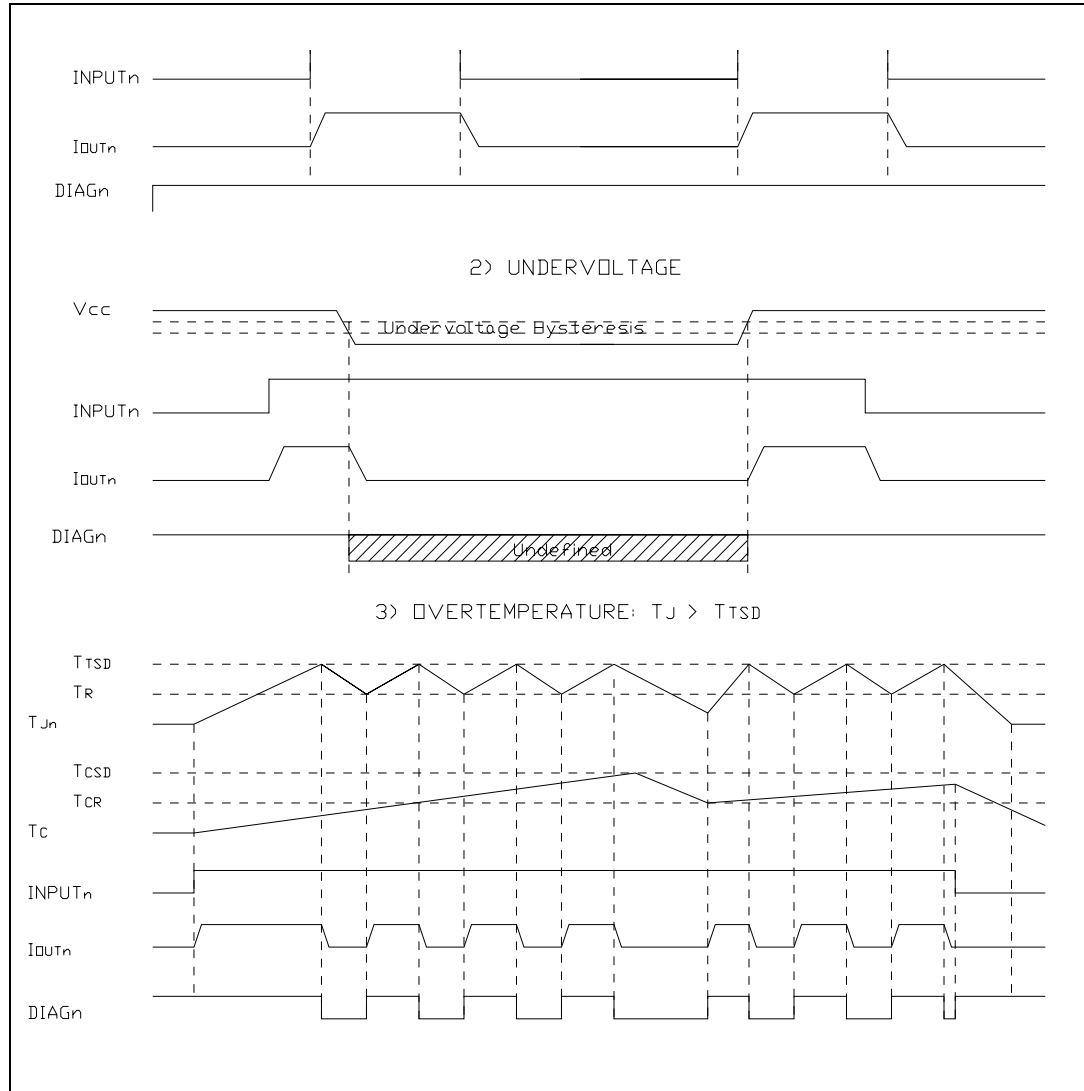


Figure 5. Switching waveforms (continued)

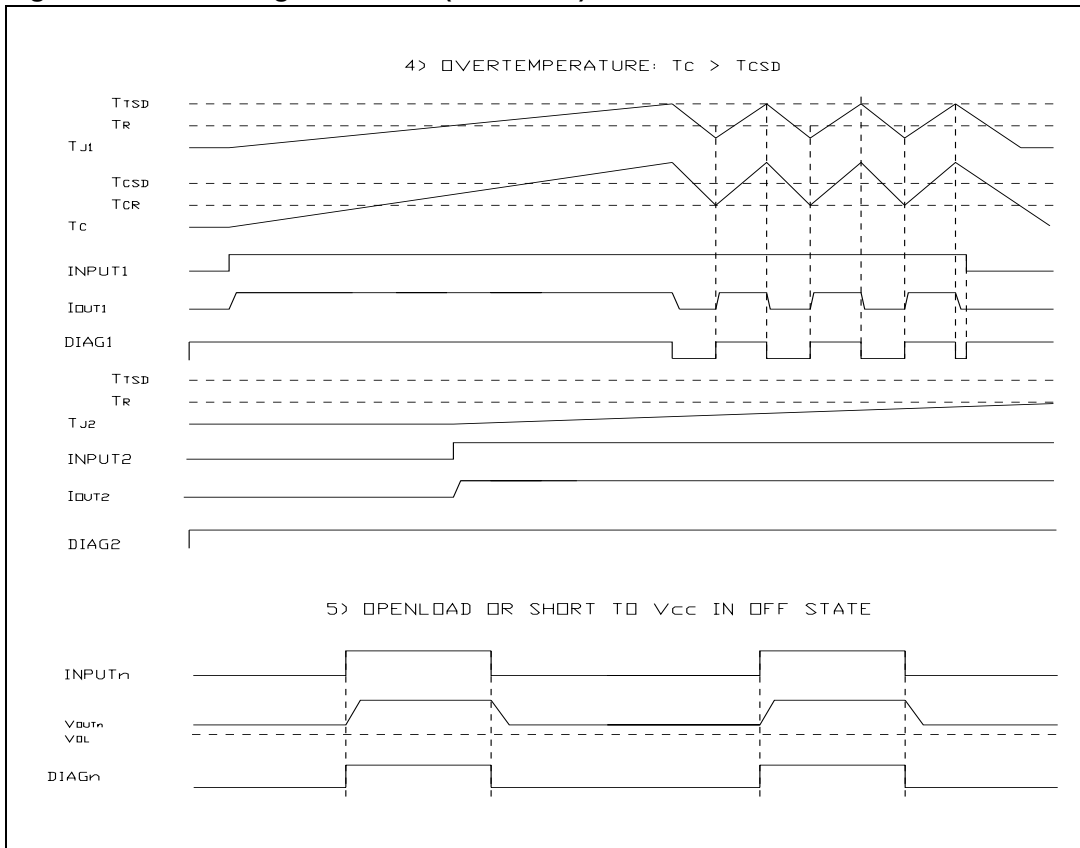


Figure 6. Switching parameter test conditions

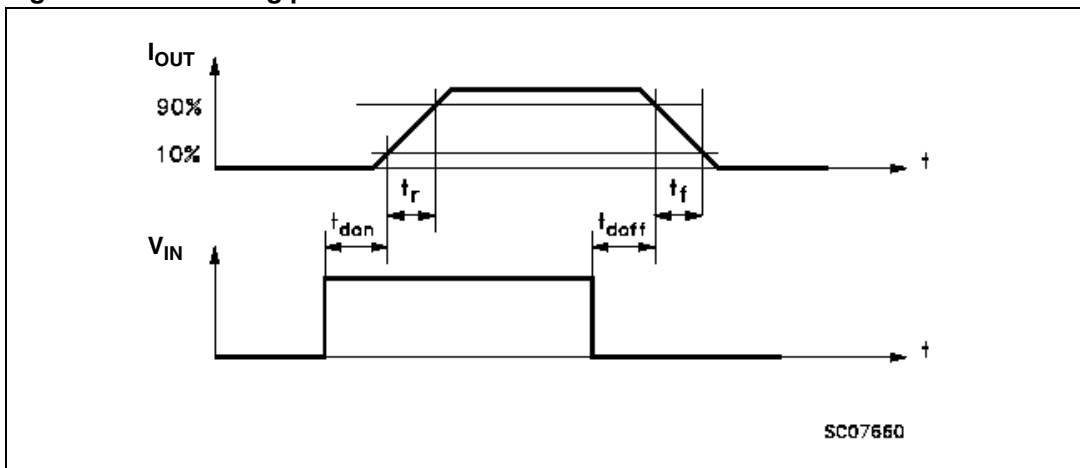
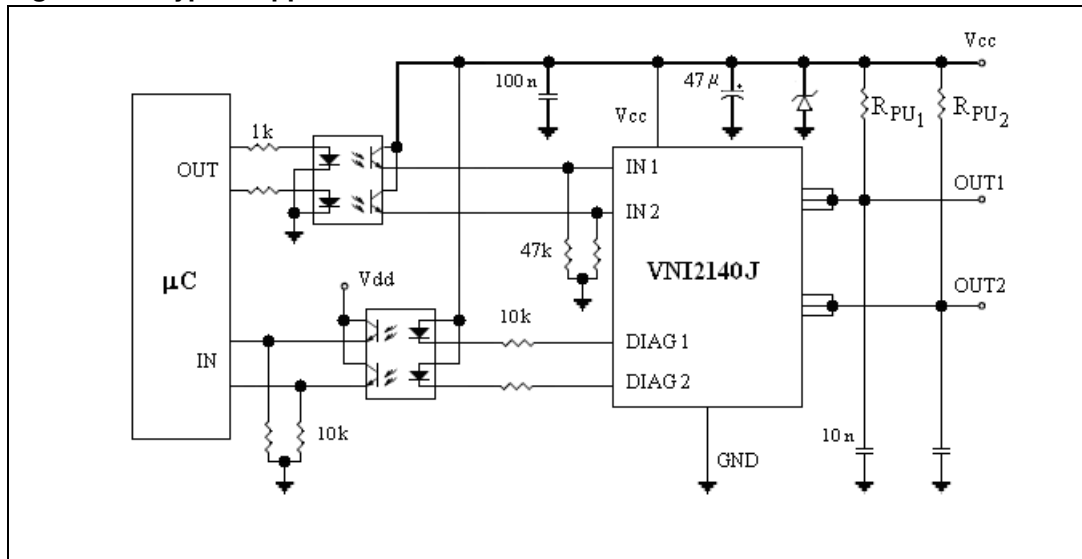


Figure 7. Typical application circuit



## 7 Open load

In order to detect the open load fault a pull-up resistor must be connected between the  $V_{CC}$  line and the output pin.

In a normal condition a current flows through the network made up of a pull-up resistor and a load. The voltage across the load is less than  $V_{OLMIN}$ ; so the diag pin is kept high.

This is the result in the condition:

### Equation 1

$$V_{CC} \frac{R_{LOAD}}{R_{LOAD} + R_{PU}} < V_{OLMIN}$$

or

### Equation 2

$$\left( \frac{V_{CC}}{V_{OLMIN}} - 1 \right) \cdot R_{LOAD} < R_{PU}$$

When a open load event occurs the voltage on the output pin rises to a value higher than  $V_{OLMAX}$  (depending on the pull-up resistor). The diag pin will go down.

This result in the condition:

### Equation 3

$$R_{PU} < \frac{V_{CC} - V_{OLMAX}}{|I_{OUT(OFF1)MIN}|}$$

Figure 8. Open load detection

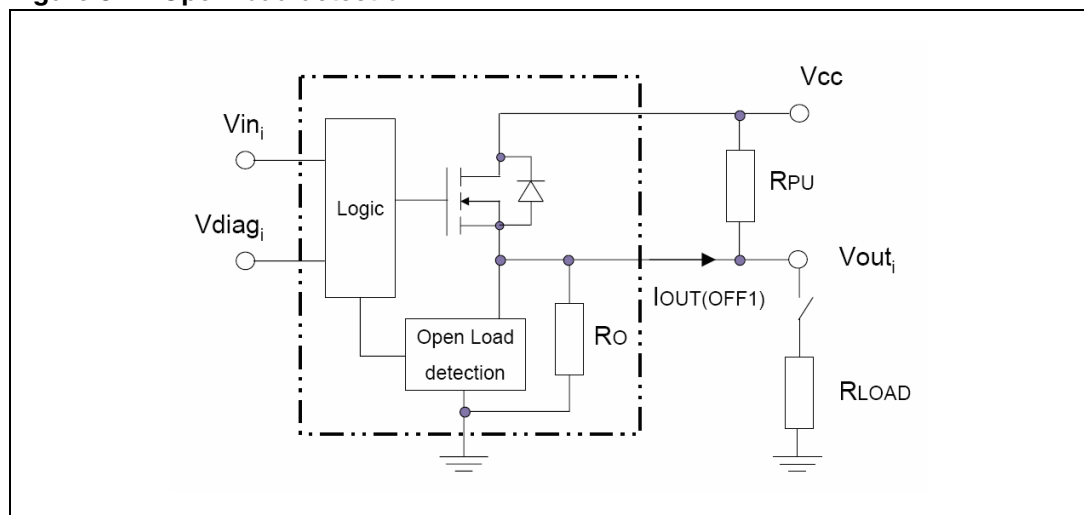
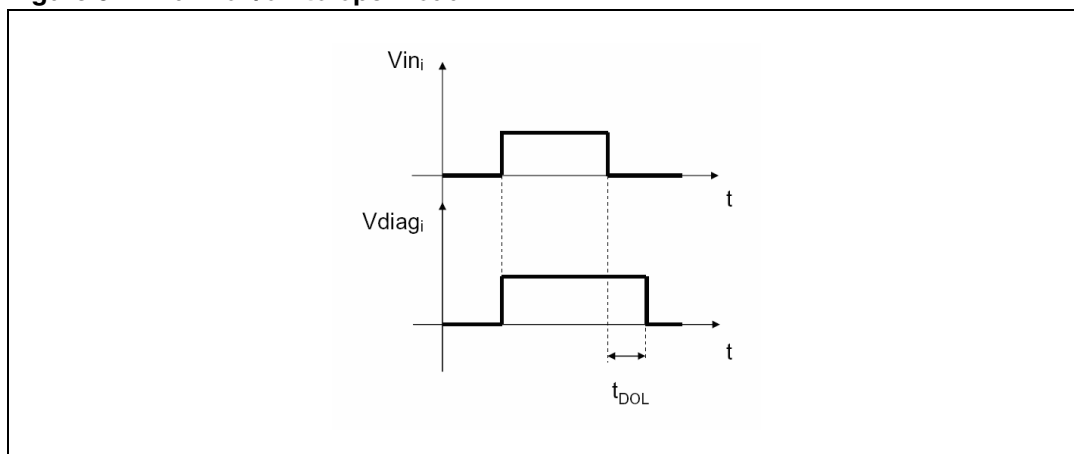


Figure 9. Turn on/off to open load



# 8 Package and PCB thermal data

Figure 10. PowerSSO-12 PC board

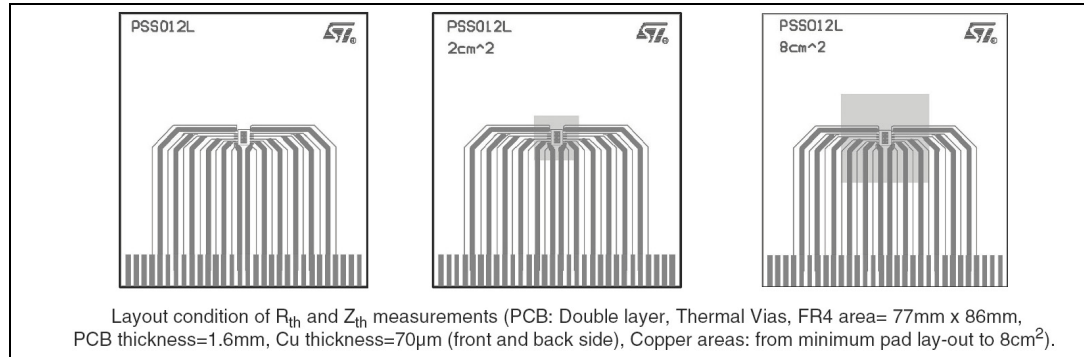


Figure 11.  $R_{thJA}$  vs PCB copper area in open box free air condition

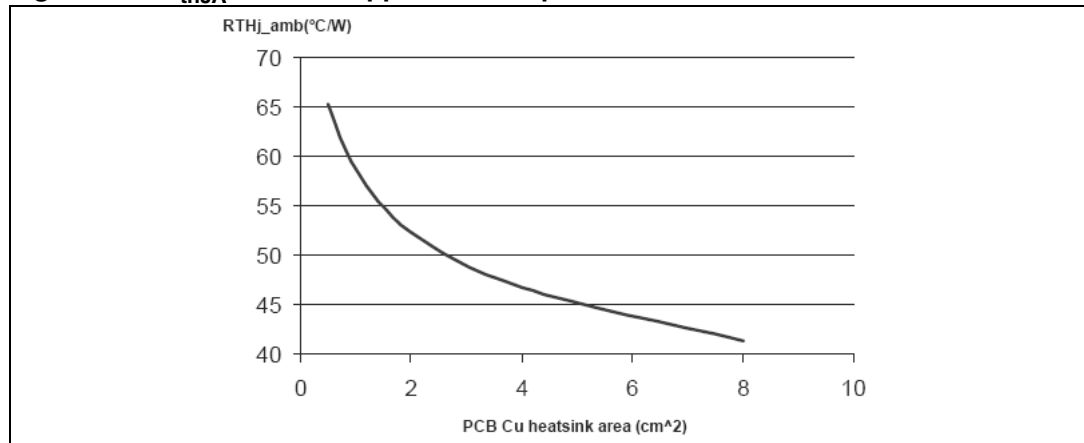
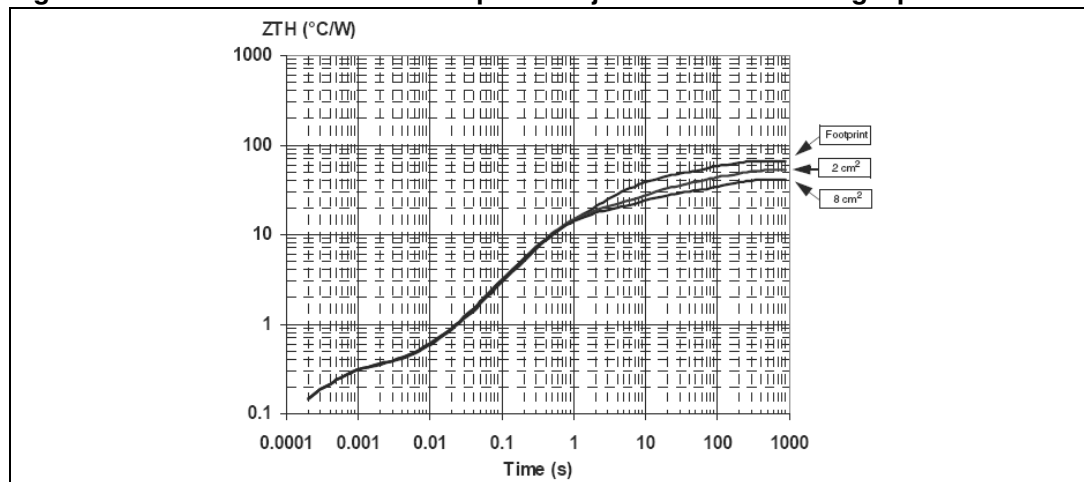


Figure 12. PowerSSO-12 thermal Impedance junction ambient single pulse



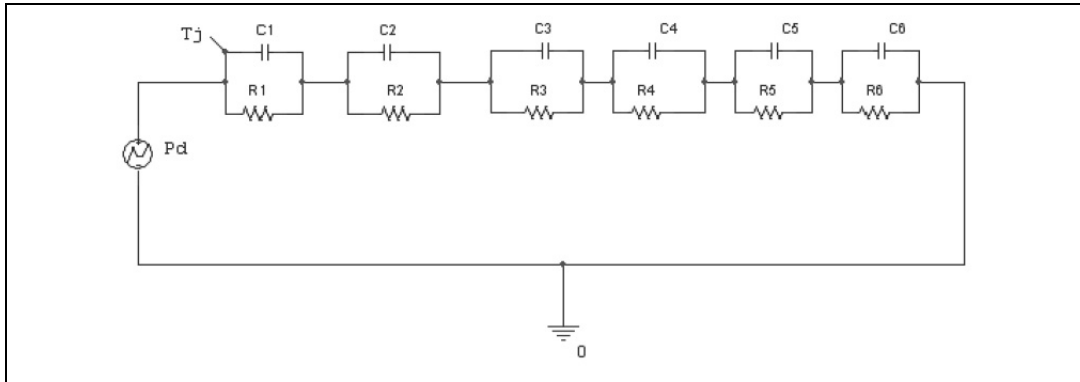
Pulse calculation formula

**Equation 4**

$$Z_{TH\delta} = R_{TH} \times \delta + Z_{THtp} (1 - \delta)$$

where  $\delta = t_p/T$

**Figure 13. Thermal fitting model of a double channel HSD in PowerSSO-12**



**Table 10. Thermal parameter**

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1 (°C/W)	0.1		
R2 (°C/W)	0.2		
R3 (°C/W)	7		
R4 (°C/W)	10	10	9
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.0001		
C2 (W.s/°C)	0.002		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

## 9 Reverse polarity protection

This schematic can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

$$R_{GND} = (-V_{CC}) / (-I_{GND})$$

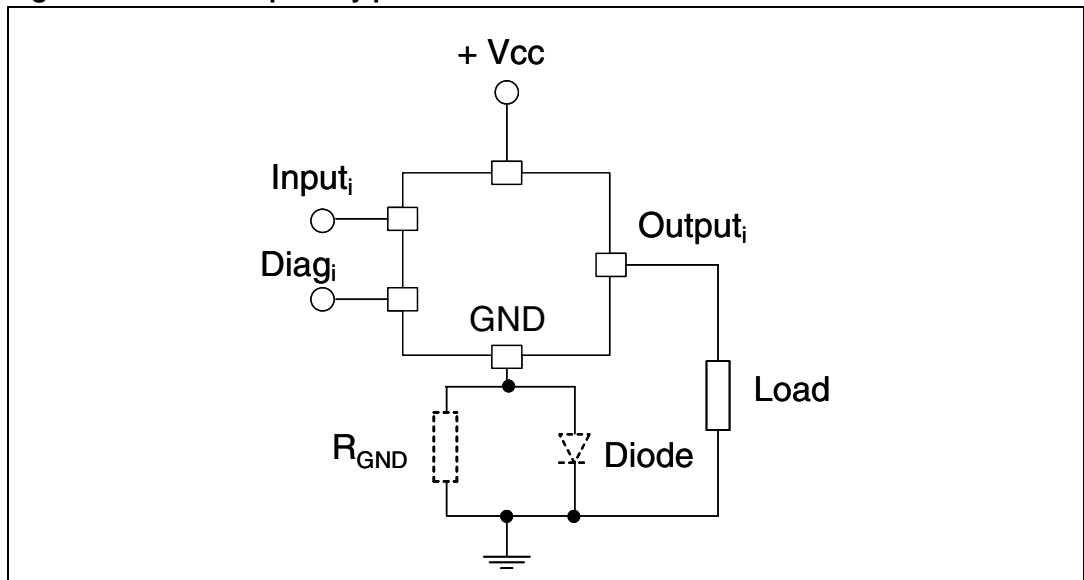
where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse polarity situations) is:

$$PD = (-V_{CC})^2 / R_{GND}$$

*Note:* In normal condition (no reverse polarity) due to the diode there will be a voltage drop between GND of the device and GND of the system.

**Figure 14. Reverse polarity protection**



## 10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 11. PowerSSO-12™ mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Figure 15. PowerSSO-12™ package dimensions

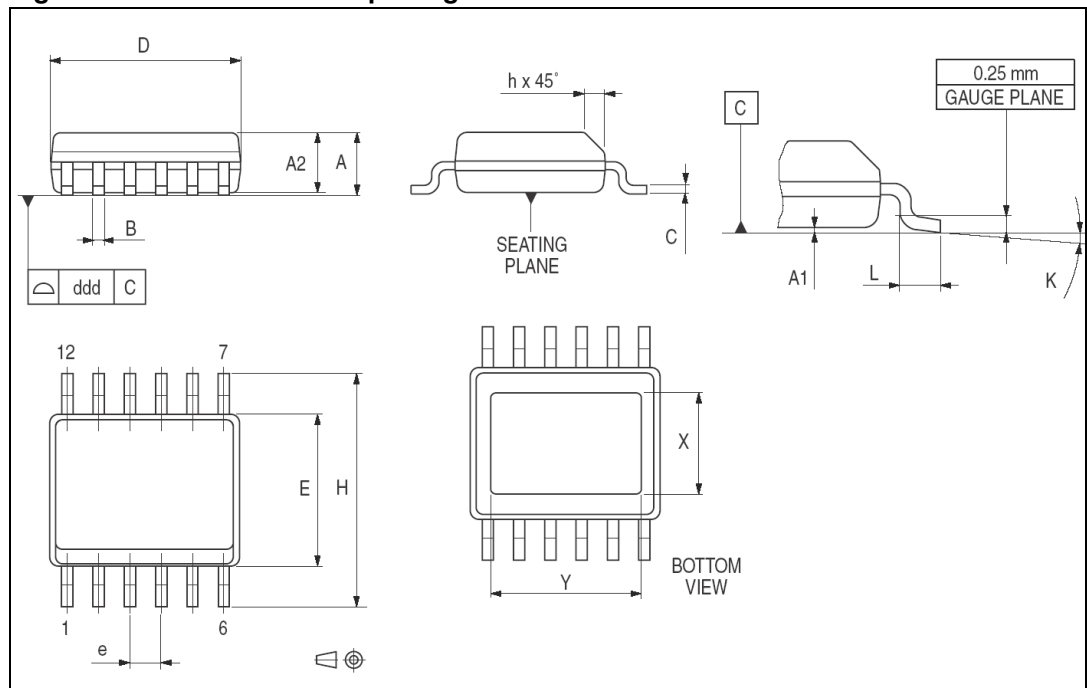


Figure 16. PowerSSO-12™ tube shipment (no suffix)

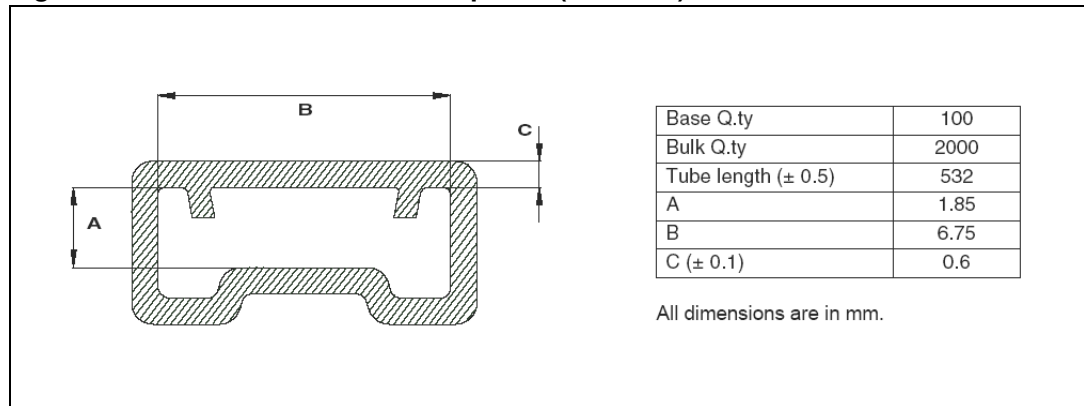
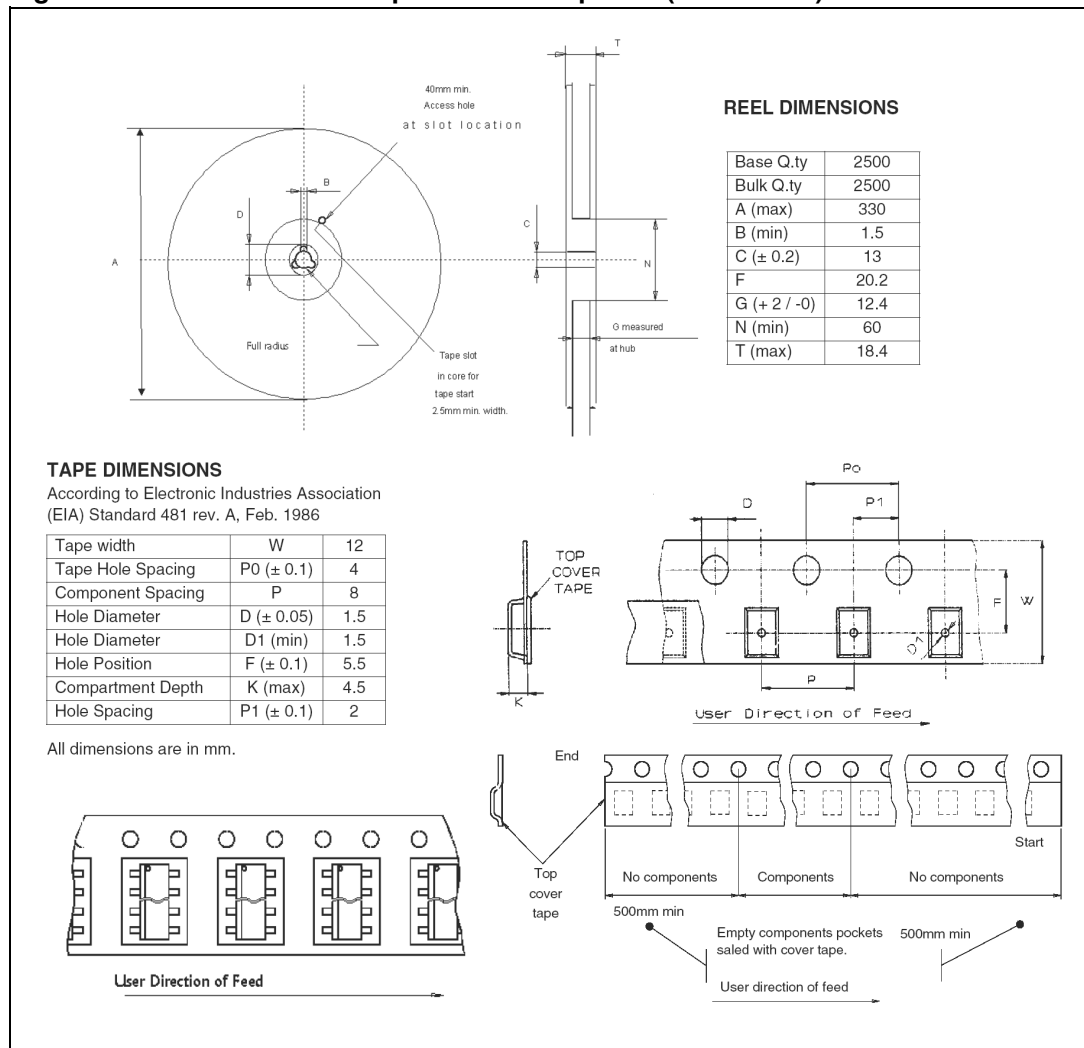


Figure 17. PowerSSO-12™ tape and reel shipment (suffix “TR”)





## 11 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
16-Dec-2008	1	Initial release
29-Apr-2009	2	Updated <a href="#">Table 5 on page 6</a>
03-Jul-2009	3	Updated features in coverpage and <a href="#">Table 5 on page 6</a>
27-Aug-2009	4	Updated <a href="#">Section 9: Reverse polarity protection</a>
25-Mar-2010	5	Updated Coverpage and <a href="#">Table 4 on page 5</a>
26-Apr-2010	6	Updated <a href="#">Table 5 on page 6</a>
21-Jul-2010	7	Updated <a href="#">Table 8 on page 7</a>
15-Nov-2011	8	Updated <a href="#">Figure 18 on page 21</a>

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[VNI2140J](#) [VNI2140JTR](#)