

## MAP Block Power Module Single Thyristor, 500 A



MAP Block Power

### FEATURES

- Electrically isolated base plate
- 3000 V<sub>RMS</sub> isolating voltage
- Industrial standard package
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL approved file E78996 
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

PRODUCT SUMMARY	
I <sub>T(AV)</sub>	500 A
Type	Modules - Thyristor, Standard
Package	MAP BLOCK
Circuit	Single Thyristor

### APPLICATIONS

- Battery chargers
- Welders
- Power converters
- Alternators

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
V <sub>DRM</sub> /V <sub>RRM</sub>		800	V
I <sub>T(AV)</sub>	76 °C	500	A
I <sub>TSM</sub>	50 Hz	14 000	A
	60 Hz	14 658	
I <sup>2</sup> t	50 Hz	980	kA <sup>2</sup> s
	60 Hz	894	
I <sup>2</sup> √t		9800	kA <sup>2</sup> √s
T <sub>J</sub>	Range	- 40 to 130	°C

### ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS			
TYPE NUMBER	V <sub>RRM</sub> /V <sub>DRM</sub> , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V <sub>RSM</sub> /V <sub>DSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I <sub>RRM</sub> /I <sub>DRM</sub> AT 130 °C mA
VS-VSKS500/08PbF	800	900	80



ON-STATE CONDUCTION					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction half sine wave		500	A
				76	°C
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch		785	A
Maximum peak, one-cycle on-state, non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reappplied	16 646	
		t = 8.3 ms		17 430	
		t = 10 ms	100 % $V_{RRM}$ reappplied	14 000	
		t = 8.3 ms		14 658	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reappplied	1385	kA <sup>2</sup> s
		t = 8.3 ms		1265	
		t = 10 ms	100 % $V_{RRM}$ reappplied	894	
		t = 8.3 ms		894	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reappplied		1385	kA <sup>2</sup> √s
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J$ maximum		0.6839	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > $\pi \times I_{T(AV)}$ ), $T_J$ maximum		0.7598	
Low level value on-state slope resistance	$r_{t1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J$ maximum		0.393	mΩ
High level value on-state slope resistance	$r_{t2}$	(I > $\pi \times I_{T(AV)}$ ), $T_J$ maximum		0.389	
Maximum on-state voltage drop	$V_{TM}$	$T_J = 25\text{ °C}$ , 500 A $I_{pk}$		1.1	V

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Typical delay time	$t_d$	Gate current 1 A, $dI_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\% V_{DRM}$ , $T_J = 25\text{ °C}$ , $I_t = 400\text{ A}$		1.3	μs
Typical turn-off time	$t_q$	$I_{TM} = 750\text{ A}$ , $T_J = T_J$ maximum, $dI/dt = 60\text{ A}/\mu\text{s}$ , $V_R = 50\text{ V}$ $dV/dt = 20\text{ V}/\mu\text{s}$ , Gate 0 V 100 Ω, $t_p = 500\text{ μs}$		200	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	$dV/dt$	$T_J = T_J$ maximum linear to 67 % rated $V_{DRM}$		500	V/μs
Maximum peak reverse and off-state leakage current	$I_{DRM}$ , $I_{RRM}$	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied		80	mA
RMS insulation voltage	$V_{INS}$	50 Hz, circuit to base, all terminal shorted, t = 1 s		3000	V



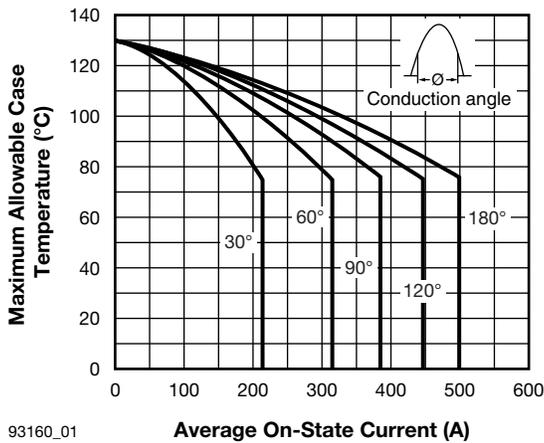
TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10.0	W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	2.0	
Maximum peak positive gate current	$I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0	A
Maximum required DC gate voltage to trigger	$V_{GT}$	$T_J = 25$ °C Anode supply: 12 V resistive load	3	V
Maximum required DC gate current to trigger	$I_{GT}$		200	mA
Maximum holding current	$I_H$		600	
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	20	V
Maximum peak negative gate voltage	$-V_{GM}$		5.0	
DC gate voltage not to trigger	$V_{GD}$	$T_J = T_J$ maximum Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated $V_{DRM}$ anode to cathode applied	0.30	V
DC gate current not to trigger	$I_{GD}$		10	mA
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 $\Omega$ , $t_r \leq 1$ $\mu$ s $T_J = T_J$ maximum, anode voltage $\leq 80\%$ $V_{DRM}$ , $I_t = 400$ A	1000	A/ $\mu$ s

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating and storage temperature range	$T_J, T_{Stg}$		- 40 to 130	°C
Maximum thermal resistance, junction to case per junction	$R_{thJC}$	DC operation	0.08	K/W
Maximum thermal resistance, case to heatsink per module	$R_{thCS}$	Mounting surface smooth, flat and greased	0.035	
Mounting torque $\pm 10\%$	MAP Block to heatsink	A mounting compound is recommended and the torque should be rechecked after a period of 3 h to allow for the spread of the compound. Lubricated threads.	6 to 8	Nm
	busbar to MAP Block		12 to 15	
Approximate weight			430	g
			15.3	oz.
Case style			MAP Block Power	

$\Delta R$ CONDUCTION PER JUNCTION											
DEVICES	SINUSOIDAL CONDUCTION AT $T_J$ MAXIMUM					RECTANGULAR CONDUCTION AT $T_J$ MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VS-VSKS500	0.013	0.0148	0.018	0.026	0.044	0.082	0.0142	0.019	0.027	0.044	K/W

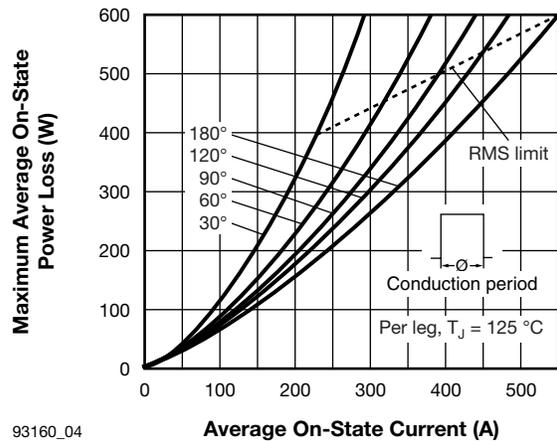
**Note**

- Table shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC



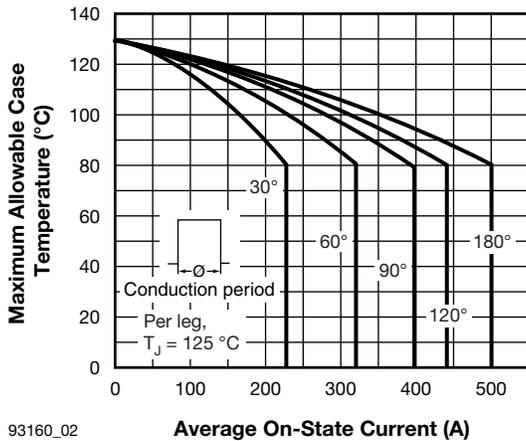
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Fig. 1 - Current Rating Characteristics



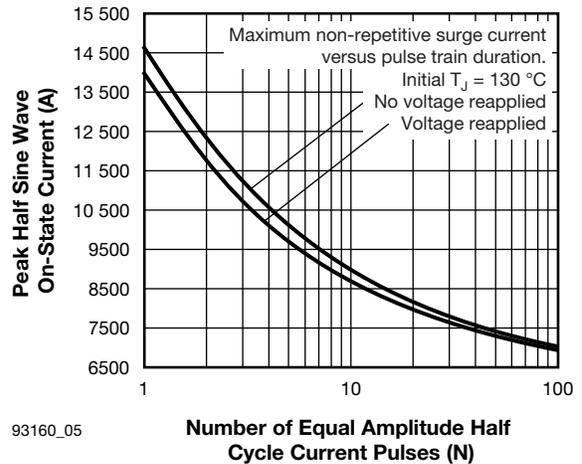
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Fig. 4 - On-State Power Loss Characteristics



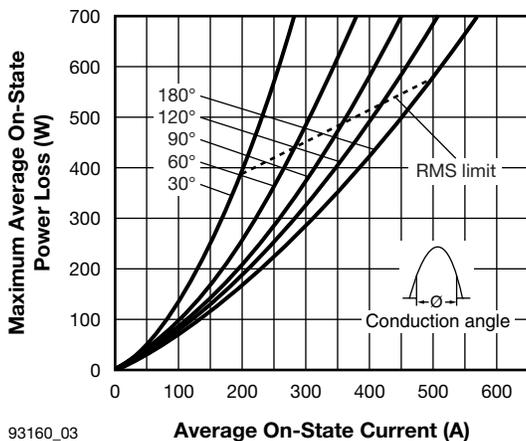
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Fig. 2 - Current Rating Characteristics



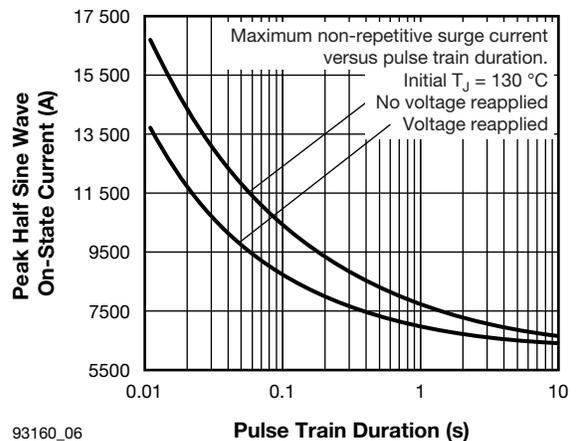
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Fig. 5 - Maximum Non-Repetitive Surge Current



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Fig. 3 - On-State Power Loss Characteristics



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Fig. 6 - Maximum Non-Repetitive Surge Current

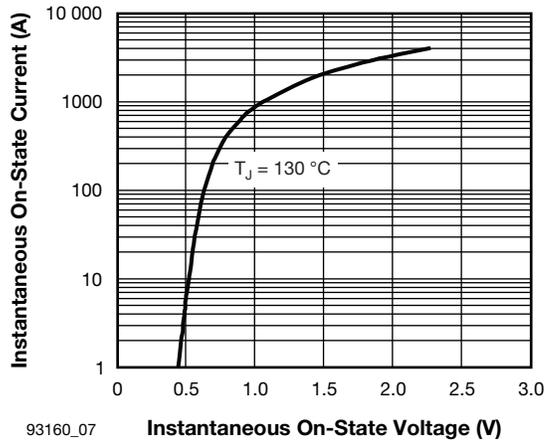


Fig. 7 - On-State Voltage Drop Characteristics

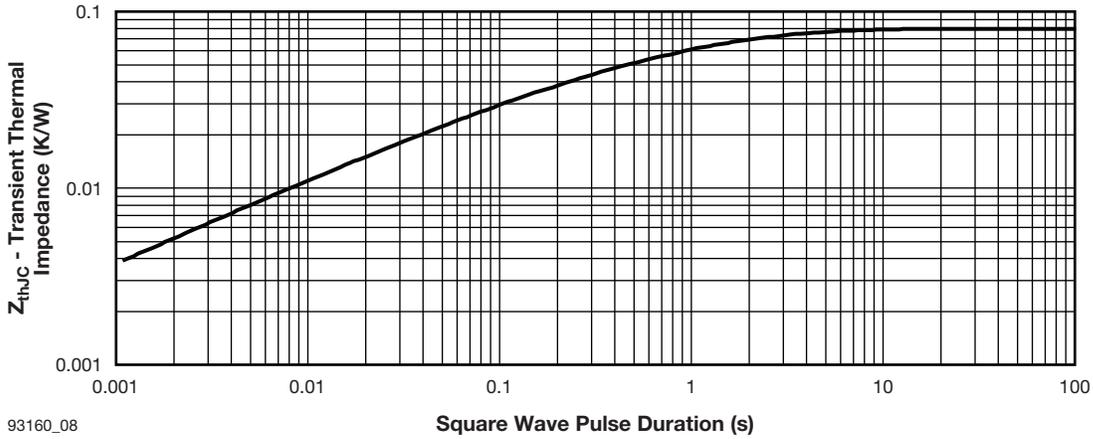


Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics

**ORDERING INFORMATION TABLE**

Device code	<b>VS-</b>	<b>VSK</b>	<b>S</b>	<b>500</b>	<b>/</b>	<b>08</b>	<b>PbF</b>
	①	②	③	④		⑤	⑥

- 1** - Vishay Semiconductors product
- 2** - Module type
- 3** - Circuit configuration (S = Single SCR)
- 4** - Current rating (500 = 500 A)
- 5** - Voltage rating (08 = 800 V)
- 6** - PbF = Lead (Pb)-free

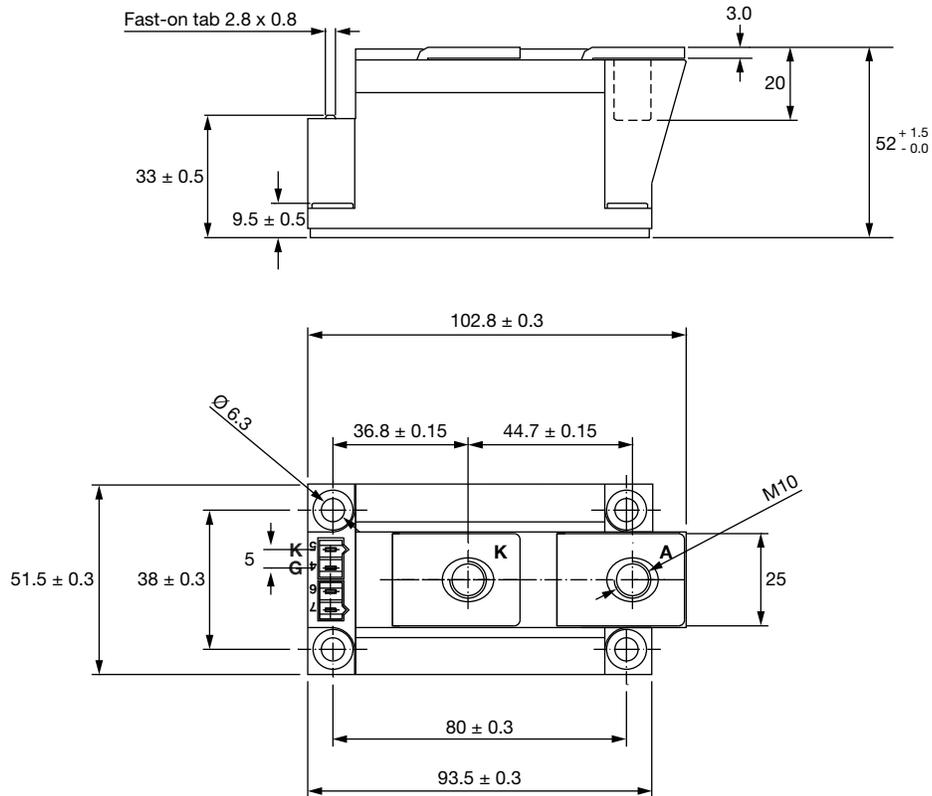


CIRCUIT CONFIGURATION	
CIRCUIT DESCRIPTION	CIRCUIT DRAWING
Single SCR	

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95379">www.vishay.com/doc?95379</a>

## Thyristor MAP Block

**DIMENSIONS** in millimeters



**Notes**

- Dimensions are nominal
- Full engineering drawings are available on request



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