Thyristor Module

3~ Rectifier		
V_{RRM} =	1600 V
I_{DAV} =	45 A
I_{FSM} =	320 A

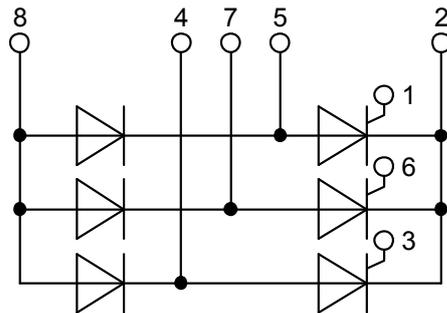3~ Rectifier Bridge, half-controlled (high-side)

Part number

VVZ40-16io1
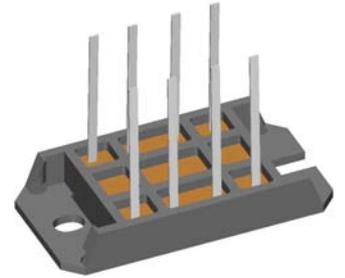
Backside: isolated

🇺🇱 E72873

Features / Advantages:
● Package with DCB ceramic base plate
● Improved temperature and power cycling
● Planar passivated chips
● Very low forward voltage drop
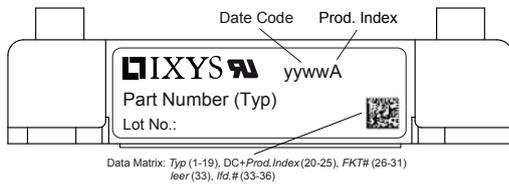● Very low leakage current

Applications:
● Line rectifying 50/60 Hz
● Drives
● SMPS
● UPS

Package: V1-B-Pack

● Isolation Voltage: 3600 V~
● Industry standard outline
● RoHS compliant
● Soldering pins for PCB mounting
● Height: 17 mm
● Base plate: DCB ceramic
● Reduced weight
● Advanced power cycling

Data according to IEC 60747and per semiconductor unless otherwise specified   20140310e

Rectifier | Ratings

Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	T_{VJ} = 25°C				1700	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	T_{VJ} = 25°C				1600	V
$I_{R/D}$	reverse current, drain current	$V_{R/D}$ = 1600 V	T_{VJ} = 25°C			300	μA
		$V_{R/D}$ = 1600 V	T_{VJ} = 125°C			5	mA
V_T	forward voltage drop	I_T = 15 A	T_{VJ} = 25°C			1.12	V
		I_T = 45 A				1.47	V
		I_T = 15 A	T_{VJ} = 125°C			1.07	V
		I_T = 45 A				1.52	V
I_{DAV}	bridge output current	T_C = 100°C	T_{VJ} = 125°C			45	A
		rectangular d = ⅓					
V_{T0}	threshold voltage } for power loss calculation only		T_{VJ} = 125°C			0.85	V
r_T	slope resistance					15	mΩ
R_{thJC}	thermal resistance junction to case					0.6	K/W
R_{thCH}	thermal resistance case to heatsink				1.00		K/W
P_{tot}	total power dissipation	T_C = 25°C				100	W
I_{TSM}	max. forward surge current	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			320	A
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			345	A
		t = 10 ms; (50 Hz), sine	T_{VJ} = 125°C			270	A
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			295	A
I^2t	value for fusing	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			510	A²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			495	A²s
		t = 10 ms; (50 Hz), sine	T_{VJ} = 125°C			365	A²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			360	A²s
C_J	junction capacitance	V_R = 400 V f = 1 MHz	T_{VJ} = 25°C		16		pF
P_{GM}	max. gate power dissipation	t_P = 30 μs	T_C = 125°C			10	W
		t_P = 300 μs				1	W
P_{GAV}	average gate power dissipation					0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	T_{VJ} = 125°C; f = 50 Hz repetitive, I_T = 45 A				150	A/μs
		t_P = 200 μs; di_G/dt = 0.3 A/μs;					
		I_G = 0.3A; V_D = ⅔ V_{DRM} non-repet., I_T = 15 A				500	A/μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	V_D = ⅔ V_{DRM}	T_{VJ} = 125°C			1000	V/μs
		R_{GK} = ∞; method 1 (linear voltage rise)					
V_{GT}	gate trigger voltage	V_D = 6 V	T_{VJ} = 25°C			1	V
			T_{VJ} = -40°C			1.2	V
I_{GT}	gate trigger current	V_D = 6 V	T_{VJ} = 25°C			65	mA
			T_{VJ} = -40°C			80	mA
V_{GD}	gate non-trigger voltage	V_D = ⅔ V_{DRM}	T_{VJ} = 125°C			0.2	V
I_{GD}	gate non-trigger current					5	mA
I_L	latching current	t_p = 30 μs	T_{VJ} = 25°C			150	mA
		I_G = 0.3A; di_G/dt = 0.3 A/μs					
I_H	holding current	V_D = 6 V R_{GK} = ∞	T_{VJ} = 25°C			100	mA
t_{gd}	gate controlled delay time	V_D = ½ V_{DRM}	T_{VJ} = 25°C			2	μs
		I_G = 0.3A; di_G/dt = 0.3 A/μs					
t_q	turn-off time	V_R = 100 V; I_T = 15 A; V_D = ⅔ V_{DRM} T_{VJ} = 125°C			150		μs
		di/dt = 10 A/μs; dv/dt = 20 V/μs; t_p = 300 μs					

Package   V1-B-Pack

Symbol	Definition	Conditions		min.	typ.	max.	Unit
I$_{RMS}$	RMS current	per terminal				100	A
T$_{VJ}$	virtual junction temperature			-40		125	°C
T$_{op}$	operation temperature			-40		100	°C
T$_{stg}$	storage temperature			-40		125	°C
Weight					30		g
M$_D$	mounting torque			2		2.5	Nm
d$_{Spp/App}$	creepage distance on surface | striking distance through air	terminal to terminal		6.0			mm
d$_{Spb/Apb}$		terminal to backside		12.0			mm
V$_{ISOL}$	isolation voltage	t = 1 second	50/60 Hz, RMS; I$_{ISOL}$ ≤ 1 mA	3600			V
		t = 1 minute		3000			V

Ratings

Date Code   Prod. Index

IXYS **RU**   yywwA
Part Number (Typ)
Lot No.:

Data Matrix: *Typ* (1-19), DC+*Prod.Index* (20-25), *FKT#* (26-31)
leer (33), *lfd.#* (33-36)

Ordering	Part Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	VVZ40-16io1	VVZ40-16io1	Box	5	466379

Equivalent Circuits for Simulation   *on die level*   T$_{VJ}$ = 125 °C

I → (V$_0$) — [R$_0$] —   **Thyristor**
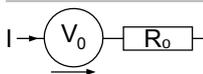
V$_{0 max}$	threshold voltage	0.85	V
R$_{0 max}$	slope resistance *	12.5	mΩ

IXYS reserves the right to change limits, conditions and dimensions.   Data according to IEC 60747and per semiconductor unless otherwise specified   20140310e

Outlines   V1-B-Pack

2

31

10

2

ca. 0.25

35 x 26

Kühlfläche
cooling area

38.6

14

14

5 • 5

11

11

5.3

1

2

3

4

5

6

7

8

0.5

27.2

31.6

5.3

1.6

48

63
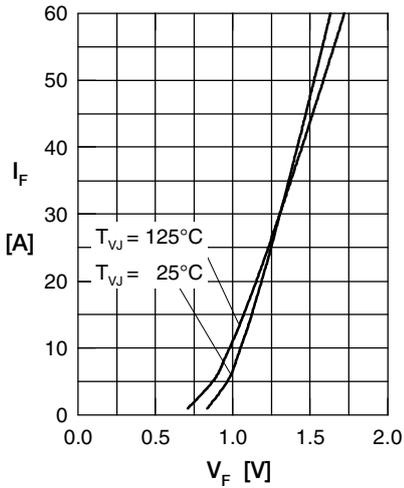
8

4

7

5

2

1

6

3
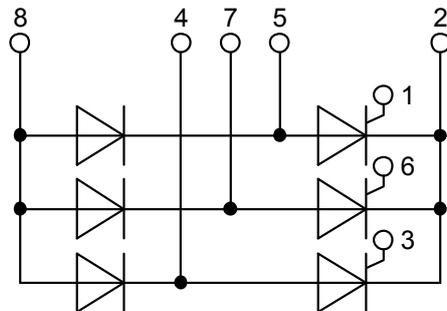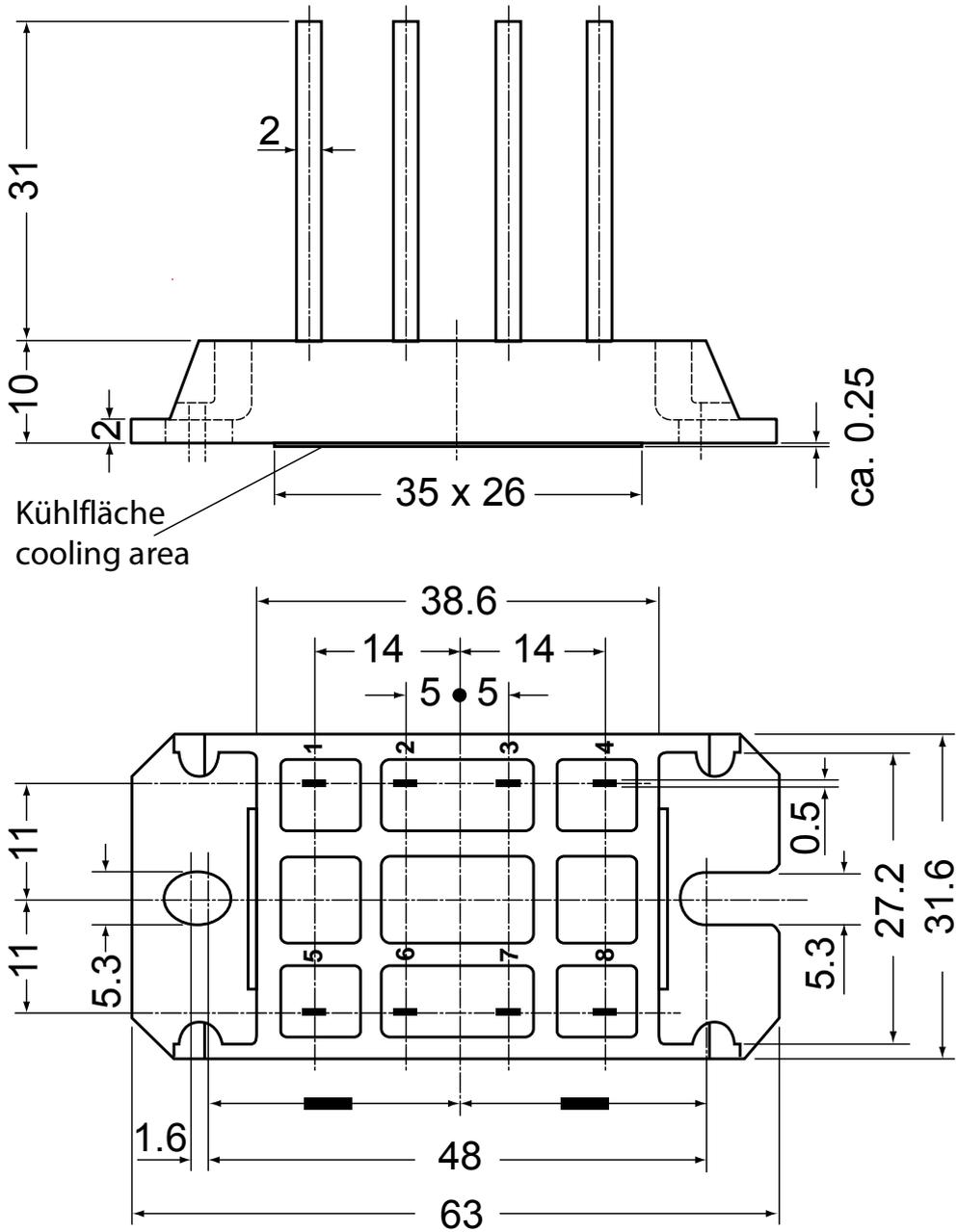
Thyristor

Fig. 1 Forward current vs.
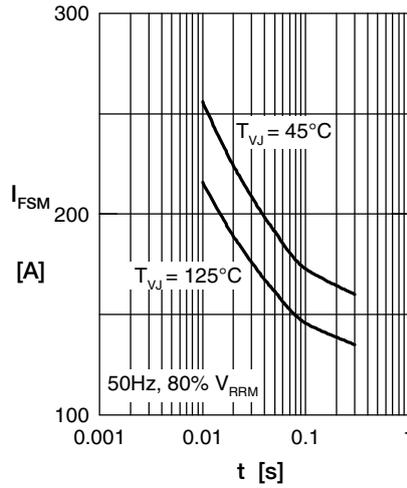voltage drop per thyristor

Fig. 2 Surge overload current
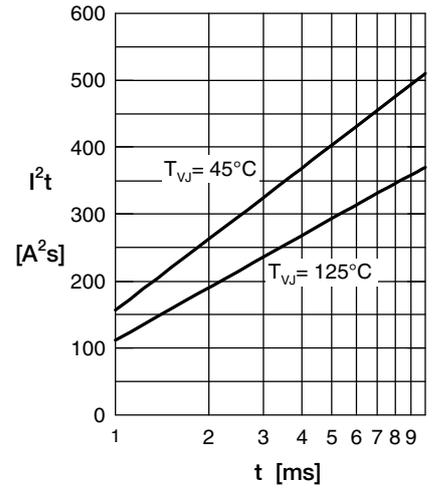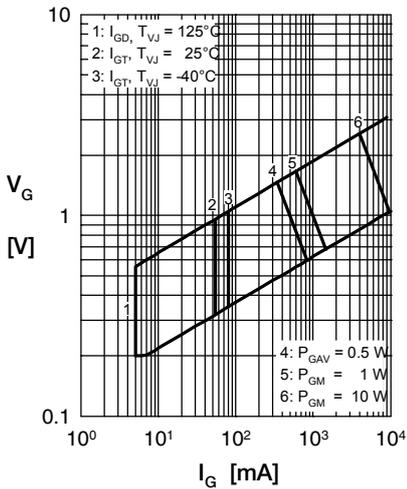vs. time per thyristor

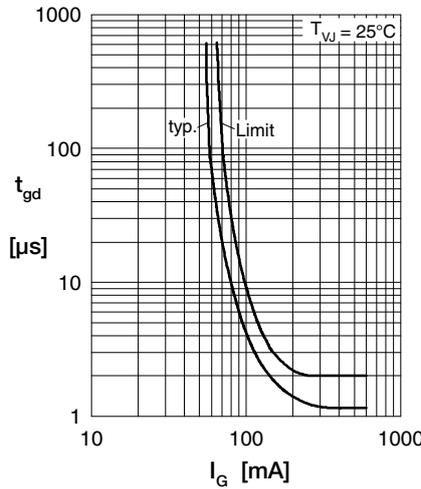Fig. 3 I^2t vs. time per thyristor

Fig. 4 Gate trigger characteristics

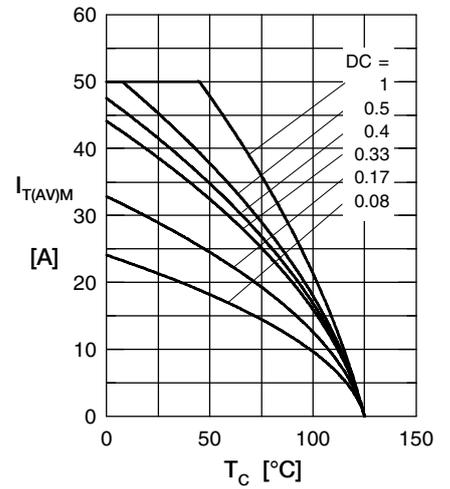Fig. 5 Gate trigger delay time

Fig. 5 Max. forward current vs.
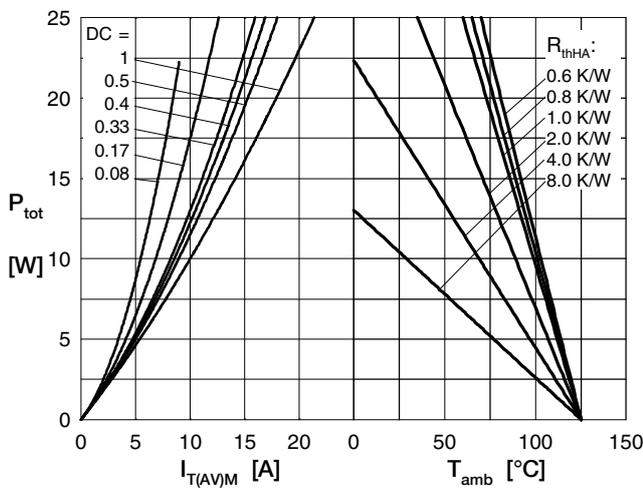case temperature per thyristor

Fig. 4 Power dissipation vs. forward current
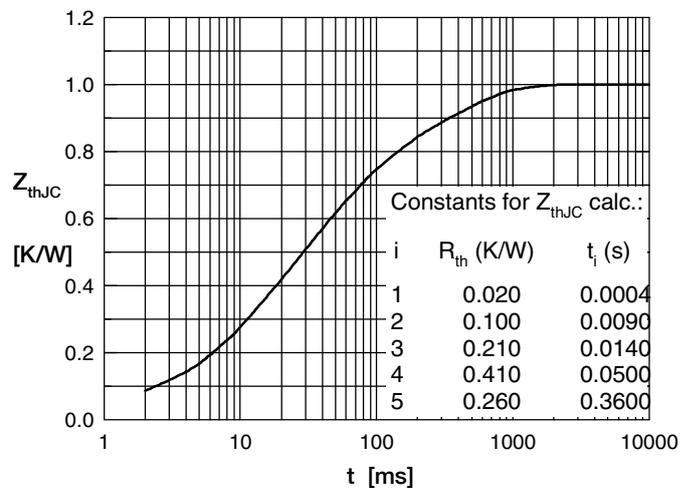and ambient temperature per thyristor

Fig. 6 Transient thermal impedance junction to case
vs. time per thyristor

i	R_{th} (K/W)	t_i (s)
1	0.020	0.0004
2	0.100	0.0090
3	0.210	0.0140
4	0.410	0.0500
5	0.260	0.3600

Constants for Z_{thJC} calc.: