REVISIONS			
REV DATE	ZONE	DESCRIPTION	APPVD
1/26/01		NR	

I. DESCRIPTION:

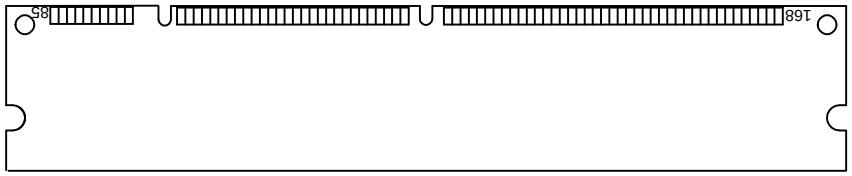
- W9Q308647PA-222 is a 8Mx64 industry standard 168-pin PC-100 SDRAM DIMM
- Manufactured with 4 8Mx16 400-mil TSOPII-54 100MHz Synchronous DRAM devices
- Requires 3.3V+/-0.3V power supply
- Inputs & outputs are LVTTL compatible
- Supports auto and self refresh modes
- Uses PC100-compliant SDRAMs
- Uses 4K refresh cycles (12/11/2 row/column/bank addressing) in 64ms
- Supports Burst Mode operation of burst length: 1, 2, 4,and 8
- With serial presence detect EEPROM
- All contacts are gold plated

III. TIMING

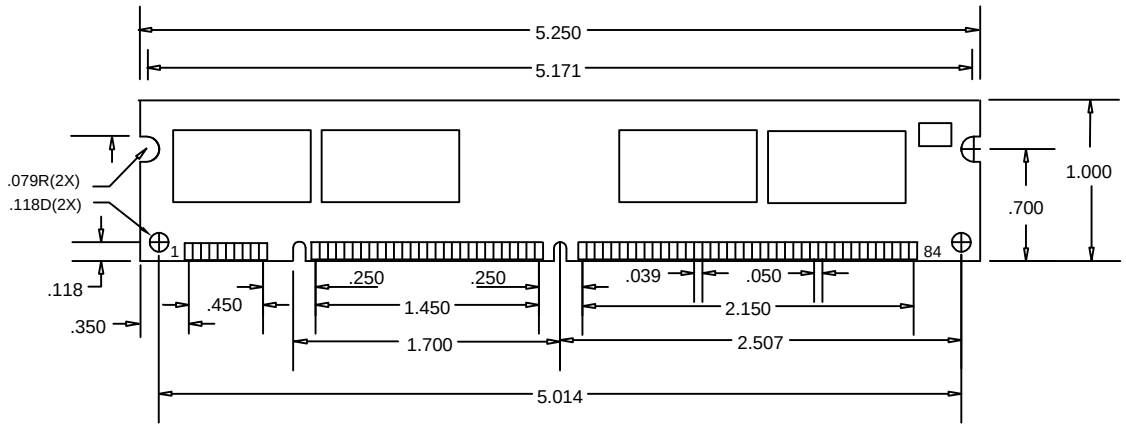
TYPE	CL=2	CL=3
Clock Cycle Time: (min)	10ns	10ns
Clock Frequency: (max)	100MHz	100MHz
Access Time From Clock: (max)	6ns	6ns
Command Setup Time: (min)	2ns	2ns
Command Hold Time: (min)	1ns	1ns

II. MECHANICAL LAYOUT:

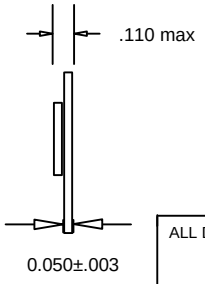
BACK



FRONT



SIDE



ALL DIMENSIONS IN INCHES ZD064M26H	**WINTEC INDUSTRIES** **8X64 PC-100 SDRAM DIMM SPECIFICATION** **W9Q308647PA-222**	
APPROVALS / DATE		
DRAW	SCALE NONE / SIZE A	DRAWINGS NO. AW9Q308647PA-222
CHECKED		
REV	DO NOT SCALE DRAWINGS	SHEET 1 OF 5

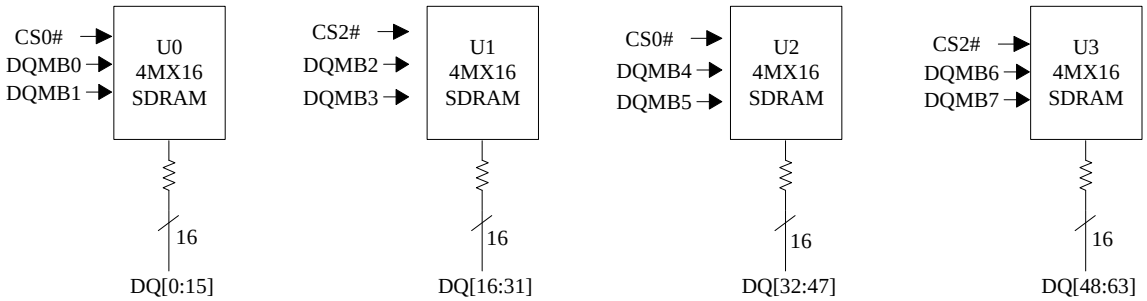
IV. PINOUT:

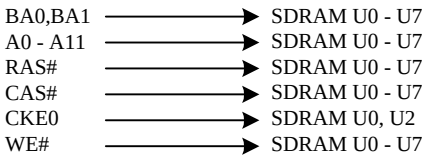
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VSS	29	DQMB1	57	DQ18	85	VSS	113	DQMB5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	CS1#	142	DQ51
3	DQ1	31	NC	59	VCC	87	DQ33	115	RAS#	143	VCC
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VCC	34	A2	62	NC	90	VCC	118	A3	146	NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VCC	68	VSS	96	VSS	124	VCC	152	VSS
13	DQ9	41	VCC	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	NC	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	VCC	101	DQ45	129	CS3#	157	VCC
18	VCC	46	DQMB2	74	DQ28	102	VCC	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	NC	160	DQ62
21	NC	49	VCC	77	DQ31	105	NC	133	VCC	161	DQ63
22	NC	50	NC	78	VSS	106	NC	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	RSVD	109	NC	137	NC	165	SA0
26	VCC	54	VSS	82	SDA	110	VCC	138	VSS	166	SA1
27	WE#	55	DQ16	83	SCL	111	CAS#	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	VCC	112	DQMB4	140	DQ49	168	VCC

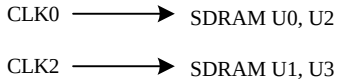
V. PIN NAMES:

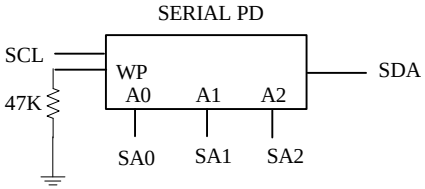
SYMBOL	DESCRIPTION
A0-A11	Address Inputs
BA0, BA1	Bank Selects
DQ0-DQ63	Data Inputs/Outputs
CS#	Chip Select
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	Outputs Disable/Write Mask
CLK0-3	Clock Input
CKE0	Clock Enable
SDA	Serial Data for PD
SCL	Clock for PD
SA0-2	Address for PD
RSVD	Reserved for future use
VCC	Power (+3.3V)
VSS	Ground
NC	No Connection

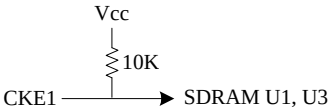
FUNCTIONAL DIAGRAM

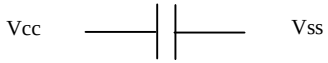












Decoupling capacitors to all SDRAMs

Note: 1. Unless otherwise noted, resistor values are 10 ohms.

WINTEC INDUSTRIES		
SPECIFICATION W9Q308647PA-222		
SCALE NONE	SIZE A	DRAWINGS NO. AW9Q308647PA-222
DO NOT SCALE DRAWINGS	SHEET 3 OF 5	

Absolute Maximum Ratings

Item	Ratings	Unit
Voltage on any pin relative to Vss	-1 to +4.6	V
Power Dissipation	4	W
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C
Short Circuit Output Current	50	mA

Recommended DC Operating Conditions

(T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	3.0	Vcc+0.3	V
Input Low Voltage	V_{IL}	-0.5	0	0.8	V

DC Characteristics

(Vcc = 3.3V±0.3V, Vss = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit	Note
Operating Current (One Bank Active)	Icc1	t_{RC}=t_{RC}min., t_{CK}=t_{CK}min. Active-precharge command cycling, w/o burst operation		-	440	mA	1
Precharge Standby Current In power-down mode	I_{CC2}P	CS# = V_{IH} (min.), CKE ≤ V_{IL}(max)	t_{CK} = min.	-	6	mA	
	I_{CC2}PS		t_{CK} = Infinity	-	4	mA	
Precharge Standby Current In non power-down mode	I_{CC2}	CS# = V_{IH} (min.), CKE ≥ V_{IH}(min)	t_{CK} = min.	-	100	mA	
	I_{CC2}S		t_{CK} = Infinity	-	10	mA	
No Operating Current	I_{CC3}	t_{CK} = min., CS# = V_{IH}(min), active state (max. 4 banks)	CKE ≥ V_{IH}(min.)	-	280	mA	
	I_{CC3}P		CKE ≤ V_{IL}(max.) (Power down mode)	-	32	mA	
Burst Operating Current	I_{CC4}	t_{CK} = min., Read/Write command cycling		-	620	mA	1
Auto Refresh Current	I_{CC5}	t_{CK} = min., Auto Refresh command cycling		-	520	mA	
Self Refresh Current	I_{CC6}	Self Refresh Mode, CKE = 0.2V		-	8	mA	
Output logic high voltage	V_{OH}	I_{OH} = -2mA		2.4	-	V	
Output logic low voltage	V_{OL}	I_{OL} = 2mA		-	0.4	V	
Input leakage current	I_{IL}	0V ≤ Vin ≤ Vcc + 0.3V		-10	10	uA	
Output leakage current	I_{OL}	0V ≤ Vout ≤ Vcc + 0.3V, Dout = Disable		-10	10	uA	

Note: 1. Measured with outputs open.

Capacitance

(T_A = 0 to 70 °C, Vcc = 3.3V±0.3V, f = 1 MHz)

Parameter	Symbol	Max	Unit
Input capacitance (A0-A11, BA0, BA1, RAS#, CAS#, WE#)	C_{I1}	23	pF
Input capacitance (CS0#,CS2#)	C_{I2}	13	pF
Input capacitance (CLK0,CLK2)	C_{I3}	13	pF
Input capacitance (CKE0, CKE1)	C_{I4}	11	pF
Input capacitance (DQMB0-DQMB7)	C_{I5}	8	pF
I/O capacitance (DQ0-DQ63)	C_{IO1}	9.5	pF
Input capacitance (SA0-SA2, SCL)	C_{S1}	8	pF
I/O capacitance (SDA)	C_{S2}	10	pF

AC Characteristics (note 1)

(T_A = 0 to +70 °C, Vcc = 3.3V±0.3V, Vss = 0V)

Parameter		Symbol	Min	Max	Unit	Note
Clock and Clock Enable						
System Frequency	CAS# Latency =3	f_{CK}	-	100	MHz	
	CAS# Latency =2		-	100	MHz	
Clock Cycle Time	CAS# Latency =3	t_{CK}	10	-	ns	
	CAS# Latency =2		10	-	ns	
Access Time from Clock	CAS# Latency =3	t_{AC}	-	6	ns	2
	CAS# Latency =2		-	6	ns	
Clock High Pulse Width		t_{CH}	3	-	ns	
Clock Low Pulse Width		t_{CL}	3	-	ns	
Transition time		t_T	1	-	ns	
Setup and Hold Times						
Command Setup Time		t_{CS}	2	-	ns	3
Address Setup Time		t_{AS}	3	-	ns	3
Data In Setup Time		t_{DS}	3	-	ns	3
CKE Setup Time		t_{CKS}	2	-	ns	3
CKE Setup Time (Self Refresh exit)		t_{CKSR}	10	-	ns	3
Command Hold Time		t_{CH}	1	-	ns	3
Address Hold Time		t_{AH}	1	-	ns	3
Data In Hold Time		t_{DH}	1	-	ns	3
CKE Hold Time		t_{CKH}	1	-	ns	3
Common Parameters						
Row to Column Delay Time		t_{RCD}	20	-	ns	4
Row Active Time		t_{RAS}	45	-	ns	4
Row Cycle Time		t_{RC}	70	120K	ns	4
Row Precharge Time		t_{RP}	20	-	ns	4
Activate(a) to Activate(b) Command period		t_{RRD}	16	-	ns	4
CAS#(a) to CAS#(b) Command period		t_{CCD}	1	-	CLK	
Mode Register Set-up time		t_{RSC}	20	-	ns	
Power Down Mode Entry Time		t_{SB}	0	10	ns	

Parameter	Symbol	Min	Max	Unit	Note
Refresh Cycle					
Refresh Period (4096 cycles)	t_{REF}	-	64	ms	
Self Refresh Exit Time	t_{SREX}	10	-		5
Read Cycle					
Data Out Hold Time	t_{OH}	3	-	ns	
Data Out to Low Impedance Time	t_{LZ}	0	-	ns	
Data Out to High Impedance Time	t_{HZ}	3	8	ns	6
DQM Data Out Disable Latency	t_{DQZ}	2	-	CLK	
Write Cycle					
Write Recovery Time	t_{WR}	8	-	CLK	
DQM Write Mask Latency	t_{DQW}	0	-	CLK	

Note:

1. AC timing tests have V_{IL} = 0.4V and V_{IH} = 2.4V with the timing referenced to the 1.4V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1ns.
2. If clock rising time is longer than 1ns, a time ($t_T/2 - 0.5$) ns has to be added to this parameter.
3. If t_T is longer than 1ns, a time (t_T-1) ns has to be added to this parameter.
4. These parameters account for the number of clock cycles and depend on the operating frequency of the clock as follows:
   the number of clock cycle = specified value of timing period
5. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
6. In reference to the time which the output achieves the open circuit condition, not to output voltage levels.