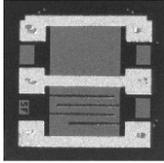


Thin Film, Center-Tapped Resistor



Product may not be to scale

The CTA series resistor chips combine the best tolerances, stability and low shunt capacitance. The CTA offers the designer flexibility in use as either a single value resistor or as two resistors with a center tap feature. The CTAs six bonding pads allows the user increased layout flexibility. The CTAs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTAs are 100 % electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

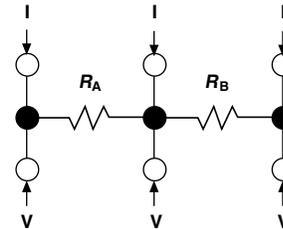
The CTA center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, low shunt capacitance and tracking between two resistors is critical.

Recommended for hermetic environments where chip is not exposed to moisture.

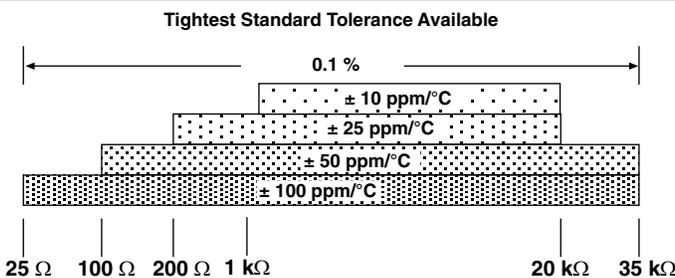
For lower values, the resistance of the six bonding-pad configurations can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four-wire Kelvin technique. The measuring method is illustrated in the diagram to the right.

FEATURES

- Wire bondable
- Center tap feature
- Tight ratio tolerances to: $\pm 0.1\%$
- Chip size: 0.030 inches square
- Resistance range total: $25\ \Omega$ to $35\ k\Omega$
- Alumina substrate, low shunt capacitance: $< 0.2\ pF$
- Resistor material nichrome
- Excellent stability: $\pm 0.025\%$ maximum $\Delta R/R$



TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



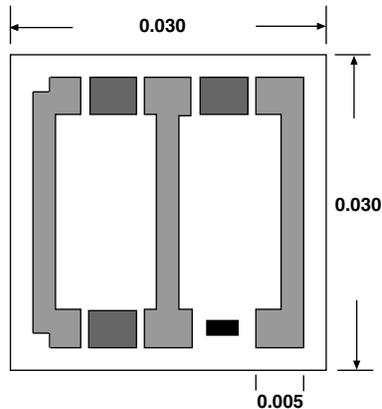
PROCESS CODE	
CLASS H*	CLASS K*
203	233
202	232
200	230
201	231

*MIL-PRF-38534 inspection criteria

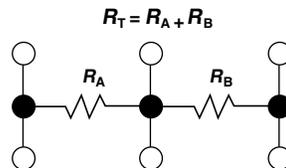
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR Tracking Between Halves (R_A/R_B)	$\pm 2\ ppm/^\circ C^*$
Center Tap Ratio, R_A/R_B : Tolerance	$1 \pm 1\%$ standard
Noise, MIL-STD-202, Method 308	- 35 dB typ.
Moisture Resistance, MIL-STD-202, Method 106, (Passivated only)	$\pm 0.5\%$ max. $\Delta R/R$
Stability, 1000 h, + 125 °C, 62 mW	$\pm 0.025\%$ max. $\Delta R/R$
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	$\pm 0.1\%$ max. $\Delta R/R$
High Temperature Exposure, + 150 °C, 100 h	$\pm 0.1\%$ max. $\Delta R/R$
Insulation Resistance	10^{12} min.
Operating Voltage	100 V max.
DC Power Rating at + 70 °C (Derated to Zero at + 150 °C)	125 mW
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	$\pm 0.25\%$ max. $\Delta R/R\%$

*10ppm/°C for $R < 100$

DIMENSIONS in inches

STANDARD CONFIGURATION

*Six locations. All pads 0.005 x 0.005

SCHEMATIC


MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.050 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	99.6 % alumina
Resistor Material	Nichrome
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127 mm)
Number of Pads	6
Pad Material	25 kÅ minimum gold
Backing	None

Options: Aluminum bonding pads, 10 kÅ minimum
 Center-tap ratio tolerances to 0.02 % $R > 1$ kΩ
 Consult Applications Engineer

ORDERING INFORMATION					
Example: 100% visual, 10 kΩ, ± 1 %, ± 100 ppm/°C TCR, gold pads, class H visual inspection					
W INSPECTION/ PACKAGING	CTA PRODUCT FAMILY	201 PROCESS CODE	1000 RESISTANCE VALUE	1 MULTIPLIER CODE	F TOLERANCE CODE
W = 100 % visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4 % AQL)		See Process Code table	Use first 4 digits significant digits of the resistance (R_T)	B = 0.01 A = 0.1 0 = 1 1 = 10	A = 0.05 % B = 0.1 % C = 0.2 % D = 0.5 % F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 %



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