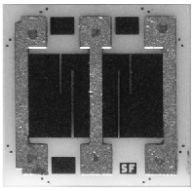
Thin Film, Center-Tapped Resistors



Product may not be to scale

The CTT series resistor chips offer a combination of low shunt capacitance and excellent stability. The CTT offers the designer flexibility in use as either a single value resistor or as two resistor with a center tap feature.

The CTTs six bonding pads allows the user increased layout flexibility. The CTTs tantalum nitride resistor material offers excellent resistance to high moisture environments.

The CTTs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTTs are 100 % electrically tested and visually inspected to MIL-STD-883.

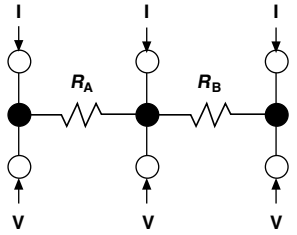
APPLICATIONS

The CTT center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, tracking, low shunt capacitance and better frequency response are necessary.

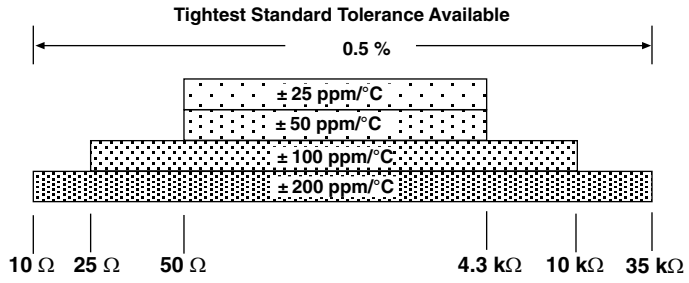
Vishay EFI measures low-value resistors by the four-wire kelvin technique.

FEATURES

- Wire bondable
- Center tap feature
- Chip size: 0.030 inches square
- Resistance range R_T: 10 Ω to 36 kΩ
- Alumina substrate, low shunt capacitance: < 0.2 pF
- Resistor material: Tantalum nitride
- Moisture resistant



TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
202	207
200	205
201	206
204	209

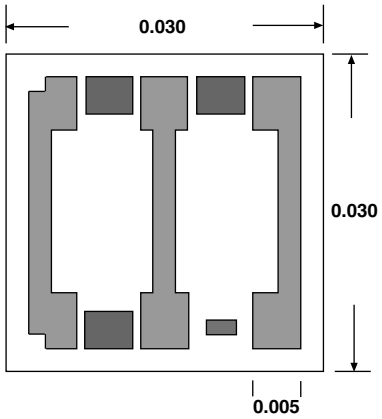
*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
TCR Tracking Between Halves (R_A/R_B)	± 2 ppm/°C*
Center Tap Ratio, R_A/R_B: Tolerance	1 ± 1 %
Noise, MIL-STD-202, Method 308	- 35 dB typ.
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 % max. ΔR/R
Stability, 1000 h, + 125 °C, 62 mW	± 0.25 % max. ΔR/R
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 % max. ΔR/R
High Temperature Exposure, + 150 °C, 100 h	± 0.2 % max. ΔR/R
Insulation Resistance	10^{12} min.
Operating Voltage	100 V max.
DC Power Rating at + 70 °C (Derated to Zero at + 150 °C)	125 mW
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 % max. ΔR/R %

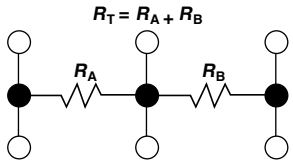
*10 ppm/°C for R < 100

DIMENSIONS in inches



STANDARD CONFIGURATION
*Six locations. All pads 0.005 x 0.005

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.050 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	99.6 % alumina
Resistor Material	Tantalum nitride
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127 mm)
Number of Pads	6
Pad Material	25 kÅ minimum gold
Backing	None

Options: Alphanumeric part marking, up to six characters
Aluminum bonding pads, 10 kÅ minimum
Consult Applications Engineer

ORDERING INFORMATION

Example: 100 % visual, 10 kΩ, ± 1 %, ± 100 ppm/°C TCR, gold pads, class H visual inspection

W	**CTT**	**201**	**1000**	**1**	**F**
INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100 % visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4 % AQL)		See Process Code table	Use first 4 digits significant digits of the resistance (R_T)	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000 **4** = 10 000	**D** = 0.5 % **F** = 1.0 % **G** = 2.0 % **H** = 2.5 % **J** = 5.0 % **K** = 10 % **M** = 20 % **L** = 25 %

Disclaimer

All product specifications and data are subject to change without notice.

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