WM8783

Stereo Low Power 96kHz ADC

DESCRIPTION

The WM8783 is a compact, low cost ADC designed for set-top boxes and DVD applications.

Stereo analogue inputs accept 1Vrms line level inputs; the Hi-Fi ADCs output 24-bit stereo data on the I2S digital audio interface.

Sample rates from 8kHz to 96kHz are supported; this is configured automatically according to the external master clock (MCLK) frequency.

A power on reset (POR) circuit ensures correct start-up and shut-down. The device is held in reset when MCLK is not present, offering a low-power standby state.

The WM8783 is supplied in an 8-pin SOIC package.

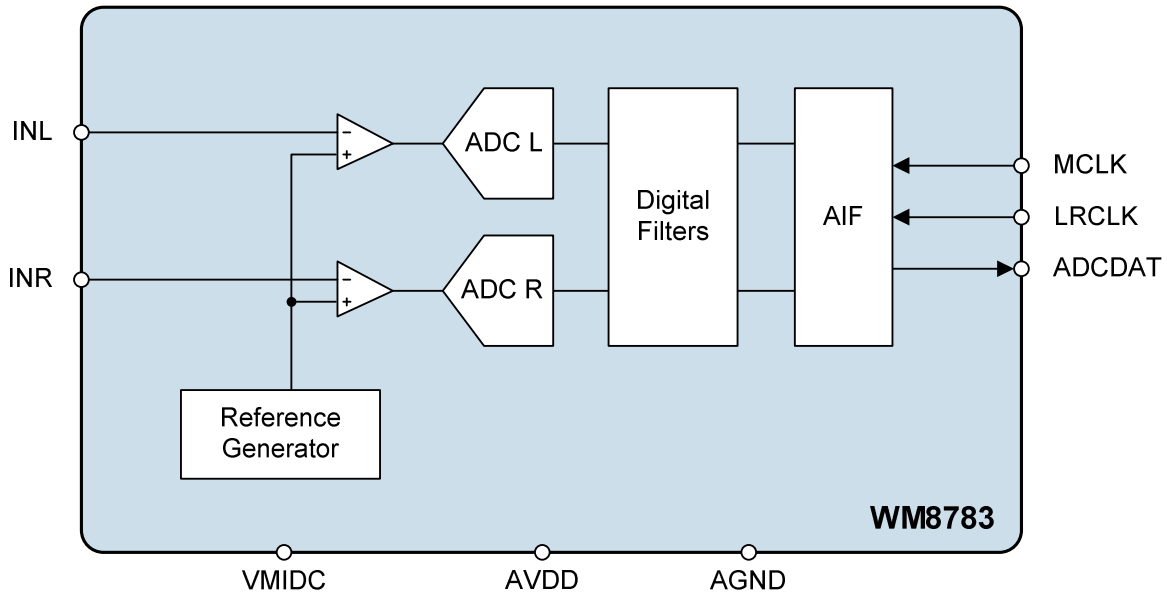
FEATURES

- Hi-fi audio ADC (96dB SNR - 'A' weighted)
- 2 analogue audio inputs
- I2S digital audio interface - sample rates 8kHz to 96kHz
- Automatic clocking configuration from MCLK and LRCLK
- Integrated voltage reference circuits
- 8-pin SOIC package

APPLICATIONS

- LCD televisions
- Set-top boxes (STB)
- DVD recorders

BLOCK DIAGRAM



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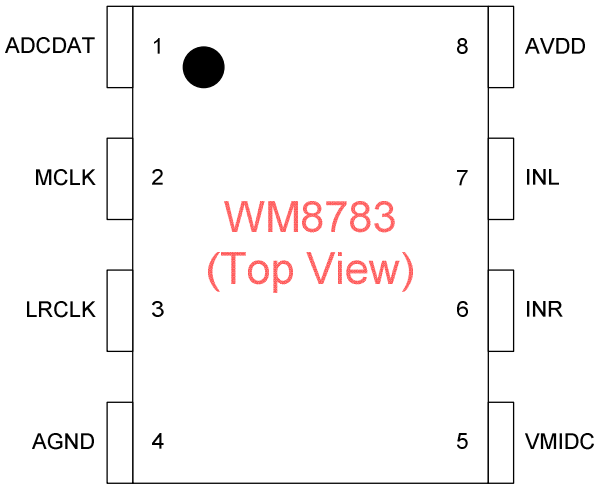
PIN CONFIGURATION

The WM8783 is supplied in a 8-pin SOIC format. The pin configuration is illustrated below, showing the top-down view from above the chip.



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8783GED/V	-40°C to +85°C	8-pin SOIC (Pb-free)	MSL3	260°C
WM8783GED/RV	-40°C to +85°C	8-pin SOIC (Pb-free, tape and reel)	MSL3	260°C

Note:
Reel quantity = 3000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	ADCDAT	Digital Output	ADC digital audio data
2	MCLK	Digital Input	Master clock
3	LRCLK	Digital Input	Audio interface left / right clock
4	AGND	Supply	Ground
5	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
6	IN1R	Analogue Input	Right channel analogue input
7	IN1L	Analogue Input	Left channel analogue input
8	AVDD	Supply	Positive supply

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltage (AVDD)	-0.3V	4.5V
Voltage range digital inputs	-0.7V	AVDD +0.7V
Voltage range analogue inputs	-0.7V	AVDD +0.7V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analogue and digital I/O supply range	AVDD	3.0	3.3	3.6	V
Ground	GND		0		V

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM8783 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND pin through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package pins to PCB (conduction).

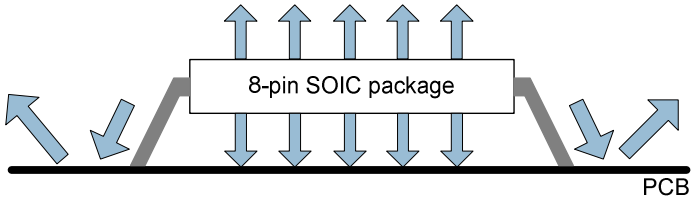


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		125	°C
Thermal Resistance	Θ_{JA}		TBD		°C/W

Note:

1. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and junction temperature limits must both be observed.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 3.3V, GND = 0V, T_A = +25°C, 1kHz signal, fs = 48kHz, MCLK = 256fs unless otherwise stated. LRCLK transition as per Figure 4.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (IN1L, IN1R)						
Maximum input signal level		Single-ended input		AVDD/3.3		Vrms
Input resistance				66		kΩ
Input capacitance				20		pF
ADC Input Path Performance (Analogue Input to ADC)						
Signal to Noise Ratio	SNR	A-weighted, fs = 48kHz		96		dB
		Unweighted, fs = 48kHz		94		
		A-weighted, fs = 96kHz		96		
		Unweighted, fs = 96kHz		94		
Total Harmonic Distortion	THD	-1dBFS input, fs = 48kHz		-83		dB
		-1dBFS input, fs = 96kHz		-83		
Channel separation (Left/Right)				85		dB
Power Supply Rejection Ratio (with respect to AVDD)	PSRR	1kHz 100mV pk-pk applied to AVDD		50		dB
Digital Inputs / Outputs						
Input high level			0.7 x AVDD			V
Input low level					0.3 x AVDD	V
Output high level		I_{OL} = 1mA	0.9 x AVDD			V
Output low level		I_{OH} = -1mA			0.1 x AVDD	V
Input capacitance				5		pF
Input leakage			-1		1	µA
Clocking						
MCLK frequency			2.048		12.288	MHz
Analogue Reference Levels						
Midrail Reference Voltage	VMID		-4%	AVDD/2	+4%	V
VMID resistance to Ground	R_{VMID}			33		kΩ
Current Consumption						
AVDD Current Consumption	I_{AVDD}	Quiescent fs = 48kHz, MCLK = 256fs		7.93		mA
		Quiescent fs = 96kHz, MCLK = 128fs		8.74		
		Quiescent No clocks applied		0.24		

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. This ratio is also called idle channel noise. (No Auto-zero or Mute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz reference sine wave output signal and the first seven harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the next seven harmonics and expressed as a ratio.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the difference in level between a 1kHz reference sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Channel Separation (L/R) (dB) – is a measure of the coupling between left and right channels. A full scale signal is applied to the left channel only, and the right channel amplitude is measured. Next, a full scale signal is applied to the right channel only, and the left channel amplitude is measured. The worst case channel separation is quoted; this is the difference in level between the full-scale output and the cross-channel output signal level, expressed as a ratio.
5. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between a power supply rail and a signal output path. With the signal path idle, a small sine wave ripple is applied to power supply rail. The amplitude of the supply ripple is compared to the amplitude of the output signal generated and is expressed as a ratio.
6. All performance measurements are carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise; although it is not audible, it may affect dynamic specification values.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

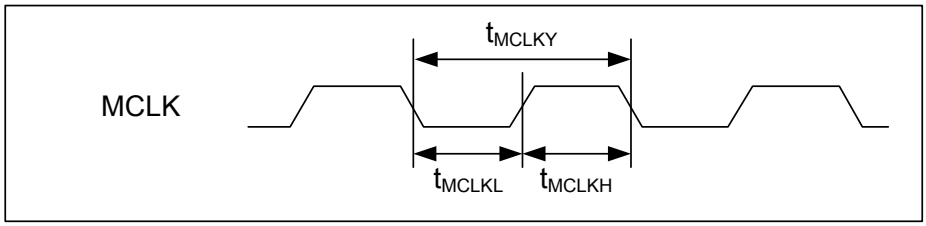


Figure 2 Master Clock Timing

Test Conditions
AVDD = 3.3V, GND = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing						
MCLK frequency	1 / T_{MCLKY}	fs = 8kHz		2.048		MHz
		fs = 16kHz		4.096		
		fs = 32kHz		8.192		
		fs = 44.1kHz		11.2896		
		fs = 48kHz		12.288		
		fs = 88.2kHz		11.2896		
		fs = 96kHz		12.288		
MCLK duty cycle (= T_{MCLKH} : T_{MCLKL})			60:40		40:60	

AUDIO INTERFACE TIMING

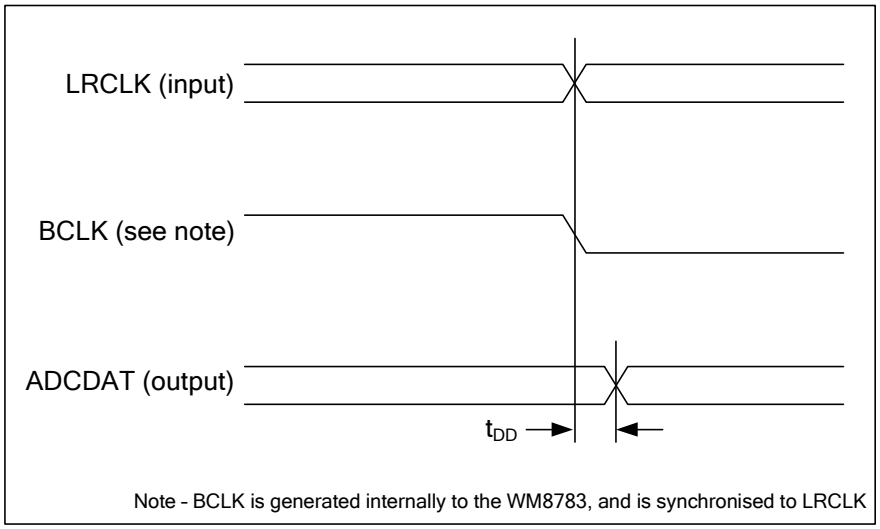


Figure 3 Audio Interface Timing

Test Conditions

AVDD = 3.3V, GND = 0V, T_A = +25°C.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing					
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns

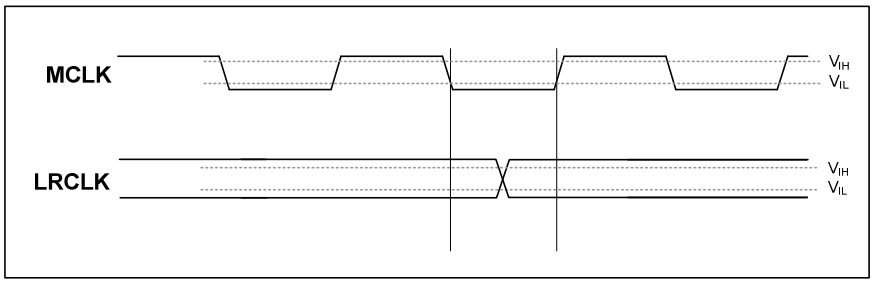


Figure 4 Recommended LRCLK Transition Area for Optimum Performance

It is recommended that for optimum performance the LRCLK transition occurs during the MCLK low, as shown in Figure 4 above.

DEVICE DESCRIPTION

INTRODUCTION

The WM8783 is a low-cost ADC designed for set-top boxes and DVD applications. It is packaged in an 8-pin SOIC.

The device comprises two analogue input pins, each accepting line signals up to 1Vrms. The signal path gain is fixed.

The stereo hi-fi ADCs operate at sample rates from 8kHz up to 96kHz. A high pass filter is provided in the ADC path for removing DC offsets and suppressing low frequency noise.

The digital audio interface supports the ADC output in stereo 24-bit I2S format. The device requires no configuration instructions and automatically selects the ADC sample rate according to the external master clock (MCLK) frequency.

The WM8783 incorporates an internal voltage reference and LDO regulator for power-efficient operation from a single AVDD power supply. External clocking is required via the MCLK and LRCLK pins.

A power on reset circuit ensures correct start-up and shut-down when AVDD is switched on or off. The WM8783 is held in reset when MCLK not present, offering a low-power standby state.

ANALOGUE-TO-DIGITAL CONVERTER (ADC)

The WM8783 has two analogue input pins, INL and INR. The maximum analogue input signal level varies with AVDD, but is typically 0dBV (1Vrms) when AVDD = 3.3V. This is suitable for single-ended connection to line level input signals.

The WM8783 uses two 24-bit sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The sample rate is set automatically according to the external clocks connected to LRCLK and MCLK. Many common sample rates from 8kHz to 96kHz are supported, as described in the “Digital Audio Interface” section.

Digital filters are also incorporated on the ADC output signal path to remove DC offsets and other unwanted noise. The cut-off frequency of the ADC high-pass filter varies with the ADC sample rate (fs), but is typically 4Hz when fs = 48kHz.

Filter response plots for the ADC high-pass filter are shown in “Digital Filter Characteristics”.

DIGITAL AUDIO INTERFACE

The digital audio interface is used for outputting ADC data from the WM8783. It uses three pins:

- ADCDAT - ADC data output
- LRCLK - Left / Right data alignment clock
- MCLK - Master clock

The WM8783 operates as a Slave device only; LRCLK and MCLK must be provided as inputs.

It is a requirement of the WM8783 digital audio interface that the bit rate of the ADCDAT data is 64fs only, where fs is the audio sample rate.

Note that the Bit Clock (BCLK) associated with the digital audio interface is configured and generated automatically within the WM8783. This allows the ADCDAT to be synchronised to the BCLK in the host processor, even though the BCLK is not connected externally to the WM8783.

The digital audio interface supports many common sample rates, as detailed in Table 1. The required MCLK frequency in each case is also noted.

The WM8783 will automatically determine the MCLK / fs ratio according to the supplied LRCLK and MCLK inputs. Note that the BCLK frequency is 64 x fs in all cases.

SAMPLE RATE	MCLK	MCLK RATIO
8kHz	2.048MHz	256 x fs
16kHz	4.096MHz	256 x fs
32kHz	8.192MHz	256 x fs
44.1kHz	11.2896MHz	256 x fs
48kHz	12.288MHz	256 x fs
88.2kHz	11.2896MHz	128 x fs
96kHz	12.288MHz	128 x fs

Table 1 Digital Audio Interface Clocking

The WM8783 supports 24-bit stereo operation in I2S digital audio format.

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition, as illustrated in Figure 5. The other bits up to the LSB are then transmitted in order.

Note that there are unused BCLK cycles between the LSB of one sample and the MSB of the next.

Note that BCLK is generated internally and is not transmitted or received externally to the WM8783.

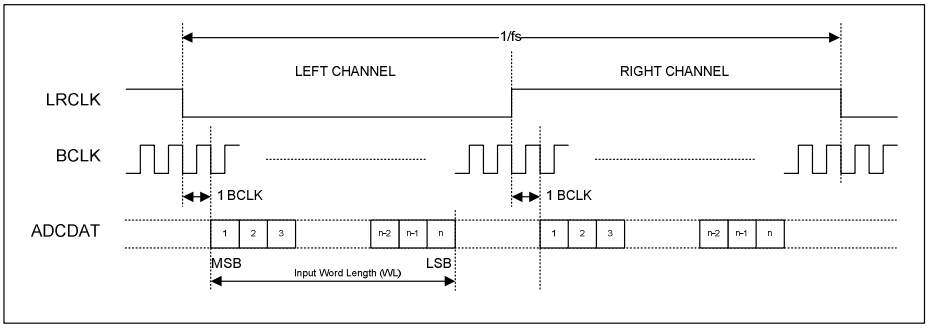


Figure 5 I^2S Digital Audio Interface format (assuming n-bit word length)

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband	+/- 0.1dB	0		0.454 fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.1	dB
Stopband		0.546s			
Stopband Attenuation	f > 0.546 fs	-60			dB
Group Delay			16.5 / fs		s

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

ADC FILTER RESPONSE

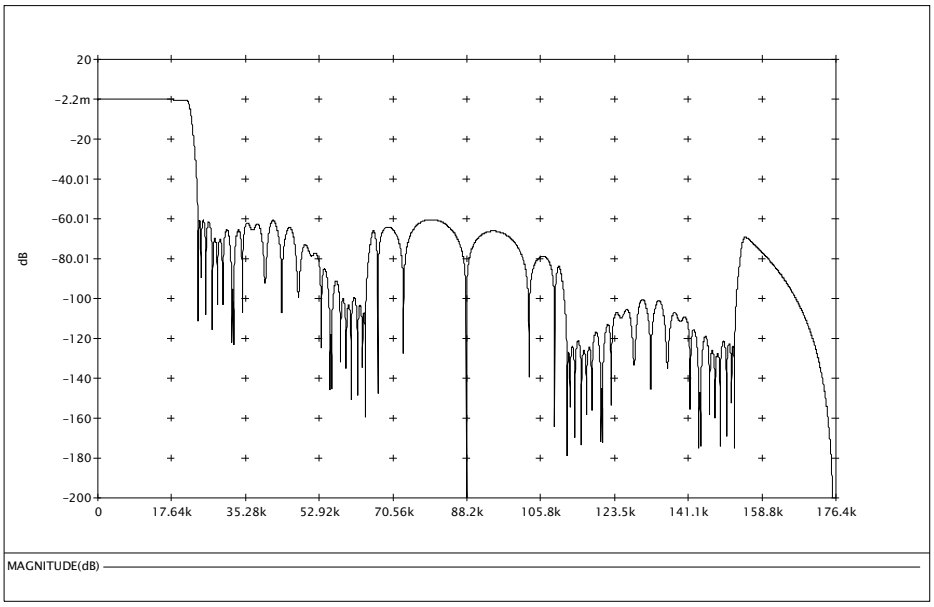


Figure 6 ADC Frequency Response up to 4 x fs (Sample rate, fs = 48kHz)

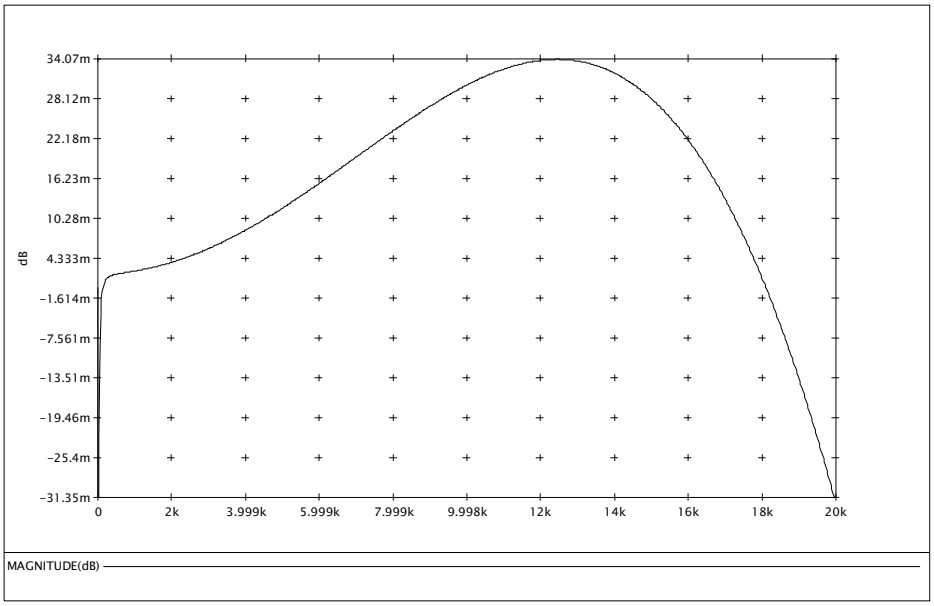


Figure 7 ADC Pass Band Frequency Response up to fs/2 (Sample rate, fs = 48kHz)

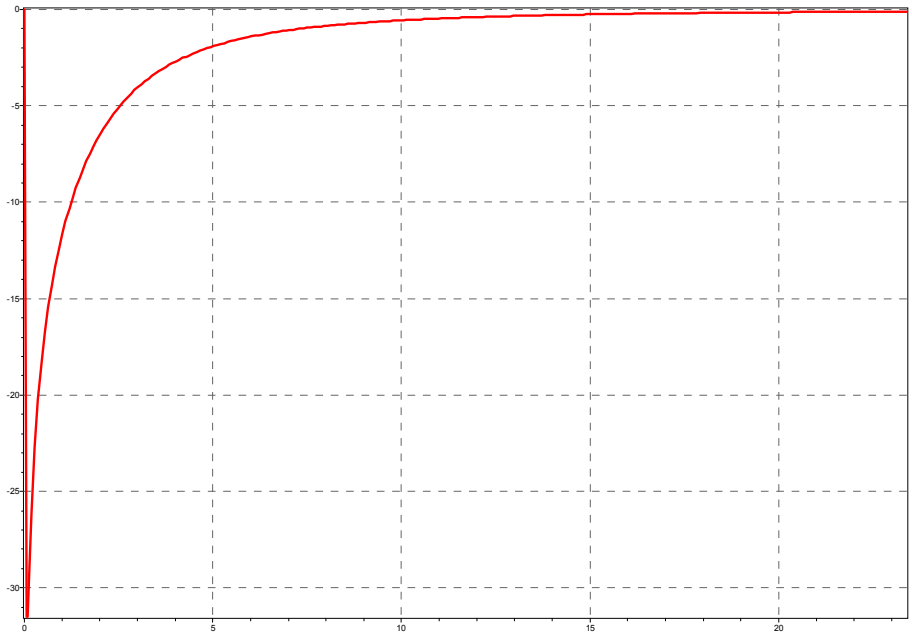


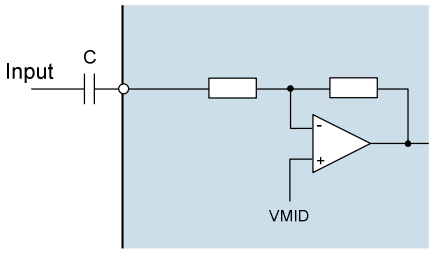
Figure 8 ADC High Pass Filter Frequency Response (Sample rate, fs = 48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

AUDIO INPUT PATHS

The WM8783 provides 2 analogue audio inputs. Each of these inputs is referenced to the internal DC reference, VMID. A DC blocking capacitor is required for each input pin. The choice of capacitor is determined by the filter that is formed between that capacitor and the input impedance of the input pin. The circuit is illustrated in Figure 9.



$$Fc = \frac{1}{2\pi RC}$$

Fc = high pass 3dB cut-off frequency

Figure 9 Audio Input Path DC Blocking Capacitor

The input impedance is noted in the "Electrical Characteristics". It is recommended that an input capacitor is selected such that the Fc cut-off frequency is less than 20Hz.

It is recommended that a 1μF capacitance is used for all WM8783 input connections. Tantalum electrolytic capacitors are particularly suitable as they offer high stability in a small package size.

See Wolfson Applications Note WAN_0176 for further guidance on the choice of capacitor types.

POWER SUPPLY DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations (or 'spikes') in the power supply voltage can cause malfunctions and unintentional behavior in other components. A decoupling (or 'bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the WM8783, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling (or 'bypass') capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply decoupling capacitors for WM8783 are listed below in Table 2.

POWER SUPPLY	DECOUPLING CAPACITOR
AVDD	4.7μF ceramic
VMIDC	4.7μF ceramic

Table 2 Power Supply Decoupling Capacitors

All decoupling capacitors should be placed as close as possible to the WM8783 device.

The VMIDC capacitor is not, technically, a decoupling capacitor. However, it does serve a similar purpose in filtering noise on the VMID reference. The connection between GND, the VMID decoupling capacitor and the main system ground should be made at a single point as close as possible to the GND ball of the WM8783.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

See Wolfson Applications Note WAN_0176 for further guidance on the choice of capacitor types.

RECOMMENDED EXTERNAL COMPONENTS DIAGRAM

Figure 10 provides a summary of recommended external components for WM8783. Note that the actual requirements may differ according to the specific target application.

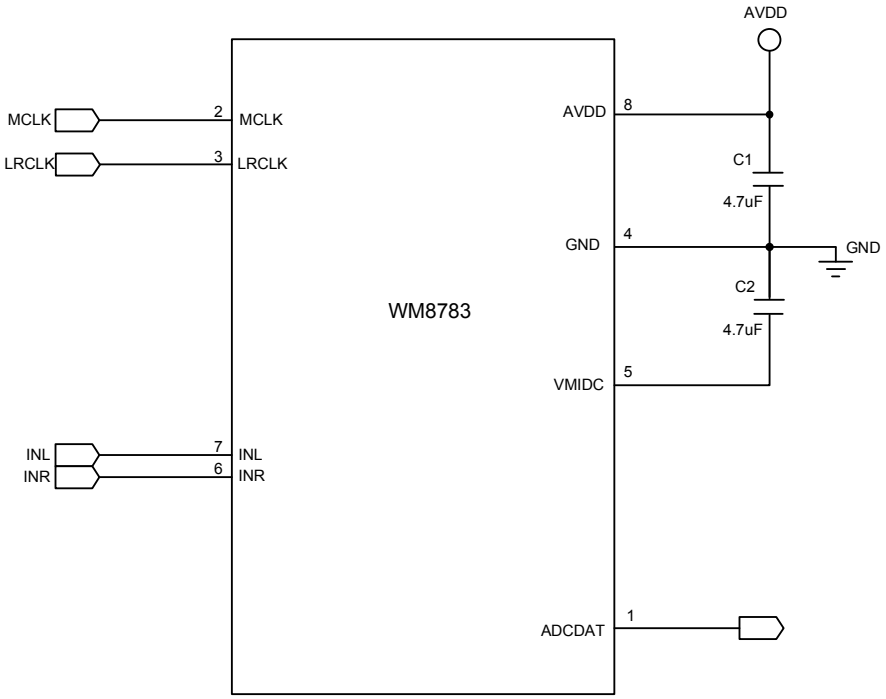


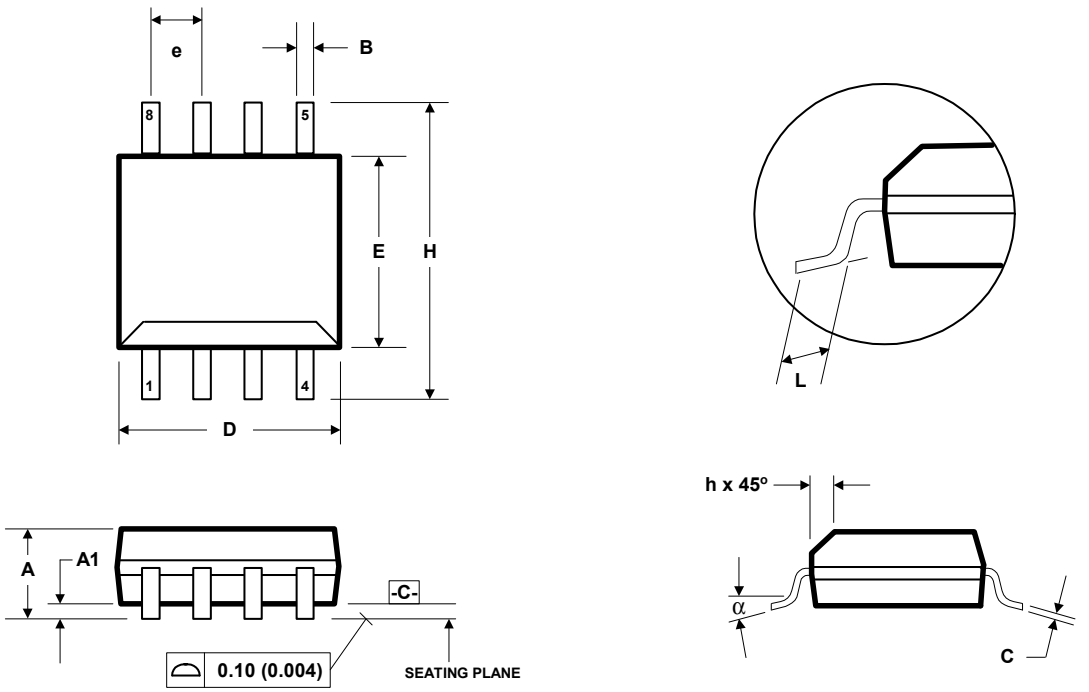
Figure 10 WM8783 Recommended External Components Diagram

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM8783 device as possible, with current loop areas kept as small as possible.

PACKAGE DIMENSIONS

D: 8 PIN SOIC 3.9mm Wide Body **DM009.B**



Symbols	Dimensions (mm)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.0532	0.0688
A_1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
D	4.80	5.00	0.1890	0.1968
e	1.27 BSC		0.050 BSC	
E	3.80	4.00	0.1497	0.1574
h	0.25	0.50	0.0099	0.0196
H	5.80	6.20	0.2284	0.2440
L	0.40	1.27	0.0160	0.0500
α	0^o	8^o	0^o	8^o
REF:	JEDEC.95, MS-012			

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D. MEETS JEDEC.95 MS-012, VARIATION = AA. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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