128Kx8 MONOLITHIC NOR FLASH, SMD 5962-96690

FEATURES

- Access Times of 50*, 60, 70, 90, 120, 150ns
- Packaging
  - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
  - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
  - 32 lead, Flatpack (Package 220)
  - 32 lead, Formed Flatpack (Package 221)
  - 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- 100,000 Erase/Program Cycles Minimum
- Sector Erase Architecture
  - 8 equal size sectors of 16KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time.

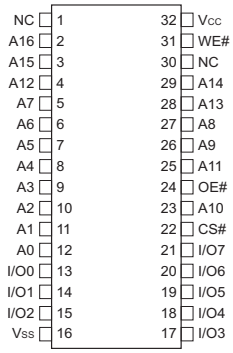
This product is subject to change without notice.

Note: For programming information refer to Flash Programming 1M5 Application Note.

* The access time of 50ns is available in Industrial and Commercial temperature ranges only.

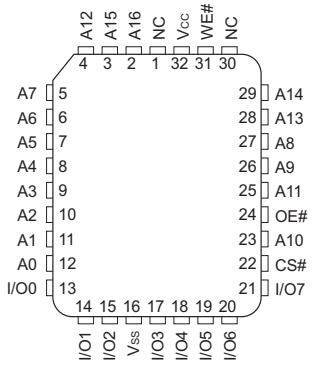
PIN CONFIGURATION FOR WMF128K8-XXX5

32 DIP
32 CSOJ
32 Flatpack
Top View



PIN CONFIGURATION FOR WMF128K8-XCLX5

32 CLCC
Top View



PIN DESCRIPTION

A0-16	Address Inputs
I/O0-7	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
Vcc	+5.0V Power
Vss	Ground

ABSOLUTE MAXIMUM RATINGS (1)

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage (V_{CC})	-2.0 to +7.0	V
Signal Voltage Range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention Mil Temp	10	years
Endurance (write/erase cycles) (Mil Temp)	10,000 min	cycles
A9 Voltage for sector protect (V_{ID}) (3)	-2.0 to +14.0	V

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to Vcc + 2.0 V for periods of up to 20ns.
3. Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot Vss to -2V for periods of up to 20ns. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C
A9 Voltage for Sector Protect	V_{ID}	11.5	12.5	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	C_{AD}	$V_{I/O}$ = 0 V, f = 1.0 MHz	15	pF
Output Enable capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	15	pF
Write Enable capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	15	pF
Chip Select capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	15	pF

This parameter is guaranteed by design but not tested.

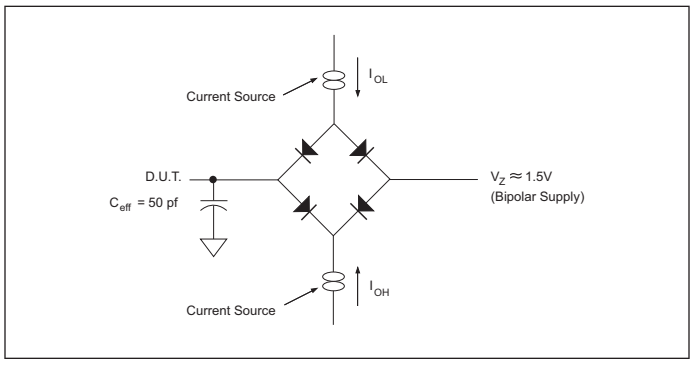
DC CHARACTERISTICS — CMOS COMPATIBLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}		35	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	CS# = V_{IL}, OE# = V_{IH}		50	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 5.5, CS# = V_{IH}, f = 5MHz		1.6	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Output High Voltage	V_{OH2}	I_{OH} = -100 µA, V_{CC} = 4.5	V_{CC} - 0.4		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2		V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	VIL = 0, VIH = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, WE# CONTROLLED

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	50		60		70		90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	25		30		35		45		50		50		ns
Address Setup Time	t_{AVWH}	t_{AS}	0		0		0		0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	25		30		30		45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		0		0		ns
Address Hold Time	t_{WHAX}	t_{AH}	40		45		45		45		50		50		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	0		0		0		0		0		0		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		20		20		20		ns
Duration of Byte Programming Operation (min)	t_{WHWH1}		14		14		14		14		14		14		µs
Sector Erase Time	t_{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		0		0		0		ms
V_{CC} Set-up Time		t_{VCS}	50		50		50		50		50		50		µs
Chip Programming Time				12.5		12.5		12.5		12.5		12.5		12.5	sec
Output Enable Setup Time		t_{OES}	0		0		0		0		0		0		ns
Output Enable Hold Time (1)		t_{OEH}	10		10		10		10		10		10		ns

NOTES:
1. For Toggle and Data# Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	50		60		70		90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		50		60		70		90		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		50		60		70		90		120		150	ns
OE# to Output Valid	t_{GLQV}	t_{OE}		25		30		35		40		50		55	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		20		25		30		35	ns
OE# High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20		20		25		30		35	ns
Output Hold from Address, CS# or OE# Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		0		0		0		ns

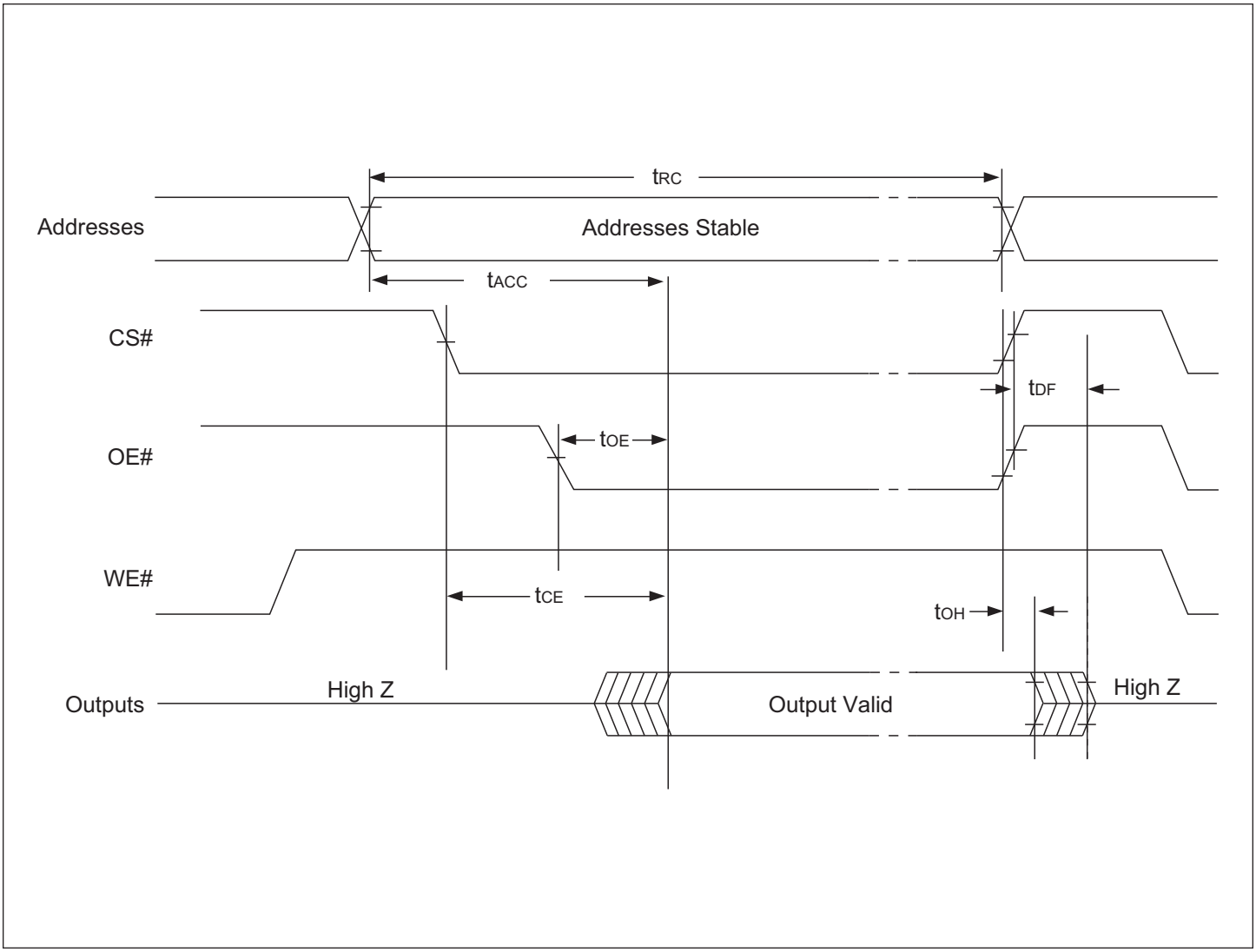
NOTES:
1. Guaranteed by design, but not tested

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,CS# CONTROLLED

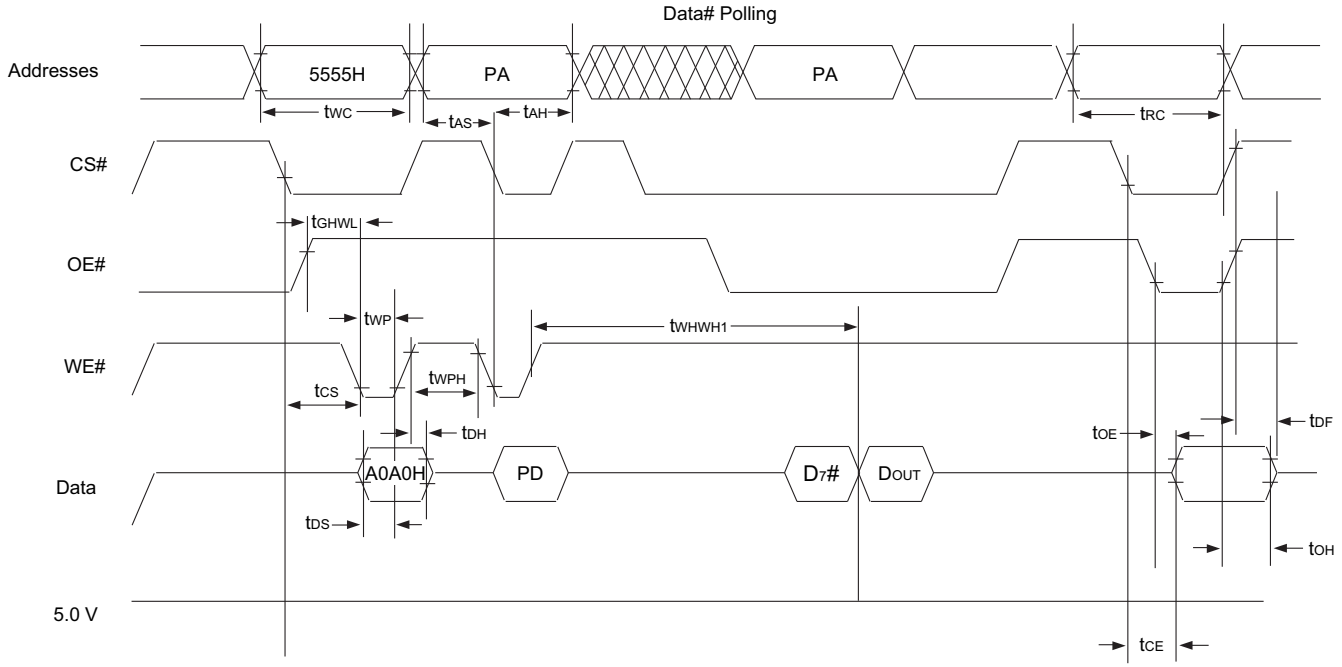
V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	50		60		70		90		120		150		ns
WE# Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		0		0		ns
CS# Pulse Width	t_{ELEH}	t_{CP}	25		30		35		45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	25		30		30		45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	40		45		45		45		50		50		ns
WE# Hold from WE# High	t_{EHWH}	t_{WH}	0		0		0		0		0		0		ns
CS# Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		20		20		20		ns
Duration of Programming Operation	t_{WHWH1}		14		14		14		14		14		14		µs
Duration of Erase Operation	t_{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery before Write	t_{GHEL}		0		0		0		0		0		0		ns
Chip Programming Time				12.5		12.5		12.5		12.5		12.5		12.5	sec

AC WAVEFORMS FOR READ OPERATIONS

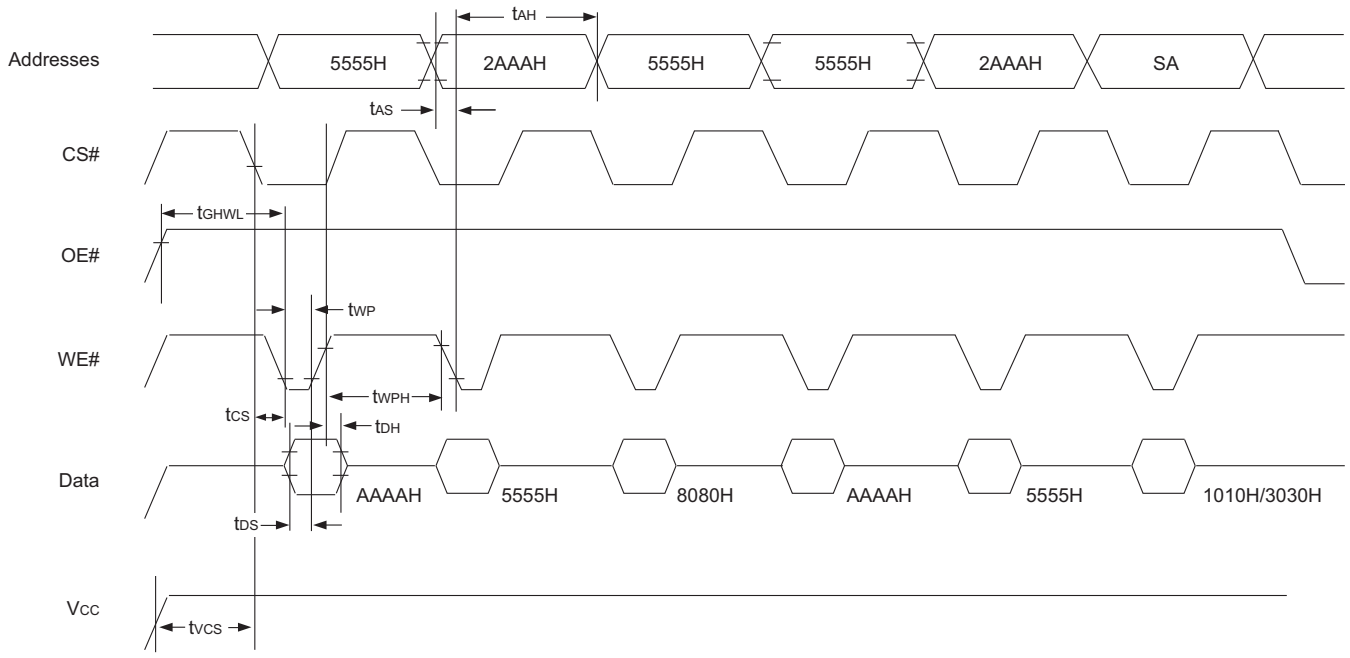


WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



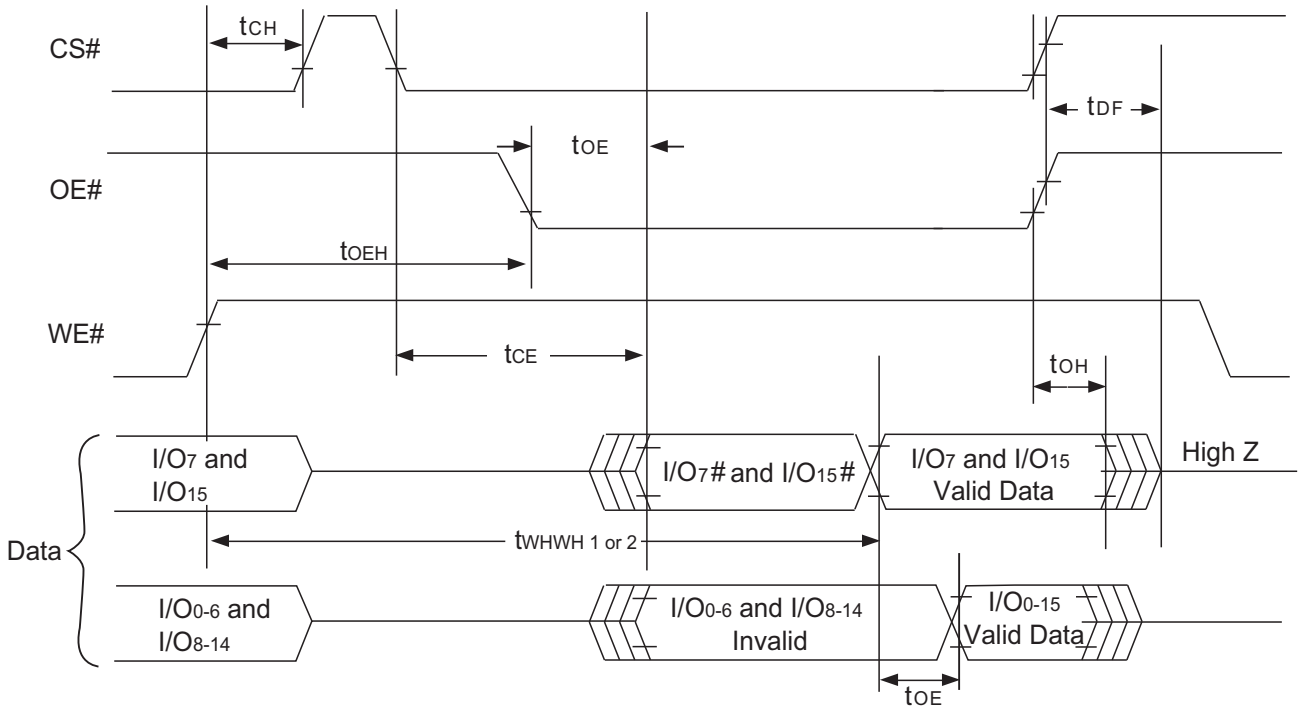
NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to each chip.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

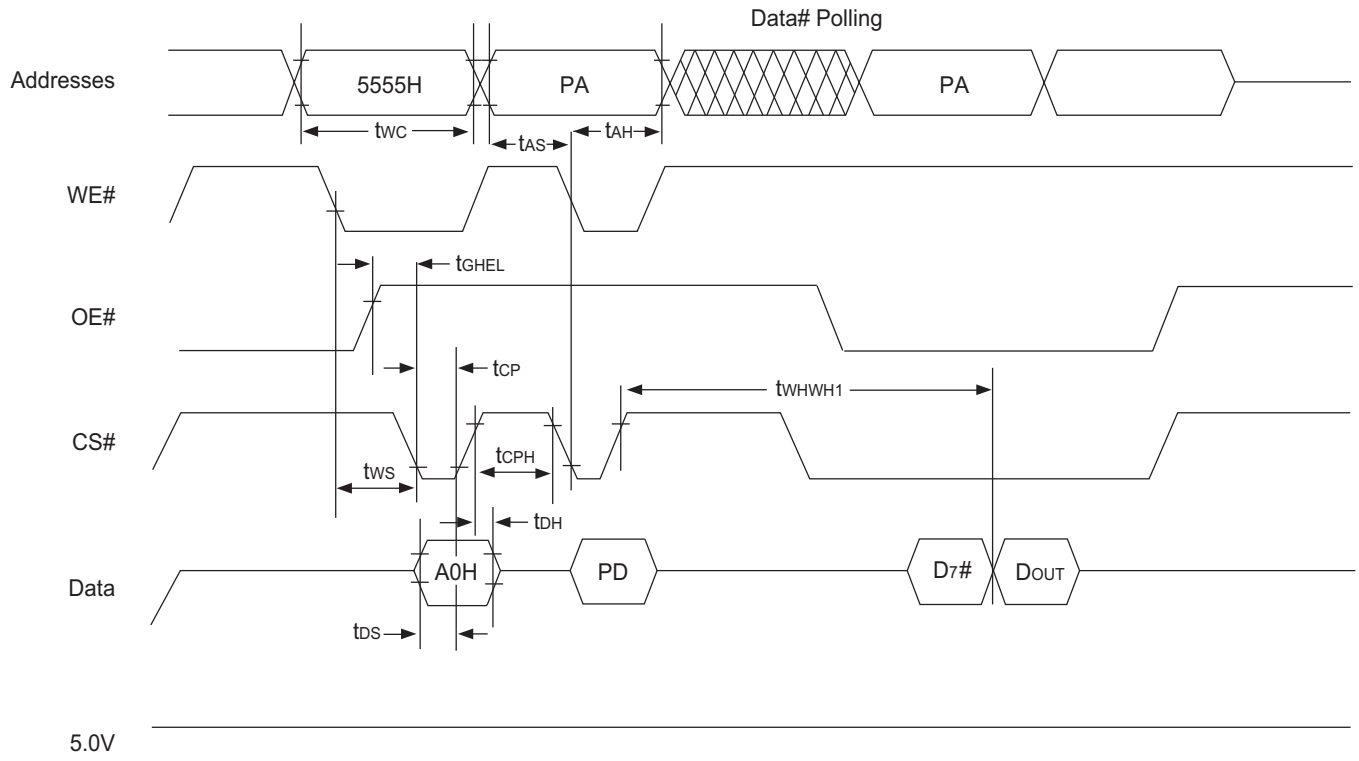


NOTE:
1. SA is the sector address for Sector Erase.

AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS

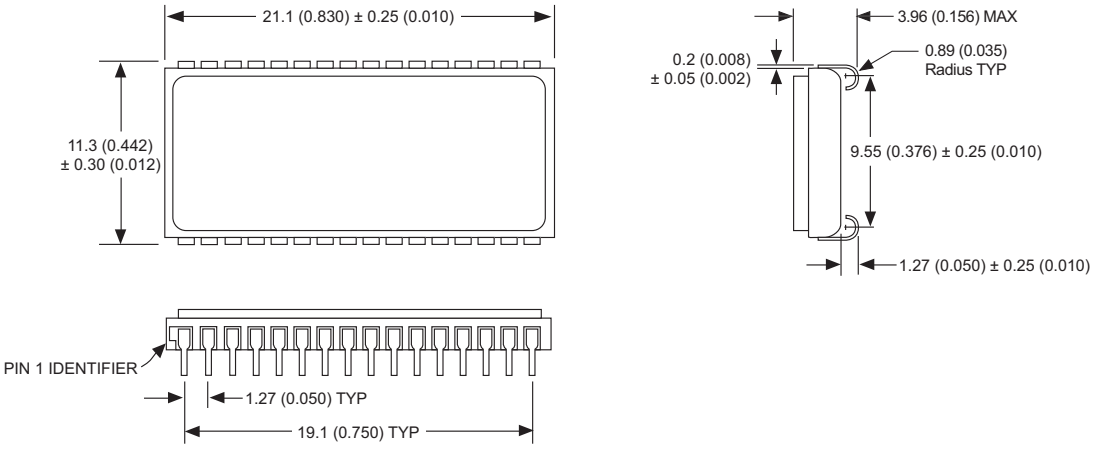


ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



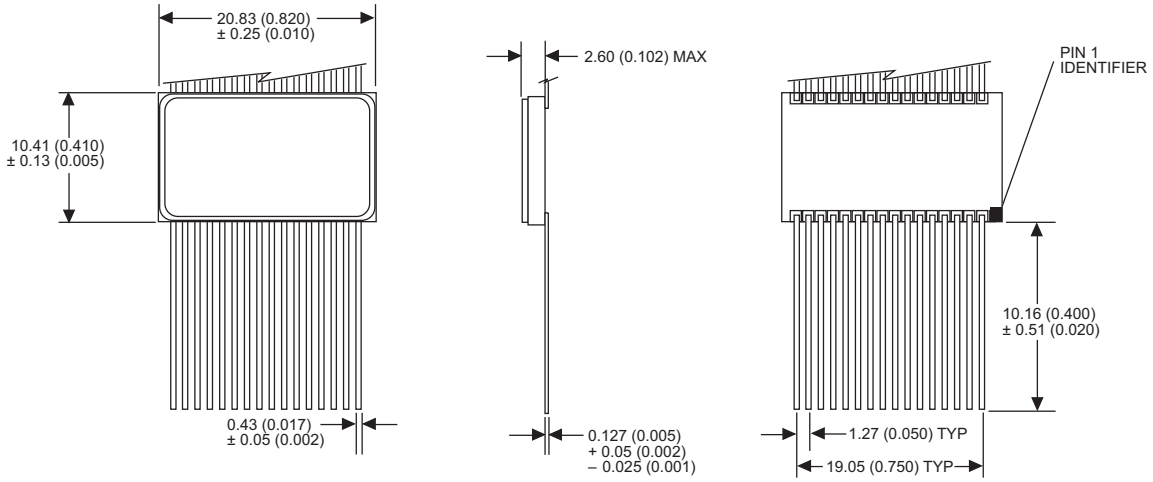
NOTES:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

PACKAGE 101 – 32 LEAD, CERAMIC SOJ



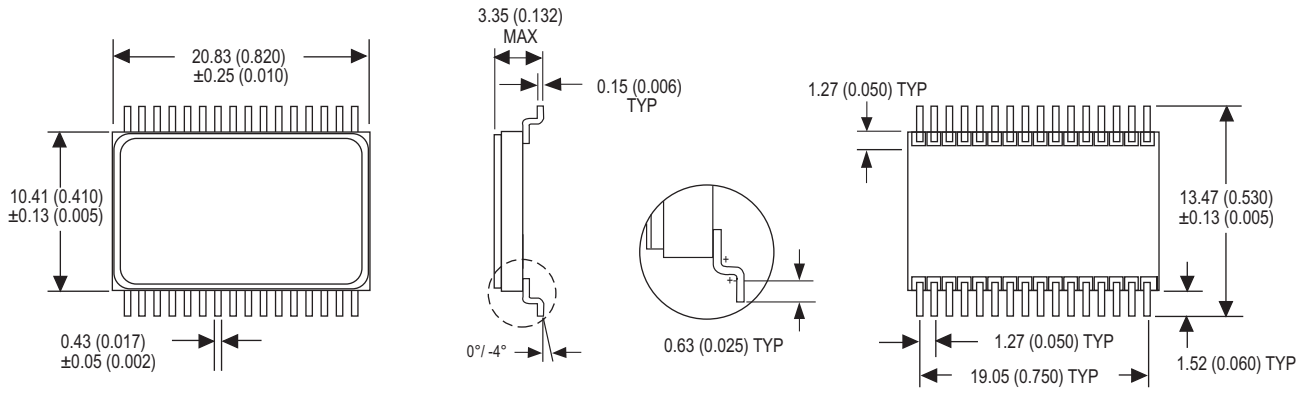
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 220 – 32 LEAD, CERAMIC FLATPACK



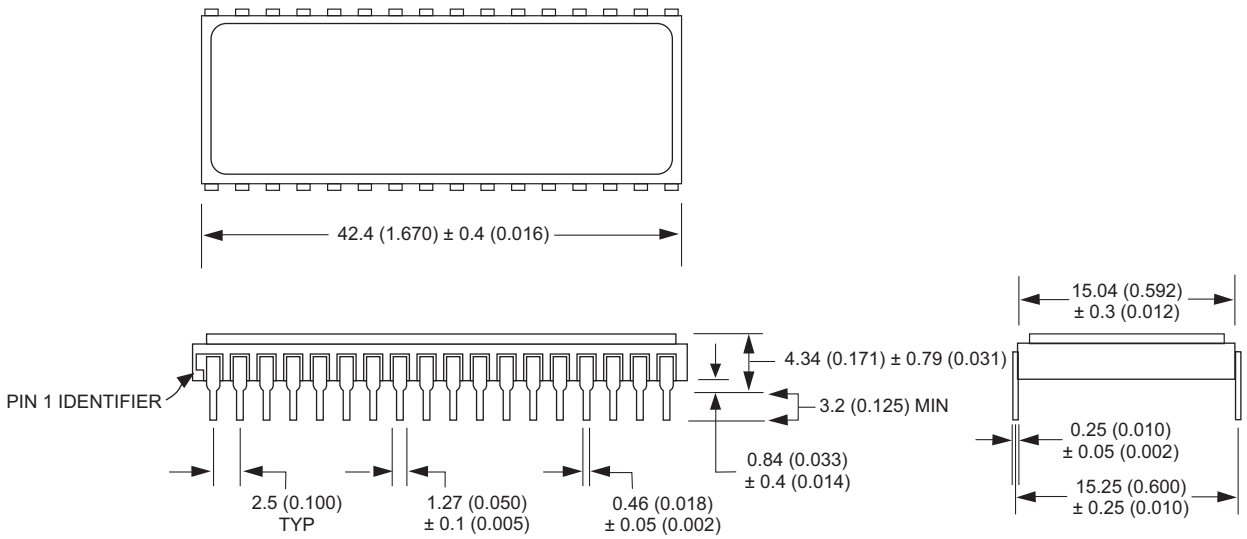
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 221 – 32 LEAD, FORMED CERAMIC FLATPACK



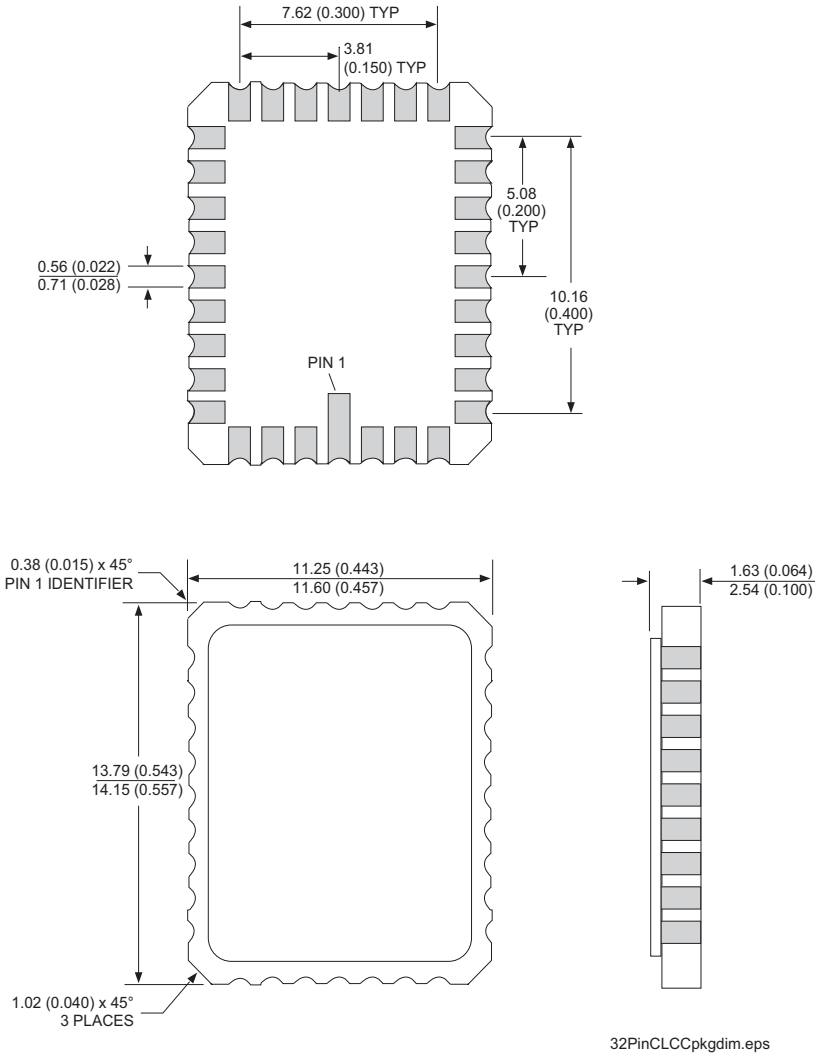
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300 – 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 601 – 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W M F 128K8 - XXX X X 5 X

MICROSEMI CORPORATION

MONOLITHIC

FLASH

ORGANIZATION, 128K x 8

ACCESS TIME (ns)

PACKAGE TYPE:

- DE = 32 Lead Ceramic SOJ (Package 101)
- C = 32 Pin Ceramic DIP (Package 300)
- FE = 32 Lead Ceramic Flatpack (Package 220)
- FF = 32 Lead Formed Ceramic Flatpack (Package 221)
- CL = 32 Pin rectangular Ceramic Leadless Chip Carrier (Package 601)

DEVICE GRADE:

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

V_{PP} PROGRAMMING VOLTAGE

- 5 = 5V

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
128K x 8 Flash Monolithic	16KByte	150ns	32 pin DIP (C)	5962-96690 01HYX
128K x 8 Flash Monolithic	16KByte	120ns	32 pin DIP (C)	5962-96690 02HYX
128K x 8 Flash Monolithic	16KByte	90ns	32 pin DIP (C)	5962-96690 03HYX
128K x 8 Flash Monolithic	16KByte	70ns	32 pin DIP (C)	5962-96690 04HYX
128K x 8 Flash Monolithic	16KByte	60ns	32 pin DIP (C)	5962-96690 05HYX
128K x 8 Flash Monolithic	16KByte	150ns	32 lead SOJ (DE)	5962-96690 01HXX
128K x 8 Flash Monolithic	16KByte	120ns	32 lead SOJ (DE)	5962-96690 02HXX
128K x 8 Flash Monolithic	16KByte	90ns	32 lead SOJ (DE)	5962-96690 03HXX
128K x 8 Flash Monolithic	16KByte	70ns	32 lead SOJ (DE)	5962-96690 04HXX
128K x 8 Flash Monolithic	16KByte	60ns	32 lead SOJ (DE)	5962-96690 05HXX
128K x 8 Flash Monolithic	16KByte	150ns	32 lead Flatpack (FE)	5962-96690 01HTX
128K x 8 Flash Monolithic	16KByte	120ns	32 lead Flatpack (FE)	5962-96690 02HTX
128K x 8 Flash Monolithic	16KByte	90ns	32 lead Flatpack (FE)	5962-96690 03HTX
128K x 8 Flash Monolithic	16KByte	70ns	32 lead Flatpack (FE)	5962-96690 04HTX
128K x 8 Flash Monolithic	16KByte	60ns	32 lead Flatpack (FE)	5962-96690 05HTX
128K x 8 Flash Monolithic	16KByte	150ns	32 lead Formed Flatpack (FF)	5962-96690 01HUX
128K x 8 Flash Monolithic	16KByte	120ns	32 lead Formed Flatpack (FF)	5962-96690 02HUX
128K x 8 Flash Monolithic	16KByte	90ns	32 lead Formed Flatpack (FF)	5962-96690 03HUX
128K x 8 Flash Monolithic	16KByte	70ns	32 lead Formed Flatpack (FF)	5962-96690 04HUX
128K x 8 Flash Monolithic	16KByte	60ns	32 lead Formed Flatpack (FF)	5962-96690 05HUX

Document Title

128Kx8 MONOLITHIC NOR FLASH, SMD 5962-96690

Revision History

Rev #	History	Release Date	Status
Rev 6	Changes (Pg. 1-14) 6.1 Change document layout from White Electronic Designs to Microsemi 6.2 Add document Revision History page	June 2011	Final
Rev 7	Changes (Pg. 1, 14) 7.1 Add "NOR" to headline	August 2011	Final