PGA970 LVDT Sensor Signal Conditioner

1 Features

- Analog Features
  - Programmable-Gain Analog Front End for LVDT Sensors
  - Excitation Waveform Generator and Amplifier
  - Dual 24-Bit ADC With Amplitude and Phase Demodulators
  - 24-Bit Auxilary ADC
  - On-Chip Internal Temperature Sensor
  - 14-Bit Output DAC With Programmable Gain
  - Built-In Diagnostics
- Digital Features
  - ARM® Cortex®-M0 Microcontroller
  - 16KB Ferroelectric RAM (FRAM) Program Memory
  - 2KB General-Pupose RAM
  - 512B RAM Waveform-Generator Look-Up Table
  - 8-MHz On-Chip Oscillator
- Peripheral Features
  - Serial Peripheral Interface (SPI)
  - One-Wire Interface (OWI)
  - Ratiometric and Absolute Voltage Output
- General Features
  - Operational Supply Range: 3.5 V to 30 V
  - Ambient Temperature Range: –40°C to +125°C
  - DMOS Gate Controller for Extended Supply Range >30 V

2 Applications

- Position Sensor Signal Conditioning
- Linear Variable Differential Transformer (LVDT)
- Rotational Variable Differential Transformer (RVDT)
- Resolver
- RLC Measurement

3 Description

The PGA970 device is a highly integrated system-on-chip LVDT sensor-signal conditioner with advanced signal-processing capabilities. It contains a three-channel, low-noise, programmable-gain, analog front end that allows direct connection to the sense element, followed by three independent 24-bit delta-sigma ADCs.

Further, the device contains a digital signal-demodulation block that interfaces to an integrated ARM-Cortex M0 MCU, allowing implementation of custom sensor-compensation algorithms stored in the device nonvolatile memory. External system communication is achieved by using any of the SPI, OWI, GPIO, or PWM digital interfaces. Analog output is supported through a 14-bit DAC and programmable-gain amplifier offering reference or absolute-voltage output. Sensing-element excitation is achieved by the use of an integrated waveform generator and waveform amplifier. The waveform signal data is user-defined and stored in a designated RAM memory area.

Besides the primary functional components, the PGA970 device is equipped with additional support circuitry. The device diagnostics, sensor diagnostics, and integrated temperature sensor provide protection and information about the integrity of the overall system and sensing element. The device also includes a gate-controller circuit which when used with an external depletion MOSFET can regulate the device supply voltage in systems where the supply voltage exceeds 30 V.

Device Information(1)

ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
PGA970QPHPR	HTQFP (48)	7.00 mm × 7.00 mm
PGA970QPHPT		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Diagram

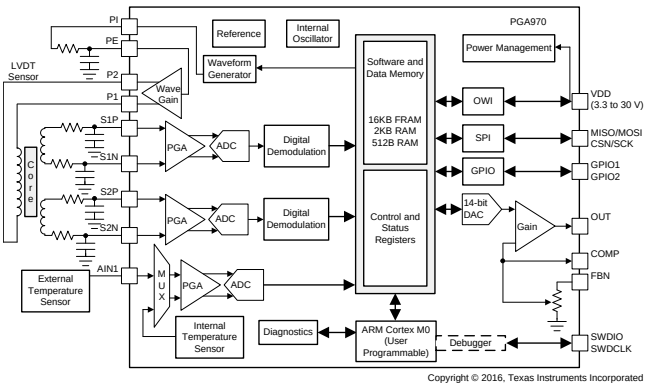


Table of Contents

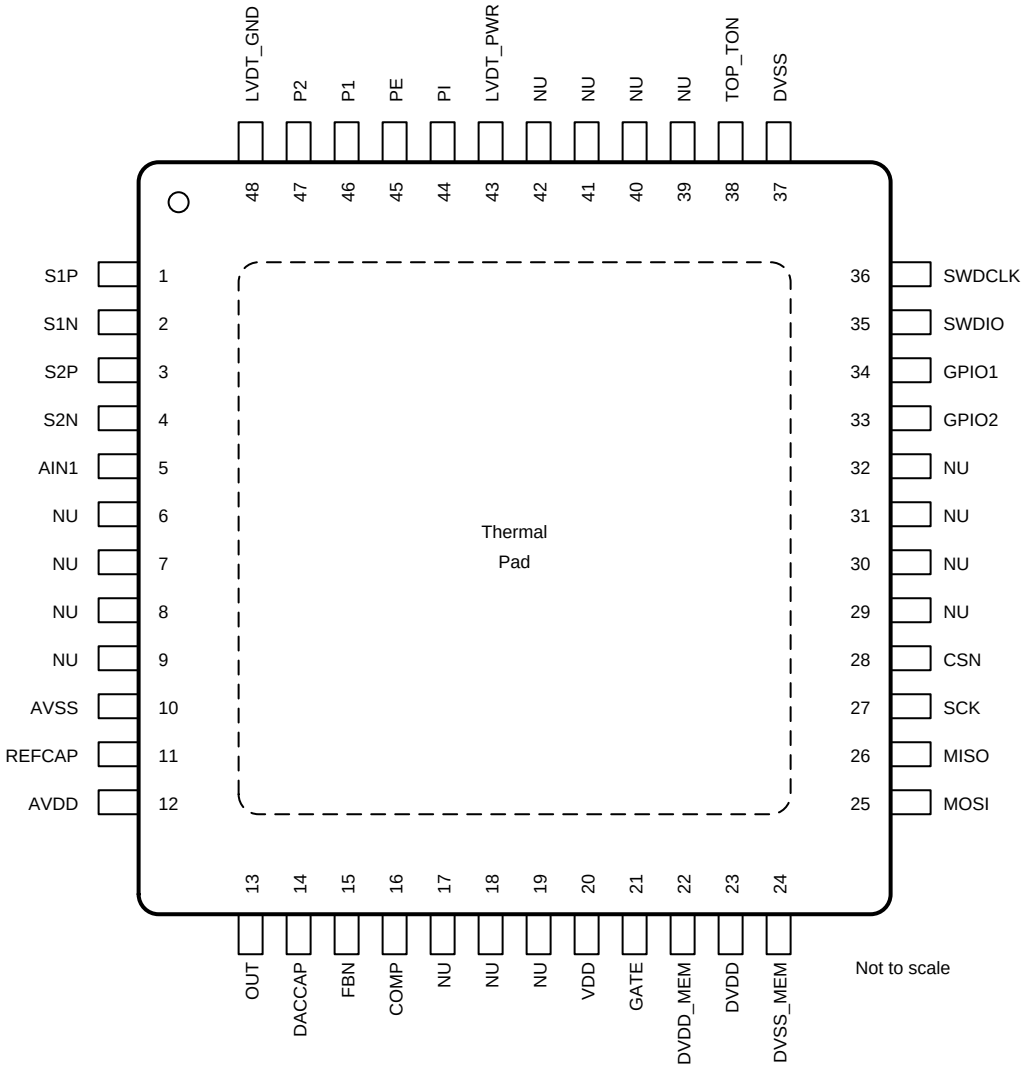
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2016) to Revision A	Page
• Changed the device status from *Product Preview* to *Production Data*	1

5 Pin Configuration and Functions

PHP PowerPAD™ Package
48-Pin HTQFP With Thermal Pad
Top View



NU – Make no external connection.

PGA970 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AIN1	5	I	General-purpose ADC S3 Input. Multiplexed with the internal temperature sensor and output in an alternating format.
AVDD	12	O	Internal 3-V analog regulator output. Connect a 100-nF decoupling capacitor to ground.
AVSS	10	—	Analog ground. Tie to system ground.
COMP	16	I	Output amplifier stability compensation
CSN	28	I	SPI chip select
DACCAP	14	O	DAC output filtering access. Connect a 100-nF capacitor to system ground for increased noise filtering.
DVDD	23	O	Internal 1.8-V digital regulator output. Connect a 100-nF decoupling capacitor to ground
DVDD_MEM	22	O	FRAM power supply
DVSS	37	—	Digital ground
DVSS_MEM	24	—	FRAM power-supply ground
FBN	15	I	Output negative feedback
GATE	21	O	N-channel depletion MOSFET gate drive
GPIO1	34	I/O	General-purpose input or output. Function defined in user-generated firmware.
GPIO2	33	I/O	General-purpose input or output. Function defined in user-generated firmware.
LVDT_GND	48	—	LVDT primary power ground. Tie to system ground.
LVDT_PWR	43	I	LVDT primary power
MISO	26	O	SPI slave data out
MOSI	25	I	SPI slave data in
NU	6, 7, 8, 9, 17, 18, 19, 29, 30, 31, 32, 39, 40, 41, 42	—	Not used
OUT	13	O	14-bit DAC amplifier output
P1	46	O	Primary-side LVDT excitation 1 for waveform amplifier single-ended or differential output
P2	47	O	Primary-side LVDT excitation 2 for waveform amplifier differential output
PE	45	I	Waveform DAC output
PI	44	O	Waveform GAIN input
REFCAP	11	O	Reference capacitor
S1N	2	I	Secondary 1 negative. Connected to S1 input stage and demodulator
S1P	1	I	Secondary 1 positive. Connected to S1 input stage and demodulator
S2N	4	I	Secondary 2 negative. Connected to S2 input stage and demodulator
S2P	3	I	Secondary 2 positive. Connected to S2 input stage and demodulator
SCK	27	I	SPI clock
SWDCLK	36	I	Serial wire debug clock
SWDIO	35	I/O	Serial wire debug input and output
TOP_TON	38	O	Test output positive or negative
V_{DD}	20	I	Supply voltage. 3.3-V to 30-V operating range
Thermal pad	—	—	Connect to ground and solder to ground plane. Thermal vias allow for additional heat dispersion.

6 Specifications

6.1 Absolute Maximum Ratings

See (1).

			MIN	MAX	UNIT
V_{DD}	V_{DD} voltage		–0.3	33	V
	GATE voltage		–0.3	33	V
	Voltage at sensor input and drive pins P1, P2, S1P, S1N, S2P, and S2N		–0.3	3.45	V
	Voltage at any I/O pin		–0.3	3.45	V
	Voltage at FBN pin		–0.3	V_{DD} + 0.3	V
I_{DD}	Supply current	Short on OUT		40	mA
		Short on LVDT		40	mA
T_J	Maximum junction temperature			155	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* are not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) – EIA/JESD22-A114 (1)	±2000	V
		Field-induced charged-device model (CDM) – JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating ambient temperature range at V_{DD} = 5 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Power supply voltage		3.5		30	V
	Slew rate	V_{DD} = 0 to 30 V			0.5	V/µs
I_{DD}	Power supply current, normal operation	V_{DD} = 14 V, waverform generator at 5 kHz, S1, S2 enabled, no LVDT primary load, no load on OUT, M0 running at 8 MHz			12.5	mA
T_J	Operating junction temperature		–40		125	°C
	Programming temperature	FRAM	–40		125	°C
	Capacitor on V_{DD} pin		470	680		nF

6.4 Thermal Information

THERMAL METRIC (1)		PGA970 PHP (HTQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics – External N-Channel Depletion MOSFET Gate Drive

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	V_{DD} voltage when using GATE control	Gate control bit is 0		3.75		V
	PSRR while in regulation			110		dB
	Capacitor on GATE pin			330		pF
	N-channel depletion MOSFET $V_{GS(th)}$			–1.5		V

6.6 Electrical Characteristics - Regulators

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVDD}	AVDD voltage	C_{AVDD} = 100 nF		3		V
I_{AVDD}	External load on AVDD pin				5	mA
V_{DVDD}	DVDD voltage – operating	C_{DVDD} = 470 nF		1.85		V
$V_{DVDD(POR)}$	DVDD voltage – digital POR			1.65		V
	DVDD voltage – digital POR hysteresis			0.1		V
$I_{(VDD + LVDT\_PWR)}$	V_{DD} constant current control	EN_CCS bit in CCS_CTRL = 1 (only CCS enabled, M0 not running, waveform generator not running, ADCs not enabled) ADJ_CCS = 0b0000		13.6		mA
		ADJ_CCS = 0b0001		14.6		
		ADJ_CCS = 0b0010		15.7		
		ADJ_CCS = 0b0011		16.7		
		ADJ_CCS = 0b0100		17.8		
		ADJ_CCS = 0b0101		18.8		
		ADJ_CCS = 0b0110		19.8		
		ADJ_CCS = 0b0111		20.8		
		ADJ_CCS = 0b1000		21.8		
		ADJ_CCS = 0b1001		22.9		
		ADJ_CCS = 0b1010		23.9		
		ADJ_CCS = 0b1011		24.9		
		ADJ_CCS = 0b1100		26		
		ADJ_CCS = 0b1101		27		
		ADJ_CCS = 0b1110		28		
		ADJ_CCS = 0b1111		29		

6.7 Electrical Characteristics – Internal Reference

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	High-voltage reference voltage			1.2		V
	Accurate reference voltage			2.5		V
	Accurate reference initial error		–1%		1%	
	Accurate reference voltage TC		–185	25	185	ppm/°C
	Capacitor value on REFCAP pin		100	200	1000	nF

6.8 Electrical Characteristics – Internal Oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal oscillator frequency	T_A = 25°C		8		MHz
	Internal oscillator frequency variation	Drift across temperature range	–3%		7%	

6.9 Electrical Characteristics – LVDT Primary Supply Waveform Generator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC resolution			14		Bits
DAC range			1.25		V
DAC sample rate			1		MHz
Waveform generator FIFO depth				256	14-bit samples

6.10 Electrical Characteristics – LVDT Primary Supply Waveform Gain

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER AMPLIFIER						
	Gain settlings	DAC gain control bits = 0b00		1		V/V
		DAC gain control bits = 0b01		1.18		
		DAC gain control bits = 0b10		1.4		
		DAC gain control bits = 0b11		1.67		
	Gain error (end-point line)	At 25°C, single-ended Includes DAC gain error, waveform gain = 1.67 V/V, 5-kHz DAC waveform amplitude from 100 mV to 400 mV		0.8%		
	Gain linearity (end-point line)	At 25°C, single-ended Includes DAC linearity, waveform gain = 1.67V/V, 5 kHz DAC waveform amplitude from 100 mV to 400 mV		0.02		%FSR
	Total temperature drift	Pullup disabled Differential sine voltage between P1 and P2 pins 100 mVrms to 390 mVrms Drift formula: [(Amplitude (at T) – Amplitude (at 25°C)] / [(T – 25°C)) × (Amplitude (at 25°C)] × 10^6			200	ppm/°C
	LVDT supply voltage THD	At 5 kHz, 25°C		–60		dB
I_{LVDT_P}	Current supply to LVDT primary	Single-ended mode DAC code = 7 012d to 15 532d			20	mA
	Short-circuit current			25		mA
	Differential-mode output common mode (Common mode voltage at P1 or P2 when LVDT drive is configured for differential mode)	DIFF_VOCM_CTRL = 0b00		0.75		V
		DIFF_VOCM_CTRL = 0b01		1		
		DIFF_VOCM_CTRL = 0b10		1.25		
		DIFF_VOCM_CTRL = 0b11		1.5		
	Differential offset adjustment(1)	DACVCM_CTRL = 0b00		0.82		V
		DACVCM_CTRL = 0b01		0.84		
		DACVCM_CTRL = 0b10		0.86		
		DACVCM_CTRL = 0b11		0.88		
	Unity-gain bandwidth(2)			6		MHz

(1) See *LVDT Primary Supply Waveform Gain* for a detailed description of the DACVCM_CTRL code stored in FRAM.
(2) Specified by Design

6.11 Electrical Characteristics – Internal Temperature Sensor

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature range		–40		125	°C
Gain under 25ºC	24-bit ADC, –40ºC to +25ºC		6950.8		LSB/°C
Gain above 25ºC	25ºC to 125ºC		See the available 25ºC and 125ºC values in FRAM(1)		LSB/ºC
Offset			See the 25ºC value in FRAM(1)		LSB
Internal temperature sensor accuracy	–40ºC to +25ºC		±2.8		°C

(1) See *Internal Temperature Sensor* for a detailed description of the temperature code stored in FRAM.

6.12 Electrical Characteristics – S1 and S2 Gain

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain steps (2 bits)	Gain control bits = 00b at dc		1		V/V
	Gain control bits = 01b		1.33		
	Gain control bits = 10b		1.67		
	Gain control bits =11b		2.00		
Gain bandwidth product(1)			350		kHz
Input bias current			5		nA
Input voltage at each pin		0.05		2	V
Common-mode voltage control (for ac-coupled secondary connection)	BIAS_VCM_CTRL = 00b, pullup disabled		1.25		V
	BIAS_VCM_CTRL = 01b; pullup disabled		0.5		
	BIAS_VCM_CTRL = 10b; pullup disabled		0.75		
	BIAS_VCM_CTRL = 11b; pullup disabled		1		
Input impedance(1)	Fault diagnostics resistors disabled	500			kΩ

(1) Defined in design, not tested by manufacturer

6.13 Electrical Characteristics – S3 Gain Stage

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain steps (2 bits)	Gain control bits = 00b at dc		1		V/V
	Gain control bits = 01b		1.33		
	Gain control bits = 10b		2		
	Gain control bits = 11b		5		
Gain bandwidth productFigure 76			350		kHz
Input bias current			5		nA
Input voltage at pin		0.01		2.1	V
Input impedance	Fault resistor disabled		50		MΩ

6.14 Electrical Characteristics – Digital Demodulators 1 and 2

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sampling frequency			1		MHz
Demodulator voltage input range		0		2.5	V
Number of bits			24		bits
Demodulator code for sinusoid input voltage of amplitude 0 V			$00\ 0000_{hex}$		LSB
Demodulator code for sinusoid input voltage of amplitude 2.4 V at output of S1 or S2 gain			$27\ 1D29_{hex}$		LSB
24-bit peak-to-peak noise	at • 25°C • 5-kHz LVDT excitation • Input signal amplitude = 0.8 V • Common-mode voltage = 0.86 V • S1 or S2 gain = 1 V/V • Output rate = 256 µs • Pullup disabled • LPF cutoff frequency = 20 Hz Includes gain noise, reference noise, and SDM thermal noise and quantization noise		50		LSBs
Effective number of bits (ENOB)(1)			15		bits
Demodulator-1, -2 nonlinearity	At 25°C at 5-kHz carrier frequency, LPF cutoff frequency = 250 Hz, gain = 1.33 V/V Includes nonlinearity of gain, reference, and SDM Method to calculate linearity: • Disable pullup • Sweep input sine amplitude from 63 mVrms to 236 mVrms • End-point fit a straight line between the demodulator output at these amplitudes • Calculate linearity using the formula: [(max. deviation from straight line) / (max. demod – min. demod)] × 100		±0.01		%FSO
Demodulator-1, -2 output total temperature drift	5-kHz carrier frequency, LPF cutoff frequency = 250 Hz, gain = 1.33 V/V Includes drift of gain, reference, and SDM Method to calculate drift: • Disable pullup • Sweep input sine amplitude from 63 mVrms to 236 mVrms at temperature • At each amplitude and temperature setting, record demodulator ouptut • Calculate drift using the formula: Drift formula: [demod (at T) – demod (at 25°C)] / [(T – 25°C) × demod (at 25)] × 10^6		±9	50	ppm/°C
Ratiometric (DEMOD1 – DEMOD2) / (DEMOD1 + DEMOD2) total temperature drift	At • Pullup disabled • 5-kHz carrier frequency • DEMOD1 input signal amplitude = 157 mVrms • DEMOD2 input signal amplitude = 116 mVrms • Common-mode voltage = 0.86 V • S1 or S2 gain = 1.33 V/V • Output rate = 256 µs • LPF cutoff frequency = 20 Hz Drift formula: {[ratio (at T) – ratio (at 30°C)] / 1.4792} × 100			0.05	%FS
PSRR	V_{DD} = 14 V, ripple = 5%, frequency = 10 kHz		115		dB

(1) ENOB = ln[(Full-Scale Range) / (Peak-to-Peak Noise)] / ln(2)

6.15 Electrical Characteristics – Analog-to-Digital Converter 3

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sampling frequency			4		MHz
ADC voltage input range		0		2.5	V
Number of bits			24		bits
ADC code for 0 V			00 0000_{hex}		
ADC code for 2.5 V			7F $FFFF_{hex}$		
16-bit peak-to-peak noise for the AIN1 input	At • 25°C • DC • S3 gain = 1 V/V • Output period = 192 µs • LPF cutoff frequency = 20 Hz Includes gain noise, ADC reference noise, ADC thermal noise, and ADC quantization noise		7		LSBs
Effective number of bits (ENOB) for the AIN1 input			12.2		bits
Minimum Input voltage for linearity (input-referred at S3 gain)	At • 25°C • DC • S3 gain = 1 V/V • Output period = 192 µs • LPF cutoff frequency = 20 Hz	10			mV
GAIN + ADC offset	At • 25°C • DC • Output period = 192 µs • LPF cutoff frequency = 20 Hz Method to calculate linearity for each S3 gain setting: • Sweep input from 200 mV to 2 V (divided by S3 gain) • End-point fit a straight line between the demodulator output at these amplitudes • Calculate linearity using the formula: [(max. deviation from straight line) / (max. ADC3 – min. ADC3)] × 100 • Offset determined by Y-intercept of linearity equation		5		mV
GAIN + ADC nonlinearity	At • 25°C • DC • Output period = 192 µs • LPF cutoff frequency = 20 Hz Method to calculate linearity for each S3 gain setting: • Sweep input from 200 mV to 2 V (divided by S3 gain) • End-point fit a straight line between the demodulator output at these amplitudes • Calculate linearity using the formula: [(max. deviation from straight line) / (max. ADC3 – min. ADC3)] × 100		0.15		%FSO
GAIN + ADC total temperature drift	At • DC • Output period = 192 µs • LPF cutoff frequency = 20 Hz Method to calculate temperature drift: • Sweep input voltage from 200 mV to 2 V (divided by S3 gain) at 25°C and at temperature • Drift formula: {[ADC3 (at T) – ADC3 (at 25°C)] / [(T – 25°C) × ADC3 (at 25ºC)]} × 10^6		125		ppm/°C

6.16 Electrical Characteristics – One-Wire Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Communication baud rate(1)		320		9600	Bits per second
$V_{(OWI\_ENH)}$	OWI activation high		5.95			V
$V_{(OWI\_ENL)}$	OWI activation low				5.75	V
	Low time of activation-signal pulse		1 10			ms
	High time of activation-signal pulse		1 10			ms
$V_{IH(OWI)}$	OWI transceiver Rx threshold for high		4.8		5.1	V
$V_{IL(OWI)}$	OWI transceiver Rx threshold for low		3.9		4.2	V
$I_{OH(OWI)}$	OWI transceiver Tx threshold for high		500		1379	µA
$I_{OL(OWI)}$	OWI transceiver Tx threshold for low		2		5	µA

(1) OWI over power line does not work if there is an LDO between the supply to the sensor and the V_{DD} pin, and if the OWI high and low voltages are greater than the regulated voltage.

6.17 Electrical Characteristics – SPI

Over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level voltage (CSN, SCK, MOSI, MISO)		2		AVDD + 0.3	V
V_{IL}	Low-level voltage (CSN, SCK, MOSI, MISO)		–0.3		0.8	V
V_{OH}	High-level output voltage		2.4			V
V_{OL}	Low-level output voltage				0.4	V
f_{SCK}	SPI frequency				1	MHz
$C_{L(MISO)}$	Capacitive load for data output (MISO)			10		pF

6.18 DAC Output

over operating ambient temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC reference voltage	Reference bit = 1		1.25		V
	Reference bit = 0 (ratiometric)		0.25 × $V_{(ddp)}$		
DAC resolution			14		bits

6.19 DAC Gain

over operating ambient temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Buffer gain (see Figure 3)	DAC_GAIN = 0b100, absolute			2		V/V
	DAC_GAIN = 0b010, absolute			4		
	DAC_GAIN = 0b110, absolute			6.67		
	DAC_GAIN = 0b001, absolute			10		
	DAC_GAIN = 0b010, ratiometric			4		
Linearity	Calculation of linearity at each gain: At 25 °C 1. Set OUT to drive a 100-nF capacitive load with appropriate compensation circuit. No DACCAP 2. Sweep DAC code from 819d to 15 565d and measure OUT voltage. 3. Fit a straight line using the end-point method. 4. Calculate linearity using the formula: [(max. deviation from straight line) / (max. OUT – min. OUT)] × 100	DAC_GAIN = 0b100, absolute		0.02		%FSR
		DAC_GAIN = 0b010, absolute		0.025		
		DAC_GAIN = 0b110, absolute		0.04		
		DAC_GAIN = 0b001, absolute		0.05		
		DAC_GAIN = 0b010, ratiometric		0.025		
Total temperature drift	Calculation of temperature drift: 1. Set OUT to drive a 100-nF capacitive load with appropriate compensation circuit. No DACCAP 2. Set DAC mid-code (8192d) and measure OUT voltage. 3. Measure OUT at 25°C and at temperature. 4. Calculate drift using the formula: {[OUT (at T) – OUT (at 25°C)] / [OUT (at 25°C) × (T – 25)]} × 10^6	DAC_GAIN = 0b100, absolute			235	ppm/°C
		DAC_GAIN = 0b010, absolute			235	
		DAC_GAIN = 0b110, absolute			235	
		DAC_GAIN = 0b001, absolute			235	
Ratiometric error due to change in temperature and load current for DAC mid-code (8192d).	Calculate ratiometric error at V_{DD} = 5 V and at DAC codes as follows: 1. Apply DAC Code at 25°C and 0-mA load, and measure voltage at OUT. 2. Change temperature between –40°C and 125°C, and measure voltage at OUT. 3. Change load current between 0 mA and 0.5 mA, and measure voltage at OUT. 4. Ratiometric error = [(OUT at TEMPERATURE and LOAD) – (OUT at 25°C and 0 mA)]			19		mV
Ratiometric error due to change in V_{DD} for DAC mid-code (8192d).	Calculate ratiometric error at DAC codes as follows: 1. Apply DAC code at 25°C and 0-mA load, and measure voltage at OUT. 2. Change V_{DD} between 4.5 V and 5.5 V, and measure voltage at OUT. 3. Change temperature between –40°C and 125°C, and measure voltage at OUT. 4. Ratiometric error = [(OUT at V_{DD} and TEMPERATURE) – (OUT at 5 V and 25°C)] × V_{DD} / 5 V			25	50	mV
DAC gain noise	f = 10 Hz to 1 kHz, V_{DD} = 4.5 V, absolute mode, gain = 4 V/V, no capacitors for COMP or DACCAP pins, 25°C			95		µVpp
Settling time (first-order response)(1)	DAC code 819d to 15 564d step and C_{LOAD} = 100 nF. Output is 99% of final value.				200	µs
Zero code voltage	DAC code = 0000h, I_{DAC_GAIN} = –2.5 mA, Gain = 4 V/V				20	mV
Full code voltage	V_{DD} = 14 V, DAC code is 7FFFh, I_{DAC_GAIN} = 2.5 mA, Gain = 4 V/V		4.8			V
Output current	DAC code = 7FFFh, DAC code = 0000h				±2.5	mA
Short-circuit source current	DAC code = 0000h			21		mA
Short-circuit sink current	DAC code = 7FFFh			40		mA
Gain bandwidth product(1)				1		MHz
Maximum capacitance	Without compensation				100	pF
PSRR	V_{DD} = 14 V, ripple = 5%, frequency = 10 kHz			–50		dB

(1) Specified by design

6.20 GPIO, Digital Test-In and Test-Out Buffers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	R_{LOAD} ≥ 10 kΩ to V_{AVDD} or to 0 V	2		AVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH1}	High-level output voltage	I_{OH} = –2 mA	2.4			V
V_{OH2}	High-level output voltage	I_{OH} = –0.2 mA	2.78			V
V_{OL1}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = 0.2 mA			0.04	V
I_{OH}	High-level output current	V_{OH} = 2.4 V	–2			mA
I_{OL}	Low-level output current	V_{OL} = 0.8 V			2	mA

6.21 Non-Volatile Memory

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FRAM	Size			16		KB
	Programming time	Per word		250		ns
	Data retention			10		years
	Erase and write cycles				10^{15}	cycles

6.22 Diagnostics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Software watchdog-timer resolution			2		ms
	Software watchdog-timer high range			8		bits
	Software watchdog-timer low range			8		bits
OSC_OK	Oscillator-good flag			±25%		
AVDD_OV	AVDD OV threshold			3.3		V
AVDD_UV	AVDD UV threshold			2.7		V
DVDD_OV	DVDD OV threshold			2		V
DVDD_UV	DVDD UV threshold			1.53		V
REF_OV	Accurate reference overvoltage threshold		2.75			V
P1P2_SOURCE_OC	P1 and P2 source overcurrent			25		mA
P1P2_SINK_OC	P1 and P2 sink overcurrent			25		mA
P1_OV	P1 overvotlage			2.95		V
P1_UV	P1 undervoltage			50		mV
P2_OV	P2 overvotlage			2.95		V
P2_UV	P2 undervoltage			50		mV
PE_OV	PE overvotlage			2.2		V
REF_OV	Accurate-reference overvoltage threshold			2.75		V
REF_UV	Accurate-reference undervoltage threshold			2.25		V
S3_INPUT_OV	S3 input overvoltage			2.95		V
S1_I_OV	Input overvoltage (single-ended) threshold for S1 gain			2.4		V
S1_O_OV	Output overvoltage (single-ended) threshold for S1 gain			2.4		V
S2_I_OV	Input overvoltage (single-ended) threshold for S2 gain			2.4		V
S2_O_OV	Output overvoltage (single-ended) threshold for S2 gain			2.4		V

Diagnostics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
S3_I_OV	Input overvoltage (single-ended) threshold for S3 gain			2.4		V
S3_O_OV	Output overvoltage (single-ended) threshold for S3 gain			2.7		V
PULL_UP	PE, S1, S2, S3 input pullup resistance			1		MΩ
DAC_LB1	DAC loopback voltage gain from waverform DAC to S1 and S2			1		V/V
DAC_LB2	DAC loopback voltage gain from OUT DAC to S3			1		V/V
HARNESS_FAULT1	Open-wire leakage current 1, open V_{DD} with pullup on OUT			2		µA
HARNESS_FAULT2	Open-wire leakage current 2, open GND with pulldown on OUT			20		µA

6.23 M0

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	M0 core frequency (including FRAM)	M0 frequency control bit = 00b		1		MHz
		M0 frequency control bit = 01b		2		
		M0 frequency control bit = 10b		4		
		M0 frequency control bit = 11b		8		
	Start-up time (including analog and digital)	V_{DD} ramp rate 1 V/µs			20	µs

6.24 Digital Demodulation

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Demodulator output rate configurable modes			128		µs
				256		µs

6.25 SPI Timing Requirements

Over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CSNSCK)}$	CSN low to first SCK rising edge		25			ns
$t_{(SCKCSN)}$	Last SCK rising edge to CSN rising edge		125			ns
$t_{dis(CSN)}$	CSN disable time		4000			ns
$t_{su(MOSI)}$	MOSI setup time		25			ns
$t_{h(MOSI)}$	MOSI hold time		25			ns
$t_{r(MOSI)}$, $t_{f(MOSI)}$	MOSI rise and fall times				7	ns
$t_{r(SCK)}$	SCK rise time				7	ns
$t_{f(SCK)}$	SCK fall time				7	ns
$t_{(SCKH)}$	SCK high time		125			ns
$t_{(SCKL)}$	SCK low time		125			ns
$t_{en(MISO)}$	MISO enable time		15			ns
$t_{d(ACCS)}$	SCK rising edge to MISO data valid		15			ns
$t_{dis(MISO)}$	MISO disable time				15	ns
$t_{r(MISO)}$, $t_{f(MISO)}$	MISO rise and fall times		3		11	ns

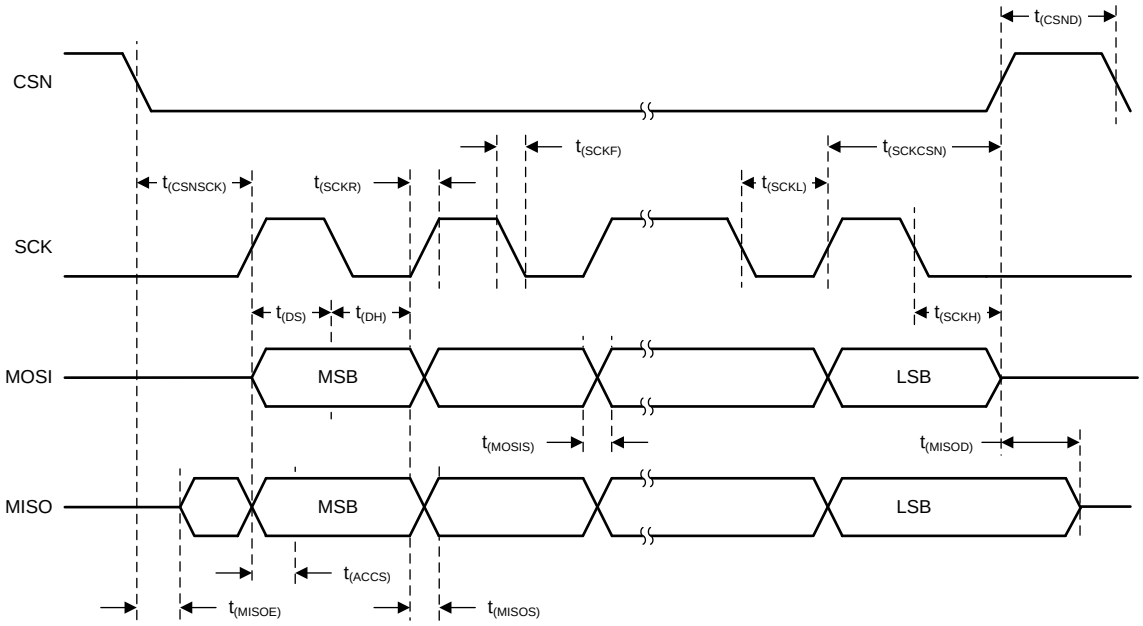


Figure 1. SPI Timing

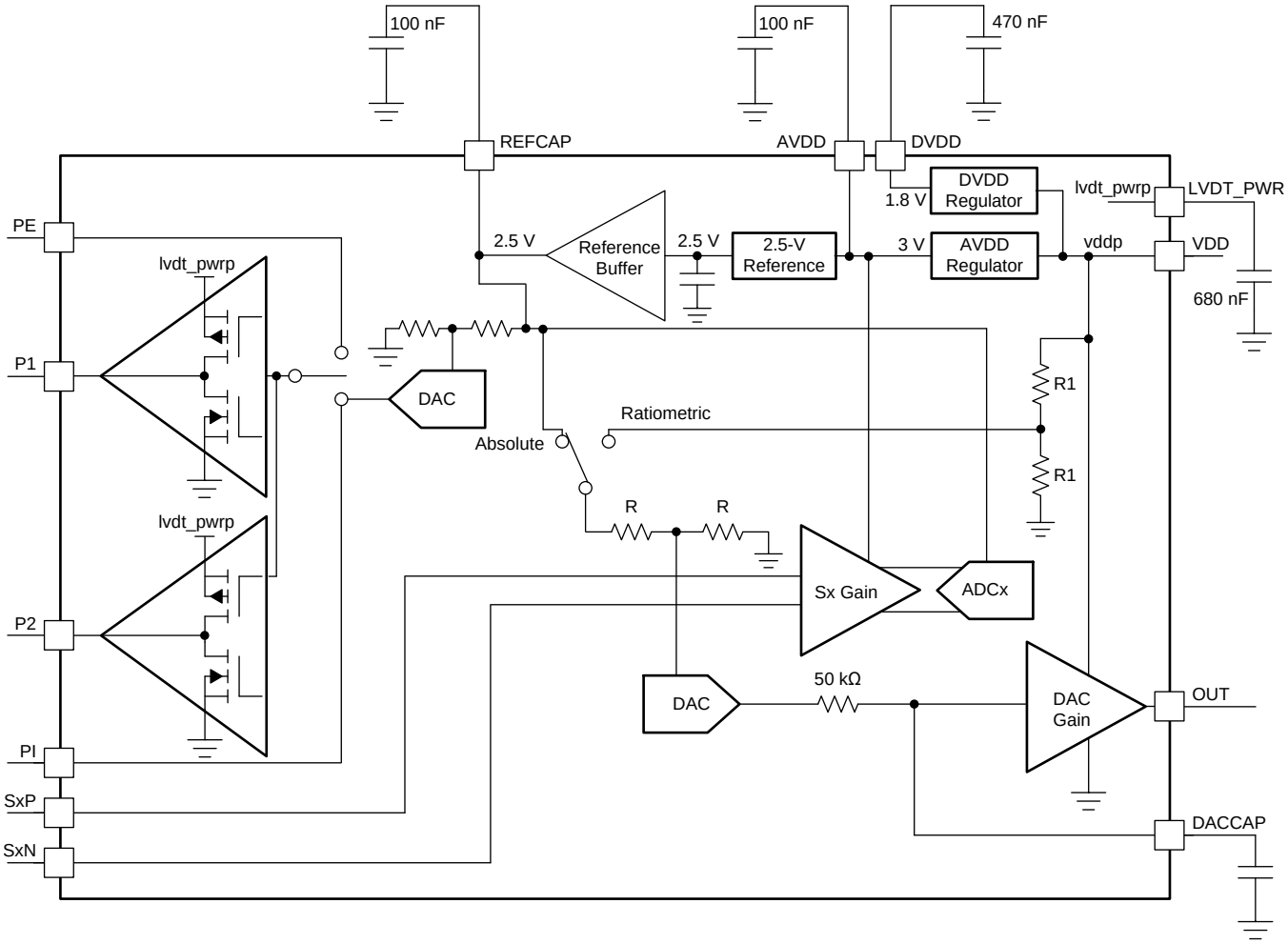


Figure 2. LVDT Supply and ADC Reference Are Ratiometric

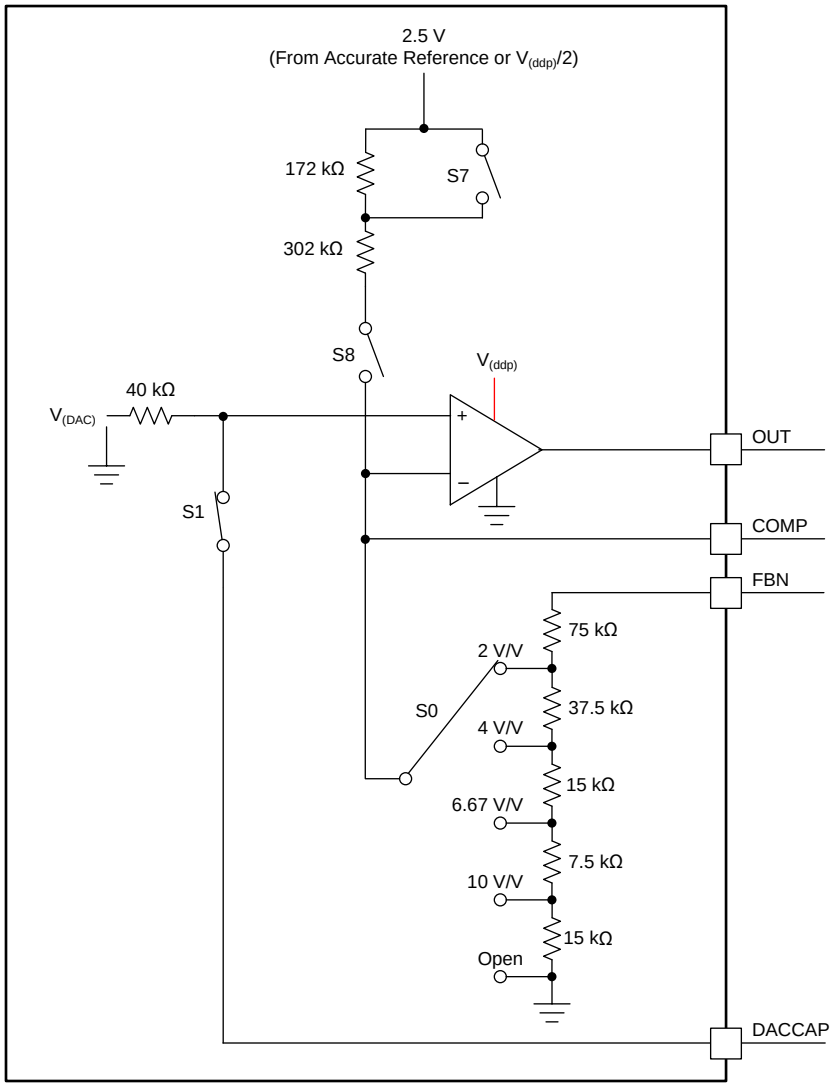


Figure 3. PGA970 Output Buffer

6.26 Typical Characteristics

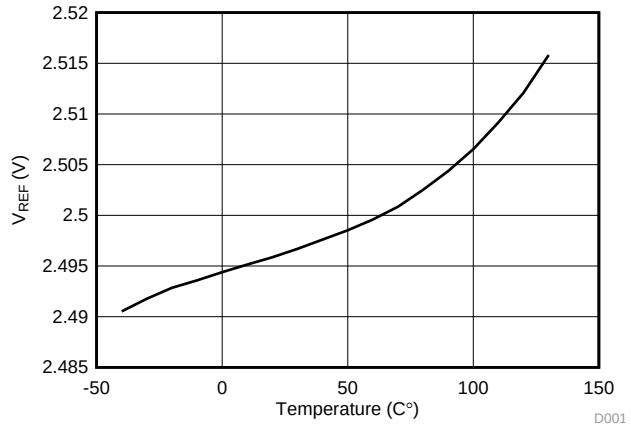


Figure 4. Reference Voltage V_{REF} Over Temperature

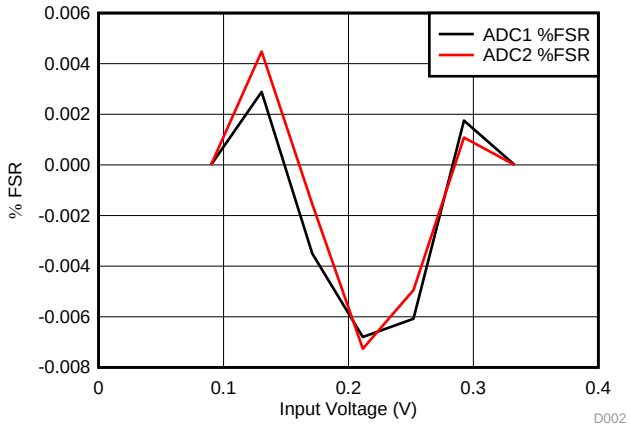


Figure 5. Demodulator 1 and 2 Linearity at 25°C

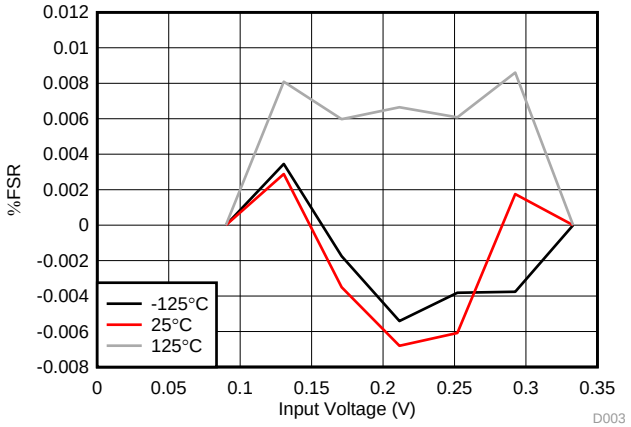


Figure 6. Demodulator 1 Linearity Across Temperature

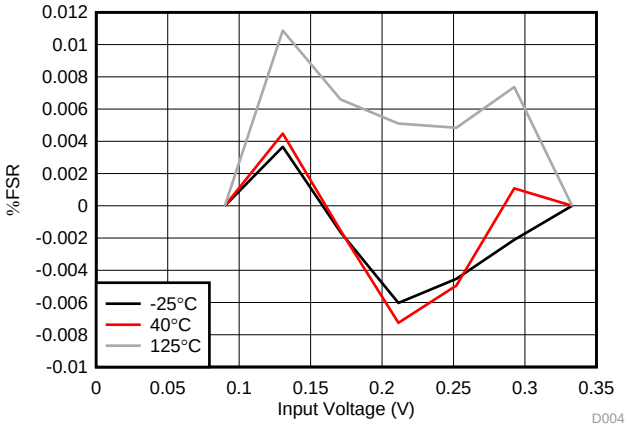


Figure 7. Demodulator 2 Linearity Across Temperature

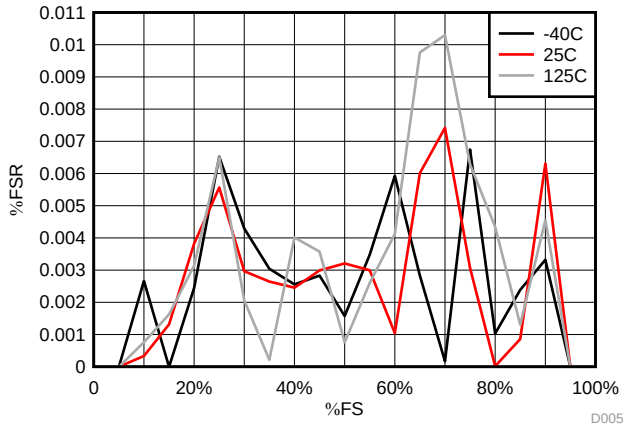


Figure 8. DAC Linearity, 2 V/V Gain

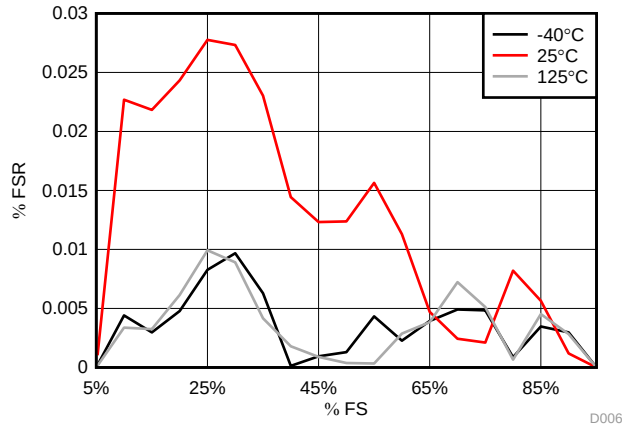


Figure 9. DAC Linearity, 4 V/V Gain

Typical Characteristics (continued)

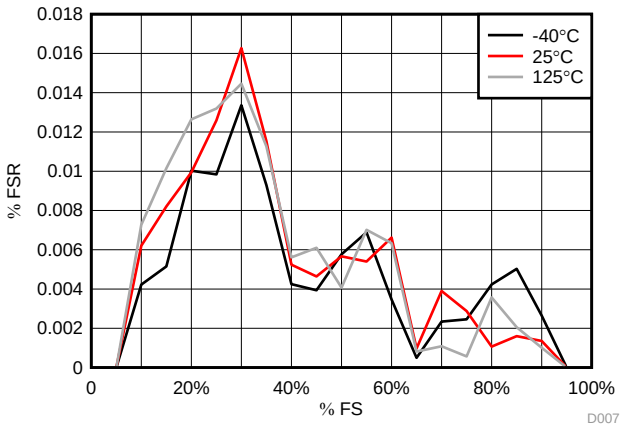


Figure 10. DAC Linearity, 6.67 V/V Gain

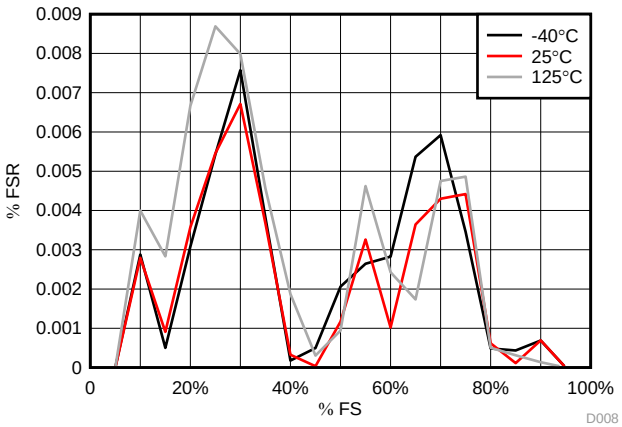


Figure 11. DAC Linearity, 10 V/V Gain

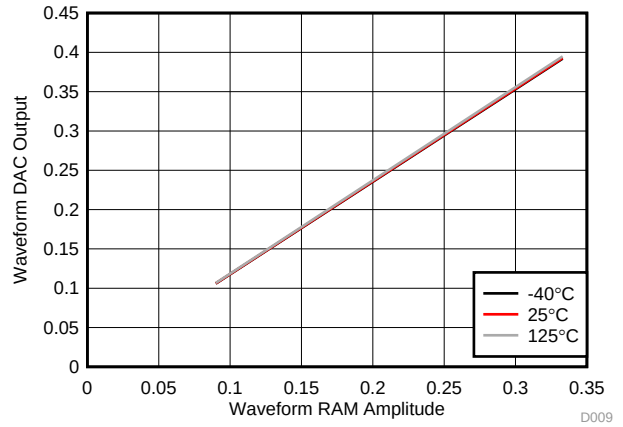


Figure 12. Waveform DAC Linearity, Waveform Gain = 1.18 V/V

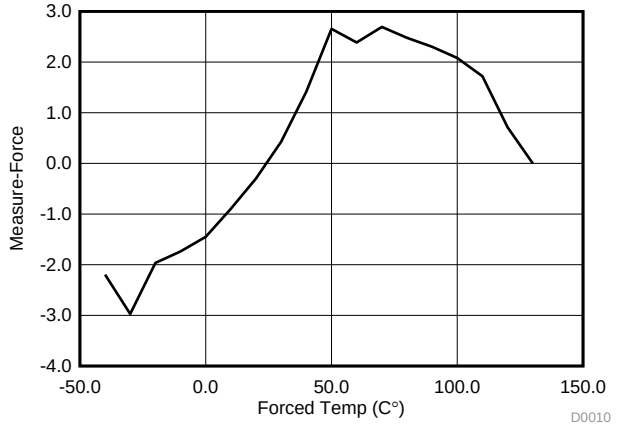


Figure 13. Temperature Sensor Measured Accuracy after Two-Point Calibration

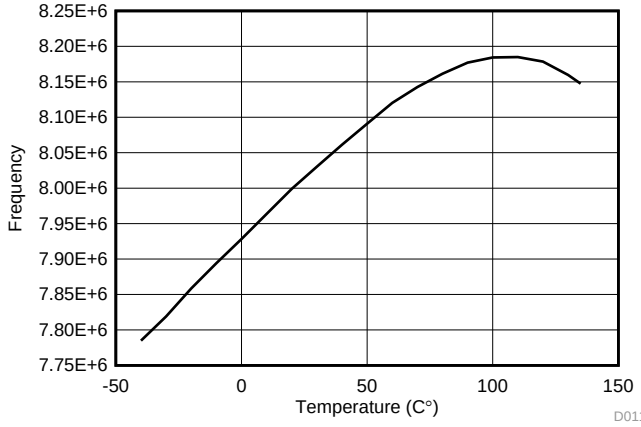


Figure 14. Oscillator Frequency vs Temperature

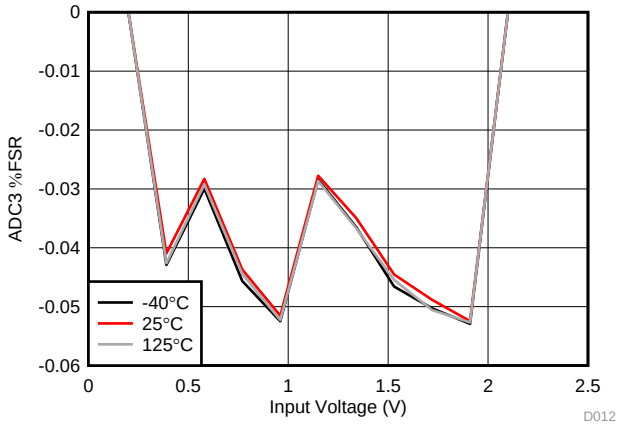


Figure 15. Auxiliary ADC3 Linearity

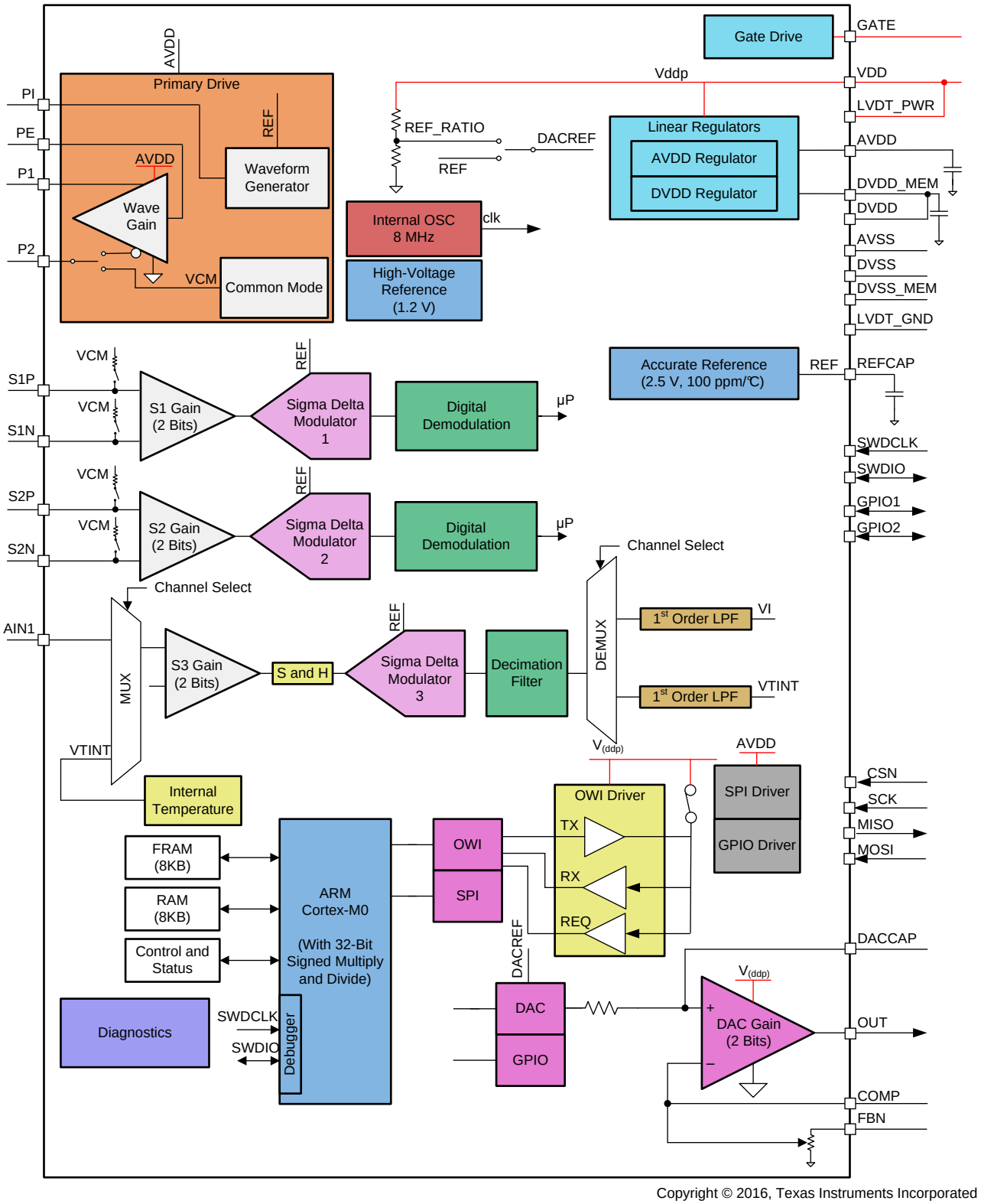
7 Detailed Description

7.1 Overview

The PGA970 device is a high-accuracy, extremely low-drift, low-noise, and versatile signal conditioner for linear variable differential transformer (LVDT) applications. The PGA970 device accommodates various multi-wire LVDT types, as well as being functionally capable of operating with rotary variable differential transformers (RVDT) and resolver sensors.

The PGA970 device provides a waveform generator for primary-side excitation of the LVDT, capable of generating sine waves up to 20 kHz. The PGA970 device conditions up to two differential secondary-side waveforms through the analog front end and digital demodulator. These signals can then be conditioned with compensation and linearization algorithms by the on-chip ARM Cortex-M0 processor. The resultant conditioned signals can then be output in analog or digital form. The signal data can also be accessed by multiple digital interfaces, including SPI, multiple GPIO ports, and the unique one-wire interface (OWI), which allows communication through the power-supply line.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Functional Block Descriptions

This section describes individual functional blocks.

7.3.1.1 Gate Drive for N-Channel Depletion MOSFET

The PGA970 device includes gate control for an external N-channel depletion MOSFET used as the pass element for an LDO. When the device is used in this mode, V_{DD} is regulated to 14 V by the PGA970 device. Figure 16 shows a block diagram representation of the MOSFET gate drive.

If the gate-drive mode is not used, then the user must do the following:

- Connect the GATE pin to ground.
- Disable gate control by setting the GATE_CTRL_SD bit in the ALPWR register to 1.

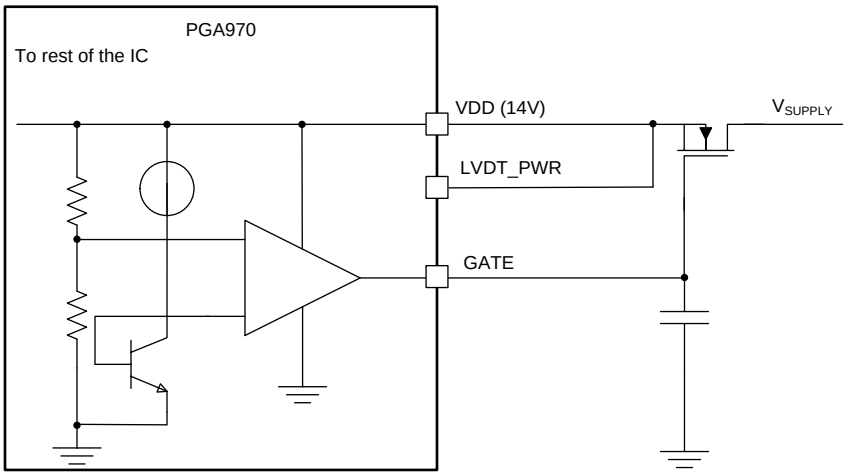


Figure 16. Gate Drive for N-Channel Depletion MOSFET

CAUTION

If the PGA970 device is operated in gate-drive mode, then V_{DD} cannot be driven directly from an external voltage source.

7.3.1.2 Linear Regulators

The PGA970 device has two main linear regulators: the AVDD regulator and the DVDD regulator. The AVDD regulator provides the 3-V voltage source for internal analog circuitry, whereas the DVDD regulator provides the 1.8-V regulated voltage for the digital circuitry. The user must connect bypass capacitors on the AVDD and DVDD pins of the device.

Feature Description (continued)

The power-on-reset signal to the digital core is deasserted when both AVDD and DVDD are in regulation. Figure 17 shows the block diagram representation of the digital power-on-reset (POR) signal generation and Figure 18 shows the digital POR signal assertion and deassertion timing during V_{DD} ramp-up and ramp-down. This timing shows that during power up, the digital core and the microprocessor remain in the reset state until both AVDD and DVDD are at stable levels.

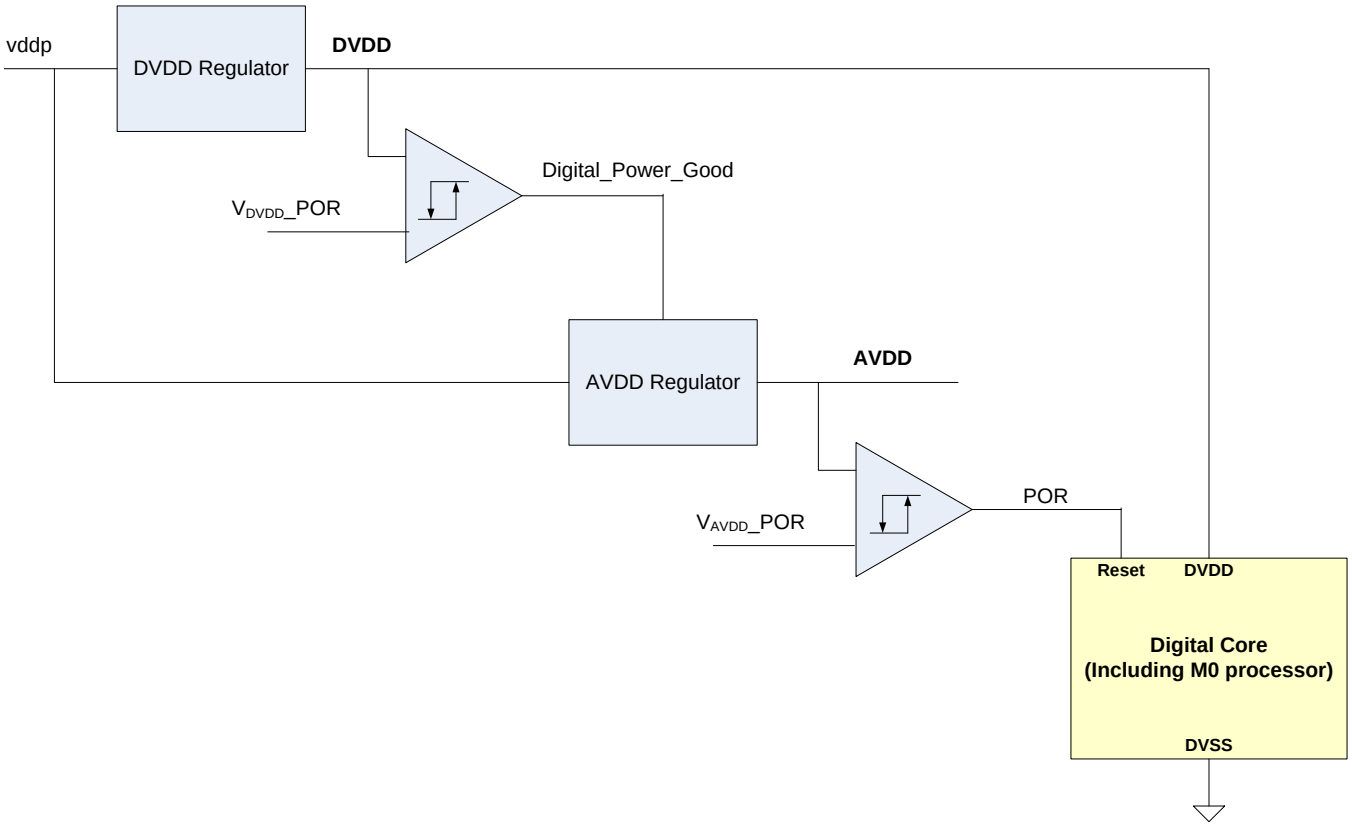


Figure 17. Digital Power-On-Reset Signal Generation

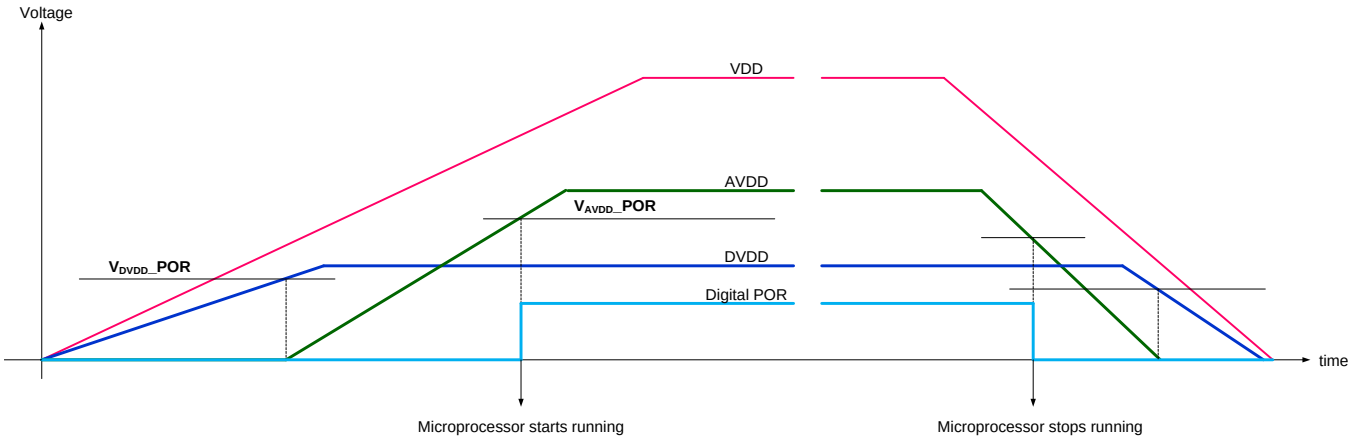


Figure 18. Digital Power-On-Reset Signal Generation

Feature Description (continued)

7.3.1.2.1 Constant-Current Control of V_{DD}

The PGA970 device implements a circuit to eliminate voltage ripple at the V_{DD} pin of device due to varying LVDT primary current and instead consume constant supply current. The control of current can be enabled by setting the EN_CCS bit in the CCS_CTRL register to 1.

7.3.1.3 Internal Reference

The PGA970 device has two internal references. Each of these reference is described as follows.

7.3.1.3.1 High-Voltage Reference

The high-voltage reference is an inaccurate reference used in the gate-drive circuit as well as diagnostic thresholds.

7.3.1.3.2 Accurate Reference

The accurate reference is used to generate reference voltage for ADC delta-sigma modulators and the DAC. A 100-nF capacitor is recommended to be placed on the REFCAP pin to limit the bandwidth of reference noise.

The accurate reference buffer can be disabled by setting the ADC_EN_VREF bit in the ALPWR register to 0. This allows the user to connect an external single-ended reference voltage to the REFCAP pin and thus provide the reference voltage to the ADCs and the DAC. Note that the default power-up state of ADC_EN_VREF is such that the reference buffer is disabled.

NOTE

The accurate reference is valid 500 µs after the digital core starts running at power up.

7.3.1.4 Internal Oscillator

The device includes an internal 8-MHz oscillator. This oscillator provides the internal clock required for the various circuits in the PGA970 device.

7.3.1.5 LVDT Primary-Supply Waveform Generator

The LVDT primary-supply waveform-generator block of the PGA970 device generates the waveform used to excite the primary coil. This nominal supply is ratiometric to the precise internal accurate reference.

The LVDT primary waverform generator is a 14-bit DAC look-up table (LUT) stored in FRAM. The LUT values are copied to waveform RAM and used to drive the waveform DAC at a fixed sample rate.

7.3.1.6 LVDT Primary Supply Waveform Gain

The LVDT primary-coil gain block of the PGA970 device supplies power to the LVDT primary-coil sensor. The amplifier is a low-distortion amplifier. The input to the amplifier is the low-pass filtered output of the waveform generator and the output of the amplifier is either single-ended or differential. Specifically, the waveform generator generates the sine wave using the look-up table values stored in FRAM. The output of the waveform generator is provided on PI pin of the device for implementing an external RC filter. The output of the RC filter is fed back into the PE pin of the device for amplification.

Feature Description (continued)

Figure 19 shows the primary-supply waveform-gain configuration. Note that the output at P2 could be either the common-mode voltage for single-ended drive configurations or a sine wave for differential-drive configurations.

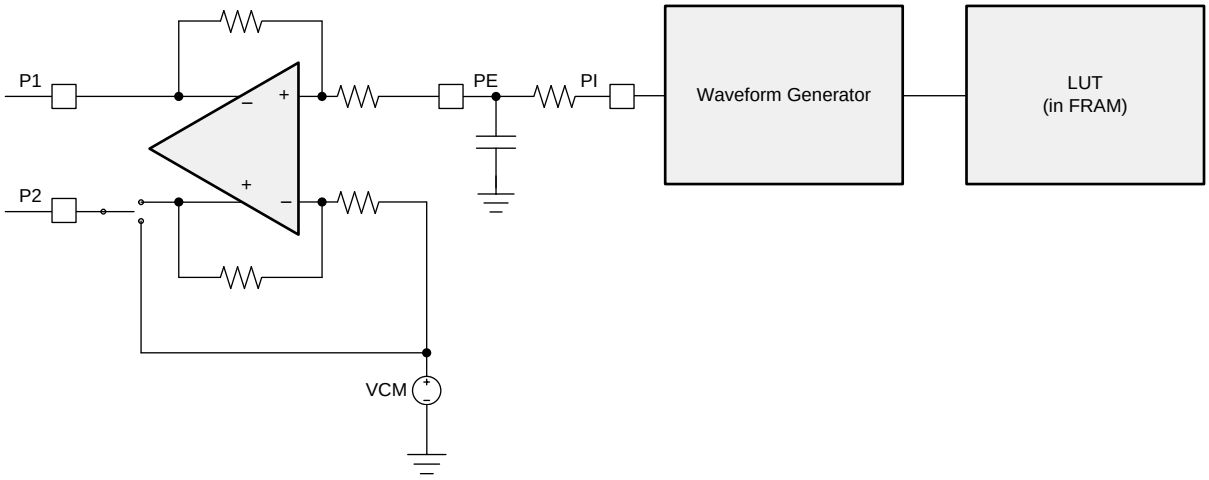


Figure 19. Primary Supply Waveform Gain

NOTE

The differential offset adjustment, DACVCM_CTRL, found in the LVDT_OP_CTRL register, has an optimal value from device to device to minimize the input offset of the waveform gain amplifier. The ideal 2-bit value to place in DACVCM_CTRL is pre-written to FRAM address 0x3FFB.

7.3.1.7 Internal Temperature Sensor

The PGA970 device includes an internal temperature sensor whose voltage output is digitized by the auxiliary ADC3 and made available to the microprocessor. This digitized value is used to implement temperature compensation algorithms in software. Note that the voltage generated by the internal temperature sensor is proportional to the junction temperature of the device.

Figure 20 shows the internal temperature-sensor AFE.

In order to improve the accuracy of the temperature sensor in the 25º to 125ºC range, every device has several unique temperature code values pre-written to the FRAM to specify more-accurate gain and offset values. A signed, 32-bit value for the 25ºC temperature point of this device is located at FRAM address 0x3FFC, and a 32-bit 125ºC temperature point is located at FRAM address 0x3FF4.

With these two temperature code values, the appropriate gain for this range can determined as

GAIN = (CODE_125C – CODE_25C) / 100

where

- CODE_125C is the 32-bit FRAM value at 0x3FF4
- CODE_25C is the 32-bit FRAM value at 0x3FFC (1)

From there, the temperature in degrees Celcius can be determined using

T = 25 + (ADC_CODE_READ – CODE_25C) / GAIN

where

- ADC_CODE_READ is the internal temperature ADC reading from S3 (2)

Feature Description (continued)

The 25ºC FRAM value should also be used as the offset value for the –40ºC to +25ºC temperature range. The gain for that temperature range is available in *Electrical Characteristics – Internal Temperature Sensor*.

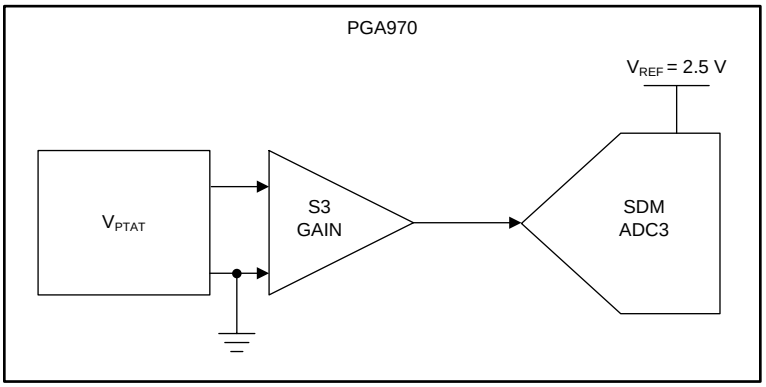


Figure 20. Temperature Sensor AFE

7.3.1.8 S1 and S2 Gain Stages

The S1 and S2 gain stages are designed with precision, low-drift, low-flicker-noise amplifiers.

The gain of each of these stages are adjustable using 2 bits in the S1_CFG and S2_CFG registers to accommodate LVDTs with different output spans.

7.3.1.9 S3 Gain Stage

The device has the ability to perform temperature compensation via an internal or external temperature sensor. Note that the device connects to an external temperature sensor via the AIN1 pin.

Table 1. S3 Gain Configuration

TEMPERATURE SOURCE	S3 GAIN CONFIGURATION
Internal temperature sensor	Single-ended
External temperature sensor with one terminal of the sensor connected to ground	Single-ended

7.3.1.10 Demodulator 1 and 2

The outputs of DEMOD1 and DEMOD2 are the amplitude and phase values of the S1 and S2 gain-stage input signals respectively. The amplitude and phase demodulation algorithm is described in the *Digital Demodulation* section.

Table 2. Input Voltage Amplitude to Output Counts for S1 and S2 ADC

SIGMA DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE AMPLITUDE (V)	16-BIT NOISE-FREE DECIMATOR OUTPUT	24-BIT NOISE-FREE DECIMATOR OUTPUT
0	0 (0x0000)	0 (0x000000)
1.25	10 430 (0x28BE)	4 194 303 (0x28 BE60)
2.5	20 860 (0x517C)	5 340 354 (0x51 7CC1)

7.3.1.11 ADC3 Architecture

ADC3 converts the AIN1 and PTAT channels at a 192-µs output period. Each of these channels has a configurable first-order Butterworth IIR low-pass filter in its path. The output of the low-pass filter is available to the M0.

7.3.1.12 Digital Interfaces

The digital interfaces are used to access (read and write) the internal memory spaces described in the *Memory* section. Each interface uses different pins for communication. The device has two separate modes of communication:

1. One-wire interface (OWI)
2. Serial peripheral interface (SPI)

The two communication modes supported by the PGA970 device are collectively referred to as digital interfaces in this document. Each communication mode has its own protocol; however, both access the same memory elements within the device. For both the communication modes, the PGA970 device operates as a slave device.

Figure 21 shows the interaction between the microprocessor, the memory block and the digital interfaces.

Both the digital interfaces can access the memories simultaneously. Each interface can be disabled using control bits. It is up to the user to ensure that both interfaces do not access the device simultaneously. Note that if security lock is enabled in the PGA970 device, then the digital interfaces cannot access any of the internal memories inside the PGA970 device.

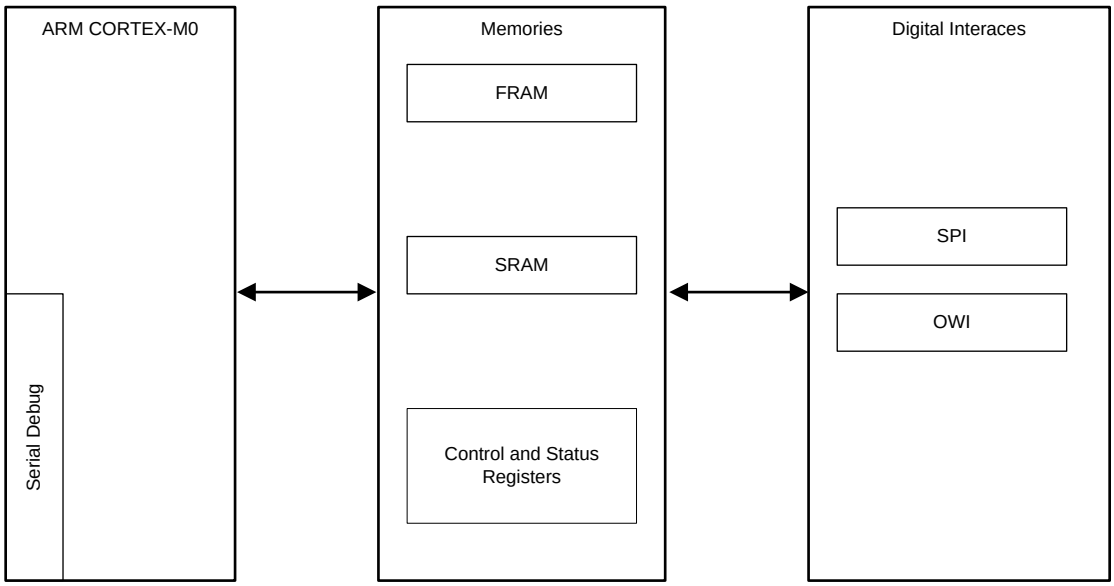


Figure 21. Digital Interfaces

7.3.1.12.1 Accessing PGA970 Memories While the Microprocessor Is Running

If the microprocessor is not in reset state, only the following registers are accessible to the digital interfaces:

- MICRO_INTERFACE_CONTROL
- COM_MCU_TO_DIF, which is read by the digital interfaces
- COM_DIF_TO_MCU, which is written by the digital interfaces
- COM_TX_STATUS

The COM_MCU_TO_DIF and COM_DIF_TO_MCU registers are used to communicate with the PGA970 device using the digital interface while the microprocessor is running. These registers are collectively referred to as COMBUF registers. Software must be implemented inside the PGA970 device so that the device can communicate with the digital-interface master using the COMBUF registers.

The digital-interface master and the PGA970 slave communicate with each other in the following way:

1. The digital-interface master writes data to the COM_DIF_TO_MCU register.
2. When COM_DIF_TO_MCU is written by the digital-interface master, a COMBUF interrupt is generated. Note that the COMBUF interrupt is enabled by writing 1 to the COM_RX_INT_EN bit in the COM_RX_INT_ENABLE register.
3. In the COMBUF interrupt service routine, the microprocessor clears the COMBUF interrupt by writing 1 to the

COM_RX_STATUS register.

4. The software then reads the COM_DIF_TO_MCU register and responds to received data by writing to the COM_MCU_TO_DIF register.
5. The master periodically polls the COM_TX_STATUS register to determine if the PGA970 device has updated the COM_MCU_TO_DIF register. The master reads the COM_MCU_TO_DIF register for the response from the PGA970 device if the COM_TX_STATUS register has been updated by the PGA970.

The PGA970 software can be written such that the PGA970 device updates the COM_MCU_TO_DIF register periodically without receiving a request from the digital-interface master. For example, the software in the PGA970 device can periodically update the processed position value. The master can read the processed position data periodically.

7.3.1.12.1.1 COMBUF Register Data Coherency

Both the COM_MCU_TO_DIF and COM_DIF_TO_MCU registers are 16-bit registers. All 16 bits can be accessed in one transfer using SPI. However, because OWI uses 8-bit transfers, this interface requires two accesses to receive all 16 bits. The PGA970 device implements data coherency schemes to maintain data coherency for transfers from the PGA970 device to the digital-interface master and for transfers from the digital-interface master to the PGA970 device.

7.3.1.12.1.1.1 Coherency for Transfer From PGA970 Device to Master

In order to maintain coherency between the two 8-bit data reads by the master, the PGA970 device implements an 8-bit shadow register. When OWI master initiates a read of the COM_MCU_TO_DIF register by reading the lower 8 bits first (COM_MCU_TO_DIF_B1 register), the PGA970 device stores the upper 8 bits (contents of COM_MCU_TO_DIF_B2) to the shadow register. When the master reads the upper 8 bits (by reading COM_MCU_TO_DIF_B2) register, the contents of the shadow register are transmitted by the PGA970 device.

Figure 22 shows data coherency with an example.

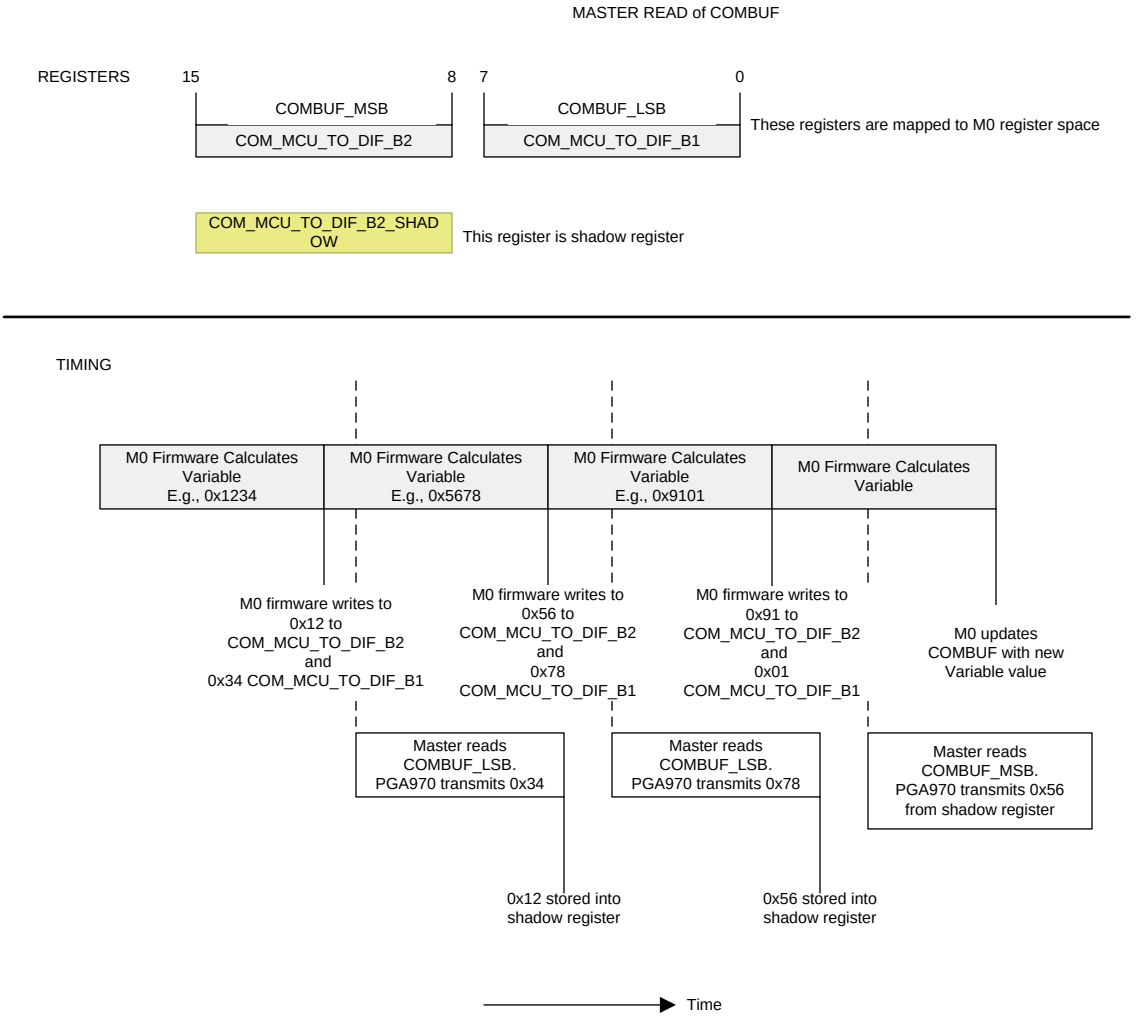


Figure 22. Master Read of COMBUF

7.3.1.12.1.1.2 Coherency for Transfer From Master to PGA970 Device

In order to maintain coherency between the two 8-bit data reads by the PGA970 device, a COMBUF interrupt is generated only when the digital-interface master writes the upper 8 bits of the COM_DIF_TO_MCU register, that is, when the master writes to the COM_DIF_TO_MCU_B2 register.

Figure 23 shows data coherency with an example.

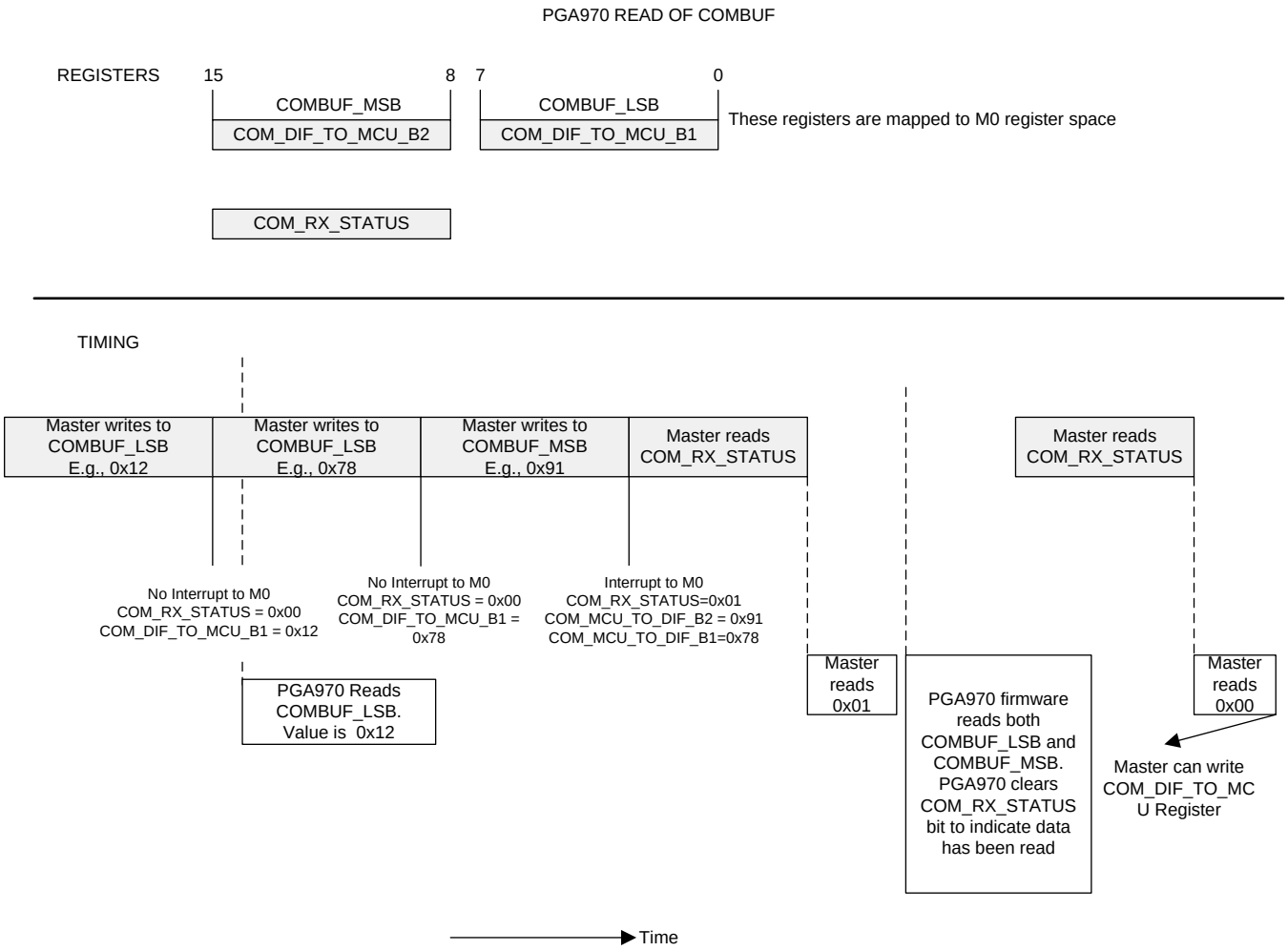


Figure 23. PGA970 Read of COMBUF

7.3.1.12.2 Accessing PGA970 Memories While the Microprocessor Is in Reset

An alternative method of using the COMBUF registers to communicate with the PGA970 device is to reset the PGA970 microprocessor using the digital interface and enabling digital-interface access. In this mode, all memories inside the PGA970 device are accessible to the digital interface without the need for software inside the PGA970 device to support communication.

The microprocessor can be put in the reset state by writing 1 to the MICRO_RESET bit in the MICRO_INTERFACE_CONTROL register using any of the digital communication peripherals. Access to the digital interface is enabled by writing 1 to the IF_SEL bit in the MICRO_INTERFACE_CONTROL register.

7.3.1.12.3 Accessing Memories Using 8-Bit Addresses

The sizes of FRAM, DEVELOPMENT RAM (DEVRAM), WAVEFORM RAM, and DATA RAM in the PGA970 device are more than 256 bytes. Each of these memories is 8-bit addressable. In order to allow the digital interface to access these memories using an 8-bit address, these memory spaces are organized as 256-byte pages. Table Table 3 lists the registers used to specify the page address for each type of memory.

Table 3. Registers Used to Set the Address

MEMORY TYPE	READ AND WRITE ACCESS REGISTER
FRAM	FRAM_PAGE_ADDR
Data RAM	DATA_WAVE_PAGE_ADDR 0–7
Waveform RAM	DATA_WAVE_PAGE_ADDR 8–9
Development RAM	DEVRAM_PAGE_ADDR

In order to address a specific memory location, the lower 8 bits of the address must be provided as part of the digital-interface 8-bit address field. The remaining upper bits (6 bits for FRAM, 6 bits for development RAM and 4 bits for waveform and data RAM)must be specified in the corresponding page address register. That is, in order to access a certain memory location, the digital interface must first set the page-address bits by writing to the corresponding page-address register. In summary, the following are the steps required to access the memories:

1. Select the page address by writing to the page-address register using the digital-interface write command
2. For writing data to memory: Send the 8-bit address (corresponding to the lower 8 bits of the memory address) as part of the write command.
3. For reading data from memory: Send the 8-bit address (corresponding to the lower 8 bits of the memory address) as part of the read command.

7.3.1.13 One-Wire Interface (OWI)

The device includes a one-wire interface (OWI) digital communication interface. The function of OWI is to enable writes to and reads from all memory locations inside the PGA970 device that are available for OWI access.

7.3.1.13.1 Overview of OWI Interface

The OWI digital communication is a master-slave communication link in which the PGA970 device operates as a slave device only. The master device controls when data transmission begins and ends. The slave device does not transmit data back to the master until the master commands it to do so.

The V_{DD} pin of the PGA970 device is used as the OWI interface, so that when the PGA970 device is embedded inside a system module, only two pins are needed (V_{DD} and GND) for communication. The OWI master communicates with the PGA970 device by modulating the voltage on V_{DD} pin, whereas the PGA970 device communicates with the master by modulating current on the V_{DD} pin. The PGA970 microprocessor has the ability to control the activation and deactivation of the OWI interface based upon the OWI activation pulse driven on the V_{DD} pin.

Figure 24 shows a functionally equivalent circuit for the structure of the OWI circuitry.

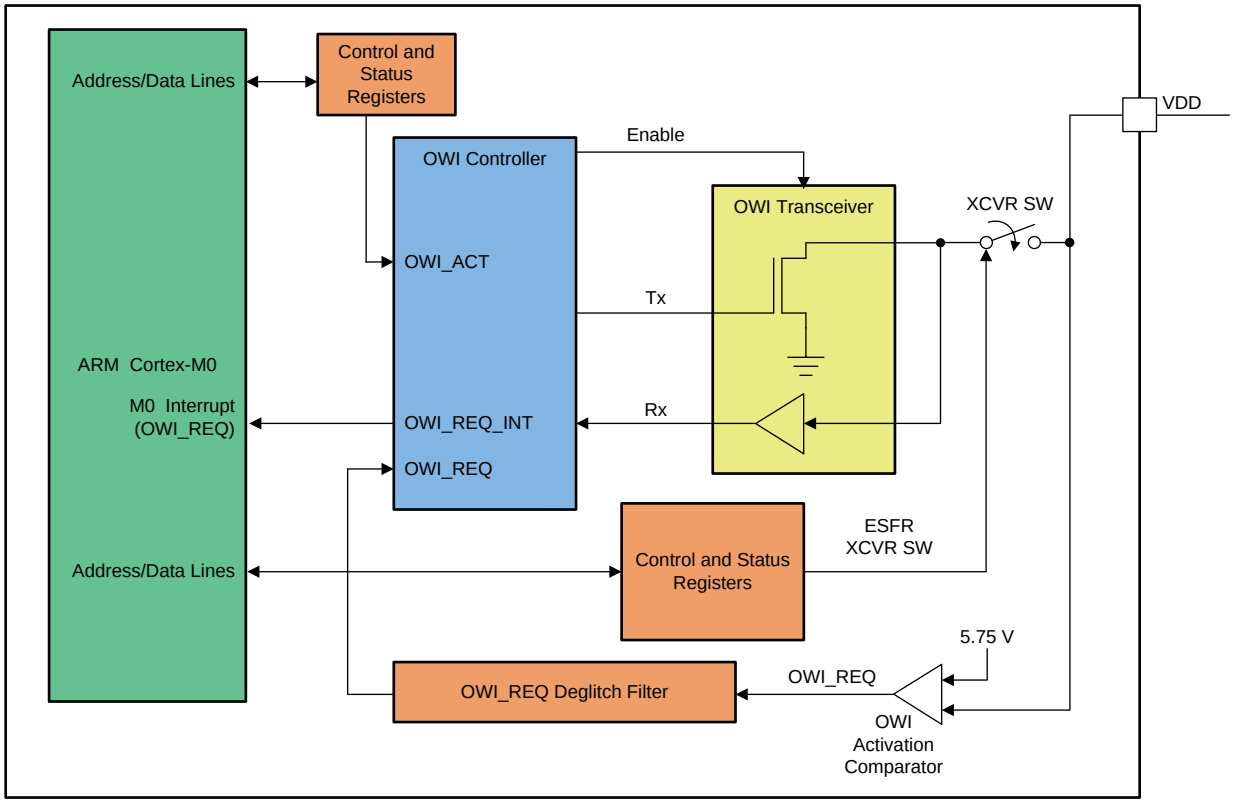


Figure 24. OWI System Components

NOTE

OWI communication is not possible if there is no program loaded in the device (that is, if the program memory is blank).

7.3.1.13.2 Activating and Deactivating the OWI Interface

7.3.1.13.2.1 Activating OWI Communication

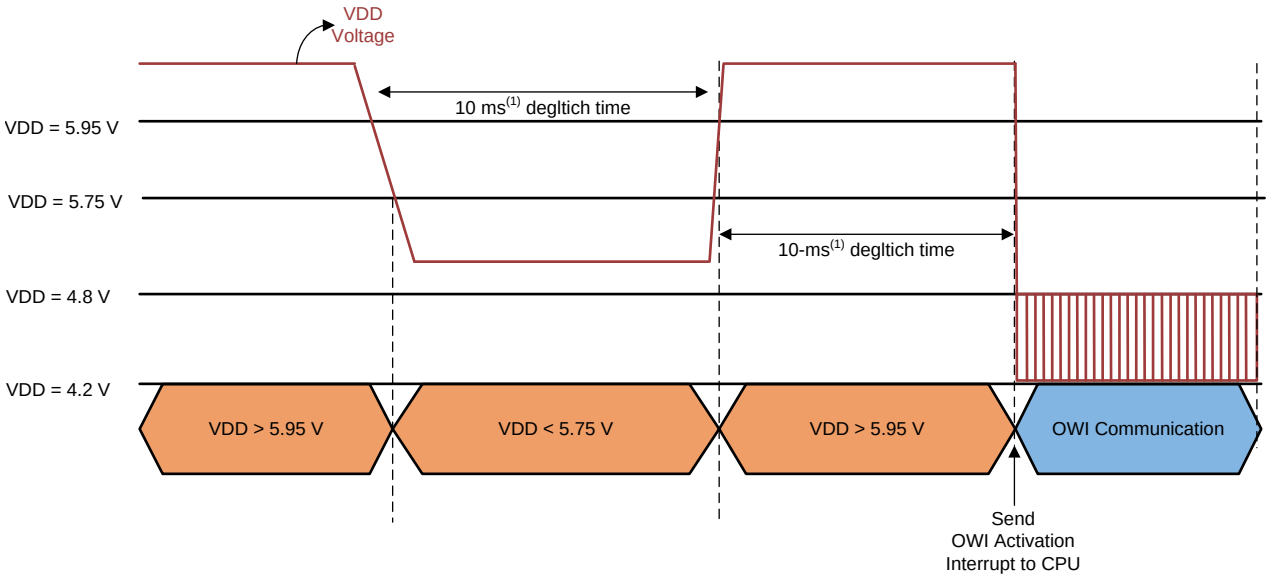
The OWI master initiates OWI communication by generating an OWI activation pulse on the V_{DD} pin. When the PGA970 device receives a valid OWI activation pulse, it prepares itself for OWI communication.

To activate OWI communication the following steps must be made in order:

1. OWI master: Generate an OWI activation pulse on the V_{DD} pin. Figure 24 shows the OWI activation pulse that is generated by the master. The OWI pulse is as follows:
   (a) Generate a *Low* pulse by driving the V_{DD} pin below 5.75 V. Note that the Low level must be greater than 3.5 V so that the PGA970 device can continue to operate. The duration of low pulse is determined by the OWI_DGL_CNT_SEL bit in the DIG_IF_CTRL register. This deglitch time is set by the OWI_DEGLITCH_SEL bit in the digital-interface control register (DIG_IF_CTRL) and has the following properties:
      – OWI_DGL_CNT_SEL = 0 → OWI activation deglitch time = 1 ms
      – OWI_DGL_CNT_SEL = 1 → OWI activation deglitch time = 10 ms
      – The default value for the OWI_DGL_CNT_SEL bit is 0, which corresponds to deglitch time of 1 ms.
   (b) Generate a *High* pulse by driving V_{DD} above 5.75 V. The duration of the high pulse is determined by the OWI_DGL_CNT_SEL bit in the DIG_IF_CTRL register.
2. PGA970 device: When the PGA970 device receives a valid OWI activation sequence on the V_{DD} pin, the

microprocessor receives an OWI activation interrupt. Note that the OWI activation interrupt is enabled by writing 1 to the OWI_INT_EN bit in the OW_INTERRUPT_EN register. The interrupt service routine for OWI activation must implement the following steps to enable OWI communication:

(a) Clear the OWI activation interrupt by writing 1 to the OWI_INT bit in the OWI_INTERRUPT register.
(b) Enable OWI by writing 1 to the OWI_EN bit in the DIG_IF_CTRL register.
(c) Connect the OWI transceiver to the V_{DD} pin by writing 1 to the OWI_XCR_EN bit in the DIG_IF_CTRL register.
(d) If the OWI master is to communicate to the PGA970 device with the microprocessor in reset, reset the microprocessor by writing 1 to the MICRO_RESET bit and 1 to the IF_SEL bit in the MICRO_INTERFACE_CONTROL register. If the OWI master is to communicate with the PGA970 device while the microprocessor is running, then the COMBUF registers are used for communication.



(1) Deglitch time can be programmed to either 1 ms or 10 ms

Figure 25. OWI Activation Using Overvoltage Drive, Deglitch Assumed to Be 10 ms

7.3.1.13.2.2 Deactivating OWI Communication

In order to deactivate OWI communication and restart the microprocessor inside the PGA970 device (if it was in reset), the microprocessor reset should be de-asserted by writing 0 to the MICRO_RESET bit in the MICRO_INTERFACE_CONTROL register.

7.3.1.13.3 OWI Protocol

7.3.1.13.3.1 OWI Frame Structure

7.3.1.13.3.1.1 Standard Field Structure:

Data is transmitted on the one-wire interface in byte-sized packets. The first bit of the OWI field is the start bit. The next 8 bits of the field are data bits to be processed by the OWI control logic. The final bit in the OWI field is the stop bit. A group of fields make up a transmission frame. A transmission frame is composed of the fields necessary to complete one transmission operation on the one-wire interface. The standard field structure for a one-wire field is shown in Figure 26

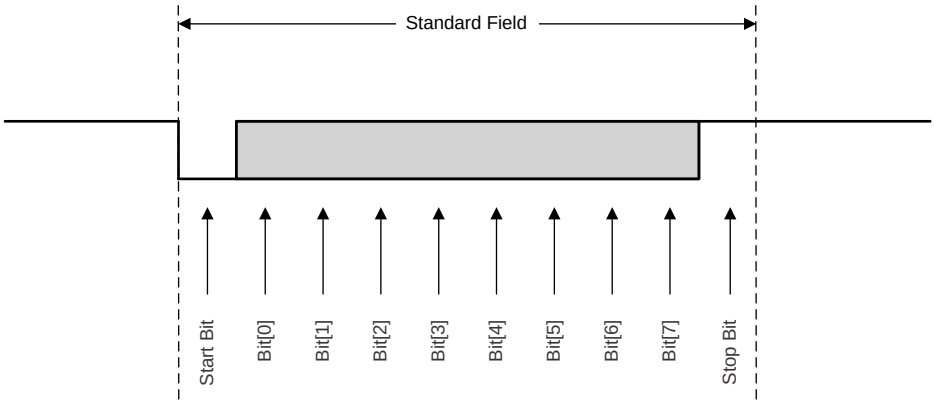


Figure 26. Standard OWI Field

7.3.1.13.3.1.2 Frame Structure

A complete one-wire data transmission operation is done in a frame with the structure is shown in Figure 27.

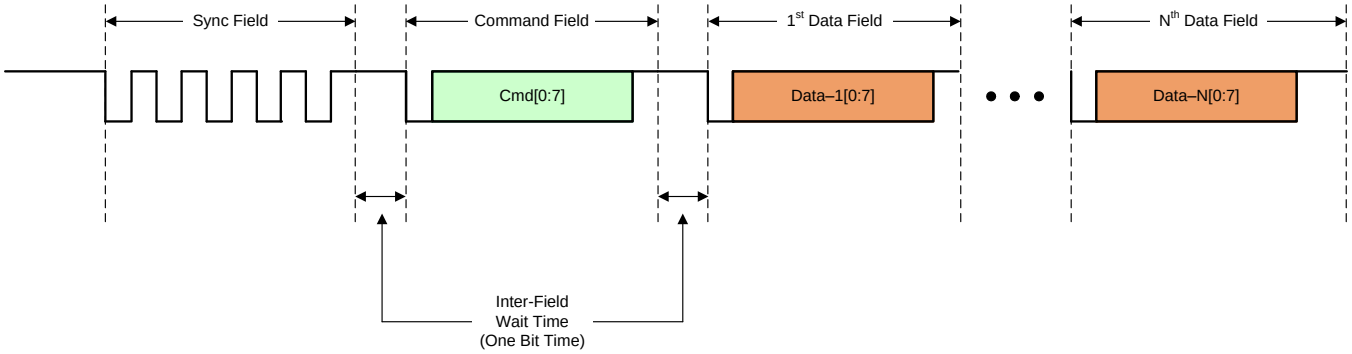


Figure 27. OWI Transmission Frame, N = 1 for Normal Read/Write and N = 8 for Burst Read/Write

Each transmission frame must have a synchronization field and command field followed by zero to a maximum of eight data fields. The sync field and command field are always transmitted by the master device. The data fields may be transmitted either by the master or the slave, depending on the command given in the command field. It is the command field which determines direction of travel of the data fields (master-to-slave or slave-to-master). The number of data fields transmitted is also determined by the command in the command field. The inter-field wait time is optional and may be necessary for the slave or the master to process data that has been received.

If OWI remains idle in either logic 0 or logic 1 state, for more than 15 ms, then the PGA970 communication resets and must receive a sync field as the next data transmission from the master.

7.3.1.13.3.1.3 Sync Field

The sync field is the first field in every frame that is transmitted by the master. The slave device uses the sync field to compute the bit width transmitted by the master. This bit width is used to receive accurately all subsequent fields transmitted by the master. The format of the sync field is shown in Figure 28.

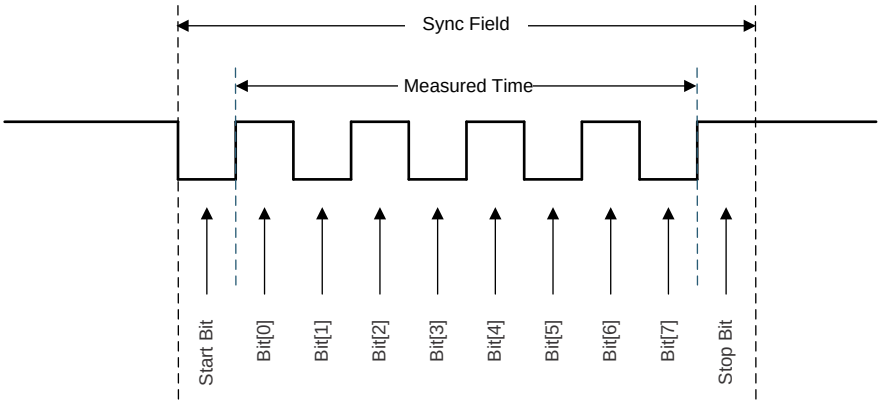


Figure 28. OWI Sync Field

NOTE

Consecutive SYNC field bits are measured and compared to determine if a valid SYNC field is being transmitted to the PGA970 device is valid. If the difference in bit widths of any two consecutive SYNC field bits is greater than ±25%, then the PGA970 device ignores the rest of the OWI frame; that is, the PGA970 device does not respond to the OWI message.

7.3.1.13.3.1.4 Command Field

The command field is the second field in every frame sent by the master. The command field contains instructions about what to do with and where to send the data that is transmitted to the slave. The command field can also instruct the slave to send data back to the master during a read operation. The number of data fields to be transmitted is also determined by the command in the command field. The format of the command field is shown in Figure 29.

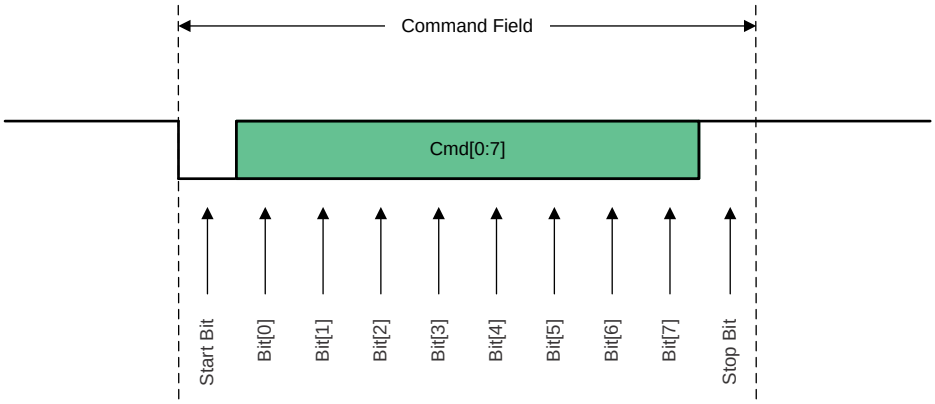


Figure 29. OWI Command Field.

7.3.1.13.3.1.5 Data Fields

After the master has transmitted the command field in the transmission frame, zero or more data fields are transmitted to the slave (write operation) or to the master (read operation). The data fields can be raw FRAM data or address locations in which to store data. The format of the data is determined by the command in the command field. The typical format of a data field is shown in Figure 30.

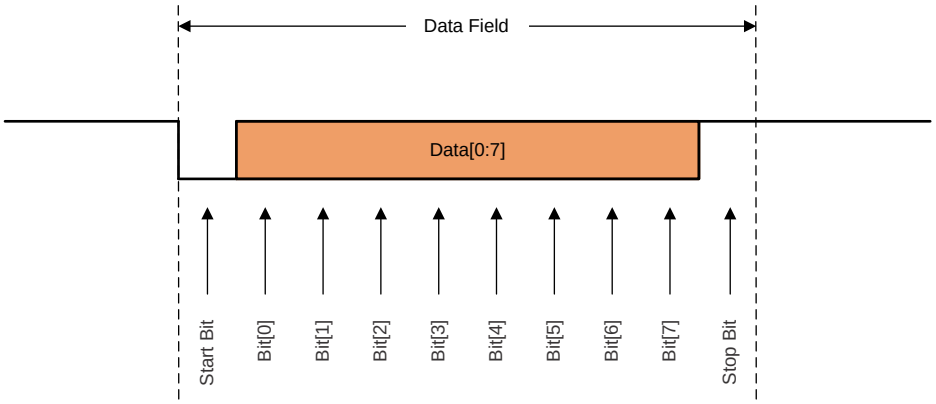


Figure 30. OWI Data Field.

7.3.1.13.3.2 OWI Commands

The following is the list of the eight OWI commands supported by the PGA970 device:

1. OWI write
2. OWI read initialization
3. OWI read response
4. OWI FRAM burst write
5. OWI development RAM burst write
6. OWI FRAM burst read
7. OWI development RAM burst read
8. OWI burst-read response

7.3.1.13.3.2.1 OWI Write Command

FIELD LOCATION	DESCRIPTION	7	6	5	4	3	2	1	0
Command field	Basic write command	**0**	P2	P1	P0	0	0	0	1
Data field 1	Destination address	A7	A6	A5	A4	A3	A2	A1	A0
Data field 2	Data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0

The P2, P1, and P0 bits in the command field determine the memory page that is being accessed by the OWI. The memory page decode is shown in Table 4.

Table 4. OWI Memory Page Decode

P2	P1	P0	MEMORY PAGE
0	0	0	Control and status registers, DI_PAGE_ADDRESS = 0x00
0	0	1	Data RAM, waveform RAM
0	1	0	Control and status registers, DI_PAGE_ADDRESS = 0x02
0	1	1	Development RAM
1	0	0	FRAM
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Control and status registers, DI_PAGE_ADDRESS = 0x07

The following sequence is an example to write 0x03 to the MICRO_INTERFACE_CONTROL register: 55 01 0C 03.

7.3.1.13.3.2.2 OWI Read Initialization Command

FIELD LOCATION	DESCRIPTION	7	6	5	4	3	2	1	0
Command field	Read initialization command	**0**	P2	P1	P0	0	0	1	0
Data field 1	Fetch address	A7	A6	A5	A4	A3	A2	A1	A0

The P2, P1, and P0 bits in the command field determine the memory page that is being accessed by the OWI. The memory page decode is shown in Table 4.

The following sequence is an example to initialize a read from the MICRO_INTERFACE_CONTROL register: 55 02 0C.

7.3.1.13.3.2.3 OWI Read Response Command

FIELD LOCATION	DESCRIPTION	7	6	5	4	3	2	1	0
Command field	Read response command	**0**	1	1	1	0	0	1	1
Data field 1	Data retrieved (OWI drives data out)	D7	D6	D5	D4	D3	D2	D1	D0

The following sequence is an example to read from the MICRO_INTERFACE_CONTROL register after a read initialization command is sent: 55 73.

7.3.1.13.3.2.4 OWI FRAM Burst Write Command

FIELD LOCATION	DESCRIPTION	7	6	5	4	3	2	1	0
Command field	FRAM write-command cache bytes (0–7)	1	1	0	0	0	0	0	1
Address field	Address to FRAM (lower 8 bits of the 14-bit FRAM address, right-shifted by 3)	0	0	0	0	0	0	0	0
Data field 1	1st data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 2	2nd data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 3	3rd data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 4	4th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 5	5th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 6	6th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 7	7th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 8	8th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0

The following sequence is an example to program 8 bytes of FRAM starting at memory address 0x1760 using the OWI digital interface:

1. Write 0x17 to the FRAM_PAGE_ADDR register using the OWI write command.

   55 21 18 17
2. Write 8 bytes using the OWI FRAM burst-write command. The address field value is 0xEC. This is obtained by right-shifting 0x1760 by 3 bits and taking the lower 8 bits.

   55 C1 EC <data1> <data2> <data3> <data4> <data5> <data6> <data7> <data8>

7.3.1.13.3.2.5 OWI Development RAM Burst-Write Command

FIELD LOCATION	DESCRIPTION	7	6	5	4	3	2	1	0
Command field	Development RAM write-command cache bytes (0–7)	1	0	1	1	0	0	0	1
Address field	Address to development RAM (lower 8 bits of the 14-bit development RAM address, right shifted by 3)	0	0	0	0	0	0	0	0
Data field 1	1st data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 2	2nd data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 3	3rd data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 4	4th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 5	5th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 6	6th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 7	7th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 8	8th data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0

The following sequence is an example to program 8 bytes of DEVELOPMENT RAM starting at memory address 0x1760 using the OWI digital interface:

1. Write 0x17 to the DEVRAM_PAGE_ADDR register using the OWI write command.
   55 21 1A 17
2. Write 8 bytes using the OWI DEVELOPMENT RAM burst-write command. The address field value is 0xEC. This is obtained by right-shifting 0x1760 by 3 bits and taking the lower 8 bits.
   55 B1 EC <data1> <data2> <data3> <data4> <data5> <data6> <data7> <data8>

7.3.1.13.3.2.6 OWI FRAM Burst Read Command

FIELD LOCATION	DESCRIPTION	7	6	5	4	3	2	1	0
Command field	FRAM burst read response (8 bytes)	1	1	0	0	0	0	1	0
Address field	Address to FRAM (lower 8 bits of the 14-bit FRAM address right shifted by 3)	0	0	0	0	0	0	0	0

The following sequence is an example to burst read from FRAM starting at address 0x1760 using the OWI digital interface:

1. Write 0x17 to the FRAM_PAGE_ADDR register using the OWI write command.
   55 21 18 17
2. Send a FRAM burst-read command. The address field value is 0xEC. This is obtained by right-shifting 0x1760 by 3 bits and taking the lower 8 bits.
   55 C2 EC

7.3.1.13.3.2.7 OWI Development RAM Burst-Read Command

FIELD LOCATION	DESCRIPTION	7	6	5	4	3	2	1	0
Command field	Development RAM burst-read response (8 bytes)	1	0	1	1	0	0	1	0
Address field	Address to development RAM (lower 8 bits of the 14-bit development RAM address, right-shifted by 3)	0	0	0	0	0	0	0	0

The following sequence is an example to burst read from development RAM starting at address 0x1760 using OWI Digital Interface:

1. Write 0x17 to DEVRAM_PAGE_ADDR register using the OWI write command.
   55 21 19 17
2. Send the development RAM burst-read command. The address field value is 0xEC. This is obtained by right-shifting 0x1760 by 3 bits and taking the lower 8 bits.
   55 B2 EC

7.3.1.13.3.2.8 OWI Burst-Read Response Command

FIELD LOCATION	DESCRIPTION	7	6	5	4	3	2	1	0
Command field	Burst-read response (8-bytes)	1	1	0	1	0	0	1	1
Data field 1	1st data byte to be read	D7	D6	D5	D4	D3	D2	D1	D0
Data field 2	2nd data byte to be read	D7	D6	D5	D4	D3	D2	D1	D0
Data field 3	3rd data byte to be read	D7	D6	D5	D4	D3	D2	D1	D0
Data field 4	4th data byte to be read	D7	D6	D5	D4	D3	D2	D1	D0
Data field 5	5th data byte to be read	D7	D6	D5	D4	D3	D2	D1	D0
Data field 6	6th data byte to be read	D7	D6	D5	D4	D3	D2	D1	D0
Data field 7	7th data byte to be read	D7	D6	D5	D4	D3	D2	D1	D0
Data field 8	8th data byte to be read	D7	D6	D5	D4	D3	D2	D1	D0

After sending FRAM or development RAM burst-read initialization command, read data by sending the following burst-read response command sequence: 55 D3.

7.3.1.13.3.3 OWI Operations

7.3.1.13.3.3.1 Write Operation

The write operation on the one-wire interface is fairly straightforward. The command field specifies the write operation, where the subsequent data bytes are to be stored in the slave, and how many data fields are to be sent. Additional command instructions can be sent in the first few data fields if necessary. The write operation is illustrated in Figure 31.

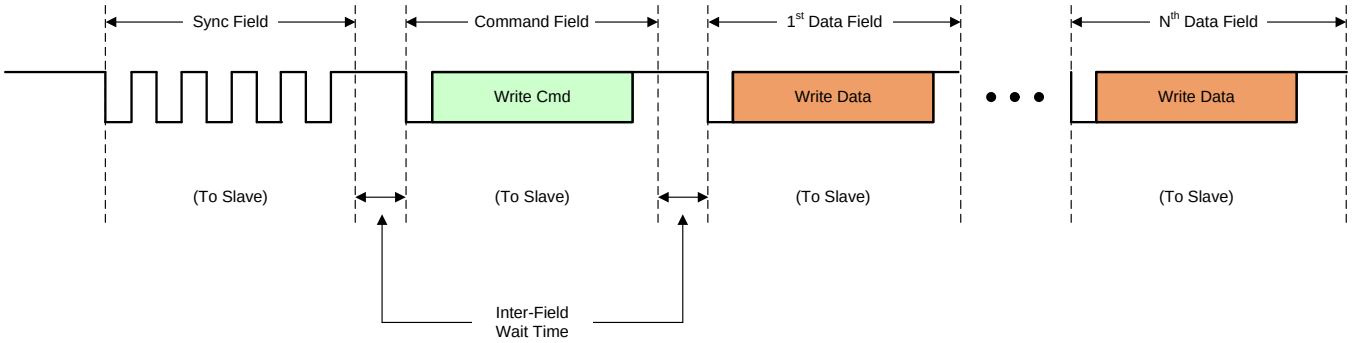


Figure 31. Write Operation, N = 1 for Normal Write and N = 8 for Burst Write

7.3.1.13.3.3.2 Read Operation

The read operation requires two consecutive transmission frames to move data from the slave to the master. The first frame is the read-initialization frame. It tells the slave to retrieve data from a particular location within the slave device and prepare to send it over the OWI. The data location may be specified in the command field or may require additional data fields for complete data location specification. The data is not sent until the master commands it to be sent in the subsequent frame called the read-response frame. During the read-response

frame, the data direction changes from master → slave to slave → master right after the read-response command field is sent. Enough time exists between the command field and data field in order to allow the signal drivers time to change direction. This wait time is 20 µs, and the timer for this wait time is located on the slave device. After this wait time is complete, the slave transmits the requested data. The master device is expected to have switched its signal drivers and be ready to receive data. The read frames are shown in Figure 32.

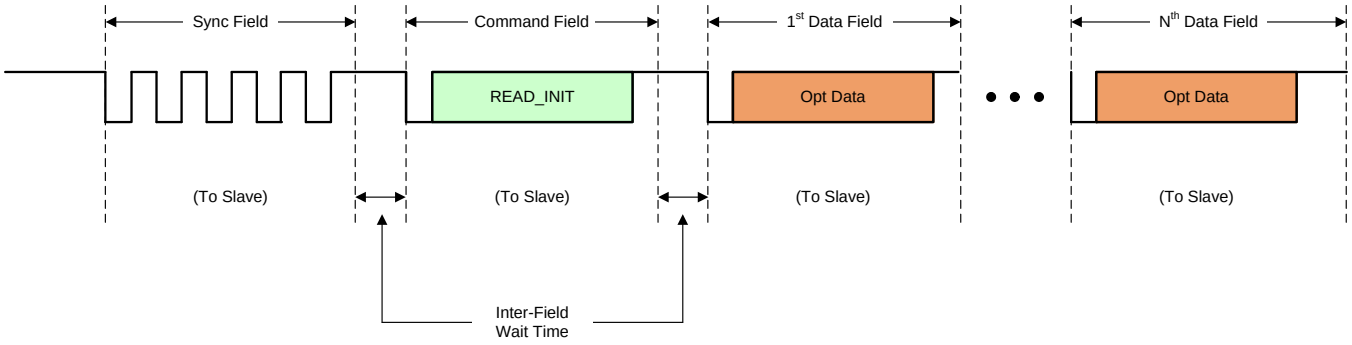


Figure 32. Read-Initialization Frame, N = 1

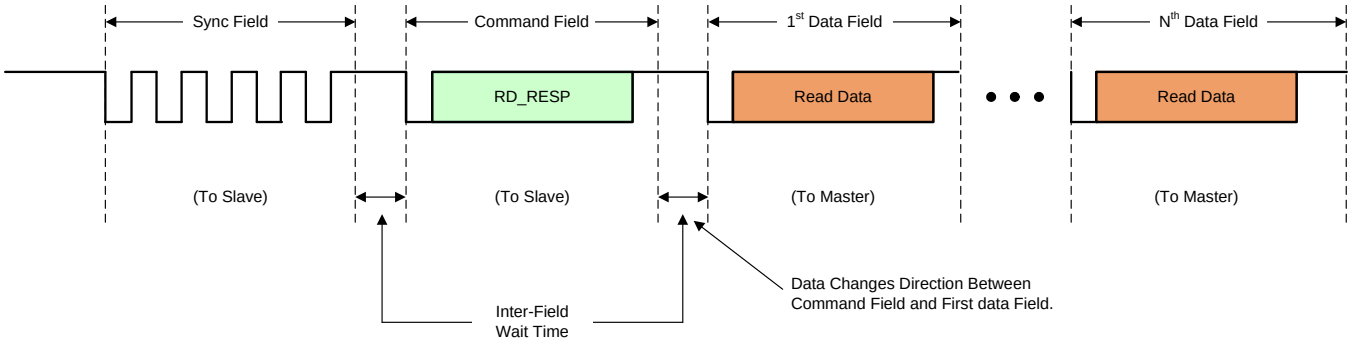


Figure 33. Read-Response Frame, N = 1 for Normal Read and N = 8 for Burst Read

7.3.1.13.3.3.3 FRAM and DEVELOPMENT RAM Burst Writes

The FRAM or development RAM burst write is used to write 8 bytes of data to FRAM or development RAM, respectively, using one OWI frame. This allows fast programming of FRAM in the manufacturing line.

7.3.1.13.3.3.4 FRAM and Development RAM Burst Read

The FRAM or development RAM burst read is used to read 8 bytes of data from FRAM or development RAM, respectively, using one OWI frame. The burst-read command is used for fast read of the FRAM contents in the manufacturing line. The read process is used to verify the writes to the FRAM.

7.3.1.13.4 OWI Communication Error Status

The PGA970 device detects errors in OWI communication. The OWI_ERROR_STATUS_LO and OWI_ERROR_STATUS_HI registers contain OWI communication error bits. The communication errors detected include

- Out-of-range communication baud rate
- Invalid SYNC field
- Invalid STOP bits in command and data
- Invalid OWI command

7.3.1.14 Serial Peripheral Interface (SPI) Interface

The device includes a serial peripheral interface (SPI) digital communication interface. The main function of the SPI is to enable writes to and reads from all addresses available for SPI access.

7.3.1.14.1 Overview of SPI Interface

SPI is a synchronous, serial, master-slave, communication standard that requires the following four pins:

- MOSI: SPI master-out, slave-in input pin
- MISO: SPI master-in, slave-out, serial output pin (high-impedance output)
- SCK: SPI clock, which controls the communication.
- CSN: Chip select (active-low)

SPI communicates in a master-slave style where only one device, the master, can initiate data transmissions. The PGA970 device always acts as the slave in SPI communication, where whatever external device that is communicating to it becomes the master. Both devices begin data transmission with the most-significant bit (MSB) first.

Because multiple slave devices can exist on one bus, the master node is able to notify the specific slave node that it is ready to begin communicating with by driving the CSN line to a low logic level.

7.3.1.14.2 Activating the SPI Interface

To activate SPI communication, perform the following steps in order:

1. Enable SPI by writing 1 to the SPI_EN bit in the DIG_IF_CTRL register.
2. Enable the digital interface by writing 1 to the IF_SEL bit in the MICRO_INTERFACE_CONTROL register.
3. If the SPI master is to communicate to the PGA970 device with the microprocessor in reset, reset the microprocessor by writing 1 to the MICRO_RESET bit in the MICRO_INTERFACE_CONTROL register. If the SPI master is to communicate with the PGA970 device while the microprocessor is running, then the COMBUF registers are used for communication.

7.3.1.14.3 SPI Interface Protocol

7.3.1.14.3.1 SPI Master to PGA970 Commands

The serial peripheral interface (SPI) is a 24-bit protocol with a 3-bit memory-access control word, a read-write bit, an 8-bit address, and an 8-bit data word. The command codes are described in Table 5.

Table 5. SPI Command Codes

BITS	FUNCTION	DESCRIPTION
23:21	DI PAGE ADDRESS	
	TEST = 000b	Access to control and status registers with DI PAGE ADDRESS = 0x0
	DATA and waveform RAM = 001b	Bits [11:8] of the data RAM address are specified by the DATA_WAVE_PAGE_ADDR register. Bits [7:0] of the data RAM address are specified by the data-address field of the SPI transaction.
	Control and status registers = 010b	Access to control and status registers with DI PAGE ADDRESS = 0x2
	Development RAM = 011b	Bits [13:8] of the development RAM address are specified by the DEVRAM_PAGE_ADDR register. Bits [7:0] of the development RAM address are specified by the data address field of the SPI transaction.
	FRAM = 100b	Bits [13:8] of the FRAM address are specified by the FRAM_PAGE_ADDR register. Bits [7:0] of the FRAM address are specified by the data address field of the SPI transaction.
	Reserved = 101b	Reserved
	Reserved = 110b	Reserved
	Reserved = 111b	Access to control and status registers with DI PAGE ADDRESS = 0x7
20:13	Data address	Address of register to read or write During reads, bit 13 is always zero. The reads always happen at 16-bit aligned addresses.
12	Write if 1, read if 0	
11:4	Data	
3:0	Don't care	

7.3.1.14.3.2 PGA970 Device to SPI Master Response

For SPI transfers to all the memories, the read data is available on the next SPI transfer, as shown in Figure 34. That is, when reading from a memory location, the user must send a subsequent transfer to get the data back. Further, the SPI response contains 16 bits of data. The logic returns data from a 16-bit aligned address; that is, SPI reads should not straddle a 16-bit address boundary.

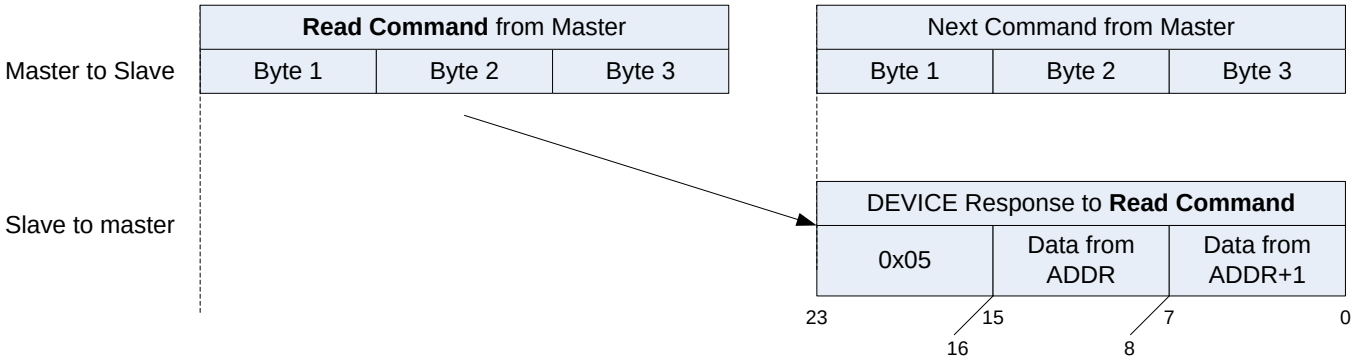


Figure 34. Response to SPI Read Commands Is Available When the Next Command Is Sent

The SPI response is described in Table 6. Note that only 2 bytes of data can be read with one SPI read command.

Table 6. SPI Response

BIT	FUNCTION
23:20	0000b
19:16	0101b
15:8	Read data from ADDR, where ADDR is received in the previous SPI command
7:0	Read data from ADDR + 1, where ADDR is received in the previous SPI command

7.3.1.14.3.3 SPI Command Examples

Table 7 lists a few examples of SPI transfers.

Table 7. SPI Transfer Examples

COMMAND	MASTER-TO-SLAVE DATA ON SPI MOSI
Read COM_MCU_TO_DIF_B0	000 00000100 0 XXXXXXXX 0000
Write 0x80 to control and status registers 0x30 (DAC_REG0_1)	010 00110000 1 10000000 0000
Write 0x34 to data SRAM 0x7F	1. Write 0 to DATA_WAVE_PAGE_ADDR: 010 00011001 1 00000000 0000 2. Send the following command to write data: 001 01111111 1 00110100 0000
Read from FRAM byte 7	101 00000111 0 XXXXXXXX 0000

7.3.1.14.4 Clocking Details of SPI Interface

Input data on the MOSI pin must be driven from the rising edge of the SCK clock, whereas output data on the MISO pin changes during the rising edge of the SCK clock. For SPI timing information, see *SPI Timing Requirements*.

7.3.1.15 DAC Output

The device includes a 14-bit digital-to-analog converter that produces an absolute output voltage with respect to the accurate reference voltage or ratiometric output voltage with respect to the V_{DD} supply. The DAC can be disabled by writing 0 to the DAC_ENABLE bit in the DAC_CTRL_STATUS register.

When the microprocessor undergoes a reset, the DAC registers are driven to 0x000 code.

7.3.1.15.1 Ratiometric vs Absolute

The DAC output can be configured to be either in ratiometric-to-V_{DD} mode or independent-of-V_{DD} (or absolute) mode using the DAC_RATIOMETRIC bit in DAC_CONFIG.

NOTE

In ratiometric mode, changes in the V_{DD} voltage result in a proportional change in the output voltage because the current reference for the DAC is derived from V_{DD}.

7.3.1.16 DAC Gain

The DAC gain buffer is a configurable buffer stage for the DAC output. The DAC gain amplifier can be configured to operate in voltage-amplification mode for voltage output or current-amplification mode for 4-mA to 20-mA applications. In voltage-output mode, DAC gain can be configured for a specific gain value by setting the DAC_GAIN bits in the DAC_CONFIG register to a specific value. The DAC gain can be configured to one of four possible gain configurations using the 2-bit DAC_GAIN field.

The final stage of DAC gain is connected to $V_{(ddp)}$ and ground. This gives the ability to drive the OUT voltage close to V_{DD}.

The DAC gain buffer also implements a COMP pin in order to allow implementation of compensation when driving large capacitive loads.

7.3.1.17 General-Purpose Input/Output (GPIO)

7.3.1.17.1 GPIO1 Through GPIO2

The device includes six general-purpose digital input/output pins. The two GPIO pins can be independently configured as input pin or output using the GPIOx_DIR bit in the GPIO_DIR register for the GPIO1–GPIO2 pins. When configured as an output pin, the output buffers can be configured in either open-drain output mode or push-pull output mode using the GPIOx_CFG bit in the GPIO_DIR register.

The microprocessor reads the state of the GPIO1–GPIO2 pins using the GPIOx_I bit in GPIO_INPUT register.

When the GPIO1–GPIO2 pins are configured as output pins, the microprocessor controls the output state by writing the desired value to the GPIOx_O bit in the GPIO_OUTPUT register.

7.3.1.18 Memory

7.3.1.18.1 FRAM Memory

The FRAM memory space is 16KB. This memory space contains program instructions for the M0 microprocessor, calibration data, and scratchpad RAM. If M0 is configured for 8-MHz operation, then appropriate WAIT states are used to allow access of FRAM.

The device has the ability to lock out access to all memory spaces from the digital interface. This allows users to protect firmware intellectual property.

7.3.1.18.1.1 FRAM Programming Using SPI

The FRAM memory can be programmed 1 byte at a time. The upper 6 bits of the 14-bit FRAM memory address must be loaded into the FRAM_PAGE_ADDR register. The remaining 8 bits of the FRAM address are included in the SPI protocol.

The following sequence is an example to program 0x12 to FRAM memory address 0x1764 using the SPI digital Interface:

1. Write 0x17 to the FRAM_PAGE_ADDR register: 010 00011000 1 00010111 0000
2. Write 0x12 to FRAM address 0x64: 100 01100100 1 00010010 0000

The programming sequence shows that two 24-bit commands must be transmitted to the PGA970 device in order to program 1 byte of FRAM. At 1 MHz, this translates to 48 µs. In addition, the SPI protocol requires 4 µs of chip-select disable time between two consecutive commands, and setup and hold times as shown in the SPI timing diagram in the *SPI Timing Requirements* section. Thus the total time to transmit 1 byte of FRAM data is 48 + (8) = 56 µs. In order to program all 16K bytes, the total time is 917.504 ms.

If the programming is done 256 bytes at a time with the starting address aligned to a 256-byte boundary, then the FRAM_PAGE_ADDR register must be programmed only once for programming 256 bytes. The total time to transmit 256 bytes of data is 257 × (24 + 4) = 7196 µs. In order to program all 16K bytes, the total time is 460.544 ms.

7.3.1.18.2 Development RAM Memory

The development RAM memory space is 16KB. This memory space contains is a shadow of FRAM. If M0 is configured for 8 MHz, then the instructions execute without WAIT states.

Note that in order for M0 to fetch instructions from development RAM, the firmware in FRAM must copy instructions from nonvolatile FRAM to volatile development RAM and must set the REMAP bit in the REMAP register to 1.

The device has the ability to lock out access to all memory spaces from the digital interface. This allows users to protect firmware intellectual property.

7.3.1.18.2.1 Development RAM Programming Using SPI

The DEVELOPMENT RAM memory can be programmed 1 byte at a time. The upper 6 bits of the 14-bit development RAM memory address must be loaded into the DEVRAM_PAGE_ADDR register. The remaining 8 bits of the DEVELOPMENT RAM address are included in the SPI protocol.

The following sequence is an example to program 0x35 to DEVELOPMENT RAM memory address 0x14A6 using the SPI digital interface:

1. Write 0x14 to the DEVRAM_PAGE_ADDR register: 010 00011010 1 00010100 0000
2. Write 0x35 to development RAM address 0xA6: 011 10100110 1 00110101 0000

The programming sequence shows that two 24-bit commands are to be transmitted to PGA970 in order to program 1 byte of developmenT RAM. At 1 MHz, this translates to 48 µs. In addition, the SPI protocol requires 4 µs of chip-select disable time between two consecutive commands, and setup and hold times as shown in the SPI timing diagram in the *SPI Timing Requirements* section. Thus the total time to transmit 1 byte of DEVELOPMENT RAM data is 48 + (8) = 56 µs. In order to program all 16K bytes, the total time is 802.816 ms.

If the programming is done 256 bytes as a time with the starting address aligned to a 256-byte boundary, then the DEVRAM_PAGE_ADDR register must be programmed only once for programming 256 bytes. The total time to transmit 256 bytes of data is 257 × (24 + 4) = 7196 µs. In order to program all 14K bytes, the total time is 402.976 ms.

7.3.1.18.3 Data and Waveform RAM Memory

The data RAM memory space is used for M0 scratchpad memory, such as intermediate calculation results. It is 2K bytes of RAM memory space, and located at memory page 1.

The waveform RAM memory space, used for waveform generation, is 512 bytes of RAM memory space located at memory page 1.

7.3.1.18.3.1 Data and Waveform RAM Programming Using SPI

The data and waveform RAM memory can be programmed 1 byte at a time. The upper 4 bits of the 12-bit data and waveform RAM memory address must be loaded into the DATA_WAVE_PAGE_ADDR register. The remaining 8 bits of the data and waveform RAM address are included in the SPI protocol.

The following sequence is an example to program 0x35 to DATA RAM memory address 0x2A6 using the SPI digital interface:

1. Write 0x02 to the DATA_WAVE_PAGE_ADDR register: 010 00011001 1 00000010 0000
2. Write 0x35 to data RAM address 0xA6: 001 10100110 1 00110101 0000

The programming sequence shows that two 24-bit commands must be transmitted to the PGA970 device in order to program 1 byte of DATA RAM. At 1 MHz, this translates to 48 µs. In addition, the SPI protocol requires 4 µs of chip-select disable time between two consecutive commands, and setup and hold times as shown in the SPI timing diagram in the *SPI Timing Requirements* section.

The following sequence is an example to program 0x35 to WAVEFORM RAM memory address 0x1A6 using the SPI digital interface:

1. Write 0x09 to DATA_WAVE_PAGE_ADDR register: 010 00011010 1 00001001 0000
2. Write 0x35 to WAVEFORM RAM address 0xA6: 001 10100110 1 00110101 0000

The programming sequence shows that two 24-bit commands must be transmitted to the PGA970 device in order to program 1 byte of WAVEFORM RAM. At 1 MHz, this translates to 48 µs. In addition, the SPI protocol requires 4 µs of chip-select disable time between two consecutive commands, and setup and hold times as shown in the SPI timing diagram in the *SPI Timing Requirements* section.

7.3.1.18.4 Control and Status Registers Memory

The M0 uses the control and data registers to interact with the analog blocks of the device.

7.3.1.18.5 FRAM Security

7.3.1.18.5.1 Definition of FRAM Security

FRAM security is defined as the inability to read FRAM memory contents via the digital interfaces (SPI and OWI) and software debugger. This feature is implemented in the PGA970 device in order to prevent download of FRAM contents once the device is deployed in the field.

7.3.1.18.5.2 FRAM Security in the PGA970 Device

In the PGA970 device, if FRAM security is enabled, access to all memories is disabled. That is, once security is enabled, the digital interface cannot access FRAM and RAM via the digital interfaces and debugger.

However, the COMBUF register is accessible even when security is enabled.

7.3.1.18.5.3 Enabling FRAM Security in the PGA970 Device

The PGA970 device has two registers to enable FRAM security.

1. SECLOCK register (8 bits)
   (a) Writing 0x00 enables access to all memories via the digital interface.
   (b) Writing 0xAA disables access to all memories via the digital interface.

   The reset value of the register is such that FRAM security is disabled.
2. The DEBUG_LOCK bit in the MICRO_INTERFACE_CONTROL register
   (a) Writing a 0 to this bit enables access via the software debugger.
   (b) Writing a 1 to this bit disables access via the software debugger.

   The reset value of the bit is 0.

7.3.1.18.5.4 Using FRAM Security in PGA970

The M0 firmware enables FRAM security by checking a FRAM bit (or bits) reserved for FRAM security. This software is executed at M0 start-up after M0 reset is deasserted. The pseudocode is:

1. If (Security bit reserved in FRAM is 1)
   (a) SECLOCK = 0xAA;
   (b) DEBUG_LOCK bit = 1;
2. Else
   (a) SECLOCK = 0x00;
   (b) DEBUG_LOCK bit = 0;
3. End

Using this method, if FRAM security is enabled in the manufacturing line before calibration is complete, then all accesses to memories are disabled. That is, the manufacturing tester cannot communicate with the PGA970 device anymore. Hence FRAM security cannot be disabled. **Therefore, FRAM security should be enabled as a last step on the manufacturing line.**

7.3.1.18.5.5 Sequence in Manufacturing Line

1. Ensure that the FRAM bits reserved for FRAM security correspond to *FRAM Security Disable* value.
2. Program the FRAM with firmware.
3. Perform all calibrations.
4. As a final step on the manufacturing line, program the FRAM bits corresponding to FRAM security to the *FRAM Security Enable* value.

7.3.1.19 Diagnostics

This section describes the diagnostics.

7.3.1.19.1 Power Supply Diagnostics

The device includes modules to monitor the power supply for faults. The internal power rails that are monitored are :

1. AVDD voltage, thresholds are generated using the high-voltage reference.
2. DVDD voltage, thresholds are generated using the high-voltage reference.
3. LVDT supply voltage, thresholds are generated using the internal voltage reference.
4. Reference output voltage, thresholds are generated using the high-voltage reference.

The *Diagnostics* section lists the voltage thresholds for each of power rails.

When a fault is detected, an appropriate bit in the PSMON1 and PSMON2 registers – a total of 16 bits and 16 individual faults – is set. Even after the faulty condition is removed, the appropriate fault bit remains latched. To remove the fault, M0 software should read the fault bit and write a logic 1 back to the bit. In addition, a system reset clears the fault.

NOTE

In case M0 is reset, OUT is driven to 0 V and all GPIO states are high-impedance.

7.3.1.19.2 LVDT Sensor Connectivity Diagnostics

The PGA970 device does not include specific circuits to monitor for the LVDT primary and secondary for open and short-circuit faults. Instead, the PGA970 device relies on the *sum of secondary voltages* method implemented in software to detect LVDT sensor connectivity faults (open and short-circuit faults).

7.3.1.19.3 S1 and S2 Gain Input Faults

The device implements a 1-MΩ pullup resistor and comparator to detect overvoltage conditions at each input of the S1 and S2 gain amplifiers.

In case of S1 or S2 input-open faults, the corresponding input pins are pulled up to AVDD.

When a fault is detected, the corresponding bit in the AFEDIAG register is set. Even after the faulty condition is removed, the fault bits remain latched. To remove the fault, M0 software should read the fault bit and write a logic zero back to the bit. In addition, a system reset clears the fault.

7.3.1.19.4 S3 Gain Input Faults

The device implements a comparator to detect overvoltage conditions at the input of the S3 gain amplifier. Figure 35 shows the diagnostics scheme implemented in the PGA970 device. Note that each channel input has its corresponding OV fault flag.

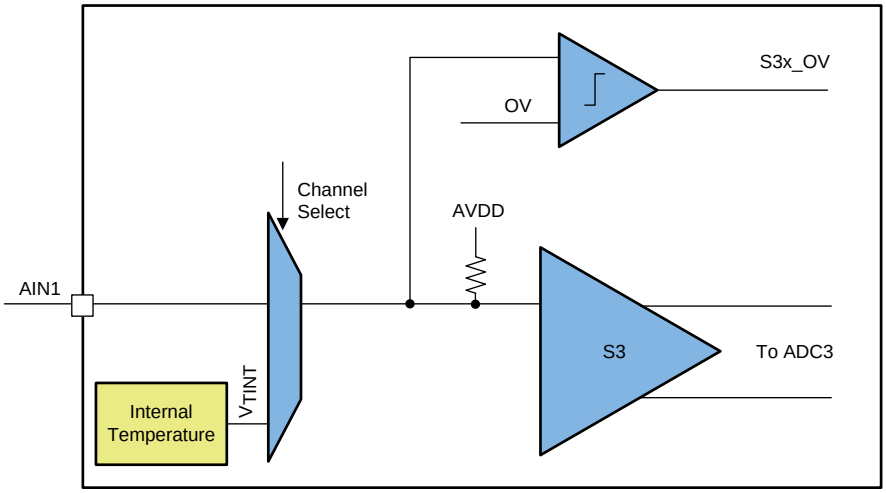


Figure 35. S3 Diagnostics

In case of S3 input-open faults, the input pins are pulled up to AVDD. The pullup, and hence the diagnostic, can be enabled or disabled using the AFEDIAG_CFG and AFEDIAG_CFG_1 registers.

When a fault is detected, the corresponding bit in the AFEDIAG register is set. Even after the faulty condition is removed, the fault bits remain latched. To remove the fault, M0 software should read the fault bit and write a logic zero back to the bit. In addition, a system reset clears the fault.

7.3.1.19.5 Sx Output Diagnostics

The device includes modules that verify that the output signal of each gain is below a threshold. This ensures that gain stages in the signal chain are working correctly. AVDD voltage is used to generate the voltage thresholds for comparison.

When a fault is detected, the corresponding bit in the AFEDIAG register is set. Even after the faulty condition is removed, the fault bits remain latched. To remove the fault, M0 software should read the fault bit and write a logic zero back to the bit. In addition, a system reset clears the fault.

7.3.1.19.6 ADC1 and ADC2 Signal-Chain Diagnostics Using Waveform Generator Loopback

The PGA970 device implements a *loopback* feature to check the integrity of the ADC1 and ADC2 signal chains. Figure 37 shows the block diagram representation of the loopback feature.

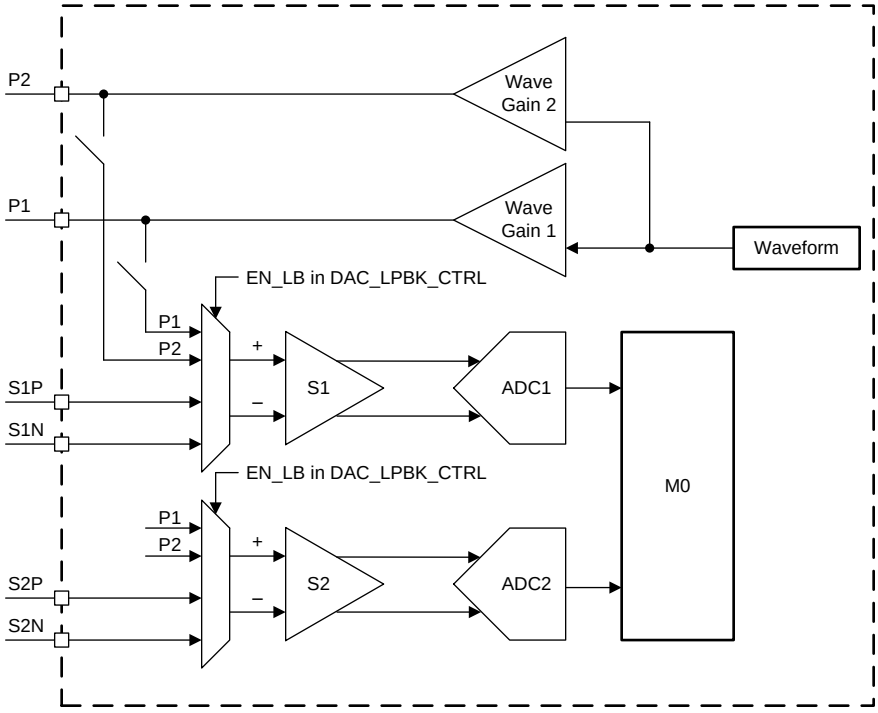


Figure 36. Waveform Loopback to ADC1 and ADC2

DAC loopback is enabled by setting the EN_LB bit in LVDT_LPBK_CTRL to 1. Note that the ADC output represents the voltage difference between DAC1 and the 1.2-V common-mode voltage scaled by the voltage divider and the AFE gains.

When loopback is enabled, the secondary coils are disconnected from the S1 and S2 gain amplifiers. If the P1 and P2 amplifiers are configured in single-ended mode, the S1 and S2 demodulator outputs have similar values.

The DAC outputs continue to be available on the OUT pin in the loopback mode.

7.3.1.19.7 ADC3 Signal Chain Diagnostics Using DAC Loopback

The PGA970 device implements a *loopback* feature to check the integrity of the signal chain. Figure 37 shows the block diagram representation of the loopback feature. This figure shows that the DAC output is connected to positive side of the differential input, and 1.5 V is connected to negative side of the differential input.

The DAC outputs are voltage-divided by a nominal factor of 5 before being connected to the AFE input.

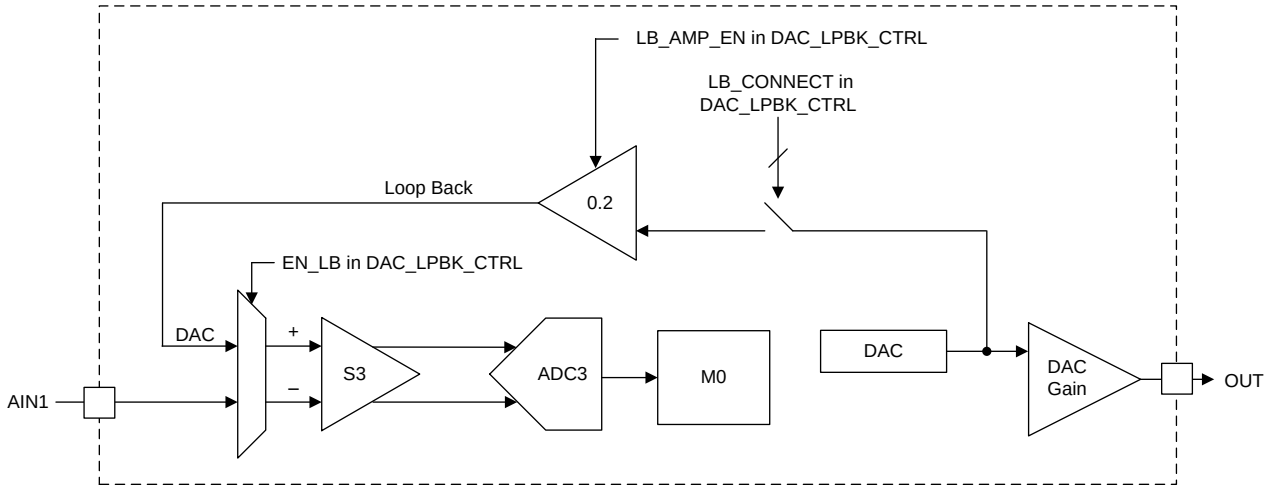


Figure 37. DAC Loopback to ADC3

DAC loopback is enabled by setting the LB_CONNECT, LB_AMP_EN, and EN_LB bits in DAC_LPBK_CTRL to 1. When loopback is enabled, the S3 mulitplexer is switched to buffered DAC output, and the analog sequential polling is disabled. However, digital polling continues, which means all the digital registers get the value corresponding to the DAC output. Note that the ADC output represents the voltage difference between DAC output and 1.2-V common-mode voltages scaled by the voltage divider and the AFE gains.

The DAC outputs continue to be available on the OUT pin in the loopback mode.

7.3.1.19.8 Harness Diagnostics

The PGA970 device allows for open-wire diagnostics to be performed in the ECU. Specifically, the solenoids are not activated when there is an open-harness condition.

Figure 38 shows the possible harness open-wire faults on the V_{DD} and GND pins.

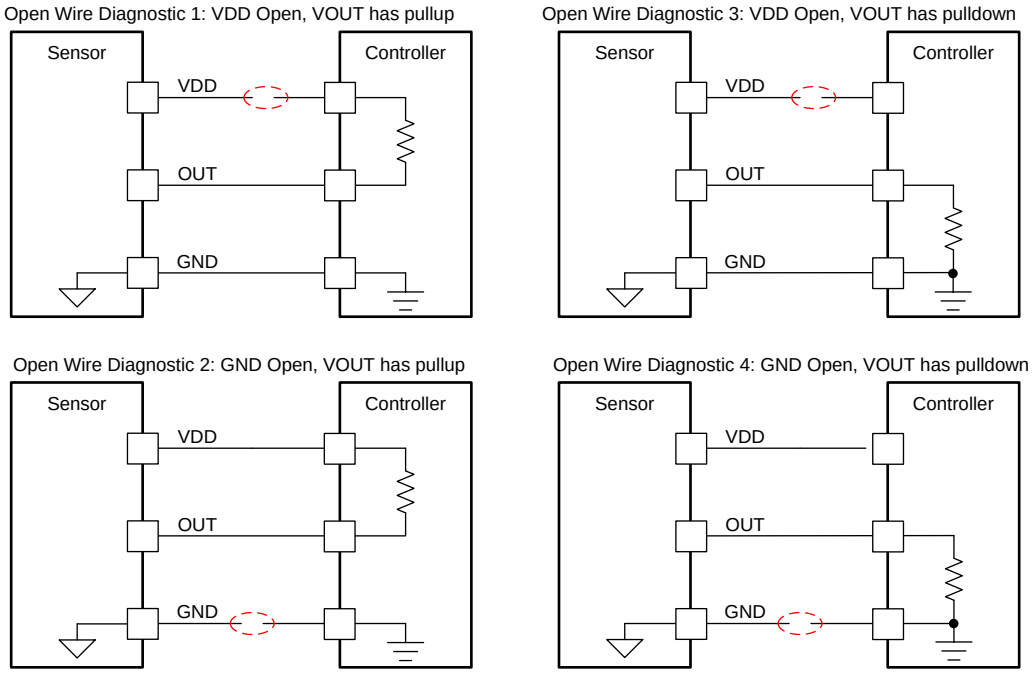


Figure 38. Harness Open-Wire Diagnostics

Table 8 lists the open-wire diagnostics and the corresponding resistor pull values that allow the ECU to detect open-harness faults.

Table 8. Typical Internal Pulldown Settings

OPEN HARNESS	ECU PULL DIRECTION	MAX. PULL VALUE (kΩ)	STATE OF PGA970 DURING FAULT CONDITION	ECU VOLTAGE LEVEL (OUT PIN)
V_{DD}	Pullup	200	PGA970 is off. Leakage currents present (especially at high temperature)	$V_{DD} – (I_{(leak1)} × R_{(pullup)})$
GND	Pullup	N/A	PGA970 is off, all power rails pulled up to V_{DD}	V_{DD}
V_{DD}	Pulldown	N/A	PGA970 is off, all power rails pulled down to ground	GND
GND	Pulldown	10	PGA970 is off, leakage current pushed into OUT pin (through the chip ground).	GND + $(I_{(leak2)} × R_{(pulldown)})$

CAUTION

If the FBN pin has intermittent disconnects, that is, the pin opens and reconnects, then the reconnect action could damage the device.

7.3.1.19.9 Software Windowed Watchdog

The PGA970 device includes a windowed software watchdog. The software watchdog can be enabled by writing 1 to the WDOG_EN bit in the WDOG_CTRL_STAT register. If the software watchdog is enabled, software must service the watchdog periodically by writing the maximum timeout value to the WDOG_TRIG_HIGH register.

The WDOG_TRIG_LOW register contains the minimum timeout value for the watchdog timer. The value written to the WDOG_TRIG_HIGH register corresponds to the maximum timeout value. The timeout value is (WDOG_TRIG_x + 1) × 2 ms. If the software does not service the watchdog before the timeout value, the microprocessor is reset. If the software services the watchdog before the minimum timeout value, the microprocessor is reset. In this case of microprocessor reset, all peripherals (including the digital interfaces) except the software watchdog are reset. That is, all control and status registers are set to their respective reset values, and the software watchdog continues to be enabled. Furthermore, the WD_RESET bit in WDOG_CTRL_STAT is set to 1 to indicate that the microprocessor recovered from a software watchdog time-out event. The WD_RESET_STS bit in the WDOG_CTRL_STAT register indicates if the watchdog reset occurred due to software servicing the watchdog before the minimum time-out value. The WD_RESET bit can be cleared by writing a 1 to the WD_RESET bit.

NOTE

The watchdog should be enabled (by writing 1 to the WDOG_EN bit) at least 10 µs after the WDOG_TRIG_LOW and WDOG_TRIG_HIGH registers have been configured.

In case M0 is reset, OUT is driven to 0 V and all GPIO states are high-impedance

7.3.1.19.10 Waveform RAM MBIST

The device implements waveform RAM memory built-in self-test (MBIST). This diagnostic checks the integrity of the internal waveform RAM on an on-demand basis.

The procedure to start this diagnostic and check for status is as follows:

1. Set the WRAM_MBIST_CTRL bits in the RAM_MBIST_CONTROL register to 11b. This starts the waveform RAM MBIST.
2. Wait for WRAM_MBIST_DONE in the RAM_MBIST_STATUS register to be set to 1 by the waveform RAM MBIST algorithm.
3. Check the WRAM_MBIST_FAIL bit in the RAM_MBIST_STATUS register after the WRAM_MBIST_DONE flag is set to 1. If WRAM_MIBIST_FAIL is 1, then waveform RAM MBIST failed, indicating faulty waveform RAM. If WRAM_MBIST_FAIL is 0, then waveform RAM has no faults.

The waveform RAM MBIST takes 2 ms to execute when M0 is configured to operate at 8 MHz. The software can continue execution as long as waveform RAM is not accessed.

NOTE

While the waveform RAM MBIST is running, the M0 should not access the waveform RAM.

The contents of waveform RAM are lost when MBIST is executed. Therefore, it is recommended that MBIST be run only at power up or microprocessor reset.

7.3.1.19.11 Data and Development RAM MBIST

The device implements data and development RAM memory built-in self-test (MBIST). This diagnostic checks the integrity of the internal data and development RAM on an on-demand basis.

The procedure to start this diagnostic and check for status is as follows:

1. Set the RAM_MBIST_CTRL bits in the RAM_MBIST_CONTROL register to 11b. This starts the data and development RAM MBIST.
2. Wait for RAM_MBIST_DONE in the RAM_MBIST_STATUS register to be set to 1 by the data and development RAM MBIST algorithm.
3. Check the RAM_MBIST_FAIL bit in the RAM_MBIST_STATUS register after the RAM_MBIST_DONE flag is set to 1. If RAM_MIBIST_FAIL is not 00b, then data and development MBIST failed, indicating faulty data and development RAM. If RAM_MBIST_FAIL is 0, then data and development RAM have no faults.

The data and development RAM MBIST takes 38 ms to execute when M0 is configured for 8 MHz. The software can continue execution as long as data and development RAM is not accessed.

NOTE

- While the data and development RAM MBIST is running, the M0 should not access the data and development RAM.
- Contents of data and development ram are lost when MBIST is executed. Therefore, it is recommended that MBIST be run only at power up or microprocessor reset.

7.3.1.19.12 Main Oscillator Watchdog

The PGA970 device includes a main-oscillator watchdog that resets the digital core when the main-oscillator frequency is out of range.

NOTE

In case M0 is reset, OUT is driven to 0 V and all GPIO states are high-impedance.

7.3.1.19.13 FRAM Parity

The PGA970 device implements even parity check for FRAM. Specifically, one parity bit is implemented for every 32 FRAM bits. When a parity error is detected during FRAM access by M0, the FRAM_ERR bit in the FRAM_STATUS register is set to 1, and the M0 microprocessor is reset to start executing code from reset vector location at 0x0000 0000.

Note that the FRAM_ERR bit is not cleared by M0 reset. The software can read this bit status at start-up and determine if a reset occurred due to a FRAM parity error.

NOTE

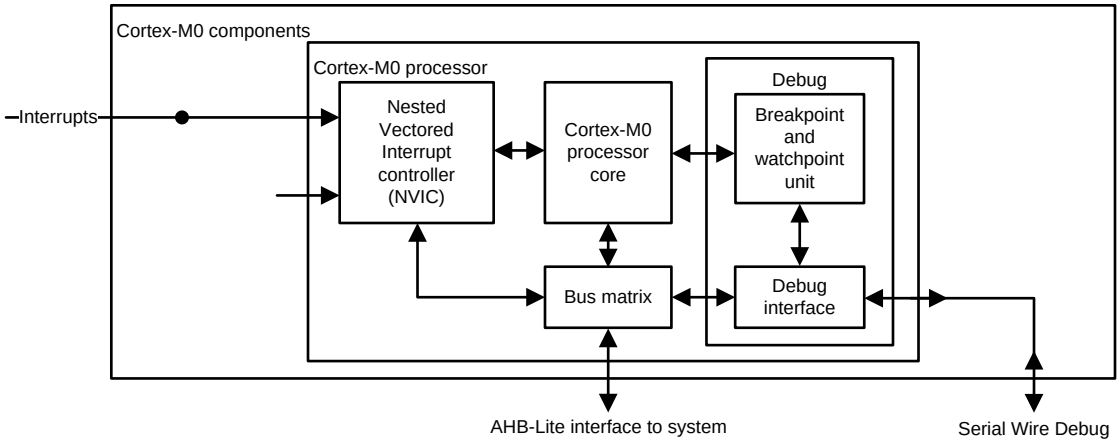
In case M0 is reset, OUT is driven to 0 V and all GPIO states are high-impedance.

7.3.1.20 ARM Cortex-M0 Microprocessor

The ARM Cortex-M0 microprocessor is an exceptionally high-performance version of this popular 32-bit microcontroller.

The microprocessor can be configured to run at different frequencies by setting the M0_FREQUENCY_CONTROL register. The reset state of the clock is 2 MHz. Note that with increased clock speed, the current consumption of the device increases.

The PGA970 device has a 32-bit signed multiplication and division operation. The multiplication operation is one clock cycle, whereas the divide operation is 10 cycles.



Note: Reproduced from ARM_M0_User_guide.

Figure 39. ARM Cortex-M0 Core

7.3.1.20.1 SYSTICK Timer

The Cortex-M0 microprocessor includes a 24-bit timer with a 1-µs update rate.

7.3.1.20.2 NVIC Controller

The Cortex-M0 microprocessor includes the nested vectored interrupt controller (NVIC). The peripheral interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. All NVIC registers are accessible using word transfers only. The NVIC in the PGA970 device is configured to support eight interrupts.

7.3.1.20.3 Software Debugger

The Cortex-M0 microprocessor includes the debugger. The PGA970 Cortex-M0 debugger includes the following features:

- Two breakpoints
- One watchpoint

7.3.1.20.4 Hardware Divider

The PGA970 device includes a 10-clock-cycle, signed 32-bit hardware-divider peripheral to speed up divide calculations. The firmware loads the numerator and denominator variables into the FAST_DIV_NUMERATOR and FAST_DIV_DENOMINATOR registers, respectively, and starts the division operation by setting the DIV_START bit in the FAST_DIV_CTRL register to 1. The DIV_COMPLETE bit in FAST_DIV_STAT is set to 1 when the division is complete. The quotient and remainder of the division process are available in the FAST_DIV_QUOTIENT and FAST_DIV_REMAINDER registers, respectively.

The DEN_ZERO bit in the FAST_DIV_STAT register is set to 1 if the denominator register is loaded with 0.

7.3.1.21 Digital Demodulation

The PGA970 device implements a demodulation algorithm that not only extracts the amplitude but also the phase of the signal with respect to the primary excitation.

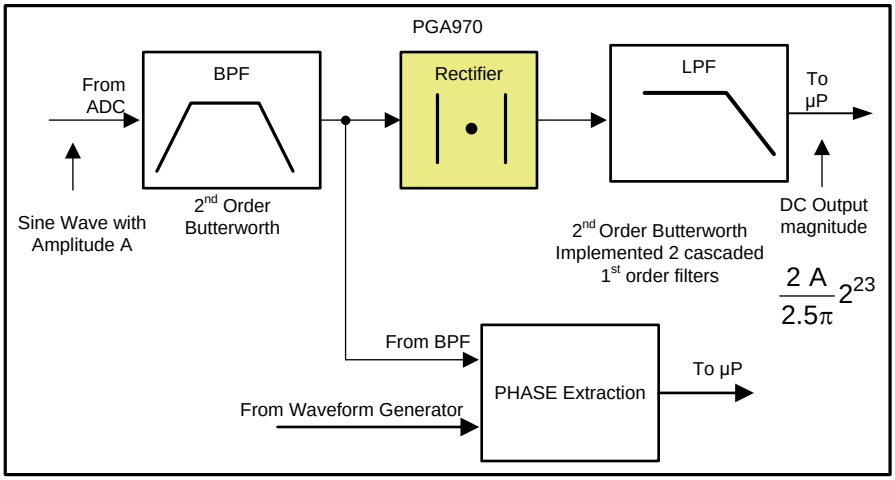


Figure 40. Digital Amplitude and Phase Demodulation

7.3.1.21.1 Amplitude

The amplitude demodulation consists of two filters – (1) band-pass filter (BPF) and (2) low-pass filter. Both filters are Butterworth filters. The bandwidth of the band-pass filter is configurable from 20 Hz to 1 kHz, and the center frequency is configurable from 1 kHz to 20 kHz. The cutoff frequency of the low-pass filter is configurable from 20 Hz to 2 kHz.

The output period of the amplitude information is either 128 µs or 256 µs.

7.3.1.21.2 Phase

The PGA970 device stores the output of the bandpass filter in two different programmable sample instances of the waveform generator in registers accessible to M0. Figure 41 shows an example in which the BPF output corresponding to 45° and 90° waveform phases are stored. Using these two values, M0 software can be used to infer the phase of the secondary output with respect to the waveform generator input.

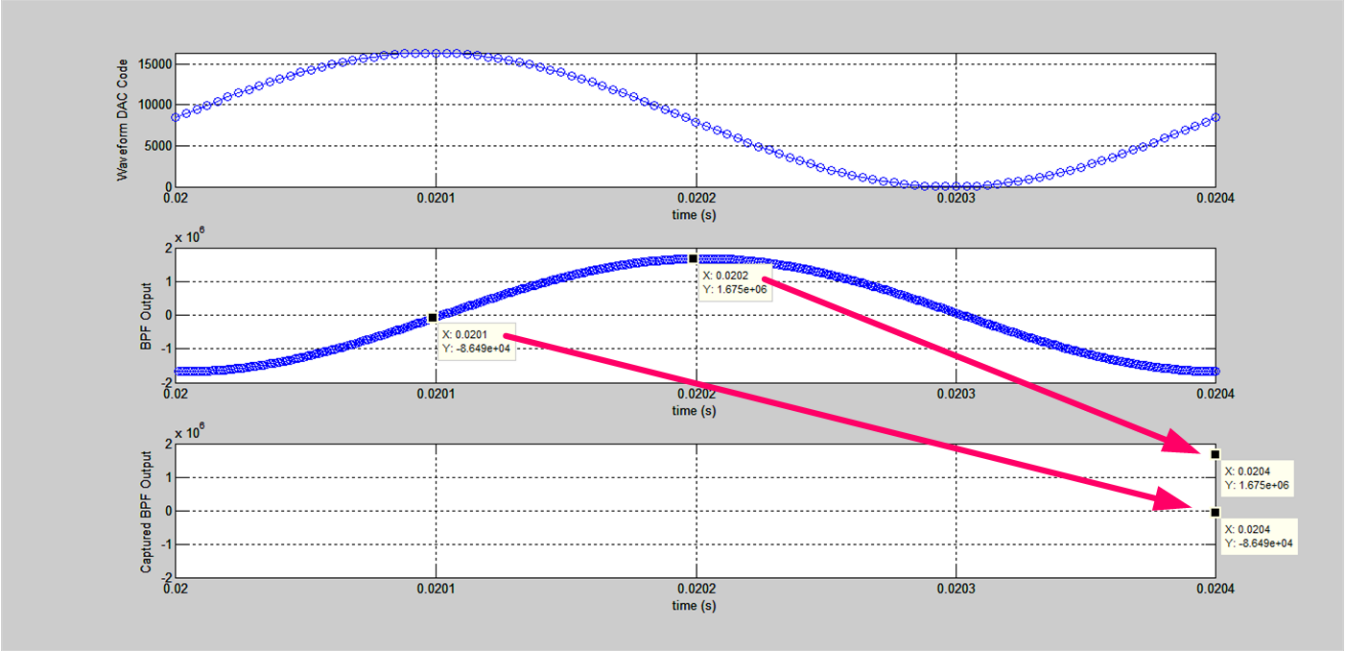


Figure 41. Phase Demodulation

7.3.1.22 Revision ID

The PGA970 device includes revision ID registers. These registers are read-only and represent the device revision and are not unique for every device in a certain revision.

7.3.1.23 Test MUX

The PGA970 device provides the ability to either stimulate the internal circuits from external sources or monitor the internal circuits by external sources. This is accomplished using the Test pins. For a description of the MUX settings, see *Control and Status Registers*.

7.4 Device Functional Modes

The PGA970 offers several analog output modes that provide flexibility for interfacing with a wide array of industrial-standard control units.

7.4.1 0-V to 10-V Absolute Output

To have a 0-V to 10-V absolute-voltage output mode, configure the DAC_GAIN bits found in the OP_STAGE_CTRL register to have a gain of 10 V/V.

Use the COMP and FBN pins to create a capacitive load-compensation network to allow the output stage of the PGA970 device to drive larger capacitive loads. Enabling the DACCAP_EN bit in the OP_STAGE_CTRL register and tying a capacitor between the DACCAP pin and GND provides additional filtering for the amplifier stage.

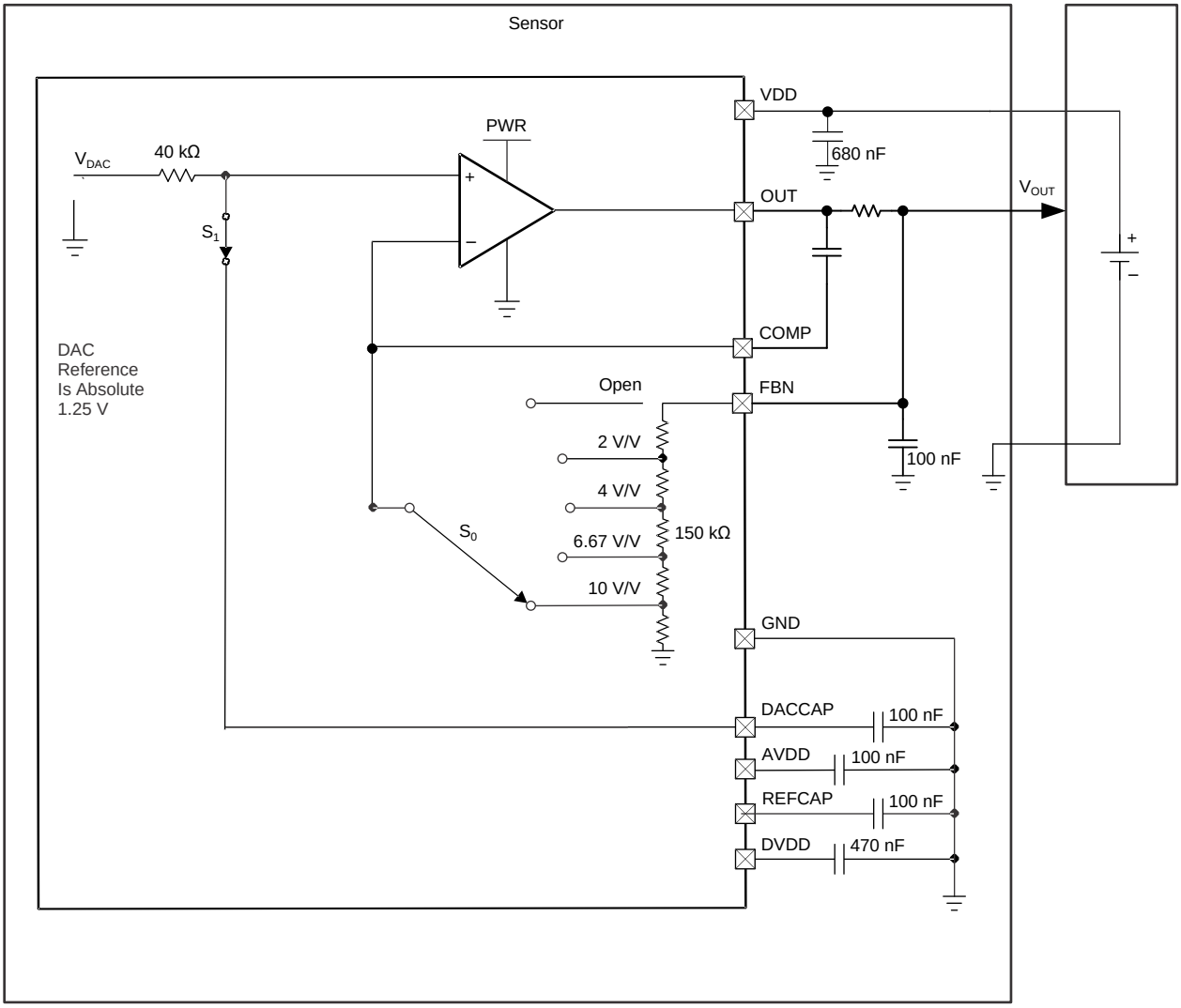


Figure 42. 0-V to 10-V Absolute Output

Device Functional Modes (continued)

7.4.2 0-V to 5-V Absolute Output

To have a 0-V to 5-V absolute-voltage output mode, configure the DAC_GAIN bits found in the OP_STAGE_CTRL register to have a gain of 4 V/V.

Use the COMP and FBN pins to create a capacitive load-compensation network to allow the output stage of the PGA970 device to drive larger capacitive loads. Enabling the DACCAP_EN bit in the OP_STAGE_CTRL register and tying a capacitor between the DACCAP pin and GND provides additional filtering for the amplifier stage.

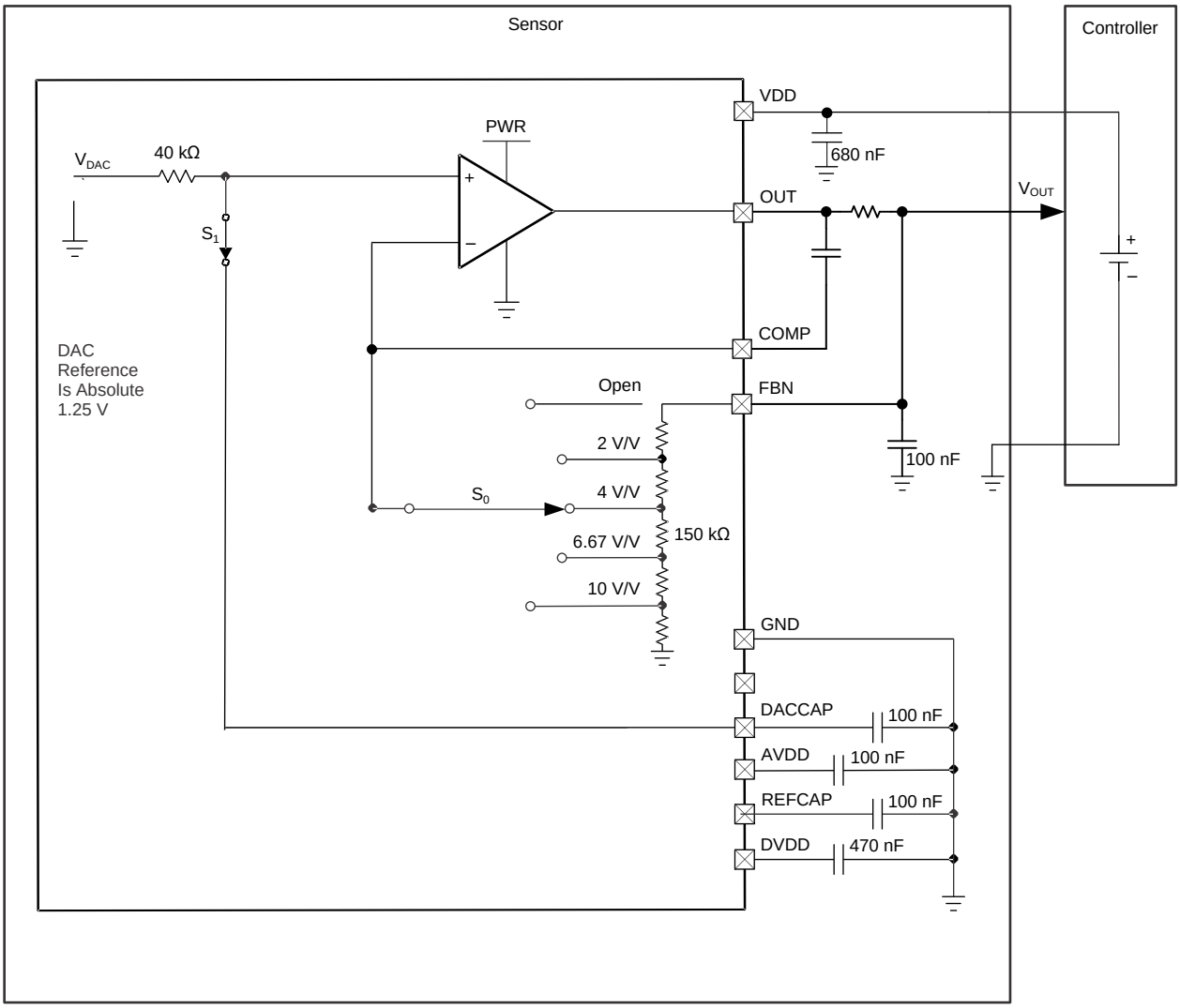


Figure 43. 0-V to 5-V Absolute or Ratiometric Mode

7.4.3 0-V to 5-V Ratiometric Output With Internal Drive

To have a 0-V to 5-V ratiometric-voltage output mode, configure the DAC_GAIN bits found in the OP_STAGE_CTRL to have a gain of 4 V/V. Additionally, the DAC_RATIOMETRIC bit in the DAC_CONFIG register should be set to 1. This causes OUT to adjust ratiometrically according to V_{DD}. Figure 43 shows the schematic for both 0-V to 5-V absolute and ratiometric mode.

Use the COMP and FBN pins to create a capacitive load-compensation network to allow the output stage of the PGA970 device to drive larger capacitive loads. Enabling the DACCAP_EN bit in the OP_STAGE_CTRL register and tying a capacitor between the DACCAP pin and GND provides additional filtering for the amplifier stage.

7.5 Programming Tips

This section provides programming tips to enable features in the device.

7.5.1 Resetting the Microprocessor and Enabling the Digital Interface

The following bits must be configured to reset the M0 microprocessor and to enable the digital interface:

1. Set the IF_SEL bit in the MICRO_INTERFACE_CONTROL register to 1.
2. Set the MICRO_RESET bit in the MICRO_INTERFACE_CONTROL register to 1.

7.5.2 Turning On the Accurate Reference Buffer (REFCAP Voltage)

The following bits must be configured to turn on the accurate reference buffer:

1. Set the SD bit in the ALPWR register to 0.
2. Set the ADC_EN_VREF bit in the ALPWR register to 1.

7.5.3 Turning On S1 Gain and S1 Demodulator

The following bits must be configured to turn on S1 Gain and S1 Demodulators:

1. Set the SD bit in the ALPWR register to 0.
2. Set ADC_EN_VREF bit in ALPWR register to 1.
3. Select the S1 gain value by writing to the S1_GAIN bits in the S1_CFG register.
4. Select single-ended or differential by writing to S1_SEM in the S1_CFG register.
5. If bias voltage is needed, write 1 to the VCM_EN bit in the S1_S2_CFG register.
6. If bias voltage is enabled, configure the bias voltage by writing to the BIAS_VCM bits in the S1_S2_CFG register.
7. Select the demodulator output rate by writing to DEMOD1_DECI_RATE in the DEMOD1_CONFIG register.
8. Configure the demodulator band-pass filter and low-pass filter by writing appropriate values to the following registers:
   - DEMOD1_BPF_B1
   - DEMOD1_BPF_A2
   - DEMOD1_BPF_A3
   - DEMOD1_LPF_B1
   - DEMOD1_LPF_A2
9. Enable the demodulator by writing 1 to DEMOD1_EN in the DEMOD1_CONFIG register.
10. Enable the demodulator clocks by writing 0x08 to the S1_S2_DEMOD_CFG_1 register.
11. Connect S1 gain to the S1 demodulator by writing 1 to the TEST_MUX_S1_EN bit in the AMUX_CTRL register.

7.5.4 Turning On S2 GAIN and S2 Demodulator

The following bits must be configured to turn on S2 Gain and S2 Demodulators:

1. Set the SD bit in the ALPWR register to 0.
2. Set the ADC_EN_VREF bit in the ALPWR register to 1.
3. Select the S2 gain value by writing to the S2_GAIN bits in the S2_CFG register.
4. Select single-ended or differential by writing to S2_SEM in the S2_CFG register.
5. If bias voltage is needed, write 1 to the VCM_EN bit in the S1_S2_CFG register.
6. If bias voltage is enabled, configure the bias voltage by writing to the BIAS_VCM bits in the S1_S2_CFG register.
7. Select the demodulator output rate by writing to DEMOD2_DECI_RATE in the DEMOD2_CONFIG register.
8. Configure the demodulator band-pass filter and low-pass filter by writing appropriate values to the following registers:
   - DEMOD2_BPF_B1
   - DEMOD2_BPF_A2

Programming Tips (continued)

- DEMOD2_BPF_A3
- DEMOD2_LPF_B1
- DEMOD2_LPF_A2

9. Enable the demodulator by writing 1 to DEMOD2_EN in the DEMOD2_CONFIG register.
10. Enable the demodulator clocks by writing 0x08 to the S1_S2_DEMOD_CFG_1 register.
11. Connect S2 gain to the S2 demodulator by writing 1 to the TEST_MUX_S2_EN bit in the AMUX_CTRL register.

7.5.5 Turning on S3 GAIN and ADC

The following bits must be configured to turn on S3 Gain and S3 ADC:

1. Set the SD bit in the ALPWR register to 0.
2. Set the ADC_EN_VREF bit in the ALPWR register to 1.
3. Select the S3 gain value by writing to the AIN1_GAIN bits in the S3_CFG register for AIN1, and the PTAT_GAIN bits in the S3_CFG_1 register for PTAT.
4. Configure the low-pass filter by writing appropriate values to the following registers:
   - ADC3_AIN1_LPF_B1
   - ADC3_AIN1_LPF_A2
   - ADC3_PTAT_LPF_B1
   - ADC3_PTAT_LPF_A2
5. Enable the S3 ADC by writing 1 to ADC3_EN in the ADC3_CONFIG register.
6. Enable the S3 ADC clock by writing 0x08 to the S3_ADC_CFG_1 register.
7. Connect S3 gain to the S3 ADC by writing 1 to the TEST_MUX_S3_EN bit in the AMUX_CTRL register.

7.5.6 Turning on the Waveform Generator

The following bits must be set to turn waveform generator:

1. Set the SD bit in the ALPWR register to 0.
2. Set the ADC_EN_VREF bit in the ALPWR register to 1.
3. Turn off the waveform DAC by writing 0 to the WAVE_EN bit in the WAVEFORM_GEN_CTRL register.
4. Load the waveform RAM with quarter-waveform values. For example, to generate a sine wave of amplitude amp and frequency freq, calculate waveform table values using the formula: amp × sin(2πfreq × (0.5 µs + n1 µs)), n = 0..N. N is the number of 1-µs samples in a quarter-sine wave.
5. Program the N – 1, where N is quarter-waveform table length (value from the previous step) into the WAVEFORM_TABLE_LEN register .
6. Program the dc bias of the waveform DAC into the WAVEFORM_DAC_OFFSET register. The value is calculated as: round(DCValue / 1.25 × 16 384). Note that the dc value generated by the waveform generator should match the waveform gain bias (configuration described as follows).
7. Configure the WAVE_GAIN gain value by writing to the GAIN_CTRL bits in the LVDT_OP_CTRL register.
8. Configure the WAVE_GAIN amplifier for single-ended or differential mode of operation by writing to the SEM bit in the LVDT_OP_CTRL register.
9. Configure the WAVE_GAIN bias voltage to match the bias value selected in the preceding Step 6 by writing to the DACVCM_CTRL bits in the LVDT_OP_CTRL register.
10. If WAVE GAIN is configured for differential mode, configure the differential-amplifier output common-mode voltage by writing to the DIFF_VOCM_CTRL bits in the LVDT_OP_CTRL register.
11. Select either internal or external connection between the PI and PE pins by configuring the SKIP_FILTER bit inthe LVDT_OP_CTRL register.
12. Connect the waveform DAC to WAVE GAIN by writing 0xF to the TEST_MUX_LVDT_EN bits in the AMUX_CTRL register.
13. Ensure EN_LB in the LVDT_LPBK_CTRL register is set to 0 to disable loopback.
14. Enable the waveform DAC by writing 1 to WAVE_EN in the WAVEFORM_GEN_CTRL register.

Programming Tips (continued)

7.5.7 Turning on DAC and DAC Gain

The following bits must be configured to turn on the DAC and DAC_GAIN amplifier stage:

1. Set the SD bit in the ALPWR register to 0.
2. Set the ADC_EN_VREF bit in the ALPWR register to 1.
3. Set DAC_ENABLE in DAC_CTRL_STATUS to 1.
4. Set the DACCAP_EN bit in OP_STAGE_CTRL to connect or disconnect an external capacitor at the DAC output.
5. Set the DAC_RATIOMETRIC bit in DAC_CONFIG register for ratiometric or absolute voltage output mode.
6. Configure DAC gain by writing to the DAC_GAIN bits in the OP_STAGE_CTRL register.
7. Set TEST_MUX_DAC_EN in AMUX_CTRL to 1.
8. Ensure loopback is disabled by writing 0 to the DAC_LPBK_CTRL register.

7.5.8 Turning On Gate Control

The following bits must be configured to turn on DAC and DAC GAIN:

1. Set the GATE_CTRL_SD bit in the ALPWR register to 0.
2. Configure the voltage by setting the GATE_3P3_CTRL bit in the OP_STAGE_CTRL register.

7.6 Register Maps

7.6.1 Memory Map

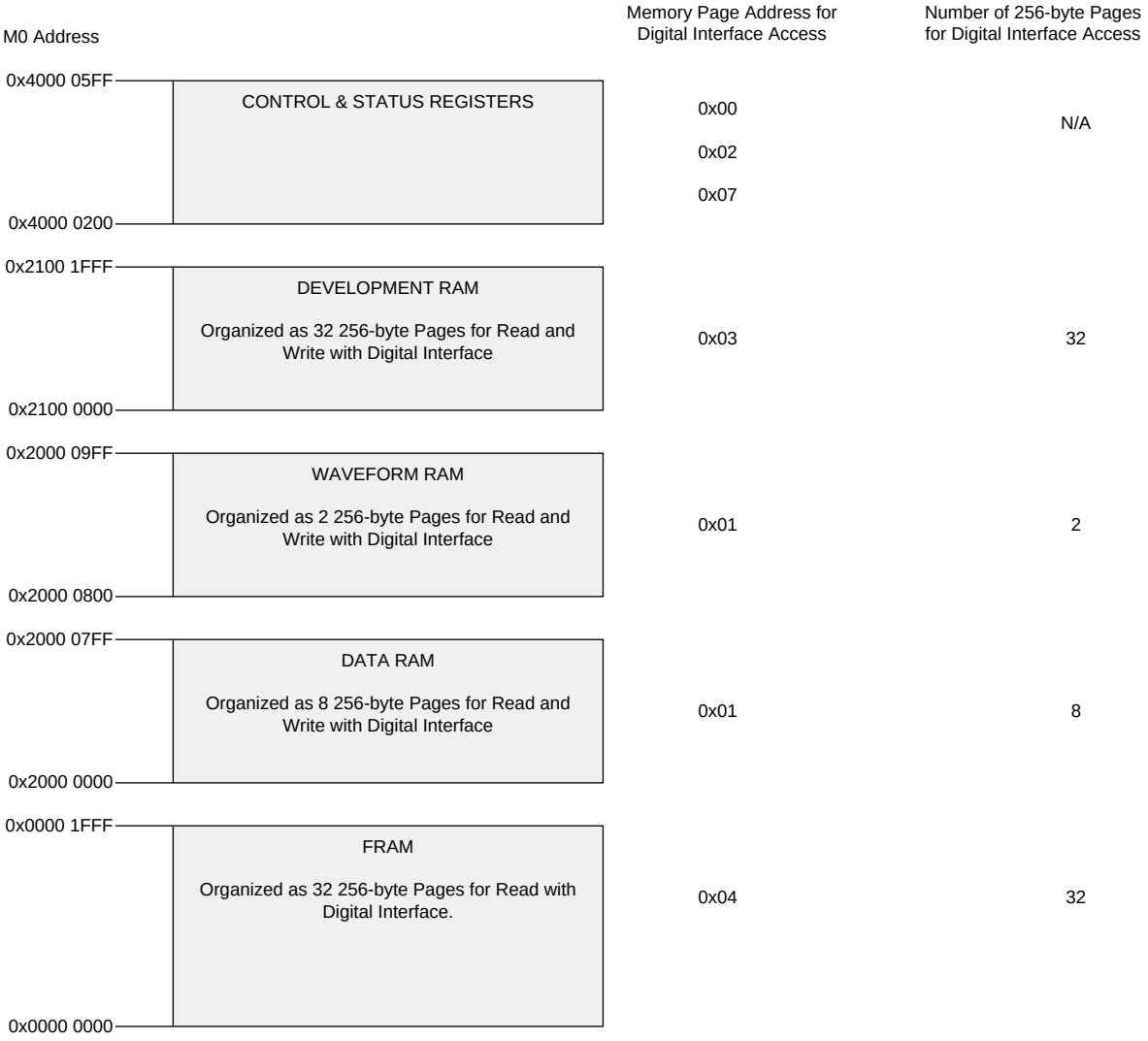


Figure 44. Memory Map When REMAP = 0

Register Maps (continued)

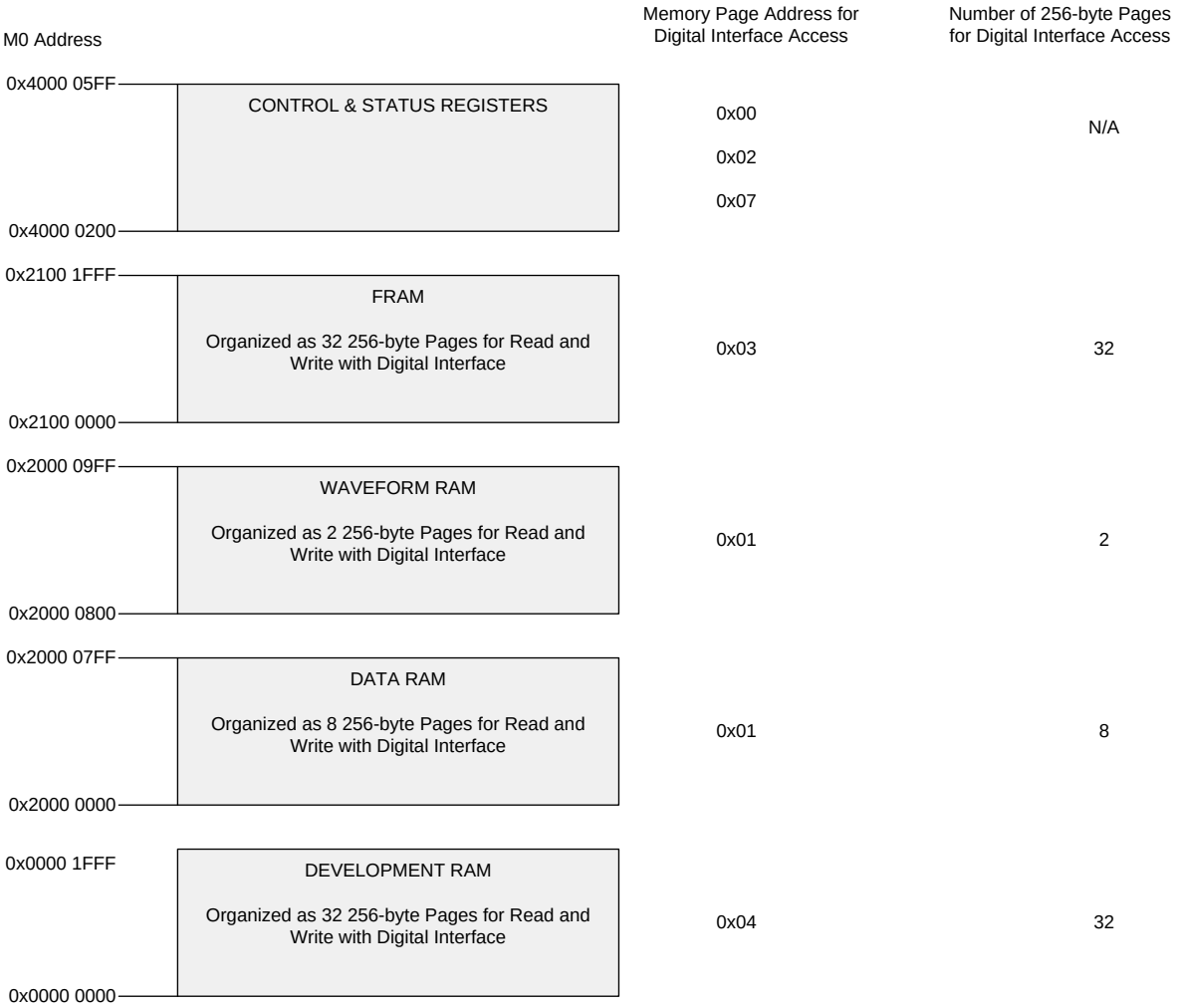


Figure 45. Memory Map When REMAP = 1

7.6.2 Control and Status Registers

Table 9. Control and Status Registers

Register Name	DI Page Address	DI Offset Address	M0 Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
RAMBIST_ CONTROL	0x2	0x02	0x4000 0502	RW					RAM_MBIST _CTRL[1]	RAM_MBIST _CTRL[0]	WRAM_MBIST _CTRL[1]	WRAM_MBIST _CTRL[0]
RAMBIST_ STATUS	0x2	0x03	0x4000 0503	R			RAM_MBIST_ FAIL[1]	RAM_MBIST_ FAIL[0]	RAM_MBIST_ DONE		WRAM_MBIST_ FAIL	WRAM_MBIST_ DONE
CLK_CTRL_STATUS	0x2	0x04	0x4000 0504	RW			CLK_STATUS[1]	CLK_STATUS[0]			CLK_CTRL[1]	CLK_CTRL[0]
FRAM_STATUS	0x2	0x04	0x4000 0505	R						FRAM_ERR		
DIG_IF_CTRL	0x2	0x06	0x4000 0506	RW				OWI_DGL_CNT_ SEL	OWI_XCVR_EN	OWI_EN		SPI_EN
OWI_ERROR_ STATUS_LO	0x2	0x08	0x4000 0508	R	OWI_ERR7	OWI_ERR6	OWI_ERR5	OWI_ERR4	OWI_ERR3	OWI_ERR2	OWI_ERR1	OWI_ERR0
OWI_ERROR_ STATUS_HI	0x2	0x09	0x4000 0509	R	OWI_ERR_CLR						OWI_ERR9	OWI_ERR8
OWI_ INTERRUPT	0x2	0x0A	0x4000 050A	RW								OWI_INT
OWI_ INTERRUPT_ ENABLE	0x2	0x0B	0x4000 050B	RW								OWI_INT_EN
FRAM_PAGE_ ADDR	0x2	0x18	0x4000 0518	RW			ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
DATA_WAVE_ PAGE_ADDR	0x2	0x19	0x4000 0519	RW					ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
DEVRAM_PAGE_ ADDR	0x2	0x1A	0x4000 051A	RW			ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
WDOG_CTRL_STAT	0x2	0x1C	0x4000 051C	RW	WD_RESET	WD_RESET _STATUS						WDOG_EN
WDOG_TRIG_HIGH	0x2	0x1D	0x4000 051D	RW	TRIG[7]	TRIG[6]	TRIG[5]	TRIG[4]	TRIG[3]	TRIG[2]	TRIG[1]	TRIG[0]
WDOG_TRIG_LOW	0x2	0x1E	0x4000 051E	RW	TRIG[7]	TRIG[6]	TRIG[5]	TRIG[4]	TRIG[3]	TRIG[2]	TRIG[1]	TRIG[0]
DEMOD1_CONFIG	0x2	0x20	0x4000 0520	RW						DEMOD1_DEC1_ RATE		DEMOD1_EN
DEMOD2_CONFIG	0x2	0x21	0x4000 0521	RW						DEMOD2_DEC1_ RATE		DEMOD2_EN
ADC3_CONFIG	0x2	0x22	0x4000 0522	RW								ADC3_EN
S1_S2_DEMOD_CFG_1	0x2	0x24	0x4000 0524	RW					DEMOD_EN		RESET_CLK	RESET_MOD
S3_ADC_CFG_1	0x2	0x26	0x4000 0526	RW						ADC_EN	RESET_CLK	RESET_MOD
S1_CFG	0x2	0x27	0x4000 0527	RW	S1_INV	S1_SEM					S1_GAIN[1]	S1_GAIN[0]
S2_CFG	0x2	0x28	0x4000 0528	RW	S2_INV	S2_SEM					S2_GAIN[1]	S2_GAIN[0]
S1_S2_CFG	0x2	0x29	0x4000 0529	RW						VCM_EN	BIAS_VCM CTRL[1]	BIAS_VCM CTRL[0]
S3_CFG	0x2	0x2A	0x4000 052A	RW	AIN1_GAIN[1]	AIN1_GAIN[0]						
S3_CFG_1	0x2	0x2B	0x4000 052B	RW	S3_INV						PTAT_GAIN[1]	PTAT_GAIN[0]
DAC_REG0_1	0x2	0x30	0x4000 0530	RW	DAC_REG0[7]	DAC_REG0[6]	DAC_REG0[5]	DAC_REG0[4]	DAC_REG0[3]	DAC_REG0[2]	DAC_REG0[1]	DAC_REG0[0]
DAC_REG0_2	0x2	0x31	0x4000 0531	RW	DAC_REG0[15]	DAC_REG0[14]	DAC_REG0[13]	DAC_REG0[12]	DAC_REG0[11]	DAC_REG0[10]	DAC_REG0[9]	DAC_REG0[8]

Table 9. Control and Status Registers (continued)

Register Name	DI Page Address	DI Offset Address	M0 Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
DAC_CTRL_ STATUS	0x2	0x38	0x4000 0538	RW								DAC_ ENABLE
DAC_CONFIG	0x2	0x39	0x4000 0539	RW								DAC_ RATIOMETRIC
DAC_LPBK_ CTRL	0x2	0x3A	0x4000 053A	RW						EN_LB	LB_AMP_ EN	LB_ CONNECT
OP_STAGE_ CTRL	0x2	0x3B	0x4000 053B	RW	GATE_3P3_CTR L		PULLUP_EN	DACCAP_EN		DAC_GAIN[2]	DAC_GAIN[1]	DAC_GAIN[0]
LVDT_OP_ CTRL	0x2	0x3C	0x4000 053C	RW	SEM	SKIP_ FILTER	GAIN_ CTRL[1]	GAIN_ CTRL[0]	DIFF_VOCM_ CTRL[1]	DIFF_VOCM_ CTRL[0]	DACVCM_ CTRL[1]	DACVCM_ CTRL[0]
LVDT_LPBK_ CTRL	0x2	0x3D	0x4000 053D	RW								EN_LB
CCS_CTRL	0x2	0x3E	0x4000 053E	RW				EN_CCS	ADJ_CCS[3]	ADJ_CCS[2]	ADJ_CCS[1]	ADJ_CCS[0]
AFEDIAG_CFG	0x2	0x45	0x4000 0545	RW					EN_R_PE	DIS_R_AIN1	EN_R_S2	EN_R_S1
ALPWR	0x2	0x50	0x4000 0550					GATE_CTRL_SD		ADC_EN_ VREF		SD
DLPWR	0x2	0x54	0x4000 0554	RW								OWI_CLK_EN
PSMON1	0x2	0x58	0x4000 0558	RW	LVDT_AVDD_UV	LVDT_AVDD_OV	AVDD_UV	AVDD_OV	REF_UV	REF_OV		
PSMON2	0x2	0x59	0x4000 0559	RW		OSC_GOOD_EN	OSC_GOOD	OSC_BAD				DVDD_OV
AFEDIAG	0x2	0x5B	0x4000 055B	RW		PE_OV	P2_OC	P2_UV	P2_OV	P1_OC	P1_UV	P1_OV
AFEDIAG1	0x2	0x5C	0x4000 055C	RW			S2_GAIN OV	S2_FAULT OV			S1_GAIN OV	S1_FAULT OV
AFEDIAG3	0x2	0x5E	0x4000 055E	RW			AIN1_GAIN_OV	AIN1_FAULT_OV				
AFEDIAG4	0x2	0x5F	0x4000 055F	RW							PTAT_GAIN OV	PTAT_FAULT OV
TOPDIG_MUX_ SEL	0x2	0x60	0x4000 0560	RW		TOPDIG[6]	TOPDIG[5]	TOPDIG[4]	TOPDIG[3]	TOPDIG[2]	TOPDIG[1]	TOPDIG[0]
AMUX_ACT	0x2	0x64	0x4000 0564	RW							TOUT_MUX_SEL	TIN_MUX_EN
AMUX_TIN_ MUX_CTRL	0x2	0x65	0x4000 0565	RW						AMUX_TIN _MUX_CTRL [2]	AMUX_TIN _MUX_CTRL [1]	AMUX_TIN _MUX_CTRL[0]
AMUX_TOUT_ MUX_CTRL	0x2	0x66	0x4000 0566	RW						AMUX_TOUT_ MUX_CTRL [2]	AMUX_TOUT _MUX_CTRL [1]	AMUX_TOUT _MUX_CTRL [0]
AMUX_CTRL	0x2	0x67	0x4000 0567	RW	TEST_ MUX_LVDT_ EN[3[	TEST_ MUX_LVDT_ EN[2]	TEST_ MUX_LVDT_ EN[1]	TEST_ MUX_LVDT_ EN[0]	TEST_ MUX_S3_ EN	TEST_ MUX_S2_ EN	TEST_ MUX_S1_ EN	TEST_ MUX_DAC_ EN
TRACE_FIFO_CTRL_ST AT	0x02	0x70	0x4000 00570	RW		TRACE_FIFO_FU LL	TRACE_FIFO_HA LF_FULL	TRACE_FIFO_E MPTY	TRACE_SOURC E[2]	TRACE_SOURC E[1]	TRACE_SOURC E[0]	TRACE_FIFO_EN ABLE
WAVEFORM_ GEN_CTRL	0x2	0x78	0x4000 0578	RW							WAVE_ STATUS	WAVE_ EN
WAVEFORM_ TABLE_LEN	0x2	0x7A	0x4000 057A	RW	WAV_TAB_LEN[7]	WAV_TAB_LEN[6]	WAV_TAB_LEN[5]	WAV_TAB_LEN[4]	WAV_TAB_LEN[3]	WAV_TAB_LEN[2]	WAV_TAB_LEN[1]	WAV_TAB_LEN[0]
WAVEFORM_ DAC_OFFSET_1	0x2	0x7C	0x4000 057C	RW	WAV_DAC_OFF[7]	WAV_DAC_OFF[6]	WAV_DAC_OFF[5]	WAV_DAC_OFF[4]	WAV_DAC_OFF[3]	WAV_DAC_OFF[2]	WAV_DAC_OFF[1]	DE1_LPF_B1[0]
WAVEFORM_ DAC_OFFSET_2	0x2	0x7D	0x4000 057D	RW	WAV_DAC_OFF[15]	WAV_DAC_OFF[14]	WAV_DAC_OFF[13]	WAV_DAC_OFF[12]	WAV_DAC_OFF[11]	WAV_DAC_OFF[10]	WAV_DAC_OFF[9]	WAV_DAC_OFF[8]
FAST_DIV_ NUMERATOR	0x2	0x80	0x4000 0580	RW								

Table 9. Control and Status Registers (continued)

Register Name	DI Page Address	DI Offset Address	M0 Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
FAST_DIV_ DENOMINATOR	0x2	0x84	0x4000 0584	RW								
FAST_DIV_ CTRL	0x2	0x88	0x4000 0588	RW								DIV_ START
FAST_DIV_ STAT	0x2	0x8A	0x4000 058A	RW							DEN_ ZERO	DIV_ COMPLETE
FAST_DIV_ QUOTIENT	0x2	0x8C	0x4000 058C	RW								
FAST_DIV_ REMAINDER	0x2	0x90	0x4000 0590	RW								
DEMOD1_BPF_ B1	0x2	0x98	0x4000 0598	RW								
DEMOD1_BPF_ A2	0x2	0x9C	0x4000 059C	RW								
DEMOD1_BPF_ A3	0x2	0xA0	0x4000 05A0	RW								
DEMOD1_LPF_ B1	0x2	0xA4	0x4000 05A4	RW								
DEMOD1_LPF_ A2	0x2	0xA8	0x4000 05A8	RW								
DEMOD2_BPF_ B1	0x2	0xB4	0x4000 05B4	RW								
DEMOD2_BPF_ A2	0x2	0xB8	0x4000 05B8	RW								
DEMOD2_BPF_ A3	0x2	0xBC	0x4000 05BC	RW								
DEMOD2_LPF_ B1	0x2	0xC0	0x4000 05C0	RW								
DEMOD2_LPF_ A2	0x2	0xC4	0x4000 05C4	RW								
ADC3_AIN1_LPF_B1	0x2	0xCC	0x4000 05CC	RW								
ADC3_AIN1_LPF_A2	0x2	0xCE	0x4000 05CE	RW								
ADC3_PTAT_LPF_B1	0x2	0xE0	0x4000 05E0	RW								
ADC3_PTAT_LPF_A2	0x2	0xE2	0x4000 05E2	RW								
DAC_SIN NDS1	0x2	0xE4	0x4000 05E4	RW								
DAC_SIN NDS2	0x2	0xE6	0x4000 05E6	RW								
REVISION_ID1	0x0	0x00	0x4000 0400	R	OPT_ID[2]	OPT_ID[1]	OPT_ID[0]		REV_ID[3]	REV_ID[2]	REV_ID[1]	REV_ID[0]
REVISION_ID2	0x0	0x01	0x4000 0401	R					DL_ID[3]	DL_ID[2]	DL_ID[1]	DL_ID[0]
COM_MCU_TO_ DIF_B1	0x0	0x04	0x4000 0404	RW	MCU2DIF[7]	MCU2DIF[6]	MCU2DIF[5]	MCU2DIF[4]	MCU2DIF[3]	MCU2DIF[2]	MCU2DIF[1]	MCU2DIF[0]
COM_MCU_TO_ DIF_B2	0x0	0x05	0x4000 0405	RW	MCU2DIF[15]	MCU2DIF[14]	MCU2DIF[13]	MCU2DIF[12]	MCU2DIF[11]	MCU2DIF[10]	MCU2DIF[9]	MCU2DIF[8]
COM_TX_STATUS	0x0	0x06	0x4000 0406	RW								COM_TXRDY
COM_DIF_TO_ MCU_B1	0x0	0x08	0x4000 0408	RW	DIF2MCU[7]	DIF2MCU[6]	DIF2MCU[5]	DIF2MCU[4]	DIF2MCU[3]	DIF2MCU[2]	DIF2MCU[1]	DIF2MCU[0]

Table 9. Control and Status Registers (continued)

Register Name	DI Page Address	DI Offset Address	M0 Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
COM_DIF_TO_MCU_B2	0x0	0x09	0x4000 0409	RW	DIF2MCU[15]	DIF2MCU[14]	DIF2MCU[13]	DIF2MCU[12]	DIF2MCU[11]	DIF2MCU[10]	DIF2MCU[9]	DIF2MCU[8]
COM_RX_STATUS	0x0	0x0A	0x4000 040A	RW								COM_RXRDY
COM_RX_INT_ENABLE	0x0	0x0B	0x4000 040B	RW								RX_INT_EN
MICRO_INTERFACE_CONTROL	0x0	0x0C	0x4000 040C	RW						DEBUG_LOCK	MICRO_RESET	IF_SEL
SECLOCK	0x0	0x0D	0x4000 040D	RW								SECLOCK
DEMOD1_DATA	0x0	0x10	0x4000 0410	R								
DEMOD2_DATA	0x0	0x14	0x4000 0414	R								
ADC3_AIN1_DATA	0x0	0x1C	0x4000 041C	R								
ADC3_PTAT_DATA	0x0	0x28	0x4000 0428	R								
DEMOD1_PH1_DATA	0x0	0x2C	0x4000 042C	R								
DEMOD1_PH2_DATA	0x0	0x30	0x4000 0430	R								
DEMOD2_PH1_DATA	0x0	0x34	0x4000 0434	R								
DEMOD2_PH2_DATA	0x0	0x38	0x4000 0438	R								
REMAP	0x7	0x20	0x4000 0220	RW								REMAP
GPIO_INPUT	0x7	0x30	0x4000 0230	R							GPIO2_I	GPIO1_I
GPIO_OUTPUT	0x7	0x31	0x4000 0231	RW							GPIO2_O	GPIO1_O
GPIO_DIR	0x7	0x32	0x4000 0232	RW							GPIO2_DIR	GPIO1_DIR
GPIO_OTYPE	0x7	0x33	0x4000 0233	RW							GPIO2_CFG	GPIO1_CFG
PIN_MUX	0x7	0x40	0x4000 0240	RW			Write 0	Write 0	Write 0	Write 0	TOPDIG	Write 0

Table 10. Cortex M0 Specific Registers

Register Name	Description	M0 Address
ISER	Interrupt set-enable register	0xE000 E100
ICER	Interrupt clear-enable register	0xE000 E180
ISPR	Interrupt set-pending register	0xE000 E200
ICPR	Interrupt clear-pending register	0xE000 E280
IPR	Interrupt priority registers	0xE000 E400–0xE000 E41C

NOTE

For details of the Cortex M0 specific registers, refer to *ARM_M0_User_guide.pdf* that can be downloaded from the ARM website (http://www.arm.com).

7.6.2.1 RAM_MBIST_CONTROL Register (M0 Address = 0x4000 0502) (DI Page Address = 0x2) (DI Page Offset = 0x02)

Figure 46. RAM_MBIST_CONTROL Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	RAM_MBIST_CTRL[1]	RAM_MBIST_CTRL[0]	WRAM_MBIST_CTRL[1]	WRAM_MBIST_CTRL[0]
N/A	N/A	N/A	N/A	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 11. RAM_MBIST_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
0:1	WRAM_MBIST_CTRL	R/W	0x00	0b00: Waveform RAM MBIST is inactive. 0b11: Waveform RAM MBIST is active. Other values: Reserved
2:3	RAM_MBIST_CTRL	R/W	0x00	0b00: DATA and DEVELOPMENT RAM MBIST is inactive. 0b11: DATA and DEVELOPMENT RAM MBIST is active. Other values: Reserved
4:7	Reserved	N/A	0x00	Reserved

7.6.2.2 RAM_MBIST_STATUS Register (M0 Address = 0x4000 0503) (DI Page Address = 0x2) (DI Page Offset = 0x03)

Figure 47. RAM_MBIST_STATUS Register

7	6	5	4	3	2	1	0
Reserved	Reserved	RAM_MBIST_FAIL[1]	RAM_MBIST_FAIL[0]	RAM_MBIST_DONE	Reserved	WRAM_MBIST_FAIL	WRAM_MBIST_DONE
N/A	N/A	R-0	R-0	R-0	N/A	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 12. RAM_MBIST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	WRAM_MBIST_DONE	R	0x00	1: Waveform RAM MBIST is complete. 0: Waveform RAM MBIST has not started or has not completed.
1	WRAM_MBIST_FAIL	R	0x00	0x00: DATA and DEVELOPMENT RAM MBIST is inactive. 0x03: DATA and DEVELOPMENT RAM MBIST is active.
2	Reserved	N/A	0x00	Reserved
3	RAM_MBIST_DONE	R	0x00	1: DATA and DEVELOPMENT RAM MBIST is complete. 0: DATA and DEVELOPMENT RAM MBIST has not started or has not completed.

Table 12. RAM_MBIST_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:5	RAM_MBIST_FAIL[1:0]	R	0x00	11: DATA and DEVELOPMENT RAM MBIST has failed. 00: DATA and DEVELOPMENT RAM MBIST has not failed. This bit is valid only when RAM_MBIST_DONE is 1.
6:7	Reserved	N/A	0x00	Reserved

7.6.2.3 M0 FREQUENCY CONTROL Register (M0 Address = 0x4000 0504) (DI Page Address = 0x2) (DI Page Offset = 0x04)

Figure 48. M0 FREQUENCY CONTROL Register

7	6	5	4	3	2	1	0
Reserved	Reserved	CLK_STATUS[1]	CLK_STATUS[0]	Reserved	Reserved	CLK_CTRL[1]	CLK_CTRL[0]
N/A	N/A	R-0	R-1	N/A	N/A	R/W-0	R/W-1

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 13. M0 FREQUENCY CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
0:1	CLK_CTRL[1:0]	R/W	0x01	0b00: Microcontroller frequency is 1 MHz. 0b01: Microcontroller frequency is 2 MHz. 0b10: Microcontroller frequency is 4 MHz. 0b11: Microcontroller frequency is 8 MHz.
2:3	Reserved	N/A	0x00	Reserved
4:5	CLK_STATUS[1:0]	R	0x01	0b00: Microcontroller frequency is 1 MHz. 0b01: Microcontroller frequency is 2 MHz. 0b10: Microcontroller frequency is 4 MHz. 0b11: Microcontroller frequency is 8 MHz.
6:7	Reserved	N/A	0x00	Reserved

7.6.2.4 FRAM_STATUS Register (M0 Address = 0x4000 0505) (DI Page Address = 0x2) (DI Page Offset = 0x05)

Figure 49. FRAM_STATUS Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	FRAM_ERR	Reserved	Reserved
N/A	N/A	N/A	N/A	N/A	R/W-0	N/A	N/A

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 14. FRAM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0:1	Reserved	N/A	0x00	Reserved
2	FRAM_ERR	R/W	0x00	**Read** 1: FRAM error 0: No error
				Write 1: Clear error 0: No effect
3:7	Reserved	N/A	0x00	Reserved

7.6.2.5 DIG_IF_CTRL Register (M0 Address = 0x4000 0506) (DI Page Address = 0x2) (DI Page Offset = 0x06)

Figure 50. DIG_IF_CTRL Register

7	6	5	4	3	2	1	0
Write 0	Reserved	Reserved	OWI_DGL_CNT_SEL	OWI_XCVR_EN	OWI_EN	Reserved	SPI_EN
R/W-0	N/A	N/A	R/W-0	R/W-0	R/W-1	N/A	R/W-1

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 15. DIG_IF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SPI_EN	R/W	0x01	1: SPI is enabled. 0: SPI is disabled.
1	Reserved	N/A	0x00	Reserved
2	OWI_EN	R/W	0x01	1: OWI is enabled. 0: OWI is disabled.
3	OWI_XCVR_EN	R/W	0x00	1: Enable OWI transceiver – OWI Transceiver is connected to VDD. 0: Disable OWI transceiver – OWI Transceiver is disconnected from VDD.
4	OWI_DGL_CNT_SEL	R/W	0x00	1: OWI activation deglitch filters are set to 10 ms. 0: OWI activation deglitch filters are set to 1 ms.
5:6	Reserved	N/A	0x00	Reserved
7	Write 0	R/W	0x00	Write 0

7.6.2.6 OWI_ERROR_STATUS_LO Register (M0 Address = 0x4000 0508) (DI Page Address = 0x2) (DI Page Offset = 0x08)

Figure 51. OWI_ERROR_STATUS_LO Register

7	6	5	4	3	2	1	0
OWI_ERR7	OWI_ERR6	OWI_ERR5	OWI_ERR4	OWI_ERR3	OWI_ERR2	OWI_ERR1	OWI_ERR0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 16. OWI_ERROR_STATUS_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
0	OWI_ERR0	R	0x00	1: SYNC field bit rate is < 320 bps. 0: No error
1	OWI_ERR1	R	0x00	Reserved
2	OWI_ERR2	R	0x00	1: SYNC field stop bit too short 0: No error
3	OWI_ERR3	R	0x00	1: COMMAND field: incorrect stop bit value 0: No Error
4	OWI_ERR4	R	0x00	1: COMMAND field: stop bit too short 0: No Error
5	OWI_ERR5	R	0x00	1: DATA field: incorrect stop bit value 0: No Error
6	OWI_ERR6	R	0x00	1: DATA field: stop bit too short 0: No error
7	OWI_ERR7	R	0x00	1: DATA field: slave transmit value overdriven to dominant value during stop bit transmit 0: No error

7.6.2.7 OWI_ERROR_STATUS_HI Register (M0 Address = 0x4000 0509) (DI Page Address = 0x2) (DI Page Offset = 0x09

Figure 52. OWI_ERROR_STATUS_HI Register

7	6	5	4	3	2	1	0
OWI_ERR_CLR	Reserved	Reserved	Reserved	Reserved	Reserved	OWI_ERR9	OWI_ERR8
R/W-0	N/A	N/A	N/A	N/A	N/A	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 17. OWI_ERROR_STATUS_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
0	OWI_ERR0	R	0x00	1: SYNC field: consecutive bits in the sync field are different by more than ±25% tolerance 0: No Error
1	OWI_ERR1	R	0x00	1: COMMAND field: invalid command sent through OWI protocol 0: No error
2:6	Reserved	N/A	0x00	Reserved
7	OWI_ERR7	R/W	0x00	1: Clear OWI_ERROR_STATUS_LO and OWI_ERROR_STATUS_HI registers 0: No action

7.6.2.8 OWI_INTERRUPT Register (M0 Address = 0x4000 050A) (DI Page Address = 0x2) (DI Page Offset = 0x0A)

Figure 53. OWI_INTERRUPT Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OWI_INT
N/A	N/A	N/A	N/A	N/A	N/A	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 18. OWI_INTERRUPT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	OWI_INT	R/W	0x00	**Read** 1: OWI interrupt is active. 0: No action
				Write 1: Clear OWI interrupt 0: No action
1:7	Reserved	N/A	0x00	Reserved

7.6.2.9 OWI_INTERRUPT_EN Register (M0 Address = 0x4000 050B) (DI Page Address = 0x2) (DI Page Offset = 0x0B)

Figure 54. OWI_INTERRUPT_EN Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OWI_INT_EN
N/A	N/A	N/A	N/A	N/A	N/A	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 19. OWI_INTERRUPT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
0	OWI_INT_EN	R/W	0x00	1: Enable OWI interrupt 0: Disable OWI interrupt
1:7	Reserved	N/A	0x00	Reserved

7.6.2.10 FRAM_PAGE_ADDR Register (M0 Address = 0x4000 0518) (DI Page Address = 0x2) (DI Page Offset = 0x18)

Figure 55. FRAM_PAGE_ADDR Register

7	6	5	4	3	2	1	0
Reserved	Reserved	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
N/A	N/A	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 20. FRAM_PAGE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
0:5	ADDR[5:0]	R/W	0x00	FRAM page address. MSB (ADDR[5]) is always 0.
6:7	Reserved	N/A	0x00	Reserved

7.6.2.11 DATA_WAVE_PAGE_ADDR Register (M0 Address = 0x4000 0519) (DI Page Address = 0x2) (DI Page Offset = 0x19)

Figure 56. DATA_WAVE_PAGE_ADDR Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
N/A	N/A	N/A	N/A	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 21. DATA_WAVE_PAGE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
0:3	ADDR[3:0]	R/W	0x00	DATA and waveform RAM page address 0x00–0x07: DATA RAM 0x08–0x09: WAVEFORM RAM 0x0A–0x0F: Reserved
4:7	Reserved	N/A	0x00	Reserved

7.6.2.12 DEVRAM_PAGE_ADDR Register (M0 Address = 0x4000 051A) (DI Page Address = 0x2) (DI Page Offset = 0x1A

Figure 57. DEVRAM_PAGE_ADDR Register

7	6	5	4	3	2	1	0
Reserved	Reserved	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
N/A	N/A	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 22. DEVRAM_PAGE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
0:5	ADDR[5:0]	R/W	0x00	Development RAM page address. MSB (ADDR[5]) is always 0.
6:7	Reserved	N/A	0x00	Reserved

7.6.2.13 WDOG_CTRL_STAT Register (M0 Address = 0x4000 051C) (DI Page Address = 0x2) (DI Page Offset = 0x1C)

Figure 58. WDOG_CTRL_STAT Register

7	6	5	4	3	2	1	0
WD_RESET	WD_RESET_STATUS	Reserved	Reserved	Reserved	Reserved	Reserved	WDOG_EN
R/W-0	R-0	N/A	N/A	N/A	N/A	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 23. WDOG_CTRL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	WDOG_EN	R/W	0x00	1:Watchdog timer is enabled. 0: Watchdog timer is disabled.
1:5	Reserved	N/A	0x00	Reserved
6	WD_RESET_STATUS	R	0x01	1: Watchdog reset occurred due to a write to WDOG_TRIG_HIGH register before the count reached the WDOG_TRIG_LOW value. 0: Watchdog reset occurred because a write to WDOG_TRIG_HIGH did not occur before the watchdog timer reached the WDOG_TRIG_HIGH value.
7	WD_RESET	R/W	0x00	1: Watchdog reset timer error. This bit is cleared when 1 is written to it. 0: Watchdog reset has not occurred.

7.6.2.14 WDOG_TRIG_HIGH Register (M0 Address = 0x4000 051D) (DI Page Address = 0x2) (DI Page Offset = 0x1D)

Figure 59. WDOG_TRIG_HIGH Register

7	6	5	4	3	2	1	0
TRIG[7]	TRIG[6]	TRIG[5]	TRIG[4]	TRIG[3]	TRIG[2]	TRIG[1]	TRIG[0]
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 24. WDOG_TRIG_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
0:7	TRIG[7:0]	R/W	0xFF	Writing any 8-bit value to this register resets the watchdog timer. The watchdog high time-out value = (TRIG[7:0] +1) × 2 ms.

7.6.2.15 WDOG_TRIG_LOW Register (M0 Address = 0x4000 051E) (DI Page Address = 0x2) (DI Page Offset = 0x1E)

Figure 60. WDOG_TRIG_LOW Register

7	6	5	4	3	2	1	0
TRIG[7]	TRIG[6]	TRIG[5]	TRIG[4]	TRIG[3]	TRIG[2]	TRIG[1]	TRIG[0]
R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 25. WDOG_TRIG_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
0:7	TRIG[7:0]	R/W	0x80	The watchdog low time-out value = TRIG[7:0] × 2 ms.

7.6.2.16 DEMOD1_CONFIG Register (M0 Address = 0x4000 0520) (DI Page Address = 0x2) (DI Page Offset = 0x20)

Figure 61. DEMOD1_CONFIG Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	DEMOD1_DECI_RATE	Reserved	DEMOD1_EN
N/A	N/A	N/A	N/A	N/A	R/W-1	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 26. DEMOD1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	DEMOD1_EN	R/W	0x00	1: DEMOD1 is enabled. 0: DEMOD1 is disabled.
1	Reserved	N/A	0x00	Reserved
2	DEMOD1_DECI_RATE	R/W	0x01	1: DEMOD1 output rate is one sample every 256 µs. 0: DEMOD1 output rate is one sample every 128 µs.
3:7	Reserved	N/A	0x00	Reserved

7.6.2.17 DEMOD2_CONFIG Register (M0 Address = 0x4000 0521) (DI Page Address = 0x2) (DI Page Offset = 0x21)

Figure 62. DEMOD2_CONFIG Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	DEMOD2_DECI_RATE	Reserved	DEMOD2_EN
N/A	N/A	N/A	N/A	N/A	R/W-1	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 27. DEMOD2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	DEMOD2_EN	R/W	0x00	1: DEMOD2 is enabled. 0: DEMOD2 is disabled.
1	Reserved	N/A	0x00	Reserved
2	DEMOD2_DECI_RATE	R/W	0x01	1: DEMOD2 output rate is one sample every 256 µs. 0: DEMOD2 output rate is one sample every 128 µs.
3:7	Reserved	N/A	0x00	Reserved

7.6.2.18 ADC3_CONFIG Register (M0 Address = 0x4000 0522) (DI Page Address = 0x2) (DI Page Offset = 0x22)

Figure 63. ADC3_CONFIG Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ADC3_EN
N/A	N/A	N/A	N/A	N/A	N/A	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 28. ADC3_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	ADC3_EN	R/W	0x00	1: ADC3 decimator is enabled. 0: ADC3 decimator is disabled.
1:7	Reserved	N/A	0x00	Reserved

7.6.2.19 S1_S2_DEMOD_CFG_1 Register (M0 Address = 0x4000 0524) (DI Page Address = 0x2) (DI Page Offset = 0x24)

Figure 64. S1_S2_DEMOD_CFG_1 Register

7	6	5	4	3	2	1	0
Reserved	Write 0	Write 0	Write 0	DEMOD_EN	Write 0	RESET_CLK	RESET_MOD
N/A	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 29. S1_S2_DEMOD_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	RESET_MOD	R/W	0x01	1: DEMOD1 and DEMOD2 delta-sigma modulators are in reset. 0: DEMOD1 and DEMOD2 delta-sigma modulators are not in reset.
1	RESET_CLK	R/W	0x01	1: DEMOD1 and DEMOD2 delta-sigma modulators clocks are reset. 0: DEMOD1 and DEMOD2 delta-sigma modulators clocks are not in reset.
2	Write 0	R/W	0x00	Always write 0.
3	DEMOD_EN	R/W	0x00	1: DEMOD interfaces and decimator clocks are enabled. 0: DEMOD interfaces and decimator clocks are disabled.
4:6	Write 0	R/W	0x00	Always write 0.
7	Reserved	N/A	0x00	Reserved

7.6.2.20 S3_ADC_CFG_1 Register (M0 Address = 0x4000 0526) (DI Page Address = 0x2) (DI Page Offset = 0x26)

Figure 65. S3_ADC_CFG_1 Register

7	6	5	4	3	2	1	0
Reserved	Write 0	Write 0	Write 0	ADC_EN	Write 0	RESET_CLK	RESET_MOD
N/A	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 30. S3_ADC_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	RESET_MOD	R/W	0x01	1: ADC3 delta-sigma modulators are in reset. 0: ADC3 delta-sigma modulators are not in reset.
1	RESET_CLK	R/W	0x01	1: ADC3 delta-sigma modulator clocks are reset. 0: ADC3 delta-sigma modulator clocks are not in reset.
2	Write 0	R/W	0x00	Always write 0.
3	ADC_EN	R/W	0x00	1: ADC3 interfaces and decimator clocks are enabled. 0: ADC3 interfaces and decimator clocks are disabled.
4:6	Write 0	R/W	0x00	Always write 0.
7	Reserved	N/A	0x00	Reserved

7.6.2.21 S1_CFG Register (M0 Address = 0x4000 0527) (DI Page Address = 0x2) (DI Page Offset = 0x27)

Figure 66. S1_CFG Register

7	6	5	4	3	2	1	0
S1_INV	S1_SEM	Reserved	Reserved	Reserved	Reserved	S1_GAIN[1]	S1_GAIN[0]
R/W-0	R/W-0	N/A	N/A	N/A	N/A	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 31. S1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
0:1	S1_GAIN	R/W	0x00	Gain Stage Setting 0b00: 1 V/V 0b01: 1.33 V/V 0b10: 1.67 V/V 0b11: 2 V/V
2:5	Reserved	R/W	0x00	Reserved
6	S1_SEM	R/W	0x00	1: S1 gain is configured in single-ended mode. 0: S1 gain is configured in differential mode.

Table 31. S1_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	S1_INV	R/W	0x00	1: Inverts the output of the S1 gain stage 0: No Inversion

7.6.2.22 S2_CFG Register (M0 Address = 0x4000 0528) (DI Page Address = 0x2) (DI Page Offset = 0x28)

Figure 67. S2_CFG Register

7	6	5	4	3	2	1	0
S2_INV	S2_SEM	Reserved	Reserved	Reserved	Reserved	S2_GAIN[1]	S2_GAIN[0]
R/W-0	R/W-0	N/A	N/A	N/A	N/A	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 32. S2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
0:1	S2_GAIN	R/W	0x00	Gain Stage Setting 0b00: 1 V/V 0b01: 1.33 V/V 0b10: 1.67 V/V 0b11: 2 V/V
2:5	Reserved	R/W	0x00	Reserved
6	S2_SEM	R/W	0x00	1: S2 Gain is configured in single-ended mode. 0: S2 Gain is configured in differential mode.
7	S2_INV	R/W	0x00	1: Inverts the output of the S2 gain stage 0: No Inversion

7.6.2.23 S1_S2_CFG Register (M0 Address = 0x4000 0528) (DI Page Address = 0x2) (DI Page Offset = 0x28)

Figure 68. S1_S2_CFG Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	VCM_EN	BIAS_VCM_CTRL[1]	BIAS_VCM_CTRL[0]
N/A	N/A	N/A	N/A	N/A	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 33. S1_S2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
0:1	BIAS_VCM_CTRL	R/W	0x00	Common Mode Voltage Bias Setting 0b00: 1.25 V 0b01: 0.5 V 0b10: 0.75 V 0b11: 1 V
2	VCM_EN	R/W	0x00	1: Enable common mode voltage bias before S1 and S2 gains for ac-coupled applications 0: Disable common mode voltage bias before S1 and S2 gains for ac-coupled applications
3:7	Reserved	R/W	0x00	Reserved

7.6.2.24 S3_CFG Register (M0 Address = 0x4000 052A) (DI Page Address = 0x2) (DI Page Offset = 0x2A)

Figure 69. S3_CFG Register

7	6	5	4	3	2	1	0
AIN1_GAIN[1]	AIN1_GAIN[0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R/W-0	R/W-0	N/A	N/A	N/A	N/A	N/A	N/A

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 34. S3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
0:5	Reserved	N/A	0x00	Reserved
6:7	AIN1_GAIN	R/W	0x00	Gain Stage Setting 0b00: 1 V/V 0b01: 1.33 V/V 0b10: 2 V/V 0b11: 5 V/V

7.6.2.25 S3_CFG_1 Register (M0 Address = 0x4000 052B) (DI Page Address = 0x2) (DI Page Offset = 0x2B)

Figure 70. S3_CFG_1 Register

7	6	5	4	3	2	1	0
S3_INV	Reserved	Reserved	Reserved	Reserved	Reserved	PTAT_GAIN[1]	PTAT_GAIN[0]
R/W-0	N/A	N/A	N/A	N/A	N/A	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 35. S3_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:1	PTAT_GAIN	R/W	0x00	0b00: 1 V/V 0b01: 1.33 V/V 0b10: 2 V/V 0b11: 5 V/V
2:6	Reserved	R/W	0x00	Reserved
7	S3_INV	R/W	0x00	1: Inverts the output of the S3 gain stage 0: No inversion

7.6.2.26 DAC_REG Register (M0 Address = 0x4000 0530, 0x4000 0531) (DI Page Address = 0x2) (DI Page Offset = 0x30, 0x31)

Figure 71. DAC_REG Register

15	14	13	12	11	10	9	8
DAC_REG0[15]	DAC_REG0[14]	DAC_REG0[13]	DAC_REG0[12]	DAC_REG0[11]	DAC_REG0[10]	DAC_REG0[9]	DAC_REG0[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DAC_REG0[7]	DAC_REG0[6]	DAC_REG0[5]	DAC_REG0[4]	DAC_REG0[3]	DAC_REG0[2]	DAC_REG0[1]	DAC_REG0[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 36. DAC_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	DAC_REG0	R/W	0x00	Digital code that is driven to the 14-bit DAC

7.6.2.27 DAC_CTRL_STATUS Register (M0 Address = 0x4000 0538) (DI Page Address = 0x2) (DI Page Offset = 0x38)

Figure 72. DAC_CTRL_STATUS Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DAC_ENABLE
N/A	N/A	N/A	N/A	N/A	N/A	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 37. DAC_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	DAC_ENABLE	R/W	0x00	1: DAC output is connected to DAC_GAIN. 0: DAC output is not connected to DAC_GAIN.
1:7	Reserved	N/A	0x00	Reserved

7.6.2.28 DAC_CONFIG Register (M0 Address = 0x4000 0539) (DI Page Address = 0x2) (DI Page Offset = 0x39)

Figure 73. DAC_CONFIG Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DAC_RATIOMETRIC
N/A	N/A	N/A	N/A	N/A	N/A	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 38. DAC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	DAC_RATIOMETRIC	R/W	0x00	1: DAC is in ratiometric mode. 0: DAC is in absolute mode.
1:7	Reserved	N/A	0x00	Resereved

7.6.2.29 DAC_LPBK_CTRL Register (M0 Address = 0x4000 053A) (DI Page Address = 0x2) (DI Page Offset = 0x3A

Figure 74. DAC_LPBK_CTRL Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	EN_LB	LB_AMP_EN	LB_CONNECT
N/A	N/A	N/A	N/A	N/A	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 39. DAC_LPBK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	LB_CONNECT	R/W	0x00	1: DAC is in ratiometric mode. 0: DAC is in absolute mode.
1	LB_AMP_EN	R/W	0x00	1: Enables loopback amplifier 0: Disables loopback amplifier
2	EN_LB	R/W	0x00	1: Connects the output of the loopback amplifier to the PGA input 0: Disconnects the output of the loopback amplifier from the PGA input
1:7	Reserved	N/A	0x00	Reserved

7.6.2.30 OP_STAGE_CTRL Register (M0 Address = 0x4000 053B) (DI Page Address = 0x2) (DI Page Offset = 0x3B)

Figure 75. OP_STAGE_CTRL Register

7	6	5	4	3	2	1	0
GATE_3P3_CTRL	Reserved	PULLUP_EN	DACCAP_EN	Reserved	DAC_GAIN[2]	DAC_GAIN[1]	DAC_GAIN[0]
R/W-0	N/A	R/W-0	R/W-0	N/A	R/W-1	R/W-0	R/W-1

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 40. OP_STAGE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0:2	DAC_GAIN	R/W	0x05	Output DAC Gain Stage Control 0b000: Voltage mode disabled 0b001: 10 V/V 0b010: 4 V/V 0b011: Reserved 0b100: 2 V/V 0b101: 10 V/V 0b110: 4 V/V 0b111: 4 V/V
3	Reserved	N/A	0x00	Reserved
4	DACCAP_EN	R/W	0x00	1: Enable DACCAP capacitor (close switch S4 in DAC Amplifier Gain Stage) 0: Disable DACCAP capacitor (open switch S4 in DAC Amplifier Gain Stage)
5	PULLUP_EN	R/W	0x00	1: Enable Pull up at the input of DAC gain (close switch S8 in DAC Amplifier Gain Stage) 0: Disable Pull up at the input of DAC gain (open switch S8 in DAC Amplifier Gain Stage)
6	Reserved	N/A	0x00	Reserved
7	GATE_3P3_CTRL	R/W	0x00	1: Gate drive regulated so that V_{DD} = 14 V 0: Gate drive regulated so that V_{DD} = 3.5 V

7.6.2.31 LVDT_OP_CTRL Register (M0 Address = 0x4000 053C) (DI Page Address = 0x2) (DI Page Offset = 0x3C)

Figure 76. LVDT_OP_CTRL Register

7	6	5	4	3	2	1	0
SEM	SKIP_FILTER	GAIN_CTRL[1]	GAIN_CTRL[0]	DIFF_VOCM_CTRL[1]	DIFF_VOCM_CTRL[0]	DACVCM_CTRL[1]	DACVCM_CTRL[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 41. LVDT_OP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0:1	DACVCM_CTRL	R/W	0x02	Differential offset adjustment 0b00: 0.82 V 0b01: 0.84 V 0b10: 0.86 V 0b11: 0.88 V
2:3	DIFF_VOCM_CTRL	R/W	0x03	Differential mode output common mode 0b00: 0.75 V 0b01: 1 V 0b10: 1.25 V 0b11: 1.5 V
4:5	GAIN_CTRL	R/W	0x00	LVDT Primary Waveform Gain 0b00: 1 V/V 0b01: 1.18 V/V 0b10: 1.4 V/V 0b11: 1.67 V/V
6	SKIP_FILTER	R/W	0x00	1: Skip external filter - PI is shorted to PE internal to PGA970 0: PI and PE are not tied internally. An external filter stage can be added between these pins if necessary
7	SEM	R/W	0x00	1: Single-ended mode 0: Differential mode

7.6.2.32 LVDT_LPBK_CTRL Register (M0 Address = 0x4000 053D) (DI Page Address = 0x2) (DI Page Offset = 0x3D)

Figure 77. LVDT_LPBK_CTRL Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EN_LB
N/A	N/A	N/A	N/A	N/A	N/A	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 42. LVDT_LPBK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EN_LB	R/W	0x00	1: Connects the output of the loopback amplifier to PGA input 0: Disconnects the output of the loopback amplifier from PGA input
1:7	Reserved	N/A	0x00	Reserved

7.6.2.33 CCS_CTRL Register (M0 Address = 0x4000 053E) (DI Page Address = 0x2) (DI Page Offset = 0x3E)

Figure 78. CCS_CTRL Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	EN_CCS	ADJ_CCS[3]	ADJ_CCS[2]	ADC_CCS[1]	ADJ_CCS[0]
N/A	N/A	N/A	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 43. CCS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0:3	ADJ_CCS[3:0]	R/W	0x00	See Electrical Characteristics - Regulators for constant-current control settings
4	EN_CCS	R/W	0x00	1: Enable constant V_{DD} current control 0: Disable constant V_{DD} current control
5:7	Reserved	N/A	0x00	Reserved

7.6.2.34 AFEDIAG_CFG Register (M0 Address = 0x4000 0545) (DI Page Address = 0x2) (DI Page Offset = 0x45

Figure 79. AFEDIAG_CFG Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	EN_R_PE	DIS_R_AIN1	EN_R_S2	EN_R_S1
N/A	N/A	N/A	N/A	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 44. AFEDIAG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EN_R_S1	R/W	0x00	0: Disables pullup used for open/short diagnostics on S1 pins 1: Enables pullup used for open/short diagnostics on S1 pins
1	EN_R_S2	R/W	0x00	0: Disables pullup used for open/short diagnostics on S2 pins 1: Enables pullup used for open/short diagnostics on S2 pins
2	DIS_R_AIN1	R/W	0x00	0: Enables pullup used for open/short diagnostics on AIN1 pin 1: Disables pullup used for open/short diagnostics on AIN1 pin
3	EN_R_PE	R/W	0x00	0: Disables pullup used for open/short diagnostics on PE pins 1: Enables pullup used for open/short diagnostics on PE pins
4:7	Reserved	N/A	0x00	Reserved

7.6.2.35 ALPWR Register (M0 Address = 0x4000 0550) (DI Page Address = 0x2) (DI Page Offset = 0x50)

Figure 80. ALPWR Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	GATE_CTRL_SD	Write 0	ADC_EN_VREF	Write 0	SD
N/A	N/A	N/A	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 45. ALPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SD	R/W	0x01	1:Shuts down position PGA, temperature PGA, and fault detection 0: Powers up position PGA, temperature PGA, and fault detection
1	Write 0	R/W	0x00	Always write 0.
2	ADC_EN_VREF	R/W	0x00	1: Enables reference voltage found at pin REF 0: Disables reference voltage
3	Write 0	R/W	0x00	Always write 0.
4	GATE_CTRL_SD	R/W	0x00	1: Gate drive disabled 0: Gate drive enabled
5:7	Reserved	N/A	0x00	Reserved

7.6.2.36 DLPWR Register (M0 Address = 0x4000 0554) (DI Page Address = 0x2) (DI Page Offset = 0x54)

Figure 81. DLPWR Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OWI_CLK_EN
N/A	N/A	N/A	N/A	N/A	N/A	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 46. DLPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	OWI_CLK_EN	R/W	0x00	1: Enables OWI clock to the OWI controller 0: Disables OWI clock to the OWI controller
1:7	Reserved	N/A	0x00	Reserved

7.6.2.37 PSMON1 Register (M0 Address = 0x4000 0558) (DI Page Address = 0x2) (DI Page Offset = 0x58)

Figure 82. PSMON1 Register

7	6	5	4	3	2	1	0
LVDT_AVDD_UV	LVDT_AVDD_OV	AVDD_UV	AVDD_OV	REF_UV	REF_OV	Reserved	Reserved
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	N/A	N/A

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 47. PSMON1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:1	Reserved	N/A	0x00	Reserved
2	REF_OV	R/W	0x00	**Read:** 1: Reference is overvoltage. 0: Reference is not overvoltage. **Write:** 1: Clears REF_OV bit 0: No action

Table 47. PSMON1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	REF_UV	R/W	0x00	**Read:** 1: Reference is undervoltage. 0: Reference is not undervoltage. **Write:** 1: Clears REF_UV bit 0: No action
4	AVDD_OV	R/W	0x00	**Read:** 1: AVDD is overvoltage. 0: AVDD is not overvoltage. **Write:** 1: Clears AVDD_OV bit 0: No action
5	AVDD_UV	R/W	0x00	**Read:** 1: AVDD is undervoltage. 0: AVDD is not undervoltage. **Write:** 1: Clears AVDD_UV bit 0: No action
6	LVDT_AVDD_OV	R/W	0x00	**Read:** 1: LVDT_AVDD_OV is overvoltage. 0: LVDT_AVDD_OV is not overvoltage. **Write:** 1: Clears LVDT_AVDD_OV bit 0: No action
7	LVDT_AVDD_UV	R/W	0x00	**Read:** 1: LVDT_AVDD_UV is undervoltage. 0: LVDT_AVDD_UV is not undervoltage. **Write:** 1: Clears LVDT_AVDD_UV bit 0: No action

7.6.2.38 PSMON2 Register (M0 Address = 0x4000 0559) (DI Page Address = 0x2) (DI Page Offset = 0x59)

Figure 83. PSMON2 Register

7	6	5	4	3	2	1	0
Reserved	OSC_GOOD_EN	OSC_GOOD	OSC_BAD	Reserved	Reserved	Reserved	DVDD_OV
N/A	R/W-0	R/W-0	R/W-0	N/A	N/A	N/A	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 48. PSMON2 Register Field Descriptions

Bit	Field	Type	Reset	Description
1	DVDD_OV			**Read:** 1: DVDD is overvoltage. 0: DVDD is not overvoltage. **Write:** 1: Clears DVDD_OV bit 0: No action
1:3	Reserved	N/A	0x00	Reserved
4	OSC_BAD	R/W	0x00	**Read:** 1: Main oscillator frequency is out of specification. 0: N/A **Write:** 1: Clears OSC_BAD bit 0: No action
5	OSC_GOOD	R/W	0x00	**Read:** 1: Main oscillator frequency is within specification. 0: N/A **Write:** N/A

Table 48. PSMON2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OSC_GOOD_EN	R/W	0x00	1: Enable oscillator-good check 0: Disable oscillator-good check
7	Reserved	N/A	0x00	Reserved

7.6.2.39 AFEDIAG Register (M0 Address = 0x4000 055B) (DI Page Address = 0x2) (DI Page Offset = 0x5B)

Figure 84. AFEDIAG Register

7	6	5	4	3	2	1	0
Reserved	PE_OV	P2_OC	P2_UV	P2_OV	P1_OC	P1_UV	P1_OV
N/A	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 49. AFEDIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	P1_OV	R/W	0x00	**Read:** 1: Indicates overvoltage condition on primary 1 0: Indicates no overvoltage condition on primary 1 **Write:** 1: Clears P1_OV bit 0: No action
1	P1_UV	R/W	0x00	**Read:** 1: Indicates undervoltage condition on primary 1 0: Indicates no undervoltage condition on primary 1 **Write:** 1: Clears P1_UV bit 0: No action
2	P1_OC	R/W	0x00	**Read:** 1: Indicates source overcurrent condition on Primary 1 0: Indicates no source overcurrent condition on Primary 1 **Write:** 1: Clears P1_OC bit 0: No Action
3	P2_OV	R/W	0x00	**Read:** 1: Indicates overvoltage condition on primary 2 0: Indicates no overvoltage condition on primary 2 **Write:** 1: Clears P2_OV bit 0: No action
4	P2_UV	R/W	0x00	**Read:** 1: Indicates undervoltage condition on primary 2 0: Indicates no undervoltage condition on primary 2 **Write:** 1: Clears P2_UV bit 0: No action
5	P2_OC	R/W	0x00	**Read:** 1: Indicates source overcurrent condition on Primary 2 0: Indicates no source overcurrent condition on Primary 2 **Write:** 1: Clears P2_OC bit 0: No Action
6	PE_OV	R/W	0x00	**Read:** 1: Indicates overvoltage on primary external 0: Indicates no overvoltage on primary external **Write:** 1: Clears PE_OV bit 0: No action
7	Reserved	N/A	0x00	Reserved

7.6.2.40 AFEDIAG1 Register (M0 Address = 0x4000 055C) (DI Page Address = 0x2) (DI Page Offset = 0x5C)

Figure 85. AFEDIAG1 Register

7	6	5	4	3	2	1	0
Reserved	Reserved	S2_GAIN_OV	S2_FAULT_OV	Reserved	Reserved	S1_GAIN_OV	S1_FAULT_OV
N/A	N/A	R/W-0	R/W-0	N/A	N/A	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 50. AFEDIAG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	S1_FAULT_OV	R/W	0x00	**Read:** 1: Indicates overvoltage condition on input pins of S1 gain 0: Indicates no overvoltage condition on input pins of S1 gain **Write:** 1: Clears S1_FAULT_OV bit 0: No Action
1	S1_GAIN_OV	R/W	0x00	**Read:** 1: Indicates overvoltage at output pins of S1 gain 0: Indicates no overvoltage at output pins of S1 gain **Write:** 1: Clears S1_GAIN_OV bit 0: No action
2:3	Reserved	N/A	0x00	Reserved
4	S2_FAULT_OV	R/W	0x00	**Read:** 1: Indicates overvoltage at input pins of S2 gain 0: Indicates no overvoltage at input pins of S2 gain **Write:** 1: Clears S2_FAULT_OV bit 0: No Action
5	S2_GAIN_OV	R/W	0x00	**Read:** 1: Indicates overvoltage at output pins of S2 gain 0: Indicates no overvoltage at output pins of S2 gain **Write:** 1: Clears S2_GAIN_OV bit 0: No action
6:7	Reserved	N/A	0x00	Reserved

7.6.2.41 AFEDIAG3 Register (M0 Address = 0x4000 055E) (DI Page Address = 0x2) (DI Page Offset = 0x5E)

Figure 86. AFEDIAG3 Register

7	6	5	4	3	2	1	0
Reserved	Reserved	AIN1_GAIN_OV	AIN1_FAULT_OV	Reserved	Reserved	Reserved	Reserved
N/A	N/A	R/W-0	R/W-0	N/A	N/A	N/A	N/A

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 51. AFEDIAG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:3	Reserved	N/A	0x00	Reserved
4	AIN1_FAULT_OV	R/W	0x00	**Read:** 1: Indicates overvoltage at input pins of S2 gain 0: Indicates no overvoltage at input pins of S2 gain **Write:** 1: Clears AIN1_FAULT_OV bit 0: No action

Table 51. AFEDIAG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	AIN1_GAIN_OV	R/W	0x00	**Read:** 1: Indicates overvoltage at S3 gain when MUX is connected to AIN1 0: Indicates no overvoltage at S3 gain when MUX is connected to AIN1 **Write:** 1: Clears AIN1_GAIN_OV bit 0: No action
6:7	Reserved	N/A	0x00	Reserved

7.6.2.42 AFEDIAG4 Register (M0 Address = 0x4000 055F) (DI Page Address = 0x2) (DI Page Offset = 0x5F)

Figure 87. AFEDIAG4 Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PTAT_GAIN_OV	PTAT_FAULT_OV
N/A	N/A	N/A	N/A	N/A	N/A	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 52. AFEDIAG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PTAT_FAULT_OV	R/W	0x00	**Read:** 1: Indicates overvoltage condition on input pins of PTAT 0: Indicates no overvoltage condition on input pins of PTAT **Write:** 1: Clears PTAT_FAULT_OV bit 0: No action
1	PTAT_GAIN_OV	R/W	0x00	**Read:** 1:Indicates overvoltage at S3 gain when MUX is connected to PTAT 0: Indicates no overvoltage at S3 gain when MUX is connected to PTAT **Write:** 1: Clears PTAT_GAIN_OV bit 0: No action
2:3	Reserved	N/A	0x00	Reserved
4:7	Reserved	N/A	0x00	Reserved

7.6.2.43 TOPDIG_MUX_SEL Register (M0 Address = 0x4000 0560) (DI Page Address = 0x2) (DI Page Offset = 0x60)

Figure 88. TOPDIG_MUX_SEL Register

7	6	5	4	3	2	1	0
Reserved	TOPDIG[6]	TOPDIG[5]	TOPDIG[4]	TOPDIG[3]	TOPDIG[2]	TOPDIG[1]	TOPDIG[0]
N/A	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 53. TOPDIG_MUX_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0:6	TOPDIG	R/W	0x00	See Table 54 for TOPDIG multiplexer selection.
7	Reserved	N/A	0x00	Reserved

Table 54. TOPDIG Test Multiplexer Selection

TOPDIG[5:0]	INTERNAL SIGNAL
0x02	REF_OV
0x03	AVDD_OV
0x04	LVDT_AVDD_OV
0x05	DVDD_OV
0x06	OSC_REF_OV
0x08	REF_UV
0x09	AVDD_UV
0x0A	LVDT_AVDD_UV
0x0B	DVDD_UV
0x0C	OSC_REF_UV
0x0D	P1_OV
0x0E	P1_UV
0x0F	P1_OC
0x10	P2_OV
0x11	P2_UV
0x12	P2_OC
0x13	PE_OV
0x14	S1_FAULT_OV
0x15	S1_GAIN_OV
0x17	S2_FAULT_OV
0x18	S2_GAIN_OV
0x1A	S3_FAULT_OV
0x1B	S3_GAIN_OV
0x1D	OWI_ERROR_STATUS_LO[0]
0x1E	OWI_ERROR_STATUS_LO[1]
0x1F	OWI_ERROR_STATUS_LO[2]
0x20	OWI_ERROR_STATUS_LO[3]
0x21	OWI_ERROR_STATUS_LO[4]
0x22	OWI_ERROR_STATUS_LO[5]
0x23	OWI_ERROR_STATUS_LO[6]
0x24	OWI_ERROR_STATUS_LO[7]
0x25	OWI_ERROR_STATUS_HI[0]
0x26	OWI_ERROR_STATUS_HI[1]
0x27	OWI receive data
0x2A	OWI transmit data
0x2D	ADC1 INTERRUPT
0x2F	OWI ACTIVATION INTERRUPT
0x30	OWI COMBUF INTERRUPT
0x3D	OSC8MHz
0x3E	Cortex M0 clock
0x3F	S1/S2 ADC clock
0x40	ADC3 clock
0x44	DEMOD1 decimator clock
0x45	DEMOD2 decimator clock
0x46	ADC3 decimator clock
0x4A	WSRAM_MBIST_DONE
0x4B	WSRAM_MBIST_FAIL

Table 54. TOPDIG Test Multiplexer Selection (continued)

TOPDIG[5:0]	INTERNAL SIGNAL
0x4D	RAM_MBIST_DONE
0x4E	RAM_MBIST_FAIL
0x59	ADC conversion start

7.6.2.44 AMUX_ACT Register (M0 Address = 0x4000 0564) (DI Page Address = 0x2) (DI Page Offset = 0x64)

Figure 89. AMUX_ACT Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TOUT_MUX_SEL	TIN_MUX_EN
N/A	N/A	N/A	N/A	N/A	N/A	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 55. AMUX_ACT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TIN_MUX_EN	R/W	0x00	1: Enables the analog input test multiplexer 0: Disables the analog input test multiplexer
1	TOUT_MUX_SEL	R/W	0x00	1: Enables TOP signals on TOP_TON test pin 0: Enables TON signals on TOP_TON test pin
2:7	Reserved	N/A	0x00	Reserved

7.6.2.45 AMUX_TIN_MUX_CTRL Register (M0 Address = 0x4000 0565) (DI Page Address = 0x2) (DI Page Offset = 0x65)

Figure 90. AMUX_TIN_MUX_CTRL Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	AMUX_TIN_MUX_CTRL[2]	AMUX_TIN_MUX_CTRL[1]	AMUX_TIN_MUX_CTRL[0]
N/A	N/A	N/A	N/A	N/A	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 56. AMUX_TIN_MUX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0:2	AMUX_TIN_MUX_CTRL	R/W	0x00	See Table 57 for analog input multiplexer selection.
3:7	Reserved	N/A	0x00	Reserved

Table 57. Analog Input Mux Selection

AMUX_TIN_MUX_CTRL[2:0]	VI Is Connected to	AIN2 is Connected to
0x00		DAC reference
0x01	Loop_Back_Amp Input	Digital oscillator
0x02	DAC_OUTPUT_STAGE input	VDT_DRIVE input
0x03	S3_MOD_CLK	REF_2p5
0x04	VOTACM_OUT	VREFCM
0x05	ADS1N	ADS1P
0x06	ADS2N	ADS2P
0x07	ADS3N	ADS3P

7.6.2.46 AMUX_TOUT_MUX_CTRL Register (M0 Address = 0x4000 0567) (DI Page Address = 0x2) (DI Page Offset = 0x67)

Figure 91. AMUX_TOUT_MUX_CTRL

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	AMUX_TOUT_MUX_CTRL [3]	AMUX_TOUT_MUX_CTR L [2]	AMUX_TOUT_MUX_CTR L [1]	AMUX_TOUT_MUX_CTR L [0]
N/A-0	N/A-0	N/A-0	N/A-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 58. AMUX_TOUT_MUX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0:3	AMUX_TOUT_MUX_CTRL [3:0]	R/W	0x00	See Table 59 for encoding.
4:7	Reserved	N/A	0x00	Reserved

Table 59. AMUX_TOUT_MUX_CTRL Encoding

AMUX_TOUT_MUX_CTRL[0:3]	Internal TOP Test Signal	Internal TON Test Signal
0x0	AVDD LVDT	ADC reference
0x1	VOTACM going to ADC1/2	VREFCM going to ADC1/2
0x2	REF_2p5_DAC	REF_2p5_INT
0x3	REG_AVDD	OSC_BG_1P2
0x4	VCM	Osc_buffer output
0x5	S1_VCM_OUT	AVSS
0x6	Reference current to trim V-I	14-bit waveform DAC output
0x7	AVSS	AVSS
0x8	AVSS	S2 VCM OUT
0x9	DAC loopback output	AVSS
0xA	14-bit DAC output	AGND_ADC/VREFM (core-level signal)
0xB	AVSS	AVSS
0xC	HV_REF	
0xD	S3_TOUT1	S3_TOUT1
0xE	S1_TOUT1	S1_TOUT1
0xF	S2_TOUT1	S2_TOUT1

7.6.2.47 AMUX_CTRL Register (M0 Address = 0x4000 0567) (DI Page Address = 0x2) (DI Page Offset = 0x67)

Figure 92. AMUX_CTRL Register

7	6	5	4	3	2	1	0
TEST_MUX_S1_EN[3]	TEST_MUX_LVDT_EN[2]	TEST_MUX_LVDT_EN[1]	TEST_MUX_LVDT_EN[0]	TEST_MUX_S3_EN	TEST_MUX_S2_EN	TEST_MUX_S1_EN	TEST_MUX_DAC_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 60. AMUX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TEST_MUX_DAC_ EN	R/W	0x00	0: Connects DAC output to TOP_TON pin 1: Connects DAC output to DAC gain
1	TEST_MUX_S1_ EN	R/W	0x00	0: Connects S1 output to TOP_TON pin 1: Connects S1 output to ADC1
2	TEST_MUX_S2_ EN	R/W	0x00	0: Connects S2 output to TOP_TON pin 1: Connects S2 output to ADC2

Table 60. AMUX_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TEST_MUX_S3_ EN	R/W	0x00	0: Connects S3 output to TOP_TON pin 1: Connects S3 output to ADC3
4:7	TEST_ MUX_S1_ EN[3:0]	R/W	0x00	0x0: Connects waveform DAC output to TOP/TON pins 0xF: Connects waveform DAC output to waveform gain Other values reserved

7.6.2.48 TRACE_FIFO_CTRL_STAT Register (M0 Address = 0x4000 0570) (DI Page Address = 0x2) (DI Page Offset = 0x70)

Figure 93. TRACE_FIFO_CTRL_STAT Register

7	6	5	4	3	2	1	0
Reserved	TRACE_FIFO_ FULL	TRACE_FIFO_ HALF_FULL	TRACE_FIFO_ EMPTY	TRACE_SOUR CE[2]	TRACE_SOUR CE[1]	TRACE_SOUR CE[0]	TRACE_FIFO_ ENABLE
N/A-0	R-0	R-0	R-1	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 61. TRACE_FIFO_CTRL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TRACE_FIFO_ENABLE	R/W	0x00	1: Enables trace FIFO 0: Disables trace FIFO
1:3	TRACE_SOURCE[2:0]	R/W	0x00	0b000: DEMOD1 0b001: DEMOD2 0b010: ADC3_AIN3 0b011: ADC3_AIN4 0b100: ADC3_AIN2 0b101: ADC3_AIN1 0b110: ADC3_PTAT 0b111: ADC3_AIN5
4	TRACE_FIFO_EMPTY	R/W	0x01	1: Trace FIFO is empty. 0: Trace FIFO is not empty.
5	TRACE_FIFO_HALF_FULL	R/W	0x00	1: Trace FIFO is half full. 0: Trace FIFO is less than half full.
6	TRACE_FIFO_FULL	R/W	0x00	1: Trace FIFO is full. 0: Trace FIFO is not full.
7	Reserved	N/A	0x00	Reserved

7.6.2.49 WAVEFORM_GEN_CTRL Register (M0 Address = 0x4000 0578) (DI Page Address = 0x2) (DI Page Offset = 0x78)

Figure 94. WAVEFORM_GEN_CTRL Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WAVE_STATUS	WAVE_EN
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 62. WAVEFORM_GEN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	WAVE_ EN	R/W	0x00	1: Enables waveform generator 0: Disables waveform generator
1	WAVE_ STATUS	R	0x00	1: Waveform generator is enabled and running. 0: Waveform generator is disabled.
2:7	Reserved	N/A	0x00	Reserved

7.6.2.50 WAVEFORM_TABLE_LEN Register (M0 Address = 0x4000 057A) (DI Page Address = 0x2) (DI Page Offset = 0x7A)

Figure 95. WAVEFORM_TABLE_LEN Register

7	6	5	4	3	2	1	0
WAV_TAB_LEN[7]	WAV_TAB_LEN[6]	WAV_TAB_LEN[5]	WAV_TAB_LEN[4]	WAV_TAB_LEN[3]	WAV_TAB_LEN[2]	WAV_TAB_LEN[1]	WAV_TAB_LEN[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 63. WAVEFORM_TABLE_LEN Register Field Descriptions

Bit	Field	Type	Reset	Description
0:7	WAV_TAB_LEN[7:0]	R/W	0x00	Waveform table length. Value should be changed only when WAVE_EN and WAVE_STATUS in the WAVEFORM_GEN_CTRL register are 0.

7.6.2.51 WAVEFORM_DAC_OFFSET Register (M0 Address = 0x4000 057C, 0x4000 057D) (DI Page Address = 0x2) (DI Page Offset = 0x7C, 0x7D)

Figure 96. WAVEFORM_DAC_OFFSET Register

15	14	13	12	11	10	9	8
WAV_DAC_OFF[15]	WAV_DAC_OFF[14]	WAV_DAC_OFF[13]	WAV_DAC_OFF[12]	WAV_DAC_OFF[11]	WAV_DAC_OFF[10]	WAV_DAC_OFF[9]	WAV_DAC_OFF[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
WAV_DAC_OFF[7]	WAV_DAC_OFF[6]	WAV_DAC_OFF[5]	WAV_DAC_OFF[4]	WAV_DAC_OFF[3]	WAV_DAC_OFF[2]	WAV_DAC_OFF[1]	DE1_LPF_B1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 64. WAVEFORM_DAC_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	WAV_DAC_OFF[15:0]	R/W	0x00	Waveform DAC DC offset. Value should be changed only when WAVE_EN and WAVE_STATUS in the WAVEFORM_GEN_CTRL register are 0.

7.6.2.52 FAST_DIV_NUMERATOR Register (M0 Address = 0x4000 0580, 0x4000 0581, 0x4000 0582, 0x4000 0583) (DI Page Address = 0x2) (DI Page Offset = 0x80, 0x81, 0x82, 0x83)

Figure 97. FAST_DIV_NUMERATOR Register

31	30	29	28	27	26	25	24
F_DIV_NUM[31]	F_DIV_NUM[30]	F_DIV_NUM[29]	F_DIV_NUM[28]	F_DIV_NUM[27]	F_DIV_NUM[26]	F_DIV_NUM[25]	F_DIV_NUM[24]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
F_DIV_NUM[23]	F_DIV_NUM[22]	F_DIV_NUM[21]	F_DIV_NUM[20]	F_DIV_NUM[19]	F_DIV_NUM[18]	F_DIV_NUM[17]	F_DIV_NUM[16]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
F_DIV_NUM[15]	F_DIV_NUM[14]	F_DIV_NUM[13]	F_DIV_NUM[12]	F_DIV_NUM[11]	F_DIV_NUM[10]	F_DIV_NUM[9]	F_DIV_NUM[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
F_DIV_NUM[7]	F_DIV_NUM[6]	F_DIV_NUM[5]	F_DIV_NUM[4]	F_DIV_NUM[3]	F_DIV_NUM[2]	F_DIV_NUM[1]	F_DIV_NUM[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 65. FAST_DIV_NUMERATOR Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	F_DIV_NUM[31:0]	R/W	0x00	Microcontroller fast-division numerator

7.6.2.53 FAST_DIV_DENOMINATOR Register (M0 Address = 0x4000 0584, 0x4000 0585, 0x4000 0586, 0x4000 0587) (DI Page Address = 0x2) (DI Page Offset = 0x8C, 0x85, 0x86, 0x87)

Figure 98. FAST_DIV_DENOMINATOR Register

31	30	29	28	27	26	25	24
F_DIV_DEN[31]	F_DIV_DEN[30]	F_DIV_DEN[29]	F_DIV_DEN[28]	F_DIV_DEN[27]	F_DIV_DEN[26]	F_DIV_DEN[25]	F_DIV_DEN[24]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
F_DIV_DEN[23]	F_DIV_DEN[22]	F_DIV_DEN[21]	F_DIV_DEN[20]	F_DIV_DEN[19]	F_DIV_DEN[18]	F_DIV_DEN[17]	F_DIV_DEN[16]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
F_DIV_DEN[15]	F_DIV_DEN[14]	F_DIV_DEN[13]	F_DIV_DEN[12]	F_DIV_DEN[11]	F_DIV_DEN[10]	F_DIV_DEN[9]	F_DIV_DEN[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
F_DIV_DEN[7]	F_DIV_DEN[6]	F_DIV_DEN[5]	F_DIV_DEN[4]	F_DIV_DEN[3]	F_DIV_DEN[2]	F_DIV_DEN[1]	F_DIV_DEN[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 66. FAST_DIV_DENOMINATOR Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	F_DIV_DEN[31:0]	R/W	0x00	Microcontroller fast-division denominator

7.6.2.54 FAST_DIV_CTRL Register (M0 Address = 0x4000 0588) (DI Page Address = 0x2) (DI Page Offset = 0x88)

Figure 99. FAST_DIV_CTRL Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DIV_ START
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 67. FAST_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	DIV_ START	R	0x00	1: Start division 0: No action
1:7	Reserved	N/A	0x00	Reserved

7.6.2.55 FAST_DIV_STAT Register (M0 Address = 0x4000 0588) (DI Page Address = 0x2) (DI Page Offset = 0x88)

Figure 100. FAST_DIV_STAT Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DEN_ZERO	DIV_COMPLETE
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 68. FAST_DIV_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	DIV_COMPLETE	R	0x00	1: Set to 1 when division is complete 0: Set to 0 when DIV_START bit is set to 1
1	DEN_ZERO	R	0x00	1: Denominator is 0. 0: Denominator is not 0.
2:7	Reserved	N/A	0x00	Reserved

7.6.2.56 FAST_DIV_QUOTIENT Register (M0 Address = 0x4000 058C, 0x4000 058D, 0x4000 058E, 0x4000 058F) (DI Page Address = 0x2) (DI Page Offset = 0x8C, 0x8D, 0x8E, 0x8F)

Figure 101. FAST_DIV_QUOTIENT Register

31	30	29	28	27	26	25	24
F_DIV_QUO[31]	F_DIV_QUO[30]	F_DIV_QUO[29]	F_DIV_QUO[28]	F_DIV_QUO[27]	F_DIV_QUO[26]	F_DIV_QUO[25]	F_DIV_QUO[24]
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
23	22	21	20	19	18	17	16
F_DIV_QUO[23]	F_DIV_QUO[22]	F_DIV_QUO[21]	F_DIV_QUO[20]	F_DIV_QUO[19]	F_DIV_QUO[18]	F_DIV_QUO[17]	F_DIV_QUO[16]
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
15	14	13	12	11	10	9	8
F_DIV_QUO[15]	F_DIV_QUO[14]	F_DIV_QUO[13]	F_DIV_QUO[12]	F_DIV_QUO[11]	F_DIV_QUO[10]	F_DIV_QUO[9]	F_DIV_QUO[8]
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
7	6	5	4	3	2	1	0
F_DIV_QUO[7]	F_DIV_QUO[6]	F_DIV_QUO[5]	F_DIV_QUO[4]	F_DIV_QUO[3]	F_DIV_QUO[2]	F_DIV_QUO[1]	F_DIV_QUO[0]
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 69. FAST_DIV_QUOTIENT Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	F_DIV_QUO[31:0]	R	Unknown	Fast-division quotient

7.6.2.57 FAST_DIV_REMAINDER Register (M0 Address = 0x4000 0590, 0x4000 0591, 0x4000 0592, 0x4000 0593) (DI Page Address = 0x2) (DI Page Offset = 0x90, 0x91, 0x92, 0x93)

Figure 102. FAST_DIV_REMAINDER Register

31	30	29	28	27	26	25	24
F_DIV_REM[31]	F_DIV_REM[30]	F_DIV_REM[29]	F_DIV_REM[28]	F_DIV_REM[27]	F_DIV_REM[26]	F_DIV_REM[25]	F_DIV_REM[24]
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
23	22	21	20	19	18	17	16
F_DIV_REM[23]	F_DIV_REM[22]	F_DIV_REM[21]	F_DIV_REM[20]	F_DIV_REM[19]	F_DIV_REM[18]	F_DIV_REM[17]	F_DIV_REM[16]
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

15	14	13	12	11	10	9	8
F_DIV_REM[15]	F_DIV_REM[14]	F_DIV_REM[13]	F_DIV_REM[12]	F_DIV_REM[11]	F_DIV_REM[10]	F_DIV_REM[9]	F_DIV_REM[8]
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
7	6	5	4	3	2	1	0
F_DIV_REM[7]	F_DIV_REM[6]	F_DIV_REM[5]	F_DIV_REM[4]	F_DIV_REM[3]	F_DIV_REM[2]	F_DIV_REM[1]	F_DIV_REM[0]
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 70. FAST_DIV_REMAINDER Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	F_DIV_REM[31:0]	R	Unknown	Fast-division remainder

7.6.2.58 DEMOD1_BPF_B1 Register (M0 Address = 0x4000 0598, 0x4000 0599, 0x4000 059A) (DI Page Address = 0x2) (DI Page Offset = 0x98, 0x99, 0x9A)

Figure 103. DEMOD1_BPF_B1 Register

23	22	21	20	19	18	17	16
DE1_BPF_B1[23]	DE1_BPF_B1[22]	DE1_BPF_B1[21]	DE1_BPF_B1[20]	DE1_BPF_B1[19]	DE1_BPF_B1[18]	DE1_BPF_B1[17]	DE1_BPF_B1[16]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
DE1_BPF_B1[15]	DE1_BPF_B1[14]	DE1_BPF_B1[13]	DE1_BPF_B1[12]	DE1_BPF_B1[11]	DE1_BPF_B1[10]	DE1_BPF_B1[9]	DE1_BPF_B1[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE1_BPF_B1[7]	DE1_BPF_B1[6]	DE1_BPF_B1[5]	DE1_BPF_B1[4]	DE1_BPF_B1[3]	DE1_BPF_B1[2]	DE1_BPF_B1[1]	DE1_BPF_B1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 71. DEMOD1_BPF_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:23	DE1_BPF_B1[23:0]	R/W	0x00 0000	S1 demodulator band-pass filter B1 coefficient

7.6.2.59 DEMOD1_BPF_A2 Register (M0 Address = 0x4000 059C, 0x4000 059D, 0x4000 059E) (DI Page Address = 0x2) (DI Page Offset = 0x9C, 0x9D, 0x9E)

Figure 104. DEMOD1_BPF_A2 Register

23	22	21	20	19	18	17	16
DE1_BPF_A2[23]	DE1_BPF_A2[22]	DE1_BPF_A2[21]	DE1_BPF_A2[20]	DE1_BPF_A2[19]	DE1_BPF_A2[18]	DE1_BPF_A2[17]	DE1_BPF_A2[16]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
DE1_BPF_A2[15]	DE1_BPF_A2[14]	DE1_BPF_A2[13]	DE1_BPF_A2[12]	DE1_BPF_A2[11]	DE1_BPF_A2[10]	DE1_BPF_A2[9]	DE1_BPF_A2[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE1_BPF_A2[7]	DE1_BPF_A2[6]	DE1_BPF_A2[5]	DE1_BPF_A2[4]	DE1_BPF_A2[3]	DE1_BPF_A2[2]	DE1_BPF_A2[1]	DE1_BPF_A2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 72. DEMOD1_BPF_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:23	DE1_BPF_A2[23:0]	R/W	0x00 0000	S1 demodulator band-pass filter A2 coefficient

7.6.2.60 DEMOD1_BPF_A3 Register (M0 Address = 0x4000 05A0, 0x4000 05A1, 0x4000 05A2) (DI Page Address = 0x2) (DI Page Offset = 0xA0, 0xA1, 0xA2)

Figure 105. DEMOD1_BPF_A3 Register

23	22	21	20	19	18	17	16
DE1_BPF_A3[23]	DE1_BPF_A3[22]	DE1_BPF_A3[21]	DE1_BPF_A3[20]	DE1_BPF_A3[19]	DE1_BPF_A3[18]	DE1_BPF_A3[17]	DE1_BPF_A3[16]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
DE1_BPF_A3[15]	DE1_BPF_A3[14]	DE1_BPF_A3[13]	DE1_BPF_A3[12]	DE1_BPF_A3[11]	DE1_BPF_A3[10]	DE1_BPF_A3[9]	DE1_BPF_A3[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE1_BPF_A3[7]	DE1_BPF_A3[6]	DE1_BPF_A3[5]	DE1_BPF_A3[4]	DE1_BPF_A3[3]	DE1_BPF_A3[2]	DE1_BPF_A3[1]	DE1_BPF_A3[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 73. DEMOD1_BPF_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:23	DE1_BPF_A3[23:0]	R/W	0x00 0000	S1 demodulator band-pass filter A3 coefficient

7.6.2.61 DEMOD1_LPF_B1 Register (M0 Address = 0x4000 05A4, 0x4000 05A5) (DI Page Address = 0x2) (DI Page Offset = 0xA4, 0xA5)

Figure 106. DEMOD1_LPF_B1 Register

15	14	13	12	11	10	9	8
DE1_LPF_B1[15]	DE1_LPF_B1[14]	DE1_LPF_B1[13]	DE1_LPF_B1[12]	DE1_LPF_B1[11]	DE1_LPF_B1[10]	DE1_LPF_B1[9]	DE1_LPF_B1[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE1_LPF_B1[7]	DE1_LPF_B1[6]	DE1_LPF_B1[5]	DE1_LPF_B1[4]	DE1_LPF_B1[3]	DE1_LPF_B1[2]	DE1_LPF_B1[1]	DE1_LPF_B1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 74. DEMOD1_LPF_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	DE1_LPF_B1[15:0]	R/W	0x0000	S1 demodulator low-pass filter B1 coefficient

7.6.2.62 DEMOD1_LPF_A2 Register (M0 Address = 0x4000 05A8, 0x4000 05A9) (DI Page Address = 0x2) (DI Page Offset = 0xA8, 0xA9)

Figure 107. DEMOD1_LPF_A2 Register

15	14	13	12	11	10	9	8
DE1_LPF_A2[15]	DE1_LPF_A2[14]	DE1_LPF_A2[13]	DE1_LPF_A2[12]	DE1_LPF_A2[11]	DE1_LPF_A2[10]	DE1_LPF_A2[9]	DE1_LPF_A2[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE1_LPF_A2[7]	DE1_LPF_A2[6]	DE1_LPF_A2[5]	DE1_LPF_A2[4]	DE1_LPF_A2[3]	DE1_LPF_A2[2]	DE1_LPF_A2[1]	DE1_LPF_A2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 75. DEMOD1_LPF_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	DE1_LPF_A2[15:0]	R/W	0x0000	S1 demodulator low-pass filter A2 coefficient

7.6.2.63 DEMOD2_BPF_B1 Register (M0 Address = 0x4000 05B4, 0x4000 05B5, 0x4000 05B6) (DI Page Address = 0x2) (DI Page Offset = 0xB4, 0xB5, 0xB6)

Figure 108. DEMOD2_BPF_B1 Register

23	22	21	20	19	18	17	16
DE2_BPF_B1[23]	DE2_BPF_B1[22]	DE2_BPF_B1[21]	DE2_BPF_B1[20]	DE2_BPF_B1[19]	DE2_BPF_B1[18]	DE2_BPF_B1[17]	DE2_BPF_B1[16]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
DE2_BPF_B1[15]	DE2_BPF_B1[14]	DE2_BPF_B1[13]	DE2_BPF_B1[12]	DE2_BPF_B1[11]	DE2_BPF_B1[10]	DE2_BPF_B1[9]	DE2_BPF_B1[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE2_BPF_B1[7]	DE2_BPF_B1[6]	DE2_BPF_B1[5]	DE2_BPF_B1[4]	DE2_BPF_B1[3]	DE2_BPF_B1[2]	DE2_BPF_B1[1]	DE2_BPF_B1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 76. DEMOD2_BPF_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:23	DE2_BPF_B1[23:0]	R/W	0x00 0000	S2 demodulator band-pass filter B1 coefficient

7.6.2.64 DEMOD2_BPF_A2 Register (M0 Address = 0x4000 05B8, 0x4000 05B9, 0x4000 05BA) (DI Page Address = 0x2) (DI Page Offset = 0xB8, 0xB9, 0xBA)

Figure 109. DEMOD2_BPF_A2 Register

23	22	21	20	19	18	17	16
DE2_BPF_A2[23]	DE2_BPF_A2[22]	DE2_BPF_A2[21]	DE2_BPF_A2[20]	DE2_BPF_A2[19]	DE2_BPF_A2[18]	DE2_BPF_A2[17]	DE2_BPF_A2[16]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
DE2_BPF_A2[15]	DE2_BPF_A2[14]	DE2_BPF_A2[13]	DE2_BPF_A2[12]	DE2_BPF_A2[11]	DE2_BPF_A2[10]	DE2_BPF_A2[9]	DE2_BPF_A2[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE2_BPF_A2[7]	DE2_BPF_A2[6]	DE2_BPF_A2[5]	DE2_BPF_A2[4]	DE2_BPF_A2[3]	DE2_BPF_A2[2]	DE2_BPF_A2[1]	DE2_BPF_A2[0]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 77. DEMOD2_BPF_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:23	DE2_BPF_A2[23:0]	R/W	0x0000	S2 demodulator band-pass filter A2 coefficient

7.6.2.65 DEMOD2_BPF_A3 Register (M0 Address = 0x4000 05BC, 0x4000 05BD, 0x4000 05BE) (DI Page Address = 0x2) (DI Page Offset = 0xBC, 0xBD, 0xBE)

Figure 110. DEMOD2_BPF_A3 Register

23	22	21	20	19	18	17	16
DE2_BPF_A3[23]	DE2_BPF_A3[22]	DE2_BPF_A3[21]	DE2_BPF_A3[20]	DE2_BPF_A3[19]	DE2_BPF_A3[18]	DE2_BPF_A3[17]	DE2_BPF_A3[16]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
DE2_BPF_A3[15]	DE2_BPF_A3[14]	DE2_BPF_A3[13]	DE2_BPF_A3[12]	DE2_BPF_A3[11]	DE2_BPF_A3[10]	DE2_BPF_A3[9]	DE2_BPF_A3[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE2_BPF_A3[7]	DE2_BPF_A3[6]	DE2_BPF_A3[5]	DE2_BPF_A3[4]	DE2_BPF_A3[3]	DE2_BPF_A3[2]	DE2_BPF_A3[1]	DE2_BPF_A3[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 78. DEMOD2_BPF_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:23	DE2_BPF_A3[23:0]	R/W	0x00 0000	S2 demodulator band-pass filter A3 coefficient

7.6.2.66 DEMOD2_LPF_B1 Register (M0 Address = 0x4000 05C0, 0x4000 05C1) (DI Page Address = 0x2) (DI Page Offset = 0xC0, 0xC1)

Figure 111. DEMOD2_LPF_B1 Register

15	14	13	12	11	10	9	8
DE2_LPF_B1[15]	DE2_LPF_B1[14]	DE2_LPF_B1[13]	DE2_LPF_B1[12]	DE2_LPF_B1[11]	DE2_LPF_B1[10]	DE2_LPF_B1[9]	DE2_LPF_B1[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE2_LPF_B1[7]	DE2_LPF_B1[6]	DE2_LPF_B1[5]	DE2_LPF_B1[4]	DE2_LPF_B1[3]	DE2_LPF_B1[2]	DE2_LPF_B1[1]	DE2_LPF_B1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 79. DEMOD2_LPF_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	DE2_LPF_B1[15:0]	R/W	0x0000	S2 demodulator low-pass filter B1 coefficient

7.6.2.67 DEMOD2_LPF_A2 Register (M0 Address = 0x4000 05C4, 0x4000 05C5) (DI Page Address = 0x2) (DI Page Offset = 0xC4, 0xC5)

Figure 112. DEMOD2_LPF_A2 Register

15	14	13	12	11	10	9	8
DE2_LPF_A2[15]	DE2_LPF_A2[14]	DE2_LPF_A2[13]	DE2_LPF_A2[12]	DE2_LPF_A2[11]	DE2_LPF_A2[10]	DE2_LPF_A2[9]	DE2_LPF_A2[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
DE2_LPF_A2[7]	DE2_LPF_A2[6]	DE2_LPF_A2[5]	DE2_LPF_A2[4]	DE2_LPF_A2[3]	DE2_LPF_A2[2]	DE2_LPF_A2[1]	DE2_LPF_A2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 80. DEMOD2_LPF_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	DE2_LPF_A2[15:0]	R/W	0x0000	S2 demodulator low-pass filter A2 coefficient

7.6.2.68 ADC3_AIN1_LPF_B1 Register (M0 Address = 0x4000 05CE, 0x4000 05CF) (DI Page Address = 0x2) (DI Page Offset = 0xCE, 0xCF)

Figure 113. ADC3_AIN1_LPF_B1 Register

15	14	13	12	11	10	9	8
AIN1_LPF_B1[15]	AIN1_LPF_B1[14]	AIN1_LPF_B1[13]	AIN1_LPF_B1[12]	AIN1_LPF_B1[11]	AIN1_LPF_B1[10]	AIN1_LPF_B1[9]	AIN1_LPF_B1[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
AIN1_LPF_B1[7]	AIN1_LPF_B1[6]	AIN1_LPF_B1[5]	AIN1_LPF_B1[4]	AIN1_LPF_B1[3]	AIN1_LPF_B1[2]	AIN1_LPF_B1[1]	AIN1_LPF_B1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 81. ADC3_AIN1_LPF_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	AIN1_LPF_B1[15:0]	R/W	0x0000	Auxiliary S3 ADC AIN1 low-pass filter B1 coefficient

7.6.2.69 ADC3_AIN1_LPF_A2 Register (M0 Address = 0x4000 05CE, 0x4000 05CF) (DI Page Address = 0x2) (DI Page Offset = 0xCE, 0xCF)

Figure 114. ADC3_AIN1_LPF_A2 Register

15	14	13	12	11	10	9	8
AIN1_LPF_A2[15]	AIN1_LPF_A2[14]	AIN1_LPF_A2[13]	AIN1_LPF_A2[12]	AIN1_LPF_A2[11]	AIN1_LPF_A2[10]	AIN1_LPF_A2[9]	AIN1_LPF_A2[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
AIN1_LPF_A2[7]	AIN1_LPF_A2[6]	AIN1_LPF_A2[5]	AIN1_LPF_A2[4]	AIN1_LPF_A2[3]	AIN1_LPF_A2[2]	AIN1_LPF_A2[1]	AIN1_LPF_A2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 82. ADC3_AIN1_LPF_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	AIN1_LPF_A2[15:0]	R/W	0x0000	Auxiliary S3 ADC AIN1 low-pass filter A2 coefficient

7.6.2.70 ADC3_PTAT_LPF_B1 Register (M0 Address = 0x4000 05E0, 0x4000 05E1) (DI Page Address = 0x2) (DI Page Offset = 0xE0, 0xE1)

Figure 115. ADC3_PTAT_LPF_B1 Register

15	14	13	12	11	10	9	8
LPF_A2[15]	LPF_A2[14]	LPF_A2[13]	LPF_A2[12]	LPF_A2[11]	LPF_A2[10]	LPF_A2[9]	LPF_A2[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
LPF_A2[7]	LPF_A2[6]	LPF_A2[5]	LPF_A2[4]	LPF_A2[3]	LPF_A2[2]	LPF_A2[1]	LPF_A2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 83. ADC3_PTAT_LPF_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	LPF_A2[15:0]	R/W	0x0000	Auxiliary S3 ADC PTAT low-pass filter B1 coefficient

7.6.2.71 ADC3_PTAT_LPF_A2 Register (M0 Address = 0x4000 05E2, 0x4000 05E3) (DI Page Address = 0x2) (DI Page Offset = 0xE2, 0xE3)

Figure 116. ADC3_PTAT_LPF_A2 Register

15	14	13	12	11	10	9	8
LPF_A2[15]	LPF_A2[14]	LPF_A2[13]	LPF_A2[12]	LPF_A2[11]	LPF_A2[10]	LPF_A2[9]	LPF_A2[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
LPF_A2[7]	LPF_A2[6]	LPF_A2[5]	LPF_A2[4]	LPF_A2[3]	LPF_A2[2]	LPF_A2[1]	LPF_A2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 84. ADC3_PTAT_LPF_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	LPF_A2[15:0]	R/W	0x0000	Auxiliary S3 ADC PTAT low-pass filter B1 coefficient

7.6.2.72 DAC_SIN_NDS1 Register (M0 Address = 0x4000 05E4, 0x4000 05E5) (DI Page Address = 0x2) (DI Page Offset = 0xE4, 0xE5)

Figure 117. DAC_SIN_NDS1 Register

15	14	13	12	11	10	9	8
SIN_NDS1[15]	SIN_NDS1[14]	SIN_NDS1[13]	SIN_NDS1[12]	SIN_NDS1[11]	SIN_NDS1[10]	SIN_NDS1[9]	SIN_NDS1[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SIN_NDS1[7]	SIN_NDS1[6]	SIN_NDS1[5]	SIN_NDS1[4]	SIN_NDS1[3]	SIN_NDS1[2]	SIN_NDS1[1]	SIN_NDS1[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 85. DAC_SIN_NDS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	SIN_NDS1[15:0]	R/W	0x0000	Used to specify the first sample location to use for demodulator phase reading

7.6.2.73 DAC_SIN_NDS2 Register (M0 Address = 0x4000 05E6, 0x4000 05E7) (DI Page Address = 0x2) (DI Page Offset = 0xE6, 0xE7)

Figure 118. DAC_SIN_NDS2 Register

15	14	13	12	11	10	9	8
SIN_NDS2[15]	SIN_NDS2[14]	SIN_NDS2[13]	SIN_NDS2[12]	SIN_NDS2[11]	SIN_NDS2[10]	SIN_NDS2[9]	SIN_NDS2[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SIN_NDS2[7]	SIN_NDS2[6]	SIN_NDS2[5]	SIN_NDS2[4]	SIN_NDS2[3]	SIN_NDS2[2]	SIN_NDS2[1]	SIN_NDS2[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 86. DAC_SIN_NDS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:15	SIN_NDS2[15:0]	R/W	0x0000	Used to specify the second sample location to use for demodulator phase reading

7.6.2.74 REVISION_ID1 Register (M0 Address = 0x4000 0400) (DI Page Address = 0x0) (DI Page Offset = 0x01)

Figure 119. REVISION_ID1 Register

7	6	5	4	3	2	1	0
OPT_ID[2]	OPT_ID[1]	OPT_ID[0]	Reserved	REV_ID[3]	REV_ID[2]	REV_ID[1]	REV_ID[0]
Encoded	Encoded	Encoded	N/A-0	Encoded	Encoded	Encoded	Encoded

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 87. REVISION_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:3	REV_ID[3:0]	Encoded	Encoded	Die revision ID
4	Reserved	N/A	0x00	Reserved
5:7	OPT_ID[2:0]	Encoded	Encoded	Revision variant option ID

7.6.2.75 REVISION_ID2 Register (M0 Address = 0x4000 0401) (DI Page Address = 0x0) (DI Page Offset = 0x01)

Figure 120. REVISION_ID2 Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	DL_ID[3]	DL_ID[2]	DL_ID[1]	DL_ID[0]
N/A-0	N/A-0	N/A-0	N/A-0	Encoded	Encoded	Encoded	Encoded

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 88. REVISION_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:3	DL_ID[3:0]	Encoded	Encoded	Digital-logic block ID
7:4	Reserved	N/A	0x00	Reserved

7.6.2.76 COM_MCU_TO_DIF_B1 Register (M0 Address = 0x4000 0404) (DI Page Address = 0x0) (DI Page Offset = 0x04)

Bits 7:0 of the data written by the microcontroller for communication with the digital interface. This register can be written only by the microcontroller.

Figure 121. COM_MCU_TO_DIF_B1 Register

7	6	5	4	3	2	1	0
MCU2DIF[7]	MCU2DIF[6]	MCU2DIF[5]	MCU2DIF[4]	MCU2DIF[3]	MCU2DIF[2]	MCU2DIF[1]	MCU2DIF[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 89. COM_MCU_TO_DIF_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:7	MCU2DIF[15:0]	R/W	0x00	Bits 7:0 of the data written by the microcontroller for communication with the digital interface. This register can be written only by the microcontroller.

7.6.2.77 COM_MCU_TO_DIF_B2 Register (M0 Address = 0x4000 0405) (DI Page Address = 0x0) (DI Page Offset = 0x05)

Bits 15:8 of the data written by the microcontroller for communication with the digital interface. This register can be written only by the microcontroller.

Figure 122. COM_MCU_TO_DIF_B2 Register

7	6	5	4	3	2	1	0
MCU2DIF[15]	MCU2DIF[14]	MCU2DIF[13]	MCU2DIF[12]	MCU2DIF[11]	MCU2DIF[10]	MCU2DIF[9]	MCU2DIF[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 90. COM_MCU_TO_DIF_B2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0:7	MCU2DIF[15:0]	R/W	0x00	Bits 15:8 of the data written by the microcontroller for communication with the digital interface. This register can be written only by the microcontroller.

7.6.2.78 COM_TX_STATUS Register (M0 Address = 0x4000 0406) (DI Page Address = 0x0) (DI Page Offset = 0x06)

Figure 123. COM_TX_STATUS Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	COM_TXRDY
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read-only; -n = value after reset

Table 91. COM_TX_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	COM_TXRDY	R/W	0x00	**Read** 1: COM_MCU_TO_DIF_B2 has been written by the microcontroller. 0: COM_MCU_TO_DIF_B2 has not been written by the microcontroller. **Write** 1: COM_RXRDY is cleared. 0: No action
1:7	Reserved	N/A	0x00	Reserved

7.6.2.79 COM_DIF_TO_MCU_B1 Register (M0 Address = 0x4000 0408) (DI Page Address = 0x0) (DI Page Offset = 0x08)

Bits 7:0 of the data written by the digital interface for communication with the microcontroller. This register can be written only by the digital interface.

Figure 124. COM_DIF_TO_MCU_B1 Register

7	6	5	4	3	2	1	0
DIF2MCU[7]	DIF2MCU[6]	DIF2MCU[5]	DIF2MCU[4]	DIF2MCU[3]	DIF2MCU[2]	DIF2MCU[1]	DIF2MCU[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 92. COM_DIF_TO_MCU_B1 Field Descriptions

Bit	Field	Type	Reset	Description
0:7	DIF2MCU[0:7]	R/W	0x00	MCU communication data

7.6.2.80 COM_DIF_TO_MCU_B2 Register (M0 Address = 0x4000 0409) (DI Page Address = 0x0) (DI Page Offset = 0x09)

Bits 15:8 of the data written by the digital interface for communication with the microcontroller. This register can be written only by the digital interface.

Figure 125. COM_DIF_TO_MCU_B2 Register

7	6	5	4	3	2	1	0
DIF2MCU[15]	DIF2MCU[14]	DIF2MCU[13]	DIF2MCU[12]	DIF2MCU[11]	DIF2MCU[10]	DIF2MCU[9]	DIF2MCU[8]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 93. COM_DIF_TO_MCU_B2 Field Descriptions

Bit	Field	Type	Reset	Description
0:7	DIF2MCU[8:15]	R/W	0x00	MCU communication data

7.6.2.81 COM_RX_STATUS Register (M0 Address = 0x4000 040A) (DI Page Address = 0x0) (DI Page Offset = 0x0A)

Figure 126. COM_RX_STATUS Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	COM_RXRDY
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 94. COM_RX_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	COM_RXRDY	R/W	0x00	**Read** 1: COM_DIF_TO_MCU_B2 has been written by the digital interface. 0: COM_DIF_TO_MCU_B2 has not been written by the digital interface. **Write** 1: COM_RXRDY is cleared. 0: No action
1:7	Reserved	N/A	0x00	Reserved

7.6.2.82 COM_RX_INT_ENABLE Register (M0 Address = 0x4000 040B) (DI Page Address = 0x0) (DI Page Offset = 0x0B)

Figure 127. COM_RX_INT_ENABLE Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RX_INT_EN
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 95. COM_RX_INT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	RX_INT_EN	R/W	0x00	1: COM_RXRDY interrupt is enabled and propagated to the microcontroller. 0: COM_RXRDY interrupt is disabled and not propagated to the microcontroller.
1:7	Reserved	N/A	0x00	Reserved

7.6.2.83 MICRO_INTERFACE_CONTROL Register (M0 Address = 0x4000 040C, DI Page Address = 0x0, DI Page Offset = 0x0C)

Figure 128. MICRO_INTERFACE_CONTROL Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	DEBUG_LOCK	MICRO_RESET	IF_SEL
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 96. MICRO_INTERFACE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	IF_SEL	R/W	0x00	1: Digital Interface accesses the device resources. 0: Microcontroller accesses the device resources.
1	MICRO_RESET		0x00	1: Microcontroller is reset. 0: Microcontroller is running.
2	DEBUG_LOCK		0x00	1: Debugger cannot access the device resources. 0: Debugger can access the device resources if IF_SEL is 0.
3:7	Reserved	N/A	0x00	Reserved

7.6.2.84 SECLOCK Register (M0 Address = 0x4000 040D, DI Page Address = 0x0, DI Page Offset = 0x0D)

Figure 129. SECLOCK Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SECLOCK[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 97. SECLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SECLOCK	R/W	0x00	1: FRAM security is enabled. 0: FRAM security is disabled.
1:7	Reserved	R/W	0x00	Reserved

7.6.2.85 DEMOD1_DATA Register (M0 Address = 0x4000 0410, 0x4000 0411, 0x4000 0412, 0x4000 0413) (DI Page Address = 0x0) (DI Page Offset = 0x10, 0x11, 0x12, 0x13)

Figure 130. DEMOD1_DATA Register

31	30	29	28	27	26	25	24
DEMOD1[31]	DEMOD1[30]	DEMOD1[29]	DEMOD1[28]	DEMOD1[27]	DEMOD1[26]	DEMOD1[25]	DEMOD1[24]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23	22	21	20	19	18	17	16
DEMOD1[23]	DEMOD1[22]	DEMOD1[21]	DEMOD1[20]	DEMOD1[19]	DEMOD1[18]	DEMOD1[17]	DEMOD1[16]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15	14	13	12	11	10	9	8

DEMOD1[15]	DEMOD1[14]	DEMOD1[13]	DEMOD1[12]	DEMOD1[11]	DEMOD1[10]	DEMOD1[9]	DEMOD1[8]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
DEMOD1[7]	DEMOD1[6]	DEMOD1[5]	DEMOD1[4]	DEMOD1[3]	DEMOD1[2]	DEMOD1[1]	DEMOD1[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 98. DEMOD1_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	DEMOD1[31:0]	R	0x0000 0000	Demodulator 1 data output

7.6.2.86 DEMOD2_DATA Register (M0 Address = 0x4000 0414, 0x4000 0415, 0x4000 0416, 0x4000 0417) (DI Page Address = 0x0) (DI Page Offset = 0x14, 0x15, 0x16, 0x17)

Figure 131. DEMOD2_DATA Register

31	30	29	28	27	26	25	24
DEMOD2[31]	DEMOD2[30]	DEMOD2[29]	DEMOD2[28]	DEMOD2[27]	DEMOD2[26]	DEMOD2[25]	DEMOD2[24]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23	22	21	20	19	18	17	16
DEMOD2[23]	DEMOD2[22]	DEMOD2[21]	DEMOD2[20]	DEMOD2[19]	DEMOD2[18]	DEMOD2[17]	DEMOD2[16]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15	14	13	12	11	10	9	8
DEMOD2[15]	DEMOD2[14]	DEMOD2[13]	DEMOD2[12]	DEMOD2[11]	DEMOD2[10]	DEMOD2[9]	DEMOD2[8]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
DEMOD2[7]	DEMOD2[6]	DEMOD2[5]	DEMOD2[4]	DEMOD2[3]	DEMOD2[2]	DEMOD2[1]	DEMOD2[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 99. DEMOD2_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	DEMOD2[31:0]	R	0x0000 0000	Demodulator 2 data output

7.6.2.87 ADC3_AIN1_DATA Register (M0 Address = 0x4000 041C, 0x4000 041D, 0x4000 041E, 0x4000 041F) (DI Page Address = 0x0) (DI Page Offset = 0x1C, 0x1D, 0x1E, 0x1F)

Figure 132. ADC3_AIN1_DATA Register

31	30	29	28	27	26	25	24
ADC3_AIN1[31]	ADC3_AIN1[30]	ADC3_AIN1[29]	ADC3_AIN1[28]	ADC3_AIN1[27]	ADC3_AIN1[26]	ADC3_AIN1[25]	ADC3_AIN1[24]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23	22	21	20	19	18	17	16
ADC3_AIN1[23]	ADC3_AIN1[22]	ADC3_AIN1[21]	ADC3_AIN1[20]	ADC3_AIN1[19]	ADC3_AIN1[18]	ADC3_AIN1[17]	ADC3_AIN1[16]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15	14	13	12	11	10	9	8
ADC3_AIN1[15]	ADC3_AIN1[14]	ADC3_AIN1[13]	ADC3_AIN1[12]	ADC3_AIN1[11]	ADC3_AIN1[10]	ADC3_AIN1[9]	ADC3_AIN1[8]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
ADC3_AIN1[7]	ADC3_AIN1[6]	ADC3_AIN1[5]	ADC3_AIN1[4]	ADC3_AIN1[3]	ADC3_AIN1[2]	ADC3_AIN1[1]	ADC3_AIN1[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 100. ADC3_AIN1_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	ADC3_AIN1[0:31]	R	0x0000 0000	ADC3 AIN1 data output

7.6.2.88 ADC3_PTAT_DATA Register (M0 Address = 0x4000 0428, 0x4000 0429, 0x4000 042A, 0x4000 042B) (DI Page Address = 0x0) (DI Page Offset = 0x28, 0x29, 0x2A, 0x2B)

Figure 133. ADC3_PTAT_DATA Register

31	30	29	28	27	26	25	24
ADC3_PTAT[31]	ADC3_PTAT[30]	ADC3_PTAT[29]	ADC3_PTAT[28]	ADC3_PTAT[27]	ADC3_PTAT[26]	ADC3_PTAT[25]	ADC3_PTAT[24]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23	22	21	20	19	18	17	16
ADC3_PTAT[23]	ADC3_PTAT[22]	ADC3_PTAT[21]	ADC3_PTAT[20]	ADC3_PTAT[19]	ADC3_PTAT[18]	ADC3_PTAT[17]	ADC3_PTAT[16]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15	14	13	12	11	10	9	8
ADC3_PTAT[15]	ADC3_PTAT[14]	ADC3_PTAT[13]	ADC3_PTAT[12]	ADC3_PTAT[11]	ADC3_PTAT[10]	ADC3_PTAT[9]	ADC3_PTAT[8]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
ADC3_PTAT[7]	ADC3_PTAT[6]	ADC3_PTAT[5]	ADC3_PTAT[4]	ADC3_PTAT[3]	ADC3_PTAT[2]	ADC3_PTAT[1]	ADC3_PTAT[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 101. ADC3_PTAT_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	ADC3_PTAT[0:31]	R	0x0000 0000	Internal temperature ADC3 data

7.6.2.89 DEMOD1_PH1_DATA Register (M0 Address = 0x4000 042C, 0x4000 042D, 0x4000 042E, 0x4000 042F) (DI Page Address = 0x0) (DI Page Offset = 0x2C, 0x2D, 0x2E, 0x2F)

Figure 134. DEMOD1_PH1DATA Register

31	30	29	28	27	26	25	24
PH1DATA[31]	PH1DATA[30]	PH1DATA[29]	PH1DATA[28]	PH1DATA[27]	PH1DATA[26]	PH1DATA[25]	PH1DATA[24]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23	22	21	20	19	18	17	16
PH1DATA[23]	PH1DATA[22]	PH1DATA[21]	PH1DATA[20]	PH1DATA[19]	PH1DATA[18]	PH1DATA[17]	PH1DATA[16]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15	14	13	12	11	10	9	8
PH1DATA[15]	PH1DATA[14]	PH1DATA[13]	PH1DATA[12]	PH1DATA[11]	PH1DATA[10]	PH1DATA[9]	PH1DATA[8]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
PH1DATA[7]	PH1DATA[6]	PH1DATA[5]	PH1DATA[4]	PH1DATA[3]	PH1DATA[2]	PH1DATA[1]	PH1DATA[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 102. DEMOD1_PH1DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	PH1DATA[0:31]	R	0x0000 0000	Demodulator 1 phase data 1

7.6.2.90 DEMOD1_PH2_DATA Register (M0 Address = 0x4000 0430, 0x4000 0431, 0x4000 0432, 0x4000 0433) (DI Page Address = 0x0) (DI Page Offset = 0x30, 0x31, 0x32, 0x33)

Figure 135. DEMOD1_PH2DATA Register

31	30	29	28	27	26	25	24
PH2DATA[31]	PH2DATA[30]	PH2DATA[29]	PH2DATA[28]	PH2DATA[27]	PH2DATA[26]	PH2DATA[25]	PH2DATA[24]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23	22	21	20	19	18	17	16
PH2DATA[23]	PH2DATA[22]	PH2DATA[21]	PH2DATA[20]	PH2DATA[19]	PH2DATA[18]	PH2DATA[17]	PH2DATA[16]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15	14	13	12	11	10	9	8
PH2DATA[15]	PH2DATA[14]	PH2DATA[13]	PH2DATA[12]	PH2DATA[11]	PH2DATA[10]	PH2DATA[9]	PH2DATA[8]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
PH2DATA[7]	PH2DATA[6]	PH2DATA[5]	PH2DATA[4]	PH2DATA[3]	PH2DATA[2]	PH2DATA[1]	PH2DATA[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 103. DEMOD1_PH2DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	PH2DATA[0:31]	R	0x0000 0000	Demodulator 1 phase data 2

7.6.2.91 DEMOD2_PH1_DATA Register (M0 Address = 0x4000 0434, 0x4000 0435, 0x4000 0436, 0x4000 0437) (DI Page Address = 0x0) (DI Page Offset = 0x34, 0x35, 0x36, 0x37)

Figure 136. DEMOD2_PH1DATA Register

31	30	29	28	27	26	25	24
PH1DATA[31]	PH1DATA[30]	PH1DATA[29]	PH1DATA[28]	PH1DATA[27]	PH1DATA[26]	PH1DATA[25]	PH1DATA[24]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23	22	21	20	19	18	17	16
PH1DATA[23]	PH1DATA[22]	PH1DATA[21]	PH1DATA[20]	PH1DATA[19]	PH1DATA[18]	PH1DATA[17]	PH1DATA[16]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15	14	13	12	11	10	9	8
PH1DATA[15]	PH1DATA[14]	PH1DATA[13]	PH1DATA[12]	PH1DATA[11]	PH1DATA[10]	PH1DATA[9]	PH1DATA[8]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
PH1DATA[7]	PH1DATA[6]	PH1DATA[5]	PH1DATA[4]	PH1DATA[3]	PH1DATA[2]	PH1DATA[1]	PH1DATA[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 104. DEMOD2_PH1DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	PH1DATA[0:31]	R	0x0000 0000	Demodulator 2 phase data 1

7.6.2.92 DEMOD2_PH2_DATA Register (M0 Address = 0x4000 0438, 0x4000 0439, 0x4000 043A, 0x4000 043B) (DI Page Address = 0x0) (DI Page Offset = 0x38, 0x39, 0x3A, 0x3B)

Figure 137. DEMOD2_PH2DATA Register

31	30	29	28	27	26	25	24
PH2DATA[31]	PH2DATA[30]	PH2DATA[29]	PH2DATA[28]	PH2DATA[27]	PH2DATA[26]	PH2DATA[25]	PH2DATA[24]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23	22	21	20	19	18	17	16
PH2DATA[23]	PH2DATA[22]	PH2DATA[21]	PH2DATA[20]	PH2DATA[19]	PH2DATA[18]	PH2DATA[17]	PH2DATA[16]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15	14	13	12	11	10	9	8
PH2DATA[15]	PH2DATA[14]	PH2DATA[13]	PH2DATA[12]	PH2DATA[11]	PH2DATA[10]	PH2DATA[9]	PH2DATA[8]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
PH2DATA[7]	PH2DATA[6]	PH2DATA[5]	PH2DATA[4]	PH2DATA[3]	PH2DATA[2]	PH2DATA[1]	PH2DATA[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 105. DEMOD2_PH2DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
0:31	PH2DATA[0:31]	R	0x0000 0000	Demodulator 2 phase data 2

7.6.2.93 REMAP Register (M0 Address = 0x4000 0220) (DI Page Address = 0x7) (DI Page Offset = 0x20)

Figure 138. REMAP Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REMAP
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 106. REMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
0	REMAP	R/W	0x00	1: DEVELOPMENT RAM overlays FRAM; that is, DEVELOPMENT RAM is located starting at address 0x0000 0000. 0: DEVELOPMENT RAM does not overlay FRAM; that is, DEVELOPMENT RAM is located starting at address 0x2100 0000.
1:7	Reserved	N/A	0x00	

7.6.2.94 GPIO_INPUT Register (M0 Address = 0x4000 0230) (DI Page Address = 0x7) (DI Page Offset = 0x30)

Figure 139. GPIO_INPUT Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO2_I	GPIO1_I
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R-x	R-x

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 107. GPIO_INPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GPIO1_I	R	Unknown	GPIO1 pin state. Functions both in INPUT and OUTPUT mode
1	GPIO2_I	R	Unknown	GPIO2 pin state. Functions both in INPUT and OUTPUT mode

Table 107. GPIO_INPUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:7	Reserved	N/A	0x00	Reserved

7.6.2.95 M0 AddresGPIO_OUTPUT Register (s = 0x4000 0231) (DI Page Address = 0x7) (DI Page Offset = 0x31)

Figure 140. GPIO_OUTPUT Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO2_O	GPIO1_O
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 108. GPIO_OUTPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GPIO1_O	R/W	0x00	GPIO1 output state. 0 is low, 1 is high.
1	GPIO2_O	R/W	0x00	GPIO2 output state. 0 is low, 1 is high.
2:6	Reserved	N/A	0x00	Reserved

7.6.2.96 GPIO_DIR Register (M0 Address = 0x4000 0232) (DI Page Address = 0x7) (DI Page Offset = 0x32)

Figure 141. GPIO_DIR Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO2_DIR	GPIO1_DIR
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R/W-1	R/W-1

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 109. GPIO_DIR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GPIO1_DIR	R/W	0x01	1: GPIO1 is input. 0: GPIO1 is output.
1	GPIO2_DIR	R/W	0x01	1: GPIO2 is input. 0: GPIO2 is output.
2:7	Reserved	N/A	0x00	Reserved

7.6.2.97 GPIO_OPTYPE Register (M0 Address = 0x4000 0233) (DI Page Address = 0x7) (DI Page Offset = 0x33)

Figure 142. GPIO_OPTYPE Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO2_CFG	GPIO1_CFG
N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	N/A-0	R/W-0	R/W-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 110. GPIO_OPTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GPIO1_CFG	R/W	0x00	1: GPIO1 is open-drain mode in OUTPUT mode. 0: GPIO1 is push-pull mode in OUTPUT mode.
1	GPIO2_CFG	R/W	0x00	1: GPIO2 is open-drain mode in OUTPUT mode. 0: GPIO2 is push-pull mode in OUTPUT mode.
2:7	Reserved	N/A	0x00	Reserved

7.6.2.98 PIN_MUX Register (M0 Address = 0x4000 0240) (DI Page Address = 0x7) (DI Page Offset = 0x40)

Figure 143. PIN_MUX Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Write 0	Write 0	Write 0	TOPDIG	Reserved
N/A-0	N/A-0	N/A-0	R/W-0	R/W-0	W-0	R/W-0	N/A-0

LEGEND: N/A = Not Applicable; R/W = Read/Write; R = Read only; -n = value after reset

Table 111. PIN_MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
0	Reserved	N/A	0x00	Reserved
1	TOPDIG	R/W	0x00	1: TOPDIG test multiplexer drives the GPIO_2 pin. 0: GPIO_OUTPUT drives the GPIO_2 pin.
2	Write 0	W	0x00	Only write 0 to this bit.
3	Write 0	W	0x00	Only write 0 to this bit
4	Write 0	W	0x00	Only write 0 to this bit
5	Write 0	W	0x00	Only write 0 to this bit
6:7	Reserved	N/A	0x00	Reserved

7.6.3 ADC1 and ADC2 BPF Register Settings

Table 112 lists the settings ADC1 and ADC2 BPG register.

Table 112. BPF Settings

CENTER FREQUENCY (Hz)(1)	BANDWIDTH (Hz)	B1 (Hex)	A2 (Hex)	A3 (Hex)
1 000	20	41E	FF FA97	FF F7C4
1 000	100	1495	FF EA21	FF D6D6
1 000	250	336E	FF CB4C	FF 9923
2 000	20	41E	FF F6B5	FF F7C4
2 000	100	1495	FF E640	FF D6D6
2 000	250	336E	FF C76B	FF 9923
3 000	20	41E	FF F03E	FF F7C4
3 000	100	1495	FF DFC8	FF D6D6
3 000	250	336E	FF C0F5	FF 9923
4 000	20	41E	FF E730	FF F7C4
4 000	100	1495	FF D6BB	FF D6D6
4 000	250	336E	FF B7E8	FF 9923
5 000	20	41E	FF DB8C	FF F7C4
5 000	100	1495	FF CB18	FF D6D6
5 000	250	336E	FF AC47	FF 9923
6 000	20	41E	FF CD52	FF F7C4
6 000	100	1495	FF BCDF	FF D6D6
6 000	250	336E	FF 9E0F	FF 9923
7 000	20	41E	FF BC82	FF F7C4
7 000	100	1495	FF AC10	FF D6D6
7 000	250	336E	FF 8D43	FF 9923
8 000	20	41E	FF A91D	FF F7C4
8 000	100	1495	FF 98AC	FF D6D6
8 000	250	336E	FF 79E1	FF 9923
9 000	20	41E	FF 9322	FF F7C4
9 000	100	1495	FF 82B3	FF D6D6
9 000	250	336E	FF 63EA	FF 9923

(1) For frequencies not listed in the table, contact TI

Table 112. BPF Settings (continued)

CENTER FREQUENCY (Hz)(1)	BANDWIDTH (Hz)	B1 (Hex)	A2 (Hex)	A3 (Hex)
10 000	20	41E	FF 7A92	FF F7C4
10 000	100	1495	FF 6A24	FF D6D6
10 000	250	336E	FF 4B5F	FF 9923
11 000	20	41E	FF 5F6D	FF F7C4
11 000	100	1495	FF 4F01	FF D6D6
11 000	250	336E	FF 303F	FF 9923
12 000	20	41E	FF 41B3	FF F7C4
12 000	100	1495	FF 3149	FF D6D6
12 000	250	336E	FF 128A	FF 9923
13 000	20	41E	FF 2165	FF F7C4
13 000	100	1495	FF 10FD	FF D6D6
13 000	250	336E	FE F242	FF 9923
14 000	20	41E	FE FE83	FF F7C4
14 000	100	1495	FE EE1D	FF D6D6
14 000	250	336E	FE CF66	FF 9923
15 000	20	41E	FE D90D	FF F7C4
15 000	100	1495	FE C8A9	FF D6D6
15 000	250	336E	FE A9F7	FF 9923
16 000	20	41E	FE B103	FF F7C4
16 000	100	1495	FE A0A2	FF D6D6
16 000	250	336E	FE 81F5	FF 9923
17 000	20	41E	FE 8667	FF F7C4
17 000	100	1495	FE 7609	FF D6D6
17 000	250	336E	FE 5761	FF 9923
18 000	20	41E	FE 5938	FF F7C4
18 000	100	1495	FE 48DD	FF D6D6
18 000	250	336E	FE 2A3A	FF 9923
19 000	20	41E	FE 2977	FF F7C4
19 000	100	1495	FE 191F	FF D6D6
19 000	250	336E	FD FA82	FF 9923
20 000	20	41E	FD F725	FF F7C4
20 000	100	1495	FD E6D0	FF D6D6
20 000	250	336E	FD C839	FF 9923

7.6.4 ADC1 and ADC2 LPF Register Settings

Table 113 lists the settings ADC1 and ADC2 LPF register.

Table 113. LPF Settings

CUTOFF FREQUENCY (Hz)(1)	OUTPUT PERIOD (µs)	B1 (Hex)	A2 (Hex)
20	128	105	7DF5
20	256	207	7BF2
100	128	4F3	7619
100	256	98C	6CE8
250	128	BBA	688B
250	256	15AC	54A8

(1) For frequencies not listed in the table, contact TI

7.6.5 ADC3 LPF Register Settings

Table 114 lists the settings ADC3 LPF register.

Table 114. LPF Settings

CUTOFF FREQUENCY (Hz)(1)	B1 (Hex)	A2 (Hex)
20	187	7CF3
100	74A	716C
250	10E2	5E3B
1000	3435	1796
2000	5CA8	C6B0

(1) For frequencies not listed in the table, contact TI

7.6.6 Interrupt Sources

Table 115 lists the IRQ numbers for the interrupt sources.

Table 115. Interrupt Sources

INTERRUPT SOURCE	IRQ Number
ADC1	0
OWI Activation	2
COMBUF RX	3

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following section provides details for configuring the PGA970 in a typical LVDT application.

8.2 Typical Application

8.2.1 Connecting a 6-Wire LVDT

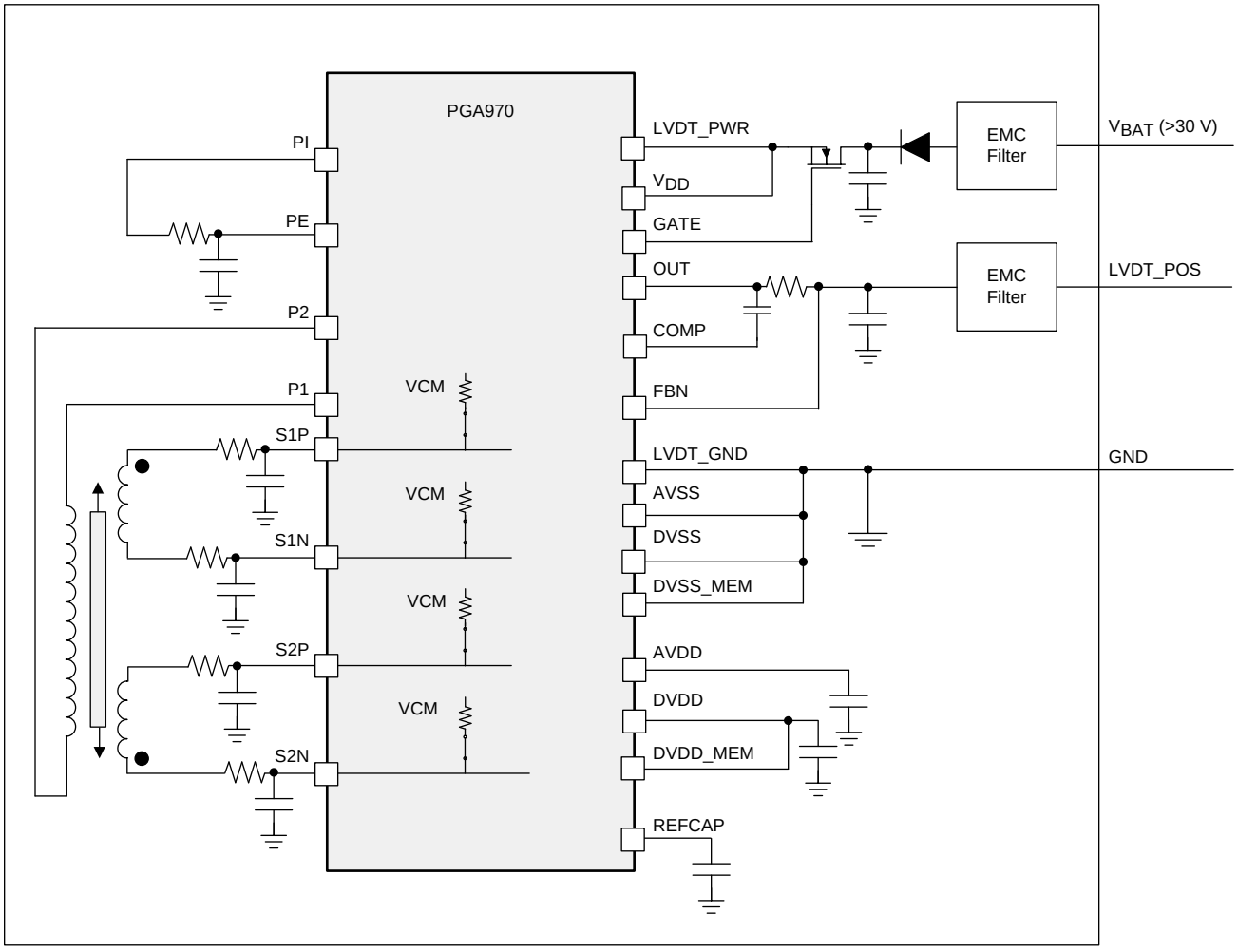


Figure 144. Typical Application for 6-Wire LVDT Connection

8.2.1.1 Design Requirements

A few requirements must be considered when using the PGA970 device in a design:

- Do not exceed the maximum slew rate of 0.5 V/µs at the V_{DD} pin.
- Place a 100-nF capacitor as close as possible to the AVDD pin and tied to ground.

Typical Application (continued)

- Place a 100-nF capacitor as close as possible to the DVDD pin and tied to ground.
- Place a capacitor between 100 nF and 1000 nF as close as possible to the REFCAP pin and tied to ground.
- Use a compensation circuit when driving large capacitive loads with the OUT pin.

8.2.1.2 Detailed Design Procedure

The number of external components necessary for a typical 6-wire LVDT application are very minimal, as shown in Figure 144. Besides the decoupling capacitors, an additional filter between the PI and PE pins, filters for the secondary input pins, and output-stage stability components must be designed from application-to-application. Typical components can be found in the schematics of the PGA970EVM. EMC filters, reverse voltage protections, and gate drive requirements and uses are largely dependent on the standards and practices necessary for the end application.

The design of the algorithm is largely dependent on the user's application; however, for basic functionality, see *Programming Tips* as well as the *PGA970 Software User's Guide* (SLDU024) for detailed guidelines on how to configure the PGA970 device in a typical operating mode.

By following the guidelines provided in *Internal Temperature Sensor*, the accuracy of the temperature sensor is within ±3% of the applied temperature in Celsius. The equations provided can be used in the firmware algorithm to ensure accuracy for the application.

8.2.1.3 Application Curve

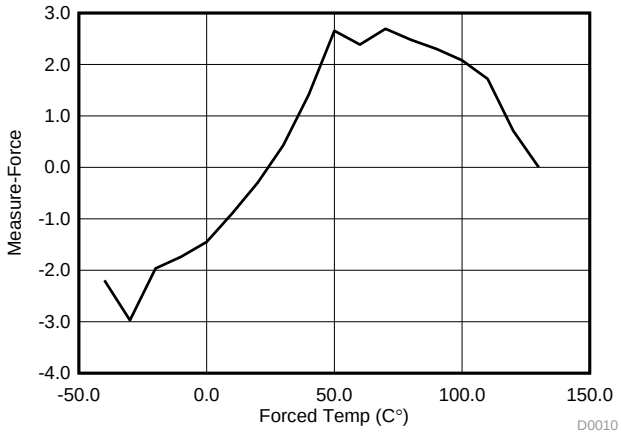


Figure 145. Temperature Sensor Accuracy Using Calibrated Reference Values

9 Power Supply Recommendations

The PGA970 has a single pin, V_{DD}, for the input power supply. The maximum slew rate for the V_{DD} pin is 0.5 V/µs as specified in the *Recommended Operating Conditions*. Faster slew rates might generate a power-on-reset (POR) state. The recommended 680-nF decoupling capacitor should be placed as closed as possible to the V_{DD} pin. The LVDT_PWR pin should be tied to V_{DD} for most typical applications. A small capacitor (1 nF to 10 nF) close to that pin can be added for additional power-supply decoupling.

10 Layout

10.1 Layout Guidelines

Standard layout best practices should be used when designing a board to evaluate and operate the PGA970 device. Depending on the number of layers in the board, one or more GND planes should be inserted as internal layers. However, given the limited number of external components needed for an application using the PGA970 device, it is very possible to design a simple two-layer board. In addition, the V_{DD} decoupling capacitor should be placed as close as possible to the pin. In a similar way, the 100-nF recommended capacitors for the AVDD and DVDD regulators as well as the 10- to 1000-nF recommended capacitor for REFCAP should be placed as close as possible to their respective pins. iIn order to minimize coupling, the signal traces for FBN, COMP, and OUT should be routed such that they do not cross one another.

Figure 146 and Figure 147 show an example layout from the PGA970EVM. In total, the board has four copper layers. The two internal layers are a large solid ground plane and a power layer with multiple power planes to power all of the additional circuitry on the EVM. Large, thick traces are used for V_{DD}, AVDD, DVDD, and REFCAP to reach their respective test points. The decoupling capacitors are placed as close as possible to each of the respective pins. A large number of vias are used on the thermal pad of the PGA970 device to both help dissipate heat and provide a low-resistance connection the ground plane.

10.2 Layout Example

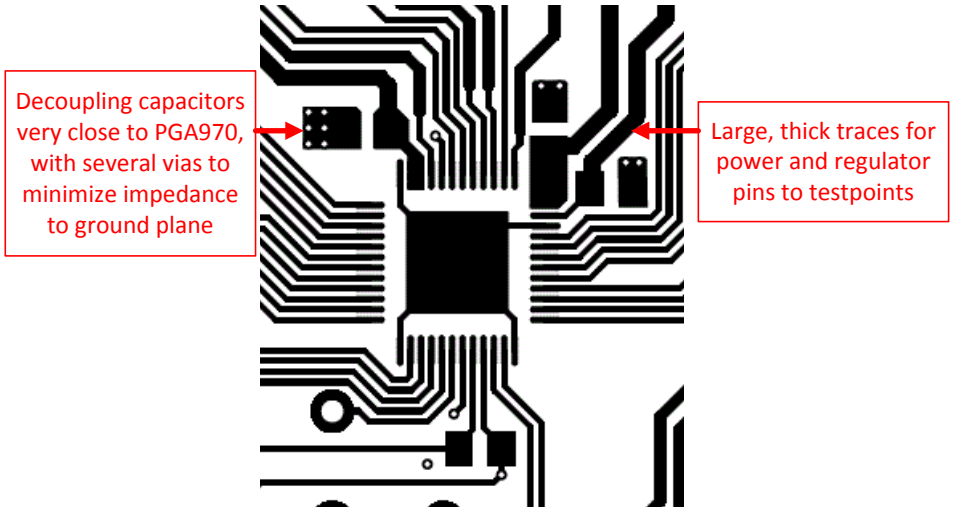


Figure 146. Top Layer Layout of the PGA970EVM

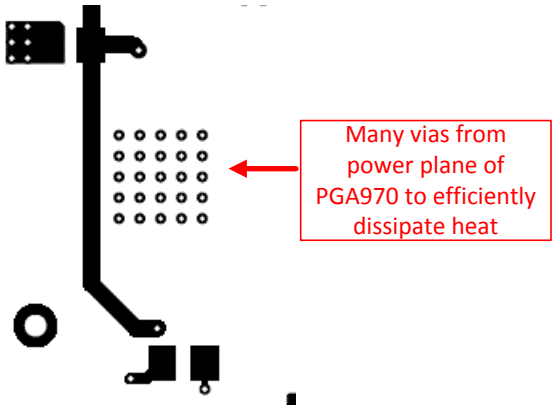


Figure 147. Bottom Layer Layout of the PGA970EVM

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *PGA970 GUI User's Guide* (SLDU023)
- *PGA970 Software Quick Start Guide* (SLDU025)
- *PGA970 Software User's Guide* (SLDU024)
- *PGA970EVM User's Guide* (SLDU017)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
ARM, Cortex are registered trademarks of ARM Limited.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA970QPHPR	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	PGA970Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

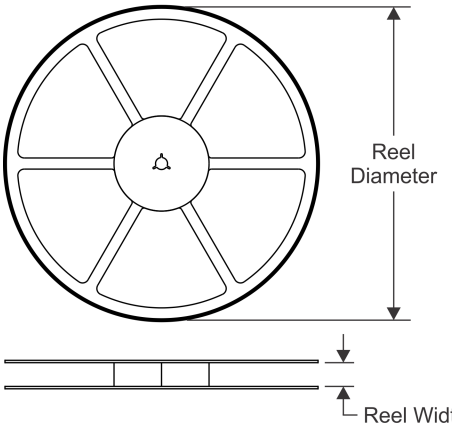
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

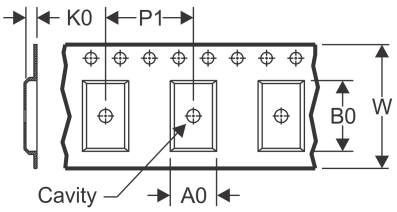
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

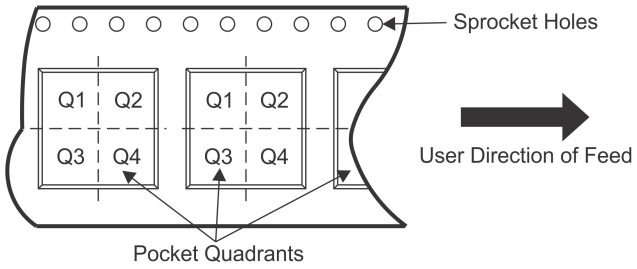


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

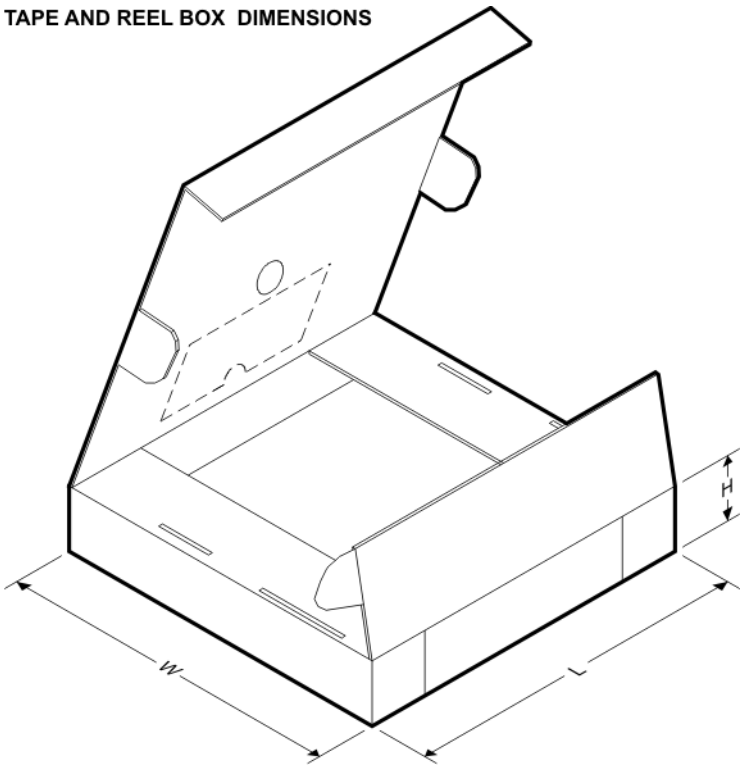
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA970QPHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

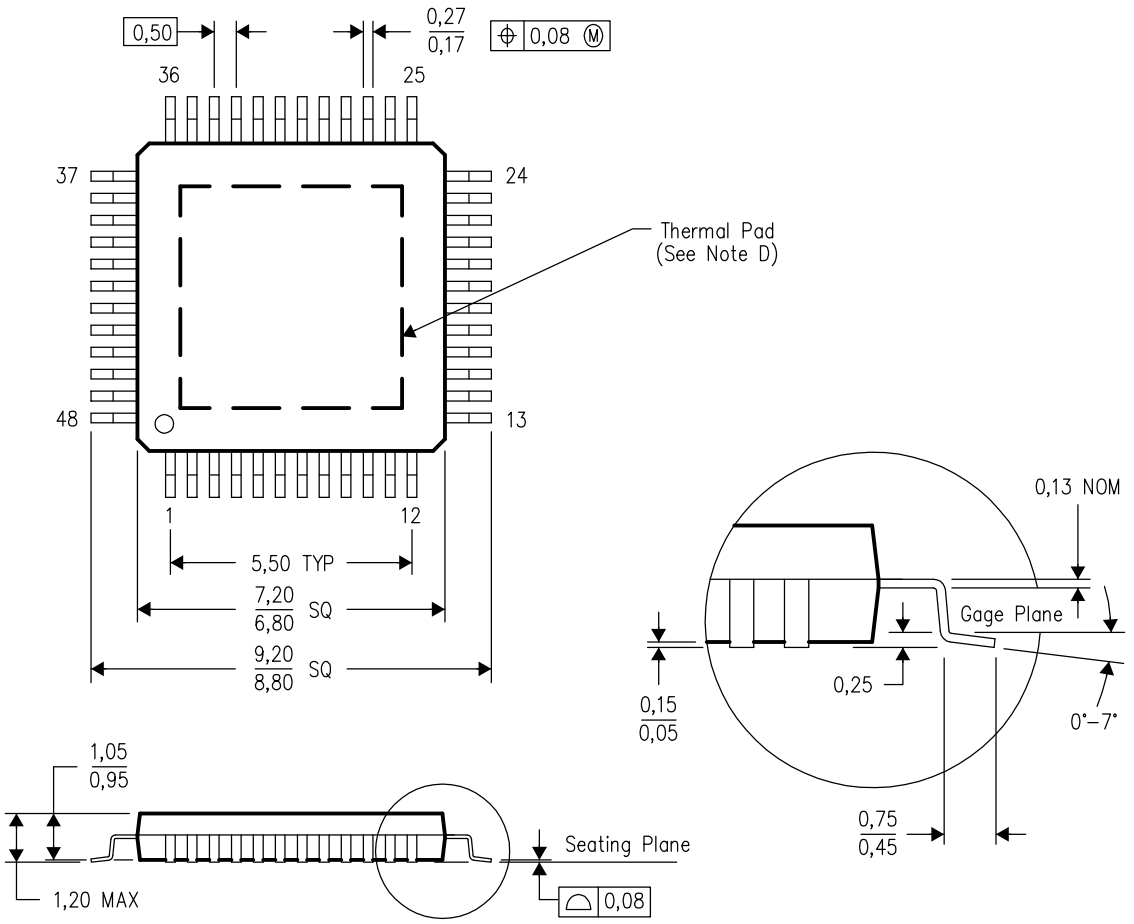
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA970QPHPR	HTQFP	PHP	48	1000	367.0	367.0	38.0

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

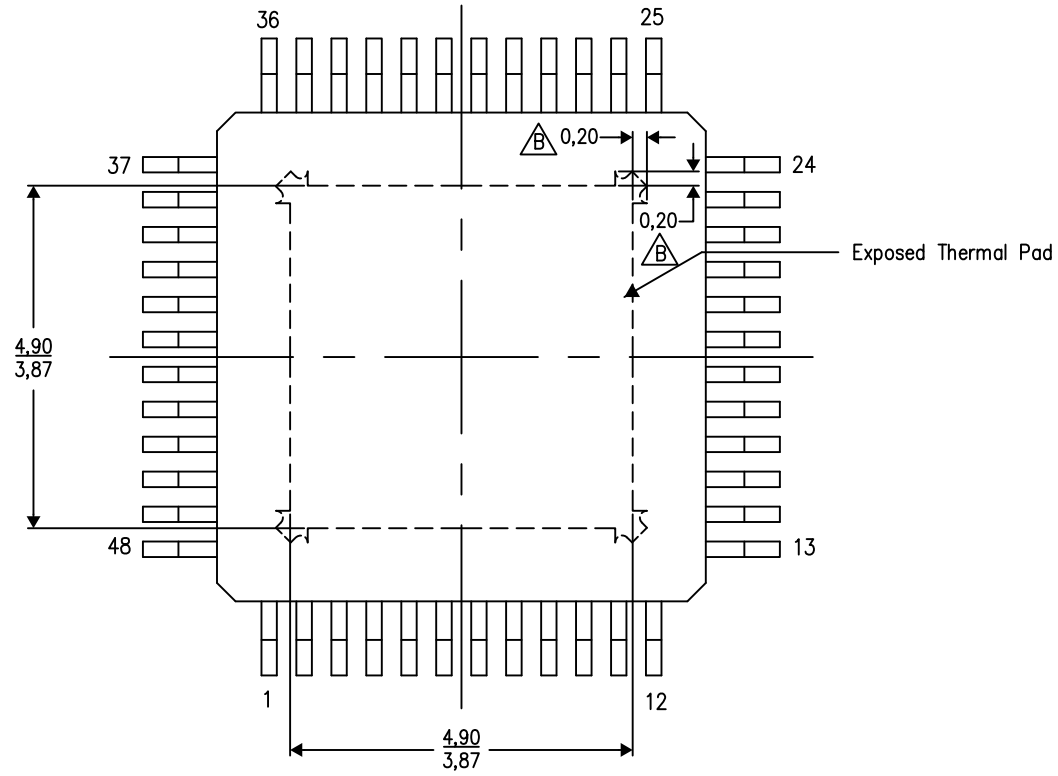
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

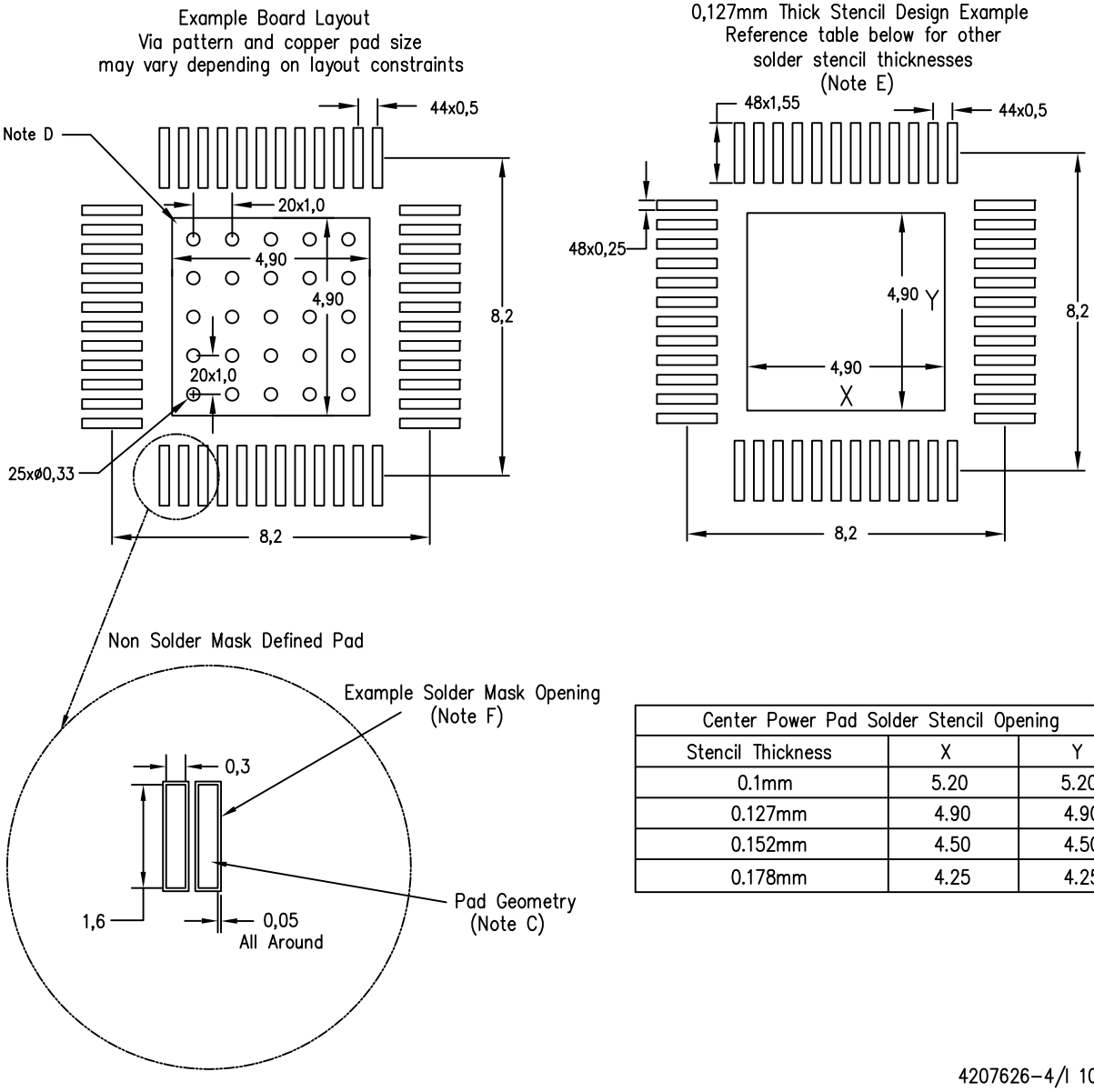
4206329–4/P 03/15

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.20	5.20
0.127mm	4.90	4.90
0.152mm	4.50	4.50
0.178mm	4.25	4.25

4207626–4/I 10/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265