

## Summary

The Xilinx® Kintex® UltraScale+™ FPGAs are available in -3, -2, -1 speed grades, with -3E devices having the highest performance. The -2LE and -1LI devices can operate at a  $V_{CCINT}$  voltage at 0.85V or 0.72V and provide lower maximum static power. When operated at  $V_{CCINT} = 0.85V$ , using -2LE and -1LI devices, the speed specification for the L devices is the same as the -2I or -1I speed grades. When operated at  $V_{CCINT} = 0.72V$ , the -2LE and -1LI performance and static and dynamic power is reduced.

DC and AC characteristics are specified in extended (E) and industrial (I) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade extended device are the same as for a -1 speed grade industrial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the Kintex UltraScale+ FPGAs, is available on the Xilinx website at [www.xilinx.com/documentation](http://www.xilinx.com/documentation).

## DC Characteristics

### Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings<sup>(1)</sup>

| Symbol                | Description                                        | Min    | Max               | Units |
|-----------------------|----------------------------------------------------|--------|-------------------|-------|
| <b>FPGA Logic</b>     |                                                    |        |                   |       |
| $V_{CCINT}$           | Internal supply voltage.                           | -0.500 | 1.000             | V     |
| $V_{CCINT\_IO}^{(2)}$ | Internal supply voltage for the I/O banks.         | -0.500 | 1.000             | V     |
| $V_{CCAUX}$           | Auxiliary supply voltage.                          | -0.500 | 2.000             | V     |
| $V_{CCBRAM}$          | Supply voltage for the block RAM memories.         | -0.500 | 1.000             | V     |
| $V_{CCO}$             | Output drivers supply voltage for HD I/O banks.    | -0.500 | 3.400             | V     |
|                       | Output drivers supply voltage for HP I/O banks.    | -0.500 | 2.000             | V     |
| $V_{CCAUX\_IO}^{(3)}$ | Auxiliary supply voltage for the I/O banks.        | -0.500 | 2.000             | V     |
| $V_{REF}$             | Input reference voltage.                           | -0.500 | 2.000             | V     |
| $V_{IN}^{(4)(6)(7)}$  | I/O input voltage for HD I/O banks. <sup>(5)</sup> | -0.550 | $V_{CCO} + 0.550$ | V     |
|                       | I/O input voltage for HP I/O banks.                | -0.550 | $V_{CCO} + 0.550$ | V     |

Table 1: Absolute Maximum Ratings<sup>(1)</sup> (Cont'd)

| Symbol                        | Description                                                                                        | Min    | Max   | Units |
|-------------------------------|----------------------------------------------------------------------------------------------------|--------|-------|-------|
| V <sub>BATT</sub>             | Key memory battery backup supply.                                                                  | −0.500 | 2.000 | V     |
| I <sub>DC</sub>               | Available output current at the pad.                                                               | −20    | 20    | mA    |
| I <sub>RMS</sub>              | Available RMS output current at the pad.                                                           | −20    | 20    | mA    |
| <b>GTH or GTY Transceiver</b> |                                                                                                    |        |       |       |
| V <sub>MGTAVCC</sub>          | Analog supply voltage for transceiver circuits.                                                    | −0.500 | 1.000 | V     |
| V <sub>MGTAVTT</sub>          | Analog supply voltage for transceiver termination circuits.                                        | −0.500 | 1.300 | V     |
| V <sub>MGTVCCAUX</sub>        | Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.                                  | −0.500 | 1.900 | V     |
| V <sub>MGTREFCLK</sub>        | Transceiver reference clock absolute input voltage.                                                | −0.500 | 1.300 | V     |
| V <sub>MGTAVTTRCAL</sub>      | Analog supply voltage for the resistor calibration circuit of the transceiver column.              | −0.500 | 1.300 | V     |
| V <sub>IN</sub>               | Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.                               | −0.500 | 1.200 | V     |
| I <sub>DCIN-FLOAT</sub>       | DC input current for receiver input pins DC coupled RX termination = floating. <sup>(8)</sup>      | −      | 10    | mA    |
| I <sub>DCIN-MGTAVTT</sub>     | DC input current for receiver input pins DC coupled RX termination = V <sub>MGTAVTT</sub> .        | −      | 10    | mA    |
| I <sub>DCIN-GND</sub>         | DC input current for receiver input pins DC coupled RX termination = GND. <sup>(9)</sup>           | −      | 0     | mA    |
| I <sub>DCIN-PROG</sub>        | DC input current for receiver input pins DC coupled RX termination = programmable. <sup>(10)</sup> | −      | 0     | mA    |
| I <sub>DCOUT-FLOAT</sub>      | DC output current for transmitter pins DC coupled RX termination = floating.                       | −      | 6     | mA    |
| I <sub>DCOUT-MGTAVTT</sub>    | DC output current for transmitter pins DC coupled RX termination = V <sub>MGTAVTT</sub> .          | −      | 6     | mA    |
| <b>System Monitor</b>         |                                                                                                    |        |       |       |
| V <sub>CCADC</sub>            | System Monitor supply relative to GNDADC.                                                          | 0.500  | 2.000 | V     |
| V <sub>REFP</sub>             | System Monitor reference input relative to GNDADC.                                                 | 0.500  | 2.000 | V     |

Table 1: Absolute Maximum Ratings<sup>(1)</sup> (Cont'd)

| Symbol             | Description                                    | Min | Max | Units |
|--------------------|------------------------------------------------|-----|-----|-------|
| <b>Temperature</b> |                                                |     |     |       |
| T <sub>STG</sub>   | Storage temperature (ambient).                 | –65 | 150 | °C    |
| T <sub>SOL</sub>   | Maximum soldering temperature. <sup>(12)</sup> | –   | 260 | °C    |
| T <sub>j</sub>     | Maximum junction temperature. <sup>(12)</sup>  | –   | 125 | °C    |

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- V<sub>CCINT\_IO</sub> must be connected to V<sub>CCBRAM</sub>.
- V<sub>CCAUX\_IO</sub> must be connected to V<sub>CCAUX</sub>.
- The lower absolute voltage specification always applies.
- If V<sub>CCO</sub> is 3.3V, the maximum voltage is 3.4V.
- For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
- When operating outside of the recommended operating conditions, refer to [Table 4](#) and [Table 5](#) for maximum overshoot and undershoot specifications.
- AC coupled operation is not supported for RX termination = floating.
- For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
- DC coupled operation is not supported for RX termination = programmable.
- For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) or *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
- For soldering guidelines and thermal considerations, see the *UltraScale and UltraScale+ FPGAs Packaging and Pinout Specifications* ([UG575](#)).

## Recommended Operating Conditions

Table 2: Recommended Operating Conditions<sup>(1)(2)</sup>

| Symbol                               | Description                                                                                          | Min    | Typ   | Max                      | Units |
|--------------------------------------|------------------------------------------------------------------------------------------------------|--------|-------|--------------------------|-------|
| <b>FPGA Logic</b>                    |                                                                                                      |        |       |                          |       |
| V <sub>CCINT</sub>                   | Internal supply voltage.                                                                             | 0.825  | 0.850 | 0.876                    | V     |
|                                      | For -1LI and -2LE devices (V <sub>CCINT</sub> = 0.72V): internal supply voltage.                     | 0.698  | 0.720 | 0.742                    | V     |
|                                      | For -3E devices: internal supply voltage.                                                            | 0.873  | 0.900 | 0.927                    | V     |
| V <sub>CCINT_IO</sub> <sup>(3)</sup> | Internal supply voltage for the I/O banks.                                                           | 0.825  | 0.850 | 0.876                    | V     |
|                                      | For -1LI and -2LE devices (V <sub>CCINT</sub> = 0.72V): internal supply voltage for the I/O banks.   | 0.825  | 0.850 | 0.876                    | V     |
|                                      | For -3E devices: internal supply voltage for the I/O banks.                                          | 0.873  | 0.900 | 0.927                    | V     |
| V <sub>CCBRAM</sub>                  | Block RAM supply voltage.                                                                            | 0.825  | 0.850 | 0.876                    | V     |
|                                      | For -3E devices: block RAM supply voltage.                                                           | 0.873  | 0.900 | 0.927                    | V     |
| V <sub>CCAUX</sub>                   | Auxiliary supply voltage.                                                                            | 1.746  | 1.800 | 1.854                    | V     |
| V <sub>CCO</sub> <sup>(4)(5)</sup>   | Supply voltage for HD I/O banks.                                                                     | 1.140  | –     | 3.400                    | V     |
|                                      | Supply voltage for HP I/O banks.                                                                     | 0.950  | –     | 1.900                    | V     |
| V <sub>CCAUX_IO</sub> <sup>(6)</sup> | Auxiliary I/O supply voltage.                                                                        | 1.746  | 1.800 | 1.854                    | V     |
| V <sub>IN</sub> <sup>(7)</sup>       | I/O input voltage.                                                                                   | –0.200 | –     | V <sub>CCO</sub> + 0.200 | V     |
| I <sub>IN</sub> <sup>(8)</sup>       | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | –      | –     | 10                       | mA    |
| V <sub>BATT</sub> <sup>(9)</sup>     | Battery voltage                                                                                      | 1.000  | –     | 1.890                    | V     |

Table 2: Recommended Operating Conditions<sup>(1)(2)</sup> (Cont'd)

| Symbol                        | Description                                                                                      | Min   | Typ   | Max   | Units |
|-------------------------------|--------------------------------------------------------------------------------------------------|-------|-------|-------|-------|
| <b>GTH or GTY Transceiver</b> |                                                                                                  |       |       |       |       |
| $V_{MGTAVCC}^{(10)}$          | Analog supply voltage for the GTH or GTY transceiver.                                            | 0.873 | 0.900 | 0.927 | V     |
| $V_{MGTAVTT}^{(10)}$          | Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.          | 1.164 | 1.200 | 1.236 | V     |
| $V_{MGTVCCAUX}^{(10)}$        | Auxiliary analog QPLL voltage supply for the transceivers.                                       | 1.746 | 1.800 | 1.854 | V     |
| $V_{MGTAVTTRCAL}^{(10)}$      | Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column. | 1.164 | 1.200 | 1.236 | V     |
| <b>SYSMON</b>                 |                                                                                                  |       |       |       |       |
| $V_{CCADC}$                   | SYSMON supply relative to GNDADC.                                                                | 1.746 | 1.800 | 1.854 | V     |
| $V_{REFP}$                    | SYSMON externally supplied reference voltage relative to GNDADC.                                 | 1.200 | 1.250 | 1.300 | V     |
| <b>Temperature</b>            |                                                                                                  |       |       |       |       |
| $T_j^{(12)}$                  | Junction temperature operating range for extended (E) temperature devices. <sup>(11)</sup>       | 0     | –     | 100   | °C    |
|                               | Junction temperature operating range for industrial (I) temperature devices.                     | –40   | –     | 100   | °C    |
|                               | Junction temperature operating range for eFUSE programming. <sup>(13)</sup>                      | –40   | –     | 125   | °C    |

**Notes:**

- All voltages are relative to GND.
- For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* ([UG583](#)).
- $V_{CCINT\_IO}$  must be connected to  $V_{CCBRAM}$ .
- For  $V_{CCO\_0}$ , the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if  $V_{CCO}$  drops to 0V.
- Includes  $V_{CCO}$  of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at  $\pm 5\%$ , and 3.3V (HD I/O only) at  $+3/-5\%$ .
- $V_{CCAUX\_IO}$  must be connected to  $V_{CCAUX}$ .
- The lower absolute voltage specification always applies.
- A total of 200 mA per bank should not be exceeded.
- If battery is not used, connect  $V_{BATT}$  to either GND or  $V_{CCAUX}$ .
- Each voltage listed requires filtering as described in *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) or *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
- Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature between 100°C and 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation up to  $T_j = 110^\circ\text{C}$  is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
- Xilinx recommends measuring the  $T_j$  of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)). The SYSMON temperature measurement errors (that are described in [Table 76](#)) must be accounted for in your design. For example, by using an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error  $\pm 3^\circ\text{C}$ . A reading of 97°C is considered the maximum adjusted  $T_j$  ( $100^\circ\text{C} - 3^\circ\text{C} = 97^\circ\text{C}$ ).
- Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

# DC Characteristics Over Recommended Operating Conditions

**Table 3: DC Characteristics Over Recommended Operating Conditions**

| Symbol                                                                                                                    | Description                                                                                                 | Min                 | Typ <sup>(1)</sup> | Max                 | Units |
|---------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|---------------------|--------------------|---------------------|-------|
| V <sub>DRINT</sub>                                                                                                        | Data retention V <sub>CCINT</sub> voltage (below which configuration data might be lost).                   | 0.68                | –                  | –                   | V     |
| V <sub>DRAUX</sub>                                                                                                        | Data retention V <sub>CCAUX</sub> voltage (below which configuration data might be lost).                   | 1.5                 | –                  | –                   | V     |
| I <sub>REF</sub>                                                                                                          | V <sub>REF</sub> leakage current per pin.                                                                   | –                   | –                  | 15                  | μA    |
| I <sub>L</sub>                                                                                                            | Input or output leakage current per pin (sample-tested). <sup>(2)</sup>                                     | –                   | –                  | 15                  | μA    |
| C <sub>IN</sub> <sup>(3)</sup>                                                                                            | Die input capacitance at the pad (HP I/O).                                                                  | –                   | –                  | 3.1                 | pF    |
|                                                                                                                           | Die input capacitance at the pad (HD I/O).                                                                  | –                   | –                  | 4.75                | pF    |
| I <sub>RPU</sub>                                                                                                          | Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 3.3V.                               | 75                  | –                  | 190                 | μA    |
|                                                                                                                           | Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 2.5V.                               | 50                  | –                  | 169                 | μA    |
|                                                                                                                           | Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 1.8V.                               | 60                  | –                  | 120                 | μA    |
|                                                                                                                           | Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 1.5V.                               | 30                  | –                  | 120                 | μA    |
|                                                                                                                           | Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 1.2V.                               | 10                  | –                  | 100                 | μA    |
| I <sub>RPD</sub>                                                                                                          | Pad pull-down (when selected) at V <sub>IN</sub> = 3.3V.                                                    | 60                  | –                  | 200                 | μA    |
|                                                                                                                           | Pad pull-down (when selected) at V <sub>IN</sub> = 1.8V.                                                    | 29                  | –                  | 120                 | μA    |
| I <sub>CCADCON</sub>                                                                                                      | Analog supply current for the SYSMON circuits in the power-up state.                                        | –                   | –                  | 8                   | mA    |
| I <sub>CCADCOFF</sub>                                                                                                     | Analog supply current for the SYSMON circuits in the power-down state.                                      | –                   | –                  | 1.5                 | mA    |
| I <sub>BATT</sub> <sup>(4)(5)</sup>                                                                                       | Battery supply current at V <sub>BATT</sub> = 1.89V.                                                        | –                   | –                  | 650                 | nA    |
|                                                                                                                           | Battery supply current at V <sub>BATT</sub> = 1.20V.                                                        | –                   | –                  | 150                 | nA    |
| I <sub>PFS</sub> <sup>(6)</sup>                                                                                           | V <sub>CCAUX</sub> additional supply current during eFUSE programming.                                      | –                   | –                  | 115                 | mA    |
| <i>Calibrated programmable on-die termination (DCI) in HP I/O banks<sup>(7)</sup> (measured per JEDEC specification).</i> |                                                                                                             |                     |                    |                     |       |
| R <sup>(9)</sup>                                                                                                          | Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_40. | –10% <sup>(8)</sup> | 40                 | +10% <sup>(8)</sup> | Ω     |
|                                                                                                                           | Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_48. | –10% <sup>(8)</sup> | 48                 | +10% <sup>(8)</sup> | Ω     |
|                                                                                                                           | Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_60. | –10% <sup>(8)</sup> | 60                 | +10% <sup>(8)</sup> | Ω     |
|                                                                                                                           | Programmable input termination to V <sub>CCO</sub> where ODT = RTT_40.                                      | –10% <sup>(8)</sup> | 40                 | +10% <sup>(8)</sup> | Ω     |
|                                                                                                                           | Programmable input termination to V <sub>CCO</sub> where ODT = RTT_48.                                      | –10% <sup>(8)</sup> | 48                 | +10% <sup>(8)</sup> | Ω     |
|                                                                                                                           | Programmable input termination to V <sub>CCO</sub> where ODT = RTT_60.                                      | –10% <sup>(8)</sup> | 60                 | +10% <sup>(8)</sup> | Ω     |
|                                                                                                                           | Programmable input termination to V <sub>CCO</sub> where ODT = RTT_120.                                     | –10% <sup>(8)</sup> | 120                | +10% <sup>(8)</sup> | Ω     |
|                                                                                                                           | Programmable input termination to V <sub>CCO</sub> where ODT = RTT_240.                                     | –10% <sup>(8)</sup> | 240                | +10% <sup>(8)</sup> | Ω     |

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

| Symbol                                                                                                  | Description                                                                                         | Min                   | Typ <sup>(1)</sup>    | Max                   | Units    |
|---------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|-----------------------|-----------------------|-----------------------|----------|
| <i>Uncalibrated programmable on-die termination in HP I/O banks (measured per JEDEC specification).</i> |                                                                                                     |                       |                       |                       |          |
| R <sup>(9)</sup>                                                                                        | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40. | –50%                  | 40                    | +50%                  | $\Omega$ |
|                                                                                                         | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48. | –50%                  | 48                    | +50%                  | $\Omega$ |
|                                                                                                         | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60. | –50%                  | 60                    | +50%                  | $\Omega$ |
|                                                                                                         | Programmable input termination to $V_{CCO}$ where ODT = RTT_40.                                     | –50%                  | 40                    | +50%                  | $\Omega$ |
|                                                                                                         | Programmable input termination to $V_{CCO}$ where ODT = RTT_48.                                     | –50%                  | 48                    | +50%                  | $\Omega$ |
|                                                                                                         | Programmable input termination to $V_{CCO}$ where ODT = RTT_60.                                     | –50%                  | 60                    | +50%                  | $\Omega$ |
|                                                                                                         | Programmable input termination to $V_{CCO}$ where ODT = RTT_120.                                    | –50%                  | 120                   | +50%                  | $\Omega$ |
|                                                                                                         | Programmable input termination to $V_{CCO}$ where ODT = RTT_240.                                    | –50%                  | 240                   | +50%                  | $\Omega$ |
| <i>Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification).</i> |                                                                                                     |                       |                       |                       |          |
| R <sup>(9)</sup>                                                                                        | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48. | –50%                  | 48                    | +50%                  | $\Omega$ |
| Internal $V_{REF}$                                                                                      | 50% $V_{CCO}$                                                                                       | $V_{CCO} \times 0.49$ | $V_{CCO} \times 0.50$ | $V_{CCO} \times 0.51$ | V        |
|                                                                                                         | 70% $V_{CCO}$                                                                                       | $V_{CCO} \times 0.69$ | $V_{CCO} \times 0.70$ | $V_{CCO} \times 0.71$ | V        |
| Differential termination                                                                                | Programmable differential termination (TERM_100) for HP I/O banks.                                  | –35%                  | 100                   | +35%                  | $\Omega$ |
| n                                                                                                       | Temperature diode ideality factor.                                                                  | –                     | 1.026                 | –                     | –        |
| r                                                                                                       | Temperature diode series resistance.                                                                | –                     | 2                     | –                     | $\Omega$ |

**Notes:**

- Typical values are specified at nominal voltage, 25°C.
- For HP I/O banks with a  $V_{CCO}$  of 1.8V and separated  $V_{CCO}$  and  $V_{CCAUX\_IO}$  power supplies, the  $I_L$  maximum current is 70  $\mu$ A.
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- $I_{BATT}$  is measured when the battery-backed RAM (BBRAM) is enabled.
- Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
- If VRP resides at a different bank (DCI cascade), the range increases to  $\pm 15\%$ .
- VRP resistor tolerance is  $(240\Omega \pm 1\%)$
- On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide (UG571)*.

# $V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot

Table 4:  $V_{IN}$  Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks<sup>(1)</sup>

| AC Voltage Overshoot | % of UI at $-40^{\circ}\text{C}$ to $100^{\circ}\text{C}$ | AC Voltage Undershoot | % of UI at $-40^{\circ}\text{C}$ to $100^{\circ}\text{C}$ |
|----------------------|-----------------------------------------------------------|-----------------------|-----------------------------------------------------------|
| $V_{CCO} + 0.30$     | 100%                                                      | $-0.30$               | 100%                                                      |
| $V_{CCO} + 0.35$     | 100%                                                      | $-0.35$               | 90%                                                       |
| $V_{CCO} + 0.40$     | 100%                                                      | $-0.40$               | 78%                                                       |
| $V_{CCO} + 0.45$     | 100%                                                      | $-0.45$               | 40%                                                       |
| $V_{CCO} + 0.50$     | 100%                                                      | $-0.50$               | 24%                                                       |
| $V_{CCO} + 0.55$     | 100%                                                      | $-0.55$               | 18.0%                                                     |
| $V_{CCO} + 0.60$     | 100%                                                      | $-0.60$               | 13.0%                                                     |
| $V_{CCO} + 0.65$     | 100%                                                      | $-0.65$               | 10.8%                                                     |
| $V_{CCO} + 0.70$     | 92%                                                       | $-0.70$               | 9.0%                                                      |
| $V_{CCO} + 0.75$     | 92%                                                       | $-0.75$               | 7.0%                                                      |
| $V_{CCO} + 0.80$     | 92%                                                       | $-0.80$               | 6.0%                                                      |
| $V_{CCO} + 0.85$     | 92%                                                       | $-0.85$               | 5.0%                                                      |
| $V_{CCO} + 0.90$     | 92%                                                       | $-0.90$               | 4.0%                                                      |
| $V_{CCO} + 0.95$     | 92%                                                       | $-0.95$               | 2.5%                                                      |

## Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5:  $V_{IN}$  Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks<sup>(1)(2)</sup>

| AC Voltage Overshoot | % of UI at $-40^{\circ}\text{C}$ to $100^{\circ}\text{C}$ | AC Voltage Undershoot | % of UI at $-40^{\circ}\text{C}$ to $100^{\circ}\text{C}$ |
|----------------------|-----------------------------------------------------------|-----------------------|-----------------------------------------------------------|
| $V_{CCO} + 0.30$     | 100%                                                      | $-0.30$               | 100%                                                      |
| $V_{CCO} + 0.35$     | 100%                                                      | $-0.35$               | 90%                                                       |
| $V_{CCO} + 0.40$     | 92%                                                       | $-0.40$               | 92%                                                       |
| $V_{CCO} + 0.45$     | 50%                                                       | $-0.45$               | 50%                                                       |
| $V_{CCO} + 0.50$     | 20%                                                       | $-0.50$               | 20%                                                       |
| $V_{CCO} + 0.55$     | 10%                                                       | $-0.55$               | 10%                                                       |
| $V_{CCO} + 0.60$     | 6%                                                        | $-0.60$               | 6%                                                        |
| $V_{CCO} + 0.65$     | 2%                                                        | $-0.65$               | 2%                                                        |
| $V_{CCO} + 0.70$     | 2%                                                        | $-0.70$               | 2%                                                        |

## Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20  $\mu\text{s}$ .

# Quiescent Supply Current

Table 6: Typical Quiescent Supply Current<sup>(1)(2)(3)</sup>

| Symbol                 | Description                                     | Device      | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |      |       |      | Units |
|------------------------|-------------------------------------------------|-------------|----------------------------------------------------------|-------|------|-------|------|-------|
|                        |                                                 |             | 0.90V                                                    | 0.85V |      | 0.72V |      |       |
|                        |                                                 |             | -3                                                       | -2    | -1   | -2    | -1   |       |
| I <sub>CCINTQ</sub>    | Quiescent V <sub>CCINT</sub> supply current.    | XCKU3P      | 1242                                                     | 1181  | 1181 | 1037  | 1037 | mA    |
|                        |                                                 | XCKU5P      | 1242                                                     | 1181  | 1181 | 1037  | 1037 | mA    |
|                        |                                                 | XCKU9P      | 1592                                                     | 1523  | 1523 | 1356  | 1356 | mA    |
|                        |                                                 | XCKU11P     | 1780                                                     | 1693  | 1693 | 1486  | 1486 | mA    |
|                        |                                                 | XCKU13P     | 1950                                                     | 1864  | 1864 | 1658  | 1658 | mA    |
|                        |                                                 | XCKU15P     | 2677                                                     | 2559  | 2559 | 2275  | 2275 | mA    |
| I <sub>CCINT_IOQ</sub> | Quiescent V <sub>CCINT_IO</sub> supply current. | XCKU3P      | 61                                                       | 59    | 59   | 59    | 59   | mA    |
|                        |                                                 | XCKU5P      | 61                                                       | 59    | 59   | 59    | 59   | mA    |
|                        |                                                 | XCKU9P      | 61                                                       | 59    | 59   | 59    | 59   | mA    |
|                        |                                                 | XCKU11P     | 120                                                      | 115   | 115  | 115   | 115  | mA    |
|                        |                                                 | XCKU13P     | 61                                                       | 59    | 59   | 59    | 59   | mA    |
|                        |                                                 | XCKU15P     | 164                                                      | 158   | 158  | 158   | 158  | mA    |
| I <sub>CCOQ</sub>      | Quiescent V <sub>CCO</sub> supply current.      | All devices | 1                                                        | 1     | 1    | 1     | 1    | mA    |
| I <sub>CCAUXQ</sub>    | Quiescent V <sub>CCAUX</sub> supply current.    | XCKU3P      | 153                                                      | 153   | 153  | 153   | 153  | mA    |
|                        |                                                 | XCKU5P      | 153                                                      | 153   | 153  | 153   | 153  | mA    |
|                        |                                                 | XCKU9P      | 227                                                      | 227   | 227  | 227   | 227  | mA    |
|                        |                                                 | XCKU11P     | 255                                                      | 255   | 255  | 255   | 255  | mA    |
|                        |                                                 | XCKU13P     | 266                                                      | 266   | 266  | 266   | 266  | mA    |
|                        |                                                 | XCKU15P     | 396                                                      | 396   | 396  | 396   | 396  | mA    |
| I <sub>CCAUX_IOQ</sub> | Quiescent V <sub>CCAUX_IO</sub> supply current. | XCKU3P      | 32                                                       | 32    | 32   | 32    | 32   | mA    |
|                        |                                                 | XCKU5P      | 32                                                       | 32    | 32   | 32    | 32   | mA    |
|                        |                                                 | XCKU9P      | 33                                                       | 33    | 33   | 33    | 33   | mA    |
|                        |                                                 | XCKU11P     | 56                                                       | 56    | 56   | 56    | 56   | mA    |
|                        |                                                 | XCKU13P     | 33                                                       | 33    | 33   | 33    | 33   | mA    |
|                        |                                                 | XCKU15P     | 74                                                       | 74    | 74   | 74    | 74   | mA    |
| I <sub>CCBRAMQ</sub>   | Quiescent V <sub>CCBRAM</sub> supply current.   | XCKU3P      | 18                                                       | 17    | 17   | 17    | 17   | mA    |
|                        |                                                 | XCKU5P      | 18                                                       | 17    | 17   | 17    | 17   | mA    |
|                        |                                                 | XCKU9P      | 25                                                       | 24    | 24   | 24    | 24   | mA    |
|                        |                                                 | XCKU11P     | 23                                                       | 22    | 22   | 22    | 22   | mA    |
|                        |                                                 | XCKU13P     | 29                                                       | 28    | 28   | 28    | 28   | mA    |
|                        |                                                 | XCKU15P     | 37                                                       | 35    | 35   | 35    | 35   | mA    |

## Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T<sub>j</sub>) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at [www.xilinx.com/power](http://www.xilinx.com/power)) to estimate static power consumption for conditions other than those specified.

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is  $V_{CCINT}$ ,  $V_{CCINT\_IO}/V_{CCBRAM}$ ,  $V_{CCAUX}/V_{CCAUX\_IO}$ , and  $V_{CCO}$  to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If  $V_{CCINT}$  and  $V_{CCINT\_IO}/V_{CCBRAM}$  have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously.  $V_{CCINT\_IO}$  must be connected to  $V_{CCBRAM}$ . If  $V_{CCAUX}/V_{CCAUX\_IO}$  and  $V_{CCO}$  have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously.  $V_{CCAUX}$  and  $V_{CCAUX\_IO}$  must be connected together.  $V_{CCADC}$  and  $V_{REF}$  can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is  $V_{CCINT}$ ,  $V_{MGTAVCC}$ ,  $V_{MGTAVTT}$  OR  $V_{MGTAVCC}$ ,  $V_{CCINT}$ ,  $V_{MGTAVTT}$ . There is no recommended sequencing for  $V_{MGTVCCAUX}$ . Both  $V_{MGTAVCC}$  and  $V_{CCINT}$  can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from  $V_{MGTAVTT}$  can be higher than specifications during power-up and power-down.

## Power Supply Requirements

Table 7 shows the minimum current, in addition to  $I_{CCQ}$  maximum, required by each Kintex UltraScale+ FPGA for proper power-on and configuration. If the current minimums shown in Table 7 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after  $V_{CCINT}$  is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 7: Power-on Current by Device<sup>(1)</sup>

| Device  | $I_{CCINTMIN}$      | $I_{CCINT\_IOMIN} + I_{CCBRAMMIN}$    | $I_{CCOMIN}$    | $I_{CCAUXMIN} + I_{CCAUX\_IOMIN}$    | Units |
|---------|---------------------|---------------------------------------|-----------------|--------------------------------------|-------|
| XCKU3P  | $I_{CCINTQ} + 770$  | $I_{CCBRAMQ} + I_{CCINT\_IOQ} + 229$  | $I_{CCOQ} + 50$ | $I_{CCAUXQ} + I_{CCAUX\_IOQ} + 386$  | mA    |
| XCKU5P  | $I_{CCINTQ} + 770$  | $I_{CCBRAMQ} + I_{CCINT\_IOQ} + 305$  | $I_{CCOQ} + 50$ | $I_{CCAUXQ} + I_{CCAUX\_IOQ} + 515$  | mA    |
| XCKU9P  | $I_{CCINTQ} + 1800$ | $I_{CCBRAMQ} + I_{CCINT\_IOQ} + 600$  | $I_{CCOQ} + 50$ | $I_{CCAUXQ} + I_{CCAUX\_IOQ} + 650$  | mA    |
| XCKU11P | $I_{CCINTQ} + 1961$ | $I_{CCBRAMQ} + I_{CCINT\_IOQ} + 654$  | $I_{CCOQ} + 55$ | $I_{CCAUXQ} + I_{CCAUX\_IOQ} + 709$  | mA    |
| XCKU13P | $I_{CCINTQ} + 2242$ | $I_{CCBRAMQ} + I_{CCINT\_IOQ} + 748$  | $I_{CCOQ} + 63$ | $I_{CCAUXQ} + I_{CCAUX\_IOQ} + 810$  | mA    |
| XCKU15P | $I_{CCINTQ} + 3433$ | $I_{CCBRAMQ} + I_{CCINT\_IOQ} + 1145$ | $I_{CCOQ} + 96$ | $I_{CCAUXQ} + I_{CCAUX\_IOQ} + 1240$ | mA    |

### Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at [www.xilinx.com/power](http://www.xilinx.com/power)) to estimate power-on current for all supplies.

Table 8 shows the power supply ramp time.

Table 8: Power Supply Ramp Time

| Symbol           | Description                                    | Min | Max | Units |
|------------------|------------------------------------------------|-----|-----|-------|
| $T_{VCCINT}$     | Ramp time from GND to 95% of $V_{CCINT}$ .     | 0.2 | 40  | ms    |
| $T_{VCCINT\_IO}$ | Ramp time from GND to 95% of $V_{CCINT\_IO}$ . | 0.2 | 40  | ms    |
| $T_{VCCO}$       | Ramp time from GND to 95% of $V_{CCO}$ .       | 0.2 | 40  | ms    |
| $T_{VCCAUX}$     | Ramp time from GND to 95% of $V_{CCAUX}$ .     | 0.2 | 40  | ms    |
| $T_{VCCBRAM}$    | Ramp time from GND to 95% of $V_{CCBRAM}$ .    | 0.2 | 40  | ms    |
| $T_{MGTAVCC}$    | Ramp time from GND to 95% of $V_{MGTAVCC}$ .   | 0.2 | 40  | ms    |
| $T_{MGTAVTT}$    | Ramp time from GND to 95% of $V_{MGTAVTT}$ .   | 0.2 | 40  | ms    |
| $T_{MGTVCCAUX}$  | Ramp time from GND to 95% of $V_{MGTVCCAUX}$ . | 0.2 | 40  | ms    |

## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Table 9: SelectIO DC Input and Output Levels For HD I/O Banks<sup>(1)(2)</sup>

| I/O Standard | $V_{IL}$ |                   | $V_{IH}$          |                   | $V_{OL}$            | $V_{OH}$            | $I_{OL}$ | $I_{OH}$ |
|--------------|----------|-------------------|-------------------|-------------------|---------------------|---------------------|----------|----------|
|              | V, Min   | V, Max            | V, Min            | V, Max            | V, Max              | V, Min              | mA       | mA       |
| HSTL_I       | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 8.0      | -8.0     |
| HSTL_I_18    | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 8.0      | -8.0     |
| HSUL_12      | -0.300   | $V_{REF} - 0.130$ | $V_{REF} + 0.130$ | $V_{CCO} + 0.300$ | 20% $V_{CCO}$       | 80% $V_{CCO}$       | 0.1      | -0.1     |
| LVC MOS12    | -0.300   | 35% $V_{CCO}$     | 65% $V_{CCO}$     | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | Note 3   | Note 3   |
| LVC MOS15    | -0.300   | 35% $V_{CCO}$     | 65% $V_{CCO}$     | $V_{CCO} + 0.300$ | 0.450               | $V_{CCO} - 0.450$   | Note 4   | Note 4   |
| LVC MOS18    | -0.300   | 35% $V_{CCO}$     | 65% $V_{CCO}$     | $V_{CCO} + 0.300$ | 0.450               | $V_{CCO} - 0.450$   | Note 4   | Note 4   |
| LVC MOS25    | -0.300   | 0.700             | 1.700             | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | Note 4   | Note 4   |
| LVC MOS33    | -0.300   | 0.800             | 2.000             | 3.400             | 0.400               | $V_{CCO} - 0.400$   | Note 4   | Note 4   |
| LV TTL       | -0.300   | 0.800             | 2.000             | 3.400             | 0.400               | 2.400               | Note 4   | Note 4   |
| SSTL12       | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 14.25    | -14.25   |
| SSTL135      | -0.300   | $V_{REF} - 0.090$ | $V_{REF} + 0.090$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 8.9      | -8.9     |
| SSTL135_II   | -0.300   | $V_{REF} - 0.090$ | $V_{REF} + 0.090$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 13.0     | -13.0    |
| SSTL15       | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.175$ | $V_{CCO}/2 + 0.175$ | 8.9      | -8.9     |
| SSTL15_II    | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.175$ | $V_{CCO}/2 + 0.175$ | 13.0     | -13.0    |
| SSTL18_I     | -0.300   | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.470$ | $V_{CCO}/2 + 0.470$ | 8.0      | -8.0     |
| SSTL18_II    | -0.300   | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.600$ | $V_{CCO}/2 + 0.600$ | 13.4     | -13.4    |

### Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
3. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.

Table 10: SelectIO DC Input and Output Levels for HP I/O Banks<sup>(1)(2)(3)</sup>

| I/O Standard                    | V <sub>IL</sub> |                          | V <sub>IH</sub>          |                          | V <sub>OL</sub>             | V <sub>OH</sub>             | I <sub>OL</sub> | I <sub>OH</sub> |
|---------------------------------|-----------------|--------------------------|--------------------------|--------------------------|-----------------------------|-----------------------------|-----------------|-----------------|
|                                 | V, Min          | V, Max                   | V, Min                   | V, Max                   | V, Max                      | V, Min                      | mA              | mA              |
| HSTL_I                          | −0.300          | V <sub>REF</sub> − 0.100 | V <sub>REF</sub> + 0.100 | V <sub>CCO</sub> + 0.300 | 0.400                       | V <sub>CCO</sub> − 0.400    | 5.8             | −5.8            |
| HSTL_I_12                       | −0.300          | V <sub>REF</sub> − 0.080 | V <sub>REF</sub> + 0.080 | V <sub>CCO</sub> + 0.300 | 25% V <sub>CCO</sub>        | 75% V <sub>CCO</sub>        | 4.1             | −4.1            |
| HSTL_I_18                       | −0.300          | V <sub>REF</sub> − 0.100 | V <sub>REF</sub> + 0.100 | V <sub>CCO</sub> + 0.300 | 0.400                       | V <sub>CCO</sub> − 0.400    | 6.2             | −6.2            |
| HSUL_12                         | −0.300          | V <sub>REF</sub> − 0.130 | V <sub>REF</sub> + 0.130 | V <sub>CCO</sub> + 0.300 | 20% V <sub>CCO</sub>        | 80% V <sub>CCO</sub>        | 0.1             | −0.1            |
| LVC MOS12                       | −0.300          | 35% V <sub>CCO</sub>     | 65% V <sub>CCO</sub>     | V <sub>CCO</sub> + 0.300 | 0.400                       | V <sub>CCO</sub> − 0.400    | Note 4          | Note 4          |
| LVC MOS15                       | −0.300          | 35% V <sub>CCO</sub>     | 65% V <sub>CCO</sub>     | V <sub>CCO</sub> + 0.300 | 0.450                       | V <sub>CCO</sub> − 0.450    | Note 5          | Note 5          |
| LVC MOS18                       | −0.300          | 35% V <sub>CCO</sub>     | 65% V <sub>CCO</sub>     | V <sub>CCO</sub> + 0.300 | 0.450                       | V <sub>CCO</sub> − 0.450    | Note 5          | Note 5          |
| LVDCI_15                        | −0.300          | 35% V <sub>CCO</sub>     | 65% V <sub>CCO</sub>     | V <sub>CCO</sub> + 0.300 | 0.450                       | V <sub>CCO</sub> − 0.450    | 7.0             | −7.0            |
| LVDCI_18                        | −0.300          | 35% V <sub>CCO</sub>     | 65% V <sub>CCO</sub>     | V <sub>CCO</sub> + 0.300 | 0.450                       | V <sub>CCO</sub> − 0.450    | 7.0             | −7.0            |
| SSTL12                          | −0.300          | V <sub>REF</sub> − 0.100 | V <sub>REF</sub> + 0.100 | V <sub>CCO</sub> + 0.300 | V <sub>CCO</sub> /2 − 0.150 | V <sub>CCO</sub> /2 + 0.150 | 8.0             | −8.0            |
| SSTL135                         | −0.300          | V <sub>REF</sub> − 0.090 | V <sub>REF</sub> + 0.090 | V <sub>CCO</sub> + 0.300 | V <sub>CCO</sub> /2 − 0.150 | V <sub>CCO</sub> /2 + 0.150 | 9.0             | −9.0            |
| SSTL15                          | −0.300          | V <sub>REF</sub> − 0.100 | V <sub>REF</sub> + 0.100 | V <sub>CCO</sub> + 0.300 | V <sub>CCO</sub> /2 − 0.175 | V <sub>CCO</sub> /2 + 0.175 | 10.0            | −10.0           |
| SSTL18_I                        | −0.300          | V <sub>REF</sub> − 0.125 | V <sub>REF</sub> + 0.125 | V <sub>CCO</sub> + 0.300 | V <sub>CCO</sub> /2 − 0.470 | V <sub>CCO</sub> /2 + 0.470 | 7.0             | −7.0            |
| MIPI_DPHY_DCI_LP <sup>(6)</sup> | −0.300          | 0.550                    | 0.880                    | V <sub>CCO</sub> + 0.300 | 0.050                       | 1.100                       | 0.01            | −0.01           |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
3. POD10 and POD12 DC input and output levels are shown in [Table 11](#), [Table 15](#), [Table 16](#), and [Table 17](#).
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI\_DPHY\_DCI.

Table 11: DC Input Levels for Single-ended POD10 and POD12 I/O Standards<sup>(1)(2)</sup>

| I/O Standard | V <sub>IL</sub> |                          | V <sub>IH</sub>          |                          |
|--------------|-----------------|--------------------------|--------------------------|--------------------------|
|              | V, Min          | V, Max                   | V, Min                   | V, Max                   |
| POD10        | −0.300          | V <sub>REF</sub> − 0.068 | V <sub>REF</sub> + 0.068 | V <sub>CCO</sub> + 0.300 |
| POD12        | −0.300          | V <sub>REF</sub> − 0.068 | V <sub>REF</sub> + 0.068 | V <sub>CCO</sub> + 0.300 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 12: Differential SelectIO DC Input and Output Levels

| I/O Standard                    | V <sub>ICM</sub> (V) <sup>(1)</sup> |       |       | V <sub>ID</sub> (V) <sup>(2)</sup> |       |       | V <sub>ILHS</sub> <sup>(3)</sup> | V <sub>IHHS</sub> <sup>(3)</sup> | V <sub>OCM</sub> (V) <sup>(4)</sup> |       |       | V <sub>OD</sub> (V) <sup>(5)</sup> |       |       |
|---------------------------------|-------------------------------------|-------|-------|------------------------------------|-------|-------|----------------------------------|----------------------------------|-------------------------------------|-------|-------|------------------------------------|-------|-------|
|                                 | Min                                 | Typ   | Max   | Min                                | Typ   | Max   | Min                              | Max                              | Min                                 | Typ   | Max   | Min                                | Typ   | Max   |
| SUB_LVDS <sup>(8)</sup>         | 0.500                               | 0.900 | 1.300 | 0.070                              | –     | –     | –                                | –                                | 0.700                               | 0.900 | 1.100 | 0.100                              | 0.150 | 0.200 |
| LVPECL                          | 0.300                               | 1.200 | 1.425 | 0.100                              | 0.350 | 0.600 | –                                | –                                | –                                   | –     | –     | –                                  | –     | –     |
| SLVS_400_18                     | 0.070                               | 0.200 | 0.330 | 0.140                              | –     | 0.450 | –                                | –                                | –                                   | –     | –     | –                                  | –     | –     |
| SLVS_400_25                     | 0.070                               | 0.200 | 0.330 | 0.140                              | –     | 0.450 | –                                | –                                | –                                   | –     | –     | –                                  | –     | –     |
| MIPI_DPHY_DCI_HS <sup>(9)</sup> | 0.070                               | –     | 0.330 | 0.070                              | –     | –     | –0.040                           | 0.460                            | 0.150                               | 0.200 | 0.250 | 0.140                              | 0.200 | 0.270 |

**Notes:**

- V<sub>ICM</sub> is the input common mode voltage.
- V<sub>ID</sub> is the input differential voltage (Q –  $\overline{Q}$ ).
- V<sub>IHHS</sub> and V<sub>ILHS</sub> are the single-ended input high and low voltages, respectively.
- V<sub>OCM</sub> is the output common mode voltage.
- V<sub>OD</sub> is the output differential voltage (Q –  $\overline{Q}$ ).
- LVDS\_25 is specified in Table 18.
- LVDS is specified in Table 19.
- Only the SUB\_LVDS receiver is supported in HD I/O banks.
- High-speed option for MIPI\_DPHY\_DCI. The V<sub>ID</sub> maximum is aligned with the standard's specification. A higher V<sub>ID</sub> is acceptable as long as the V<sub>IN</sub> specification is also met.

Table 13: Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks

| I/O Standard    | V <sub>ICM</sub> (V) <sup>(1)</sup> |       |       | V <sub>ID</sub> (V) <sup>(2)</sup> |     | V <sub>OL</sub> (V) <sup>(3)</sup> | V <sub>OH</sub> (V) <sup>(4)</sup> | I <sub>OL</sub> | I <sub>OH</sub> |
|-----------------|-------------------------------------|-------|-------|------------------------------------|-----|------------------------------------|------------------------------------|-----------------|-----------------|
|                 | Min                                 | Typ   | Max   | Min                                | Max | Max                                | Min                                | mA              | mA              |
| DIFF_HSTL_I     | 0.300                               | 0.750 | 1.125 | 0.100                              | –   | 0.400                              | V <sub>CCO</sub> – 0.400           | 8.0             | –8.0            |
| DIFF_HSTL_I_18  | 0.300                               | 0.900 | 1.425 | 0.100                              | –   | 0.400                              | V <sub>CCO</sub> – 0.400           | 8.0             | –8.0            |
| DIFF_HSUL_12    | 0.300                               | 0.600 | 0.850 | 0.100                              | –   | 20% V <sub>CCO</sub>               | 80% V <sub>CCO</sub>               | 0.1             | –0.1            |
| DIFF_SSTL12     | 0.300                               | 0.600 | 0.850 | 0.100                              | –   | (V <sub>CCO</sub> /2) – 0.150      | (V <sub>CCO</sub> /2) + 0.150      | 14.25           | –14.25          |
| DIFF_SSTL135    | 0.300                               | 0.675 | 1.000 | 0.100                              | –   | (V <sub>CCO</sub> /2) – 0.150      | (V <sub>CCO</sub> /2) + 0.150      | 8.9             | –8.9            |
| DIFF_SSTL135_II | 0.300                               | 0.675 | 1.000 | 0.100                              | –   | (V <sub>CCO</sub> /2) – 0.150      | (V <sub>CCO</sub> /2) + 0.150      | 13.0            | –13.0           |
| DIFF_SSTL15     | 0.300                               | 0.750 | 1.125 | 0.100                              | –   | (V <sub>CCO</sub> /2) – 0.175      | (V <sub>CCO</sub> /2) + 0.175      | 8.9             | –8.9            |
| DIFF_SSTL15_II  | 0.300                               | 0.750 | 1.125 | 0.100                              | –   | (V <sub>CCO</sub> /2) – 0.175      | (V <sub>CCO</sub> /2) + 0.175      | 13.0            | –13.0           |
| DIFF_SSTL18_I   | 0.300                               | 0.900 | 1.425 | 0.100                              | –   | (V <sub>CCO</sub> /2) – 0.470      | (V <sub>CCO</sub> /2) + 0.470      | 8.0             | –8.0            |
| DIFF_SSTL18_II  | 0.300                               | 0.900 | 1.425 | 0.100                              | –   | (V <sub>CCO</sub> /2) – 0.600      | (V <sub>CCO</sub> /2) + 0.600      | 13.4            | –13.4           |

**Notes:**

- V<sub>ICM</sub> is the input common mode voltage.
- V<sub>ID</sub> is the input differential voltage.
- V<sub>OL</sub> is the single-ended low-output voltage.
- V<sub>OH</sub> is the single-ended high-output voltage.

Table 14: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks<sup>(1)</sup>

| I/O Standard   | $V_{ICM}$ (V) <sup>(2)</sup> |             |                        | $V_{ID}$ (V) <sup>(3)</sup> |     | $V_{OL}$ (V) <sup>(4)</sup> | $V_{OH}$ (V) <sup>(5)</sup> | $I_{OL}$ | $I_{OH}$ |
|----------------|------------------------------|-------------|------------------------|-----------------------------|-----|-----------------------------|-----------------------------|----------|----------|
|                | Min                          | Typ         | Max                    | Min                         | Max | Max                         | Min                         | mA       | mA       |
| DIFF_HSTL_I    | 0.680                        | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.150$  | 0.100                       | –   | 0.400                       | $V_{CCO} - 0.400$           | 5.8      | –5.8     |
| DIFF_HSTL_I_12 | $0.400 \times V_{CCO}$       | $V_{CCO}/2$ | $0.600 \times V_{CCO}$ | 0.100                       | –   | $0.250 \times V_{CCO}$      | $0.750 \times V_{CCO}$      | 4.1      | –4.1     |
| DIFF_HSTL_I_18 | $(V_{CCO}/2) - 0.175$        | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.175$  | 0.100                       | –   | 0.400                       | $V_{CCO} - 0.400$           | 6.2      | –6.2     |
| DIFF_HSUL_12   | $(V_{CCO}/2) - 0.120$        | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.120$  | 0.100                       | –   | $20\% V_{CCO}$              | $80\% V_{CCO}$              | 0.1      | –0.1     |
| DIFF_SSTL12    | $(V_{CCO}/2) - 0.150$        | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.150$  | 0.100                       | –   | $(V_{CCO}/2) - 0.150$       | $(V_{CCO}/2) + 0.150$       | 8.0      | –8.0     |
| DIFF_SSTL135   | $(V_{CCO}/2) - 0.150$        | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.150$  | 0.100                       | –   | $(V_{CCO}/2) - 0.150$       | $(V_{CCO}/2) + 0.150$       | 9.0      | –9.0     |
| DIFF_SSTL15    | $(V_{CCO}/2) - 0.175$        | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.175$  | 0.100                       | –   | $(V_{CCO}/2) - 0.175$       | $(V_{CCO}/2) + 0.175$       | 10.0     | –10.0    |
| DIFF_SSTL18_I  | $(V_{CCO}/2) - 0.175$        | $V_{CCO}/2$ | $(V_{CCO}/2) + 0.175$  | 0.100                       | –   | $(V_{CCO}/2) - 0.470$       | $(V_{CCO}/2) + 0.470$       | 7.0      | –7.0     |

**Notes:**

1. DIFF\_POD10 and DIFF\_POD12 HP I/O bank specifications are shown in Table 15, Table 16, and Table 17.
2.  $V_{ICM}$  is the input common mode voltage.
3.  $V_{ID}$  is the input differential voltage.
4.  $V_{OL}$  is the single-ended low-output voltage.
5.  $V_{OH}$  is the single-ended high-output voltage.

Table 15: DC Input Levels for Differential POD10 and POD12 I/O Standards<sup>(1)(2)</sup>

| I/O Standard | $V_{ICM}$ (V) |      |      | $V_{ID}$ (V) |     |
|--------------|---------------|------|------|--------------|-----|
|              | Min           | Typ  | Max  | Min          | Max |
| DIFF_POD10   | 0.63          | 0.70 | 0.77 | 0.14         | –   |
| DIFF_POD12   | 0.76          | 0.84 | 0.92 | 0.16         | –   |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 16: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards<sup>(1)(2)</sup>

| Symbol   | Description           | $V_{OUT}$                               | Min | Typ | Max | Units    |
|----------|-----------------------|-----------------------------------------|-----|-----|-----|----------|
| $R_{OL}$ | Pull-down resistance. | $V_{OM\_DC}$ (as described in Table 17) | 36  | 40  | 44  | $\Omega$ |
| $R_{OH}$ | Pull-up resistance.   | $V_{OM\_DC}$ (as described in Table 17) | 36  | 40  | 44  | $\Omega$ |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 17: Table 16 Definitions for DC Output Levels for POD Standards

| Symbol       | Description                                               | All Speed Grades     | Units |
|--------------|-----------------------------------------------------------|----------------------|-------|
| $V_{OM\_DC}$ | DC output Mid measurement level (for IV curve linearity). | $0.8 \times V_{CCO}$ | V     |

## LVDS DC Specifications (LVDS\_25)

The LVDS\_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 18: LVDS\_25 DC Specifications

| Symbol          | DC Parameter                                                                                                      | Conditions | Min   | Typ   | Max                | Units |
|-----------------|-------------------------------------------------------------------------------------------------------------------|------------|-------|-------|--------------------|-------|
| $V_{CCO}^{(1)}$ | Supply voltage.                                                                                                   |            | 2.375 | 2.500 | 2.625              | V     |
| $V_{IDIFF}$     | Differential input voltage:<br>( $Q - \bar{Q}$ ), $Q = \text{High}$<br>( $\bar{Q} - Q$ ), $\bar{Q} = \text{High}$ |            | 100   | 350   | 600 <sup>(2)</sup> | mV    |
| $V_{ICM}$       | Input common-mode voltage.                                                                                        |            | 0.300 | 1.200 | 1.425              | V     |

### Notes:

1. LVDS\_25 in HD I/O banks supports inputs only. LVDS\_25 inputs without internal termination have no  $V_{CCO}$  requirements. Any  $V_{CCO}$  can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the  $V_{IN}$  I/O pin voltage.
2. Maximum  $V_{IDIFF}$  value is specified for the maximum  $V_{ICM}$  specification. With a lower  $V_{ICM}$ , a higher  $V_{IDIFF}$  is tolerated only when the recommended operating conditions and overshoot/undershoot  $V_{IN}$  specifications are maintained.

## LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 19: LVDS DC Specifications

| Symbol              | DC Parameter                                                                                                       | Conditions                                         | Min   | Typ   | Max                | Units |
|---------------------|--------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|-------|-------|--------------------|-------|
| $V_{CCO}^{(1)}$     | Supply voltage.                                                                                                    |                                                    | 1.710 | 1.800 | 1.890              | V     |
| $V_{ODIFF}^{(2)}$   | Differential output voltage:<br>( $Q - \bar{Q}$ ), $Q = \text{High}$<br>( $\bar{Q} - Q$ ), $\bar{Q} = \text{High}$ | $R_T = 100\Omega$ across $Q$ and $\bar{Q}$ signals | 247   | 350   | 454                | mV    |
| $V_{OCM}^{(2)}$     | Output common-mode voltage.                                                                                        | $R_T = 100\Omega$ across $Q$ and $\bar{Q}$ signals | 1.000 | 1.250 | 1.425              | V     |
| $V_{IDIFF}^{(3)}$   | Differential input voltage:<br>( $Q - \bar{Q}$ ), $Q = \text{High}$<br>( $\bar{Q} - Q$ ), $\bar{Q} = \text{High}$  |                                                    | 100   | 350   | 600 <sup>(3)</sup> | mV    |
| $V_{ICM\_DC}^{(4)}$ | Input common-mode voltage (DC coupling).                                                                           |                                                    | 0.300 | 1.200 | 1.425              | V     |
| $V_{ICM\_AC}^{(5)}$ | Input common-mode voltage (AC coupling).                                                                           |                                                    | 0.600 | –     | 1.100              | V     |

### Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the  $V_{CCO}$  levels are different from the specified level only if internal differential termination is not used. In this scenario,  $V_{CCO}$  must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the  $V_{IN}$  I/O pin voltage.
2.  $V_{OCM}$  and  $V_{ODIFF}$  values are for LVDS\_PRE\_EMPHASIS = FALSE.
3. Maximum  $V_{IDIFF}$  value is specified for the maximum  $V_{ICM}$  specification. With a lower  $V_{ICM}$ , a higher  $V_{IDIFF}$  is tolerated only when the recommended operating conditions and overshoot/undershoot  $V_{IN}$  specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ\_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ\_LEVEL0, EQ\_LEVEL1, EQ\_LEVEL2, EQ\_LEVEL3, EQ\_LEVEL4.

## AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in [Table 20](#).

*Table 20: Speed Specification Version By Device*

| 2017.2 | Device                                       |
|--------|----------------------------------------------|
| 1.09   | XCKU11P                                      |
| 1.12   | XCKU3P, XCKU5P, XCKU9P, XCKU13P, and XCKU15P |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex UltraScale+ FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 21](#) correlates the current status of the Kintex UltraScale+ FPGAs on a per speed grade basis.

**Table 21: Speed Grade Designations by Device**

| Device  | Speed Grade, Temperature Ranges, and $V_{CCINT}$ Operating Voltages                                                                                                                                                                                                                                              |                                                                             |                                                                                                                          |
|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|
|         | Advance                                                                                                                                                                                                                                                                                                          | Preliminary                                                                 | Production                                                                                                               |
| XCKU3P  | -3E ( $V_{CCINT} = 0.90V$ )<br>-2LE ( $V_{CCINT} = 0.85V$ ), -2LE ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup><br>-1LI ( $V_{CCINT} = 0.85V$ ), -1LI ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup>                                                                                                                            |                                                                             | -2E ( $V_{CCINT} = 0.85V$ )<br>-2I ( $V_{CCINT} = 0.85V$ )<br>-1E ( $V_{CCINT} = 0.85V$ )<br>-1I ( $V_{CCINT} = 0.85V$ ) |
| XCKU5P  | -3E ( $V_{CCINT} = 0.90V$ )<br>-2LE ( $V_{CCINT} = 0.85V$ ), -2LE ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup><br>-1LI ( $V_{CCINT} = 0.85V$ ), -1LI ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup>                                                                                                                            |                                                                             | -2E ( $V_{CCINT} = 0.85V$ )<br>-2I ( $V_{CCINT} = 0.85V$ )<br>-1E ( $V_{CCINT} = 0.85V$ )<br>-1I ( $V_{CCINT} = 0.85V$ ) |
| XCKU9P  | -3E ( $V_{CCINT} = 0.90V$ )<br>-2LE ( $V_{CCINT} = 0.85V$ ), -2LE ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup>                                                                                                                                                                                                         | -1LI ( $V_{CCINT} = 0.85V$ )<br>-1LI ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup> | -2E ( $V_{CCINT} = 0.85V$ )<br>-2I ( $V_{CCINT} = 0.85V$ )<br>-1E ( $V_{CCINT} = 0.85V$ )<br>-1I ( $V_{CCINT} = 0.85V$ ) |
| XCKU11P | -3E ( $V_{CCINT} = 0.90V$ )<br>-2E ( $V_{CCINT} = 0.85V$ ), -2I ( $V_{CCINT} = 0.85V$ )<br>-2LE ( $V_{CCINT} = 0.85V$ )<br>-1E ( $V_{CCINT} = 0.85V$ ), -1I ( $V_{CCINT} = 0.85V$ )<br>-1LI ( $V_{CCINT} = 0.85V$ )<br>-2LE ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup> , -1LI ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup> |                                                                             |                                                                                                                          |
| XCKU13P | -3E ( $V_{CCINT} = 0.90V$ )<br>-2LE ( $V_{CCINT} = 0.85V$ ), -2LE ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup><br>-1LI ( $V_{CCINT} = 0.85V$ ), -1LI ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup>                                                                                                                            |                                                                             | -2E ( $V_{CCINT} = 0.85V$ )<br>-2I ( $V_{CCINT} = 0.85V$ )<br>-1E ( $V_{CCINT} = 0.85V$ )<br>-1I ( $V_{CCINT} = 0.85V$ ) |
| XCKU15P | -3E ( $V_{CCINT} = 0.90V$ )<br>-2E ( $V_{CCINT} = 0.85V$ ), -2I ( $V_{CCINT} = 0.85V$ )<br>-2LE ( $V_{CCINT} = 0.85V$ )<br>-1E ( $V_{CCINT} = 0.85V$ ), -1I ( $V_{CCINT} = 0.85V$ )<br>-1LI ( $V_{CCINT} = 0.85V$ )<br>-2LE ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup> , -1LI ( $V_{CCINT} = 0.72V$ ) <sup>(1)</sup> |                                                                             |                                                                                                                          |

### Notes:

1. The lowest power -1L and -2L devices, where  $V_{CCINT} = 0.72V$ , are listed in the Vivado Design Suite as -1LV and -2LV respectively.

## Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 22 lists the production released Kintex UltraScale+ FPGAs, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 22: Kintex UltraScale+ FPGA Device Production Software and Speed Specification Release

| Device  | Speed Grade and V <sub>CCINT</sub> Operating Voltages |                           |    |     |     |       |     |
|---------|-------------------------------------------------------|---------------------------|----|-----|-----|-------|-----|
|         | 0.90V                                                 | 0.85V                     |    |     |     | 0.72V |     |
|         | -3                                                    | -2                        | -1 | -2L | -1L | -2L   | -1L |
| XCKU3P  |                                                       | Vivado tools 2017.1 v1.10 |    |     |     |       |     |
| XCKU5P  |                                                       | Vivado tools 2017.1 v1.10 |    |     |     |       |     |
| XCKU9P  |                                                       | Vivado tools 2017.1 v1.10 |    |     |     |       |     |
| XCKU11P |                                                       |                           |    |     |     |       |     |
| XCKU13P |                                                       | Vivado tools 2017.2 v1.12 |    |     |     |       |     |
| XCKU15P |                                                       |                           |    |     |     |       |     |

### Notes:

- Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

# FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex UltraScale+ FPGAs. These values are subject to the same guidelines as the [AC Switching Characteristics, page 16](#). In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 23: LVDS Component Mode Performance

| Description                                   | I/O Bank Type | Speed Grade and V <sub>CCINT</sub> Operating Voltages |      |       |      |     |      |       |      |     |      | Units |
|-----------------------------------------------|---------------|-------------------------------------------------------|------|-------|------|-----|------|-------|------|-----|------|-------|
|                                               |               | 0.90V                                                 |      | 0.85V |      |     |      | 0.72V |      |     |      |       |
|                                               |               | -3                                                    |      | -2    |      | -1  |      | -2    |      | -1  |      |       |
|                                               |               | Min                                                   | Max  | Min   | Max  | Min | Max  | Min   | Max  | Min | Max  |       |
| LVDS TX DDR (OSERDES 4:1, 8:1)                | HP            | 0                                                     | 1250 | 0     | 1250 | 0   | 1250 | 0     | 1250 | 0   | 1250 | Mb/s  |
| LVDS TX SDR (OSERDES 2:1, 4:1)                | HP            | 0                                                     | 625  | 0     | 625  | 0   | 625  | 0     | 625  | 0   | 625  | Mb/s  |
| LVDS RX DDR (ISERDES 1:4, 1:8) <sup>(1)</sup> | HP            | 0                                                     | 1250 | 0     | 1250 | 0   | 1250 | 0     | 1250 | 0   | 1250 | Mb/s  |
| LVDS RX DDR                                   | HD            | 0                                                     | 250  | 0     | 250  | 0   | 250  | 0     | 250  | 0   | 250  | Mb/s  |
| LVDS RX SDR (ISERDES 1:2, 1:4) <sup>(1)</sup> | HP            | 0                                                     | 625  | 0     | 625  | 0   | 625  | 0     | 625  | 0   | 625  | Mb/s  |
| LVDS RX SDR                                   | HD            | 0                                                     | 125  | 0     | 125  | 0   | 125  | 0     | 125  | 0   | 125  | Mb/s  |

## Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 24: LVDS Native Mode Performance<sup>(1)(2)</sup>

| Description                              | DATA_WIDTH | I/O Bank Type | Speed Grade and V <sub>CCINT</sub> Operating Voltages |      |       |      |       |      |       |      |       |      | Units |
|------------------------------------------|------------|---------------|-------------------------------------------------------|------|-------|------|-------|------|-------|------|-------|------|-------|
|                                          |            |               | 0.90V                                                 |      | 0.85V |      |       |      | 0.72V |      |       |      |       |
|                                          |            |               | -3                                                    |      | -2    |      | -1    |      | -2    |      | -1    |      |       |
|                                          |            |               | Min                                                   | Max  | Min   | Max  | Min   | Max  | Min   | Max  | Min   | Max  |       |
| LVDS TX DDR (TX_BITSLICE)                | 4          | HP            | 375                                                   | 1600 | 375   | 1600 | 375   | 1260 | 375   | 1400 | 375   | 1260 | Mb/s  |
|                                          | 8          |               | 375                                                   | 1600 | 375   | 1600 | 375   | 1260 | 375   | 1600 | 375   | 1260 | Mb/s  |
| LVDS TX SDR (TX_BITSLICE)                | 4          | HP            | 187.5                                                 | 800  | 187.5 | 800  | 187.5 | 630  | 187.5 | 700  | 187.5 | 630  | Mb/s  |
|                                          | 8          |               | 187.5                                                 | 800  | 187.5 | 800  | 187.5 | 630  | 187.5 | 800  | 187.5 | 630  | Mb/s  |
| LVDS RX DDR (RX_BITSLICE) <sup>(3)</sup> | 4          | HP            | 375                                                   | 1600 | 375   | 1600 | 375   | 1260 | 375   | 1400 | 375   | 1260 | Mb/s  |
|                                          | 8          |               | 375                                                   | 1600 | 375   | 1600 | 375   | 1260 | 375   | 1600 | 375   | 1260 | Mb/s  |
| LVDS RX SDR (RX_BITSLICE) <sup>(3)</sup> | 4          | HP            | 187.5                                                 | 800  | 187.5 | 800  | 187.5 | 630  | 187.5 | 700  | 187.5 | 630  | Mb/s  |
|                                          | 8          |               | 187.5                                                 | 800  | 187.5 | 800  | 187.5 | 630  | 187.5 | 800  | 187.5 | 630  | Mb/s  |

## Notes:

1. Native mode is supported through the [High-Speed SelectIO Interface Wizard](#) available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY\_MODE = VCO\_HALF the minimum frequency is PLL\_FVCOMIN/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 25: MIPI D-PHY Performance

| Description                         | I/O Bank Type | Speed Grade and V <sub>CCINT</sub> Operating Voltages |       |      |       |      | Units |
|-------------------------------------|---------------|-------------------------------------------------------|-------|------|-------|------|-------|
|                                     |               | 0.90V                                                 | 0.85V |      | 0.72V |      |       |
|                                     |               | -3                                                    | -2    | -1   | -2    | -1   |       |
| MIPI D-PHY transmitter or receiver. | HP            | 1500                                                  | 1500  | 1260 | 1260  | 1260 | Mb/s  |

Table 26: LVDS Native-Mode 1000BASE-X Support<sup>(1)</sup>

| Description | I/O Bank Type | Speed Grade and V <sub>CCINT</sub> Operating Voltages |       |    |       |    |
|-------------|---------------|-------------------------------------------------------|-------|----|-------|----|
|             |               | 0.90V                                                 | 0.85V |    | 0.72V |    |
|             |               | -3                                                    | -2    | -1 | -2    | -1 |
| 1000BASE-X  | HP            | Yes                                                   |       |    |       |    |

**Notes:**

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 27 provides the maximum data rates for applicable memory standards using the Kintex UltraScale+ FPGA memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* ([UG583](#)), electrical analysis, and characterization of the system.

Table 27: Maximum Physical Interface (PHY) Rate for Memory Interfaces

| Memory Standard | Package          | DRAM Type                        | Speed Grade and V <sub>CCINT</sub> Operating Voltages |       |      |       |      | Units |
|-----------------|------------------|----------------------------------|-------------------------------------------------------|-------|------|-------|------|-------|
|                 |                  |                                  | 0.90V                                                 | 0.85V |      | 0.72V |      |       |
|                 |                  |                                  | -3                                                    | -2    | -1   | -2    | -1   |       |
| DDR4            | All FFV packages | Single rank component            | 2666                                                  | 2666  | 2400 | 2400  | 2133 | Mb/s  |
|                 |                  | 1 rank DIMM <sup>(1)(2)(3)</sup> | 2400                                                  | 2400  | 2133 | 2133  | 1866 | Mb/s  |
|                 |                  | 2 rank DIMM <sup>(1)(4)</sup>    | 2133                                                  | 2133  | 1866 | 1866  | 1600 | Mb/s  |
|                 |                  | 4 rank DIMM <sup>(1)(5)</sup>    | 1600                                                  | 1600  | 1333 | 1333  | N/A  | Mb/s  |
|                 | SFVB784          | Single rank component            | 2400                                                  | 2400  | 2133 | 2133  | 1866 | Mb/s  |
|                 |                  | 1 rank DIMM <sup>(1)(2)</sup>    | 2133                                                  | 2133  | 1866 | 1866  | 1600 | Mb/s  |
|                 |                  | 2 rank DIMM <sup>(1)(4)</sup>    | 1866                                                  | 1866  | 1600 | 1600  | 1600 | Mb/s  |
| DDR3            | All FFV packages | Single rank component            | 2133                                                  | 2133  | 2133 | 2133  | 1866 | Mb/s  |
|                 |                  | 1 rank DIMM <sup>(1)(2)</sup>    | 1866                                                  | 1866  | 1866 | 1866  | 1600 | Mb/s  |
|                 |                  | 2 rank DIMM <sup>(1)(4)</sup>    | 1600                                                  | 1600  | 1600 | 1600  | 1333 | Mb/s  |
|                 |                  | 4 rank DIMM <sup>(1)(5)</sup>    | 1066                                                  | 1066  | 1066 | 1066  | 800  | Mb/s  |
|                 | SFVB784          | Single rank component            | 1866                                                  | 1866  | 1866 | 1866  | 1600 | Mb/s  |
|                 |                  | 1 rank DIMM <sup>(1)(2)</sup>    | 1600                                                  | 1600  | 1600 | 1600  | 1600 | Mb/s  |
|                 |                  | 2 rank DIMM <sup>(1)(4)</sup>    | 1600                                                  | 1600  | 1600 | 1600  | 1333 | Mb/s  |
|                 |                  | 4 rank DIMM <sup>(1)(5)</sup>    | 1066                                                  | 1066  | 1066 | 1066  | 800  | Mb/s  |

Table 27: Maximum Physical Interface (PHY) Rate for Memory Interfaces (Cont'd)

| Memory Standard | Package          | DRAM Type                            | Speed Grade and V <sub>CCINT</sub> Operating Voltages |       |      |       |      | Units |
|-----------------|------------------|--------------------------------------|-------------------------------------------------------|-------|------|-------|------|-------|
|                 |                  |                                      | 0.90V                                                 | 0.85V |      | 0.72V |      |       |
|                 |                  |                                      | -3                                                    | -2    | -1   | -2    | -1   |       |
| DDR3L           | All FFV packages | Single rank component                | 1866                                                  | 1866  | 1866 | 1866  | 1600 | Mb/s  |
|                 |                  | 1 rank DIMM <sup>(1)(2)</sup>        | 1600                                                  | 1600  | 1600 | 1600  | 1333 | Mb/s  |
|                 |                  | 2 rank DIMM <sup>(1)(4)</sup>        | 1333                                                  | 1333  | 1333 | 1333  | 1066 | Mb/s  |
|                 |                  | 4 rank DIMM <sup>(1)(5)</sup>        | 800                                                   | 800   | 800  | 800   | 606  | Mb/s  |
|                 | SFVB784          | Single rank component                | 1600                                                  | 1600  | 1600 | 1600  | 1600 | Mb/s  |
|                 |                  | 1 rank DIMM <sup>(1)(2)</sup>        | 1600                                                  | 1600  | 1600 | 1600  | 1333 | Mb/s  |
|                 |                  | 2 rank DIMM <sup>(1)(4)</sup>        | 1333                                                  | 1333  | 1333 | 1333  | 1066 | Mb/s  |
|                 |                  | 4 rank DIMM <sup>(1)(5)</sup>        | 800                                                   | 800   | 800  | 800   | 606  | Mb/s  |
| QDR II +        | All              | Single rank component <sup>(6)</sup> | 633                                                   | 633   | 600  | 600   | 550  | MHz   |
| RLDRAM 3        | All FFV packages | Single rank component                | 1200                                                  | 1200  | 1066 | 1066  | 933  | MHz   |
|                 | SFVB784          | Single rank component                | 1066                                                  | 1066  | 933  | 933   | 800  | MHz   |
| QDR IV XP       | All              | Single rank component                | 1066                                                  | 1066  | 1066 | 933   | 933  | MHz   |
| LPDDR3          | All              | Single rank component                | 1600                                                  | 1600  | 1600 | 1600  | 1600 | Mb/s  |

**Notes:**

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
2. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
3. For the DDR4 DDP components at -3 and -2 (V<sub>CCINT</sub> = 0.85V) speed grades, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 speed grades at 0.85V.
4. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
5. Includes: 2 rank 2 slot, 4 rank 1 slot.
6. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

# FPGA Logic Switching Characteristics

Table 28 (high-density IOB (HD)) and Table 29 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{\text{INBUF\_DELAY\_PAD\_I}}$  is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{\text{OUTBUF\_DELAY\_O\_PAD}}$  is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{\text{OUTBUF\_DELAY\_TD\_PAD}}$  is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than  $T_{\text{OUTBUF\_DELAY\_TD\_PAD}}$  when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than  $T_{\text{OUTBUF\_DELAY\_TD\_PAD}}$  when the INTERMDISABLE pin is used.

## IOB High Density (HD) Switching Characteristics

Table 28: IOB High Density (HD) Switching Characteristics

| I / O Standards   | $T_{\text{INBUF\_DELAY\_PAD\_I}}$ |       |       |       |       | $T_{\text{OUTBUF\_DELAY\_O\_PAD}}$ |       |       |       |       | $T_{\text{OUTBUF\_DELAY\_TD\_PAD}}$ |       |       |       |       | Units |
|-------------------|-----------------------------------|-------|-------|-------|-------|------------------------------------|-------|-------|-------|-------|-------------------------------------|-------|-------|-------|-------|-------|
|                   | 0.90V                             |       | 0.85V |       | 0.72V | 0.90V                              |       | 0.85V |       | 0.72V | 0.90V                               |       | 0.85V |       | 0.72V |       |
|                   | -3                                | -2    | -1    | -2    | -1    | -3                                 | -2    | -1    | -2    | -1    | -3                                  | -2    | -1    | -2    | -1    |       |
| DIFF_HSTL_I_18_F  | 0.723                             | 0.978 | 1.058 | 0.978 | 1.058 | 1.440                              | 1.574 | 1.718 | 1.966 | 2.101 | 1.160                               | 1.160 | 1.271 | 1.515 | 1.544 | ns    |
| DIFF_HSTL_I_18_S  | 0.723                             | 0.978 | 1.058 | 0.978 | 1.058 | 1.672                              | 1.805 | 1.950 | 2.197 | 2.333 | 1.748                               | 1.748 | 1.867 | 2.103 | 2.104 | ns    |
| DIFF_HSTL_I_F     | 0.723                             | 0.978 | 1.058 | 0.978 | 1.058 | 1.493                              | 1.611 | 1.762 | 2.003 | 2.145 | 1.313                               | 1.313 | 1.417 | 1.668 | 1.668 | ns    |
| DIFF_HSTL_I_S     | 0.723                             | 0.978 | 1.058 | 0.978 | 1.058 | 1.626                              | 1.798 | 1.913 | 2.190 | 2.296 | 1.630                               | 1.630 | 1.780 | 1.985 | 1.986 | ns    |
| DIFF_HSUL_12_F    | 0.646                             | 0.911 | 0.977 | 0.911 | 0.977 | 1.423                              | 1.573 | 1.703 | 1.965 | 2.086 | 1.222                               | 1.222 | 1.335 | 1.577 | 1.578 | ns    |
| DIFF_HSUL_12_S    | 0.646                             | 0.911 | 0.977 | 0.911 | 0.977 | 1.583                              | 1.711 | 1.864 | 2.103 | 2.247 | 1.536                               | 1.536 | 1.665 | 1.891 | 1.891 | ns    |
| DIFF_SSTL12_F     | 0.646                             | 0.906 | 0.977 | 0.906 | 0.977 | 1.507                              | 1.643 | 1.792 | 2.035 | 2.175 | 1.285                               | 1.285 | 1.423 | 1.640 | 1.640 | ns    |
| DIFF_SSTL12_S     | 0.646                             | 0.906 | 0.977 | 0.906 | 0.977 | 1.656                              | 1.784 | 1.948 | 2.176 | 2.331 | 1.567                               | 1.567 | 1.706 | 1.922 | 1.922 | ns    |
| DIFF_SSTL135_F    | 0.657                             | 0.927 | 0.995 | 0.927 | 0.995 | 1.488                              | 1.625 | 1.765 | 2.017 | 2.148 | 1.341                               | 1.341 | 1.458 | 1.696 | 1.696 | ns    |
| DIFF_SSTL135_II_F | 0.657                             | 0.927 | 0.995 | 0.927 | 0.995 | 1.490                              | 1.623 | 1.770 | 2.015 | 2.153 | 1.325                               | 1.325 | 1.470 | 1.680 | 1.689 | ns    |
| DIFF_SSTL135_II_S | 0.657                             | 0.927 | 0.995 | 0.927 | 0.995 | 1.624                              | 1.768 | 1.916 | 2.160 | 2.299 | 1.722                               | 1.722 | 1.911 | 2.077 | 2.078 | ns    |
| DIFF_SSTL135_S    | 0.657                             | 0.927 | 0.995 | 0.927 | 0.995 | 1.726                              | 1.869 | 2.025 | 2.261 | 2.408 | 1.814                               | 1.814 | 1.976 | 2.169 | 2.169 | ns    |
| DIFF_SSTL15_F     | 0.690                             | 0.928 | 1.020 | 0.928 | 1.020 | 1.489                              | 1.628 | 1.771 | 2.020 | 2.154 | 1.374                               | 1.374 | 1.483 | 1.729 | 1.729 | ns    |
| DIFF_SSTL15_II_F  | 0.690                             | 0.928 | 1.020 | 0.928 | 1.020 | 1.504                              | 1.622 | 1.778 | 2.014 | 2.161 | 1.356                               | 1.356 | 1.442 | 1.711 | 1.712 | ns    |
| DIFF_SSTL15_II_S  | 0.690                             | 0.928 | 1.020 | 0.928 | 1.020 | 1.699                              | 1.821 | 1.987 | 2.213 | 2.370 | 1.895                               | 1.895 | 2.047 | 2.250 | 2.250 | ns    |
| DIFF_SSTL15_S     | 0.690                             | 0.928 | 1.020 | 0.928 | 1.020 | 1.682                              | 1.824 | 1.977 | 2.216 | 2.360 | 1.743                               | 1.743 | 1.907 | 2.098 | 2.098 | ns    |
| DIFF_SSTL18_II_F  | 0.723                             | 0.961 | 1.038 | 0.961 | 1.038 | 1.602                              | 1.729 | 1.880 | 2.121 | 2.263 | 1.377                               | 1.377 | 1.492 | 1.732 | 1.732 | ns    |
| DIFF_SSTL18_II_S  | 0.723                             | 0.961 | 1.038 | 0.961 | 1.038 | 1.678                              | 1.796 | 1.965 | 2.188 | 2.348 | 1.616                               | 1.616 | 1.800 | 1.971 | 1.972 | ns    |
| DIFF_SSTL18_I_F   | 0.723                             | 0.961 | 1.038 | 0.961 | 1.038 | 1.469                              | 1.609 | 1.755 | 2.001 | 2.138 | 1.220                               | 1.220 | 1.313 | 1.575 | 1.575 | ns    |
| DIFF_SSTL18_I_S   | 0.723                             | 0.961 | 1.038 | 0.961 | 1.038 | 1.658                              | 1.786 | 1.942 | 2.178 | 2.325 | 1.677                               | 1.677 | 1.836 | 2.032 | 2.033 | ns    |
| HSTL_I_18_F       | 0.704                             | 0.947 | 1.021 | 0.947 | 1.021 | 1.440                              | 1.574 | 1.718 | 1.966 | 2.101 | 1.160                               | 1.160 | 1.271 | 1.515 | 1.544 | ns    |
| HSTL_I_18_S       | 0.704                             | 0.947 | 1.021 | 0.947 | 1.021 | 1.672                              | 1.805 | 1.950 | 2.197 | 2.333 | 1.748                               | 1.748 | 1.867 | 2.103 | 2.104 | ns    |

Table 28: IOB High Density (HD) Switching Characteristics (Cont'd)

| I/O Standards  | T <sub>INBUF_DELAY_PAD_I</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_O_PAD</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_TD_PAD</sub> |       |       |       |       | Units |
|----------------|--------------------------------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|----------------------------------|-------|-------|-------|-------|-------|
|                | 0.90V                          |       | 0.85V |       | 0.72V | 0.90V                           |       | 0.85V |       | 0.72V | 0.90V                            |       | 0.85V |       | 0.72V |       |
|                | -3                             | -2    | -1    | -2    | -1    | -3                              | -2    | -1    | -2    | -1    | -3                               | -2    | -1    | -2    | -1    |       |
| HSTL_I_F       | 0.598                          | 0.856 | 0.900 | 0.856 | 0.900 | 1.493                           | 1.611 | 1.762 | 2.003 | 2.145 | 1.313                            | 1.313 | 1.417 | 1.668 | 1.668 | ns    |
| HSTL_I_S       | 0.598                          | 0.856 | 0.900 | 0.856 | 0.900 | 1.626                           | 1.798 | 1.913 | 2.190 | 2.296 | 1.630                            | 1.630 | 1.780 | 1.985 | 1.986 | ns    |
| HSUL_12_F      | 0.562                          | 0.780 | 0.867 | 0.780 | 0.867 | 1.423                           | 1.573 | 1.703 | 1.965 | 2.086 | 1.222                            | 1.222 | 1.335 | 1.577 | 1.578 | ns    |
| HSUL_12_S      | 0.562                          | 0.780 | 0.867 | 0.780 | 0.867 | 1.583                           | 1.711 | 1.864 | 2.103 | 2.247 | 1.536                            | 1.536 | 1.665 | 1.891 | 1.891 | ns    |
| LVC MOS12_F_12 | 0.611                          | 0.918 | 0.976 | 0.918 | 0.976 | 1.582                           | 1.689 | 1.856 | 2.081 | 2.239 | 1.202                            | 1.202 | 1.317 | 1.557 | 1.557 | ns    |
| LVC MOS12_F_4  | 0.611                          | 0.918 | 0.976 | 0.918 | 0.976 | 1.644                           | 1.742 | 1.922 | 2.134 | 2.305 | 1.353                            | 1.353 | 1.478 | 1.708 | 1.708 | ns    |
| LVC MOS12_F_8  | 0.611                          | 0.918 | 0.976 | 0.918 | 0.976 | 1.598                           | 1.714 | 1.879 | 2.106 | 2.262 | 1.292                            | 1.292 | 1.432 | 1.647 | 1.647 | ns    |
| LVC MOS12_S_12 | 0.611                          | 0.918 | 0.976 | 0.918 | 0.976 | 1.949                           | 2.073 | 2.247 | 2.465 | 2.630 | 1.581                            | 1.581 | 1.717 | 1.936 | 1.937 | ns    |
| LVC MOS12_S_4  | 0.611                          | 0.918 | 0.976 | 0.918 | 0.976 | 1.916                           | 1.979 | 2.182 | 2.371 | 2.565 | 1.633                            | 1.633 | 1.772 | 1.988 | 1.989 | ns    |
| LVC MOS12_S_8  | 0.611                          | 0.918 | 0.976 | 0.918 | 0.976 | 2.062                           | 2.205 | 2.406 | 2.597 | 2.789 | 1.767                            | 1.767 | 1.928 | 2.122 | 2.123 | ns    |
| LVC MOS15_F_12 | 0.625                          | 0.905 | 0.958 | 0.905 | 0.958 | 1.621                           | 1.713 | 1.892 | 2.105 | 2.275 | 1.275                            | 1.275 | 1.428 | 1.630 | 1.630 | ns    |
| LVC MOS15_F_16 | 0.625                          | 0.905 | 0.958 | 0.905 | 0.958 | 1.595                           | 1.722 | 1.881 | 2.114 | 2.264 | 1.260                            | 1.260 | 1.407 | 1.615 | 1.615 | ns    |
| LVC MOS15_F_4  | 0.625                          | 0.905 | 0.958 | 0.905 | 0.958 | 1.677                           | 1.825 | 1.959 | 2.217 | 2.342 | 1.453                            | 1.453 | 1.557 | 1.808 | 1.809 | ns    |
| LVC MOS15_F_8  | 0.625                          | 0.905 | 0.958 | 0.905 | 0.958 | 1.651                           | 1.778 | 1.930 | 2.170 | 2.313 | 1.378                            | 1.378 | 1.458 | 1.733 | 1.733 | ns    |
| LVC MOS15_S_12 | 0.625                          | 0.905 | 0.958 | 0.905 | 0.958 | 1.866                           | 1.991 | 2.139 | 2.383 | 2.522 | 1.516                            | 1.516 | 1.648 | 1.871 | 1.871 | ns    |
| LVC MOS15_S_16 | 0.625                          | 0.905 | 0.958 | 0.905 | 0.958 | 2.102                           | 2.172 | 2.389 | 2.564 | 2.772 | 1.707                            | 1.707 | 1.888 | 2.062 | 2.062 | ns    |
| LVC MOS15_S_4  | 0.625                          | 0.905 | 0.958 | 0.905 | 0.958 | 2.204                           | 2.313 | 2.483 | 2.705 | 2.866 | 1.952                            | 1.952 | 2.123 | 2.307 | 2.307 | ns    |
| LVC MOS15_S_8  | 0.625                          | 0.905 | 0.958 | 0.905 | 0.958 | 2.102                           | 2.170 | 2.400 | 2.562 | 2.783 | 1.817                            | 1.817 | 1.984 | 2.172 | 2.173 | ns    |
| LVC MOS18_F_12 | 0.660                          | 0.915 | 0.958 | 0.915 | 0.958 | 1.671                           | 1.805 | 1.962 | 2.197 | 2.345 | 1.383                            | 1.383 | 1.471 | 1.738 | 1.738 | ns    |
| LVC MOS18_F_16 | 0.660                          | 0.915 | 0.958 | 0.915 | 0.958 | 1.628                           | 1.785 | 1.917 | 2.177 | 2.300 | 1.338                            | 1.338 | 1.446 | 1.693 | 1.693 | ns    |
| LVC MOS18_F_4  | 0.660                          | 0.915 | 0.958 | 0.915 | 0.958 | 1.745                           | 1.868 | 2.013 | 2.260 | 2.396 | 1.472                            | 1.472 | 1.599 | 1.827 | 1.832 | ns    |
| LVC MOS18_F_8  | 0.660                          | 0.915 | 0.958 | 0.915 | 0.958 | 1.715                           | 1.797 | 1.979 | 2.189 | 2.362 | 1.384                            | 1.384 | 1.487 | 1.739 | 1.739 | ns    |
| LVC MOS18_S_12 | 0.660                          | 0.915 | 0.958 | 0.915 | 0.958 | 2.093                           | 2.201 | 2.408 | 2.593 | 2.791 | 1.762                            | 1.762 | 1.894 | 2.117 | 2.118 | ns    |
| LVC MOS18_S_16 | 0.660                          | 0.915 | 0.958 | 0.915 | 0.958 | 2.032                           | 2.173 | 2.362 | 2.565 | 2.745 | 1.702                            | 1.702 | 1.834 | 2.057 | 2.057 | ns    |
| LVC MOS18_S_4  | 0.660                          | 0.915 | 0.958 | 0.915 | 0.958 | 2.272                           | 2.346 | 2.567 | 2.738 | 2.950 | 1.951                            | 1.951 | 2.092 | 2.306 | 2.306 | ns    |
| LVC MOS18_S_8  | 0.660                          | 0.915 | 0.958 | 0.915 | 0.958 | 2.205                           | 2.292 | 2.511 | 2.684 | 2.894 | 1.848                            | 1.848 | 2.008 | 2.203 | 2.204 | ns    |
| LVC MOS25_F_12 | 0.754                          | 0.988 | 1.042 | 0.988 | 1.042 | 2.153                           | 2.153 | 2.453 | 2.545 | 2.836 | 1.692                            | 1.692 | 1.856 | 2.047 | 2.047 | ns    |
| LVC MOS25_F_16 | 0.754                          | 0.988 | 1.042 | 0.988 | 1.042 | 2.105                           | 2.105 | 2.406 | 2.497 | 2.789 | 1.623                            | 1.623 | 1.786 | 1.978 | 1.979 | ns    |
| LVC MOS25_F_4  | 0.754                          | 0.988 | 1.042 | 0.988 | 1.042 | 2.247                           | 2.344 | 2.554 | 2.736 | 2.937 | 1.842                            | 1.842 | 2.039 | 2.197 | 2.197 | ns    |
| LVC MOS25_F_8  | 0.754                          | 0.988 | 1.042 | 0.988 | 1.042 | 2.184                           | 2.184 | 2.516 | 2.576 | 2.899 | 1.726                            | 1.726 | 1.910 | 2.081 | 2.081 | ns    |
| LVC MOS25_S_12 | 0.754                          | 0.988 | 1.042 | 0.988 | 1.042 | 2.480                           | 2.558 | 2.840 | 2.950 | 3.223 | 1.971                            | 1.971 | 2.194 | 2.326 | 2.327 | ns    |
| LVC MOS25_S_16 | 0.754                          | 0.988 | 1.042 | 0.988 | 1.042 | 2.449                           | 2.449 | 2.740 | 2.841 | 3.123 | 1.852                            | 1.852 | 2.063 | 2.207 | 2.207 | ns    |
| LVC MOS25_S_4  | 0.754                          | 0.988 | 1.042 | 0.988 | 1.042 | 2.754                           | 2.770 | 3.066 | 3.162 | 3.449 | 2.224                            | 2.224 | 2.458 | 2.579 | 2.579 | ns    |
| LVC MOS25_S_8  | 0.754                          | 0.988 | 1.042 | 0.988 | 1.042 | 2.639                           | 2.663 | 2.963 | 3.055 | 3.346 | 2.091                            | 2.091 | 2.373 | 2.446 | 2.446 | ns    |
| LVC MOS33_F_12 | 0.926                          | 1.154 | 1.213 | 1.154 | 1.213 | 2.388                           | 2.415 | 2.651 | 2.807 | 3.034 | 1.754                            | 1.754 | 1.915 | 2.109 | 2.109 | ns    |
| LVC MOS33_F_16 | 0.926                          | 1.154 | 1.213 | 1.154 | 1.213 | 2.311                           | 2.383 | 2.603 | 2.775 | 2.986 | 1.734                            | 1.734 | 1.869 | 2.089 | 2.089 | ns    |
| LVC MOS33_F_4  | 0.926                          | 1.154 | 1.213 | 1.154 | 1.213 | 2.483                           | 2.541 | 2.765 | 2.933 | 3.148 | 1.932                            | 1.932 | 2.135 | 2.287 | 2.287 | ns    |
| LVC MOS33_F_8  | 0.926                          | 1.154 | 1.213 | 1.154 | 1.213 | 2.542                           | 2.603 | 2.822 | 2.995 | 3.205 | 1.937                            | 1.937 | 2.130 | 2.292 | 2.294 | ns    |
| LVC MOS33_S_12 | 0.926                          | 1.154 | 1.213 | 1.154 | 1.213 | 2.705                           | 2.705 | 3.047 | 3.097 | 3.430 | 2.049                            | 2.049 | 2.318 | 2.404 | 2.404 | ns    |
| LVC MOS33_S_16 | 0.926                          | 1.154 | 1.213 | 1.154 | 1.213 | 2.714                           | 2.714 | 3.024 | 3.106 | 3.407 | 2.028                            | 2.028 | 2.232 | 2.383 | 2.383 | ns    |
| LVC MOS33_S_4  | 0.926                          | 1.154 | 1.213 | 1.154 | 1.213 | 2.974                           | 2.999 | 3.340 | 3.391 | 3.723 | 2.320                            | 2.320 | 2.610 | 2.675 | 2.675 | ns    |

Table 28: IOB High Density (HD) Switching Characteristics (Cont'd)

| I/O Standards | T <sub>INBUF_DELAY_PAD_I</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_O_PAD</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_TD_PAD</sub> |       |       |       |       | Units |
|---------------|--------------------------------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|----------------------------------|-------|-------|-------|-------|-------|
|               | 0.90V                          | 0.85V | 0.72V |       |       | 0.90V                           | 0.85V | 0.72V |       |       | 0.90V                            | 0.85V | 0.72V |       |       |       |
|               | -3                             | -2    | -1    | -2    | -1    | -3                              | -2    | -1    | -2    | -1    | -3                               | -2    | -1    | -2    | -1    |       |
| LVC MOS33_S_8 | 0.926                          | 1.154 | 1.213 | 1.154 | 1.213 | 2.894                           | 2.929 | 3.260 | 3.321 | 3.643 | 2.260                            | 2.260 | 2.532 | 2.615 | 2.616 | ns    |
| LVDS_25       | 0.830                          | 1.003 | 1.116 | 1.003 | 1.116 | N/A                             | N/A   | N/A   | N/A   | N/A   | N/A                              | N/A   | N/A   | N/A   | N/A   | ns    |
| LVPECL        | 0.830                          | 1.003 | 1.116 | 1.003 | 1.116 | N/A                             | N/A   | N/A   | N/A   | N/A   | N/A                              | N/A   | N/A   | N/A   | N/A   | ns    |
| LVTTL_F_12    | 0.944                          | 1.164 | 1.223 | 1.164 | 1.223 | 2.388                           | 2.415 | 2.651 | 2.807 | 3.034 | 1.754                            | 1.754 | 1.915 | 2.109 | 2.109 | ns    |
| LVTTL_F_16    | 0.944                          | 1.164 | 1.223 | 1.164 | 1.223 | 2.433                           | 2.464 | 2.732 | 2.856 | 3.115 | 1.750                            | 1.750 | 1.986 | 2.105 | 2.117 | ns    |
| LVTTL_F_4     | 0.944                          | 1.164 | 1.223 | 1.164 | 1.223 | 2.483                           | 2.541 | 2.765 | 2.933 | 3.148 | 1.932                            | 1.932 | 2.135 | 2.287 | 2.287 | ns    |
| LVTTL_F_8     | 0.944                          | 1.164 | 1.223 | 1.164 | 1.223 | 2.512                           | 2.582 | 2.787 | 2.974 | 3.170 | 1.910                            | 1.910 | 2.063 | 2.265 | 2.265 | ns    |
| LVTTL_S_12    | 0.944                          | 1.164 | 1.223 | 1.164 | 1.223 | 2.731                           | 2.731 | 3.075 | 3.123 | 3.458 | 2.072                            | 2.072 | 2.343 | 2.427 | 2.427 | ns    |
| LVTTL_S_16    | 0.944                          | 1.164 | 1.223 | 1.164 | 1.223 | 2.714                           | 2.714 | 3.024 | 3.106 | 3.407 | 2.028                            | 2.028 | 2.232 | 2.383 | 2.383 | ns    |
| LVTTL_S_4     | 0.944                          | 1.164 | 1.223 | 1.164 | 1.223 | 2.974                           | 2.999 | 3.340 | 3.391 | 3.723 | 2.320                            | 2.320 | 2.610 | 2.675 | 2.675 | ns    |
| LVTTL_S_8     | 0.944                          | 1.164 | 1.223 | 1.164 | 1.223 | 2.894                           | 2.929 | 3.260 | 3.321 | 3.643 | 2.260                            | 2.260 | 2.532 | 2.615 | 2.616 | ns    |
| SLVS_400_25   | 0.848                          | 1.020 | 1.136 | 1.020 | 1.136 | N/A                             | N/A   | N/A   | N/A   | N/A   | N/A                              | N/A   | N/A   | N/A   | N/A   | ns    |
| SSTL12_F      | 0.562                          | 0.780 | 0.867 | 0.780 | 0.867 | 1.507                           | 1.643 | 1.792 | 2.035 | 2.175 | 1.285                            | 1.285 | 1.423 | 1.640 | 1.640 | ns    |
| SSTL12_S      | 0.562                          | 0.780 | 0.867 | 0.780 | 0.867 | 1.656                           | 1.784 | 1.948 | 2.176 | 2.331 | 1.567                            | 1.567 | 1.706 | 1.922 | 1.922 | ns    |
| SSTL135_F     | 0.581                          | 0.798 | 0.881 | 0.798 | 0.881 | 1.488                           | 1.625 | 1.765 | 2.017 | 2.148 | 1.341                            | 1.341 | 1.458 | 1.696 | 1.696 | ns    |
| SSTL135_II_F  | 0.581                          | 0.798 | 0.881 | 0.798 | 0.881 | 1.504                           | 1.623 | 1.770 | 2.015 | 2.153 | 1.325                            | 1.325 | 1.470 | 1.680 | 1.689 | ns    |
| SSTL135_II_S  | 0.581                          | 0.798 | 0.881 | 0.798 | 0.881 | 1.624                           | 1.768 | 1.916 | 2.160 | 2.299 | 1.722                            | 1.722 | 1.911 | 2.077 | 2.078 | ns    |
| SSTL135_S     | 0.581                          | 0.798 | 0.881 | 0.798 | 0.881 | 1.726                           | 1.869 | 2.025 | 2.261 | 2.408 | 1.814                            | 1.814 | 1.976 | 2.169 | 2.169 | ns    |
| SSTL15_F      | 0.581                          | 0.838 | 0.880 | 0.838 | 0.880 | 1.474                           | 1.612 | 1.754 | 2.004 | 2.137 | 1.357                            | 1.357 | 1.464 | 1.712 | 1.713 | ns    |
| SSTL15_II_F   | 0.581                          | 0.838 | 0.880 | 0.838 | 0.880 | 1.518                           | 1.622 | 1.778 | 2.014 | 2.161 | 1.356                            | 1.356 | 1.442 | 1.711 | 1.712 | ns    |
| SSTL15_II_S   | 0.581                          | 0.838 | 0.880 | 0.838 | 0.880 | 1.699                           | 1.821 | 1.987 | 2.213 | 2.370 | 1.895                            | 1.895 | 2.047 | 2.250 | 2.250 | ns    |
| SSTL15_S      | 0.581                          | 0.838 | 0.880 | 0.838 | 0.880 | 1.682                           | 1.824 | 1.977 | 2.216 | 2.360 | 1.743                            | 1.743 | 1.907 | 2.098 | 2.098 | ns    |
| SSTL18_II_F   | 0.704                          | 0.947 | 1.021 | 0.947 | 1.021 | 1.629                           | 1.729 | 1.880 | 2.121 | 2.263 | 1.377                            | 1.377 | 1.492 | 1.732 | 1.732 | ns    |
| SSTL18_II_S   | 0.704                          | 0.947 | 1.021 | 0.947 | 1.021 | 1.678                           | 1.796 | 1.965 | 2.188 | 2.348 | 1.616                            | 1.616 | 1.800 | 1.971 | 1.972 | ns    |
| SSTL18_I_F    | 0.704                          | 0.947 | 1.021 | 0.947 | 1.021 | 1.496                           | 1.609 | 1.755 | 2.001 | 2.138 | 1.220                            | 1.220 | 1.313 | 1.575 | 1.575 | ns    |
| SSTL18_I_S    | 0.704                          | 0.947 | 1.021 | 0.947 | 1.021 | 1.675                           | 1.786 | 1.942 | 2.178 | 2.325 | 1.677                            | 1.677 | 1.836 | 2.032 | 2.033 | ns    |
| SUB_LVDS      | 0.721                          | 1.002 | 1.036 | 1.002 | 1.036 | N/A                             | N/A   | N/A   | N/A   | N/A   | N/A                              | N/A   | N/A   | N/A   | N/A   | ns    |

# IOB High Performance (HP) Switching Characteristics

Table 29: IOB High Performance (HP) Switching Characteristics

| I/O Standards        | T <sub>INBUF_DELAY_PAD_I</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_O_PAD</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_TD_PAD</sub> |       |       |       |       | Units |
|----------------------|--------------------------------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|----------------------------------|-------|-------|-------|-------|-------|
|                      | 0.90V                          |       | 0.85V |       | 0.72V | 0.90V                           |       | 0.85V |       | 0.72V | 0.90V                            |       | 0.85V |       | 0.72V |       |
|                      | -3                             | -2    | -1    | -2    | -1    | -3                              | -2    | -1    | -2    | -1    | -3                               | -2    | -1    | -2    | -1    |       |
| DIFF_HSTL_I_12_F     | 0.288                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.410                           | 0.423 | 0.443 | 0.423 | 0.443 | 0.514                            | 0.553 | 0.582 | 0.553 | 0.582 | ns    |
| DIFF_HSTL_I_12_M     | 0.288                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.552                           | 0.552 | 0.583 | 0.552 | 0.583 | 0.632                            | 0.641 | 0.679 | 0.641 | 0.679 | ns    |
| DIFF_HSTL_I_12_S     | 0.288                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.752                           | 0.752 | 0.800 | 0.752 | 0.800 | 0.813                            | 0.813 | 0.868 | 0.813 | 0.868 | ns    |
| DIFF_HSTL_I_18_F     | 0.259                          | 0.319 | 0.339 | 0.319 | 0.339 | 0.439                           | 0.456 | 0.474 | 0.456 | 0.474 | 0.549                            | 0.576 | 0.606 | 0.576 | 0.606 | ns    |
| DIFF_HSTL_I_18_M     | 0.259                          | 0.319 | 0.339 | 0.319 | 0.339 | 0.563                           | 0.570 | 0.603 | 0.570 | 0.603 | 0.636                            | 0.653 | 0.692 | 0.653 | 0.692 | ns    |
| DIFF_HSTL_I_18_S     | 0.259                          | 0.319 | 0.339 | 0.319 | 0.339 | 0.782                           | 0.782 | 0.834 | 0.782 | 0.834 | 0.816                            | 0.816 | 0.871 | 0.816 | 0.871 | ns    |
| DIFF_HSTL_I_DCI_12_F | 0.288                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.393                           | 0.406 | 0.429 | 0.406 | 0.429 | 0.502                            | 0.534 | 0.564 | 0.534 | 0.564 | ns    |
| DIFF_HSTL_I_DCI_12_M | 0.288                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.546                           | 0.557 | 0.587 | 0.557 | 0.587 | 0.636                            | 0.653 | 0.694 | 0.653 | 0.694 | ns    |
| DIFF_HSTL_I_DCI_12_S | 0.288                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.755                           | 0.755 | 0.806 | 0.755 | 0.806 | 0.842                            | 0.842 | 0.907 | 0.842 | 0.907 | ns    |
| DIFF_HSTL_I_DCI_18_F | 0.259                          | 0.323 | 0.339 | 0.323 | 0.339 | 0.422                           | 0.445 | 0.461 | 0.445 | 0.461 | 0.509                            | 0.566 | 0.595 | 0.566 | 0.595 | ns    |
| DIFF_HSTL_I_DCI_18_M | 0.259                          | 0.323 | 0.339 | 0.323 | 0.339 | 0.546                           | 0.555 | 0.586 | 0.555 | 0.586 | 0.626                            | 0.643 | 0.684 | 0.643 | 0.684 | ns    |
| DIFF_HSTL_I_DCI_18_S | 0.259                          | 0.323 | 0.339 | 0.323 | 0.339 | 0.762                           | 0.762 | 0.818 | 0.762 | 0.818 | 0.836                            | 0.836 | 0.900 | 0.836 | 0.900 | ns    |
| DIFF_HSTL_I_DCI_F    | 0.335                          | 0.397 | 0.417 | 0.397 | 0.417 | 0.407                           | 0.431 | 0.445 | 0.431 | 0.445 | 0.517                            | 0.555 | 0.575 | 0.555 | 0.575 | ns    |
| DIFF_HSTL_I_DCI_M    | 0.335                          | 0.397 | 0.417 | 0.397 | 0.417 | 0.549                           | 0.553 | 0.583 | 0.553 | 0.583 | 0.634                            | 0.644 | 0.684 | 0.644 | 0.684 | ns    |
| DIFF_HSTL_I_DCI_S    | 0.335                          | 0.397 | 0.417 | 0.397 | 0.417 | 0.767                           | 0.767 | 0.823 | 0.767 | 0.823 | 0.848                            | 0.848 | 0.912 | 0.848 | 0.912 | ns    |
| DIFF_HSTL_I_F        | 0.304                          | 0.404 | 0.417 | 0.404 | 0.417 | 0.409                           | 0.423 | 0.443 | 0.423 | 0.443 | 0.514                            | 0.549 | 0.581 | 0.549 | 0.581 | ns    |
| DIFF_HSTL_I_M        | 0.304                          | 0.404 | 0.417 | 0.404 | 0.417 | 0.549                           | 0.555 | 0.586 | 0.555 | 0.586 | 0.624                            | 0.640 | 0.677 | 0.640 | 0.677 | ns    |
| DIFF_HSTL_I_S        | 0.304                          | 0.404 | 0.417 | 0.404 | 0.417 | 0.767                           | 0.767 | 0.818 | 0.767 | 0.818 | 0.811                            | 0.811 | 0.866 | 0.811 | 0.866 | ns    |
| DIFF_HSUL_12_DCI_F   | 0.320                          | 0.381 | 0.400 | 0.381 | 0.400 | 0.411                           | 0.425 | 0.443 | 0.425 | 0.443 | 0.520                            | 0.558 | 0.586 | 0.558 | 0.586 | ns    |
| DIFF_HSUL_12_DCI_M   | 0.320                          | 0.381 | 0.400 | 0.381 | 0.400 | 0.546                           | 0.557 | 0.587 | 0.557 | 0.587 | 0.636                            | 0.653 | 0.694 | 0.653 | 0.694 | ns    |
| DIFF_HSUL_12_DCI_S   | 0.320                          | 0.381 | 0.400 | 0.381 | 0.400 | 0.737                           | 0.737 | 0.787 | 0.737 | 0.787 | 0.822                            | 0.822 | 0.885 | 0.822 | 0.885 | ns    |
| DIFF_HSUL_12_F       | 0.322                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.394                           | 0.412 | 0.430 | 0.412 | 0.430 | 0.494                            | 0.538 | 0.566 | 0.538 | 0.566 | ns    |
| DIFF_HSUL_12_M       | 0.322                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.552                           | 0.552 | 0.583 | 0.552 | 0.583 | 0.632                            | 0.641 | 0.679 | 0.641 | 0.679 | ns    |
| DIFF_HSUL_12_S       | 0.322                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.752                           | 0.752 | 0.800 | 0.752 | 0.800 | 0.813                            | 0.813 | 0.868 | 0.813 | 0.868 | ns    |
| DIFF_POD10_DCI_F     | 0.289                          | 0.411 | 0.430 | 0.411 | 0.430 | 0.407                           | 0.425 | 0.444 | 0.425 | 0.444 | 0.512                            | 0.555 | 0.584 | 0.555 | 0.584 | ns    |
| DIFF_POD10_DCI_M     | 0.289                          | 0.411 | 0.430 | 0.411 | 0.430 | 0.533                           | 0.542 | 0.571 | 0.542 | 0.571 | 0.618                            | 0.640 | 0.681 | 0.640 | 0.681 | ns    |
| DIFF_POD10_DCI_S     | 0.289                          | 0.411 | 0.430 | 0.411 | 0.430 | 0.754                           | 0.754 | 0.815 | 0.754 | 0.815 | 0.850                            | 0.850 | 0.917 | 0.850 | 0.917 | ns    |
| DIFF_POD10_F         | 0.288                          | 0.411 | 0.433 | 0.411 | 0.433 | 0.425                           | 0.438 | 0.459 | 0.438 | 0.459 | 0.531                            | 0.569 | 0.601 | 0.569 | 0.601 | ns    |
| DIFF_POD10_M         | 0.288                          | 0.411 | 0.433 | 0.411 | 0.433 | 0.519                           | 0.538 | 0.568 | 0.538 | 0.568 | 0.589                            | 0.630 | 0.667 | 0.630 | 0.667 | ns    |
| DIFF_POD10_S         | 0.288                          | 0.411 | 0.433 | 0.411 | 0.433 | 0.752                           | 0.766 | 0.821 | 0.766 | 0.821 | 0.821                            | 0.836 | 0.894 | 0.836 | 0.894 | ns    |
| DIFF_POD12_DCI_F     | 0.320                          | 0.407 | 0.432 | 0.407 | 0.432 | 0.411                           | 0.425 | 0.443 | 0.425 | 0.443 | 0.519                            | 0.558 | 0.586 | 0.558 | 0.586 | ns    |
| DIFF_POD12_DCI_M     | 0.320                          | 0.407 | 0.432 | 0.407 | 0.432 | 0.516                           | 0.543 | 0.572 | 0.543 | 0.572 | 0.602                            | 0.638 | 0.678 | 0.638 | 0.678 | ns    |
| DIFF_POD12_DCI_S     | 0.320                          | 0.407 | 0.432 | 0.407 | 0.432 | 0.740                           | 0.772 | 0.822 | 0.772 | 0.822 | 0.833                            | 0.862 | 0.929 | 0.862 | 0.929 | ns    |
| DIFF_POD12_F         | 0.305                          | 0.409 | 0.430 | 0.409 | 0.430 | 0.438                           | 0.455 | 0.476 | 0.455 | 0.476 | 0.549                            | 0.595 | 0.626 | 0.595 | 0.626 | ns    |
| DIFF_POD12_M         | 0.305                          | 0.409 | 0.430 | 0.409 | 0.430 | 0.551                           | 0.551 | 0.582 | 0.551 | 0.582 | 0.632                            | 0.641 | 0.679 | 0.641 | 0.679 | ns    |
| DIFF_POD12_S         | 0.305                          | 0.409 | 0.430 | 0.409 | 0.430 | 0.749                           | 0.767 | 0.817 | 0.767 | 0.817 | 0.818                            | 0.832 | 0.889 | 0.832 | 0.889 | ns    |
| DIFF_SSTL12_DCI_F    | 0.303                          | 0.381 | 0.400 | 0.381 | 0.400 | 0.411                           | 0.425 | 0.443 | 0.425 | 0.443 | 0.520                            | 0.558 | 0.586 | 0.558 | 0.586 | ns    |
| DIFF_SSTL12_DCI_M    | 0.303                          | 0.381 | 0.400 | 0.381 | 0.400 | 0.549                           | 0.557 | 0.587 | 0.557 | 0.587 | 0.643                            | 0.654 | 0.694 | 0.654 | 0.694 | ns    |
| DIFF_SSTL12_DCI_S    | 0.303                          | 0.381 | 0.400 | 0.381 | 0.400 | 0.754                           | 0.754 | 0.803 | 0.754 | 0.803 | 0.842                            | 0.842 | 0.908 | 0.842 | 0.908 | ns    |

Table 29: IOB High Performance (HP) Switching Characteristics (Cont'd)

| I/O Standards       | T <sub>INBUF_DELAY_PAD_I</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_O_PAD</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_TD_PAD</sub> |       |       |       |       | Units |
|---------------------|--------------------------------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|----------------------------------|-------|-------|-------|-------|-------|
|                     | 0.90V                          | 0.85V | 0.72V |       |       | 0.90V                           | 0.85V | 0.72V |       |       | 0.90V                            | 0.85V | 0.72V |       |       |       |
|                     | -3                             | -2    | -1    | -2    | -1    | -3                              | -2    | -1    | -2    | -1    | -3                               | -2    | -1    | -2    | -1    |       |
| DIFF_SSTL12_F       | 0.288                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.394                           | 0.412 | 0.430 | 0.412 | 0.430 | 0.494                            | 0.538 | 0.566 | 0.538 | 0.566 | ns    |
| DIFF_SSTL12_M       | 0.288                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.550                           | 0.553 | 0.584 | 0.553 | 0.584 | 0.630                            | 0.641 | 0.676 | 0.641 | 0.676 | ns    |
| DIFF_SSTL12_S       | 0.288                          | 0.394 | 0.402 | 0.394 | 0.402 | 0.758                           | 0.758 | 0.808 | 0.758 | 0.808 | 0.823                            | 0.823 | 0.879 | 0.823 | 0.879 | ns    |
| DIFF_SSTL135_DCI_F  | 0.303                          | 0.371 | 0.402 | 0.371 | 0.402 | 0.392                           | 0.411 | 0.428 | 0.411 | 0.428 | 0.494                            | 0.537 | 0.565 | 0.537 | 0.565 | ns    |
| DIFF_SSTL135_DCI_M  | 0.303                          | 0.371 | 0.402 | 0.371 | 0.402 | 0.551                           | 0.551 | 0.582 | 0.551 | 0.582 | 0.643                            | 0.645 | 0.685 | 0.645 | 0.685 | ns    |
| DIFF_SSTL135_DCI_S  | 0.303                          | 0.371 | 0.402 | 0.371 | 0.402 | 0.746                           | 0.746 | 0.799 | 0.746 | 0.799 | 0.829                            | 0.829 | 0.893 | 0.829 | 0.893 | ns    |
| DIFF_SSTL135_F      | 0.289                          | 0.375 | 0.402 | 0.375 | 0.402 | 0.393                           | 0.408 | 0.428 | 0.408 | 0.428 | 0.491                            | 0.528 | 0.561 | 0.528 | 0.561 | ns    |
| DIFF_SSTL135_M      | 0.289                          | 0.375 | 0.402 | 0.375 | 0.402 | 0.548                           | 0.555 | 0.585 | 0.555 | 0.585 | 0.621                            | 0.641 | 0.679 | 0.641 | 0.679 | ns    |
| DIFF_SSTL135_S      | 0.289                          | 0.375 | 0.402 | 0.375 | 0.402 | 0.746                           | 0.746 | 0.823 | 0.772 | 0.823 | 0.827                            | 0.827 | 0.878 | 0.827 | 0.878 | ns    |
| DIFF_SSTL15_DCI_F   | 0.335                          | 0.397 | 0.417 | 0.397 | 0.417 | 0.394                           | 0.412 | 0.429 | 0.412 | 0.429 | 0.497                            | 0.531 | 0.563 | 0.531 | 0.563 | ns    |
| DIFF_SSTL15_DCI_M   | 0.335                          | 0.397 | 0.417 | 0.397 | 0.417 | 0.549                           | 0.553 | 0.583 | 0.553 | 0.583 | 0.632                            | 0.645 | 0.685 | 0.645 | 0.685 | ns    |
| DIFF_SSTL15_DCI_S   | 0.335                          | 0.397 | 0.417 | 0.397 | 0.417 | 0.746                           | 0.746 | 0.822 | 0.768 | 0.822 | 0.847                            | 0.847 | 0.912 | 0.847 | 0.912 | ns    |
| DIFF_SSTL15_F       | 0.304                          | 0.404 | 0.417 | 0.404 | 0.417 | 0.409                           | 0.424 | 0.445 | 0.424 | 0.445 | 0.513                            | 0.551 | 0.577 | 0.551 | 0.577 | ns    |
| DIFF_SSTL15_M       | 0.304                          | 0.404 | 0.417 | 0.404 | 0.417 | 0.547                           | 0.554 | 0.585 | 0.554 | 0.585 | 0.624                            | 0.639 | 0.677 | 0.639 | 0.677 | ns    |
| DIFF_SSTL15_S       | 0.304                          | 0.404 | 0.417 | 0.404 | 0.417 | 0.746                           | 0.746 | 0.817 | 0.767 | 0.817 | 0.813                            | 0.813 | 0.867 | 0.813 | 0.867 | ns    |
| DIFF_SSTL18_I_DCI_F | 0.256                          | 0.320 | 0.336 | 0.320 | 0.336 | 0.422                           | 0.445 | 0.461 | 0.445 | 0.461 | 0.540                            | 0.566 | 0.595 | 0.566 | 0.595 | ns    |
| DIFF_SSTL18_I_DCI_M | 0.256                          | 0.320 | 0.336 | 0.320 | 0.336 | 0.552                           | 0.554 | 0.585 | 0.554 | 0.585 | 0.629                            | 0.644 | 0.683 | 0.644 | 0.683 | ns    |
| DIFF_SSTL18_I_DCI_S | 0.256                          | 0.320 | 0.336 | 0.320 | 0.336 | 0.746                           | 0.746 | 0.818 | 0.762 | 0.818 | 0.837                            | 0.837 | 0.899 | 0.837 | 0.899 | ns    |
| DIFF_SSTL18_I_F     | 0.256                          | 0.316 | 0.336 | 0.316 | 0.336 | 0.439                           | 0.454 | 0.476 | 0.454 | 0.476 | 0.549                            | 0.578 | 0.608 | 0.578 | 0.608 | ns    |
| DIFF_SSTL18_I_M     | 0.256                          | 0.316 | 0.336 | 0.316 | 0.336 | 0.567                           | 0.571 | 0.603 | 0.571 | 0.603 | 0.535                            | 0.652 | 0.692 | 0.652 | 0.692 | ns    |
| DIFF_SSTL18_I_S     | 0.256                          | 0.316 | 0.336 | 0.316 | 0.336 | 0.746                           | 0.746 | 0.835 | 0.782 | 0.835 | 0.816                            | 0.816 | 0.870 | 0.816 | 0.870 | ns    |
| HSLVDCI_15_F        | 0.336                          | 0.393 | 0.415 | 0.393 | 0.415 | 0.407                           | 0.425 | 0.443 | 0.425 | 0.443 | 0.513                            | 0.548 | 0.579 | 0.548 | 0.579 | ns    |
| HSLVDCI_15_M        | 0.336                          | 0.393 | 0.415 | 0.393 | 0.415 | 0.548                           | 0.552 | 0.581 | 0.552 | 0.581 | 0.635                            | 0.644 | 0.684 | 0.644 | 0.684 | ns    |
| HSLVDCI_15_S        | 0.336                          | 0.393 | 0.415 | 0.393 | 0.415 | 0.748                           | 0.748 | 0.802 | 0.748 | 0.802 | 0.827                            | 0.827 | 0.890 | 0.827 | 0.890 | ns    |
| HSLVDCI_18_F        | 0.367                          | 0.424 | 0.447 | 0.424 | 0.447 | 0.424                           | 0.445 | 0.461 | 0.445 | 0.461 | 0.541                            | 0.566 | 0.595 | 0.566 | 0.595 | ns    |
| HSLVDCI_18_M        | 0.367                          | 0.424 | 0.447 | 0.424 | 0.447 | 0.563                           | 0.567 | 0.598 | 0.567 | 0.598 | 0.647                            | 0.658 | 0.699 | 0.658 | 0.699 | ns    |
| HSLVDCI_18_S        | 0.367                          | 0.424 | 0.447 | 0.424 | 0.447 | 0.761                           | 0.761 | 0.817 | 0.761 | 0.817 | 0.836                            | 0.836 | 0.900 | 0.836 | 0.900 | ns    |
| HSTL_I_12_F         | 0.322                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.410                           | 0.423 | 0.443 | 0.423 | 0.443 | 0.514                            | 0.553 | 0.582 | 0.553 | 0.582 | ns    |
| HSTL_I_12_M         | 0.322                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.551                           | 0.551 | 0.582 | 0.551 | 0.582 | 0.632                            | 0.642 | 0.679 | 0.642 | 0.679 | ns    |
| HSTL_I_12_S         | 0.322                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.750                           | 0.750 | 0.799 | 0.750 | 0.799 | 0.813                            | 0.813 | 0.868 | 0.813 | 0.868 | ns    |
| HSTL_I_18_F         | 0.258                          | 0.322 | 0.339 | 0.322 | 0.339 | 0.439                           | 0.456 | 0.474 | 0.456 | 0.474 | 0.549                            | 0.576 | 0.606 | 0.576 | 0.606 | ns    |
| HSTL_I_18_M         | 0.258                          | 0.322 | 0.339 | 0.322 | 0.339 | 0.562                           | 0.569 | 0.602 | 0.569 | 0.602 | 0.637                            | 0.653 | 0.692 | 0.653 | 0.692 | ns    |
| HSTL_I_18_S         | 0.258                          | 0.322 | 0.339 | 0.322 | 0.339 | 0.781                           | 0.781 | 0.833 | 0.781 | 0.833 | 0.816                            | 0.816 | 0.871 | 0.816 | 0.871 | ns    |
| HSTL_I_DCI_12_F     | 0.322                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.393                           | 0.406 | 0.429 | 0.406 | 0.429 | 0.502                            | 0.534 | 0.564 | 0.534 | 0.564 | ns    |
| HSTL_I_DCI_12_M     | 0.322                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.551                           | 0.556 | 0.586 | 0.556 | 0.586 | 0.644                            | 0.654 | 0.694 | 0.654 | 0.694 | ns    |
| HSTL_I_DCI_12_S     | 0.322                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.754                           | 0.754 | 0.803 | 0.754 | 0.803 | 0.842                            | 0.842 | 0.907 | 0.842 | 0.907 | ns    |
| HSTL_I_DCI_18_F     | 0.258                          | 0.321 | 0.339 | 0.321 | 0.339 | 0.422                           | 0.445 | 0.461 | 0.445 | 0.461 | 0.509                            | 0.566 | 0.595 | 0.566 | 0.595 | ns    |
| HSTL_I_DCI_18_M     | 0.258                          | 0.321 | 0.339 | 0.321 | 0.339 | 0.551                           | 0.554 | 0.585 | 0.554 | 0.585 | 0.634                            | 0.643 | 0.684 | 0.643 | 0.684 | ns    |
| HSTL_I_DCI_18_S     | 0.258                          | 0.321 | 0.339 | 0.321 | 0.339 | 0.761                           | 0.761 | 0.817 | 0.761 | 0.817 | 0.836                            | 0.836 | 0.900 | 0.836 | 0.900 | ns    |
| HSTL_I_DCI_F        | 0.243                          | 0.393 | 0.415 | 0.393 | 0.415 | 0.407                           | 0.431 | 0.445 | 0.431 | 0.445 | 0.517                            | 0.555 | 0.575 | 0.555 | 0.575 | ns    |
| HSTL_I_DCI_M        | 0.243                          | 0.393 | 0.415 | 0.393 | 0.415 | 0.548                           | 0.552 | 0.581 | 0.552 | 0.581 | 0.635                            | 0.644 | 0.684 | 0.644 | 0.684 | ns    |

Table 29: IOB High Performance (HP) Switching Characteristics (Cont'd)

| I/O Standards  | T <sub>INBUF_DELAY_PAD_I</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_O_PAD</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_TD_PAD</sub> |       |       |       |       | Units |
|----------------|--------------------------------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|----------------------------------|-------|-------|-------|-------|-------|
|                | 0.90V                          | 0.85V | 0.72V |       |       | 0.90V                           | 0.85V | 0.72V |       |       | 0.90V                            | 0.85V | 0.72V |       |       |       |
|                | -3                             | -2    | -1    | -2    | -1    | -3                              | -2    | -1    | -2    | -1    | -3                               | -2    | -1    | -2    | -1    |       |
| HSTL_I_DCI_S   | 0.243                          | 0.393 | 0.415 | 0.393 | 0.415 | 0.766                           | 0.766 | 0.821 | 0.766 | 0.821 | 0.847                            | 0.847 | 0.912 | 0.847 | 0.912 | ns    |
| HSTL_I_F       | 0.322                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.409                           | 0.423 | 0.443 | 0.423 | 0.443 | 0.514                            | 0.549 | 0.581 | 0.549 | 0.581 | ns    |
| HSTL_I_M       | 0.322                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.548                           | 0.554 | 0.585 | 0.554 | 0.585 | 0.624                            | 0.640 | 0.677 | 0.640 | 0.677 | ns    |
| HSTL_I_S       | 0.322                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.766                           | 0.766 | 0.816 | 0.766 | 0.816 | 0.811                            | 0.811 | 0.866 | 0.811 | 0.866 | ns    |
| HSUL_12_DCI_F  | 0.319                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.411                           | 0.425 | 0.443 | 0.425 | 0.443 | 0.520                            | 0.558 | 0.586 | 0.558 | 0.586 | ns    |
| HSUL_12_DCI_M  | 0.319                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.551                           | 0.556 | 0.586 | 0.556 | 0.586 | 0.644                            | 0.654 | 0.694 | 0.654 | 0.694 | ns    |
| HSUL_12_DCI_S  | 0.319                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.736                           | 0.736 | 0.784 | 0.736 | 0.784 | 0.821                            | 0.821 | 0.886 | 0.821 | 0.886 | ns    |
| HSUL_12_F      | 0.305                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.394                           | 0.412 | 0.430 | 0.412 | 0.430 | 0.494                            | 0.538 | 0.566 | 0.538 | 0.566 | ns    |
| HSUL_12_M      | 0.305                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.551                           | 0.551 | 0.582 | 0.551 | 0.582 | 0.632                            | 0.642 | 0.679 | 0.642 | 0.679 | ns    |
| HSUL_12_S      | 0.305                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.750                           | 0.750 | 0.799 | 0.750 | 0.799 | 0.813                            | 0.813 | 0.868 | 0.813 | 0.868 | ns    |
| LVC MOS12_F_2  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.657                           | 0.672 | 0.692 | 0.672 | 0.692 | 0.862                            | 0.898 | 0.922 | 0.898 | 0.922 | ns    |
| LVC MOS12_F_4  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.486                           | 0.504 | 0.521 | 0.504 | 0.521 | 0.645                            | 0.664 | 0.693 | 0.664 | 0.693 | ns    |
| LVC MOS12_F_6  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.469                           | 0.485 | 0.507 | 0.485 | 0.507 | 0.585                            | 0.634 | 0.669 | 0.634 | 0.669 | ns    |
| LVC MOS12_F_8  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.457                           | 0.465 | 0.489 | 0.465 | 0.489 | 0.592                            | 0.611 | 0.666 | 0.611 | 0.666 | ns    |
| LVC MOS12_M_2  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.687                           | 0.708 | 0.727 | 0.708 | 0.727 | 0.889                            | 0.916 | 0.945 | 0.916 | 0.945 | ns    |
| LVC MOS12_M_4  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.533                           | 0.550 | 0.573 | 0.550 | 0.573 | 0.629                            | 0.664 | 0.690 | 0.664 | 0.690 | ns    |
| LVC MOS12_M_6  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.520                           | 0.527 | 0.554 | 0.527 | 0.554 | 0.608                            | 0.622 | 0.652 | 0.622 | 0.652 | ns    |
| LVC MOS12_M_8  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.532                           | 0.540 | 0.571 | 0.540 | 0.571 | 0.606                            | 0.614 | 0.649 | 0.614 | 0.649 | ns    |
| LVC MOS12_S_2  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.767                           | 0.767 | 0.803 | 0.767 | 0.803 | 0.981                            | 0.990 | 1.024 | 0.990 | 1.024 | ns    |
| LVC MOS12_S_4  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.666                           | 0.666 | 0.704 | 0.666 | 0.704 | 0.803                            | 0.803 | 0.848 | 0.803 | 0.848 | ns    |
| LVC MOS12_S_6  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.657                           | 0.657 | 0.695 | 0.657 | 0.695 | 0.732                            | 0.732 | 0.774 | 0.732 | 0.774 | ns    |
| LVC MOS12_S_8  | 0.443                          | 0.512 | 0.555 | 0.512 | 0.555 | 0.708                           | 0.708 | 0.761 | 0.708 | 0.761 | 0.745                            | 0.745 | 0.790 | 0.745 | 0.790 | ns    |
| LVC MOS15_F_12 | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.485                           | 0.500 | 0.522 | 0.500 | 0.522 | 0.584                            | 0.647 | 0.682 | 0.647 | 0.682 | ns    |
| LVC MOS15_F_2  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.686                           | 0.702 | 0.722 | 0.702 | 0.722 | 0.893                            | 0.919 | 0.940 | 0.919 | 0.940 | ns    |
| LVC MOS15_F_4  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.567                           | 0.579 | 0.601 | 0.579 | 0.601 | 0.727                            | 0.755 | 0.781 | 0.755 | 0.781 | ns    |
| LVC MOS15_F_6  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.533                           | 0.547 | 0.569 | 0.547 | 0.569 | 0.684                            | 0.711 | 0.742 | 0.711 | 0.742 | ns    |
| LVC MOS15_F_8  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.500                           | 0.518 | 0.538 | 0.518 | 0.538 | 0.635                            | 0.686 | 0.703 | 0.686 | 0.703 | ns    |
| LVC MOS15_M_12 | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.607                           | 0.607 | 0.644 | 0.607 | 0.644 | 0.637                            | 0.637 | 0.676 | 0.637 | 0.676 | ns    |
| LVC MOS15_M_2  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.736                           | 0.741 | 0.770 | 0.741 | 0.770 | 0.929                            | 0.938 | 0.962 | 0.938 | 0.962 | ns    |
| LVC MOS15_M_4  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.610                           | 0.625 | 0.651 | 0.625 | 0.651 | 0.733                            | 0.754 | 0.786 | 0.754 | 0.786 | ns    |
| LVC MOS15_M_6  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.564                           | 0.576 | 0.604 | 0.576 | 0.604 | 0.655                            | 0.674 | 0.710 | 0.674 | 0.710 | ns    |
| LVC MOS15_M_8  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.565                           | 0.568 | 0.601 | 0.568 | 0.601 | 0.634                            | 0.639 | 0.681 | 0.639 | 0.681 | ns    |
| LVC MOS15_S_12 | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.788                           | 0.788 | 0.855 | 0.788 | 0.855 | 0.695                            | 0.695 | 0.733 | 0.695 | 0.733 | ns    |
| LVC MOS15_S_2  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.829                           | 0.829 | 0.864 | 0.829 | 0.864 | 1.038                            | 1.039 | 1.079 | 1.039 | 1.079 | ns    |
| LVC MOS15_S_4  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.687                           | 0.687 | 0.725 | 0.687 | 0.725 | 0.813                            | 0.813 | 0.851 | 0.813 | 0.851 | ns    |
| LVC MOS15_S_6  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.671                           | 0.671 | 0.710 | 0.671 | 0.710 | 0.726                            | 0.726 | 0.763 | 0.726 | 0.763 | ns    |
| LVC MOS15_S_8  | 0.368                          | 0.414 | 0.445 | 0.414 | 0.445 | 0.704                           | 0.704 | 0.755 | 0.704 | 0.755 | 0.721                            | 0.721 | 0.758 | 0.721 | 0.758 | ns    |
| LVC MOS18_F_12 | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.564                           | 0.573 | 0.601 | 0.573 | 0.601 | 0.696                            | 0.731 | 0.769 | 0.731 | 0.769 | ns    |
| LVC MOS18_F_2  | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.723                           | 0.739 | 0.760 | 0.739 | 0.760 | 0.918                            | 0.945 | 0.971 | 0.945 | 0.971 | ns    |
| LVC MOS18_F_4  | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.598                           | 0.609 | 0.630 | 0.609 | 0.630 | 0.749                            | 0.778 | 0.802 | 0.778 | 0.802 | ns    |
| LVC MOS18_F_6  | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.598                           | 0.603 | 0.633 | 0.603 | 0.633 | 0.781                            | 0.781 | 0.808 | 0.781 | 0.808 | ns    |

Table 29: IOB High Performance (HP) Switching Characteristics (Cont'd)

| I/O Standards    | T <sub>INBUF_DELAY_PAD_I</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_O_PAD</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_TD_PAD</sub> |         |         |         |         | Units |
|------------------|--------------------------------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|----------------------------------|---------|---------|---------|---------|-------|
|                  | 0.90V                          | 0.85V | 0.72V |       |       | 0.90V                           | 0.85V | 0.72V |       |       | 0.90V                            | 0.85V   | 0.72V   |         |         |       |
|                  | -3                             | -2    | -1    | -2    | -1    | -3                              | -2    | -1    | -2    | -1    | -3                               | -2      | -1      | -2      | -1      |       |
| LVC MOS18_F_8    | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.567                           | 0.573 | 0.600 | 0.573 | 0.600 | 0.712                            | 0.733   | 0.767   | 0.733   | 0.767   | ns    |
| LVC MOS18_M_12   | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.640                           | 0.640 | 0.678 | 0.640 | 0.678 | 0.670                            | 0.670   | 0.709   | 0.670   | 0.709   | ns    |
| LVC MOS18_M_2    | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.785                           | 0.798 | 0.822 | 0.798 | 0.822 | 0.986                            | 0.991   | 1.016   | 0.991   | 1.016   | ns    |
| LVC MOS18_M_4    | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.658                           | 0.664 | 0.693 | 0.664 | 0.693 | 0.786                            | 0.798   | 0.836   | 0.798   | 0.836   | ns    |
| LVC MOS18_M_6    | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.625                           | 0.629 | 0.663 | 0.629 | 0.663 | 0.727                            | 0.735   | 0.775   | 0.735   | 0.775   | ns    |
| LVC MOS18_M_8    | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.626                           | 0.626 | 0.661 | 0.626 | 0.661 | 0.705                            | 0.705   | 0.746   | 0.705   | 0.746   | ns    |
| LVC MOS18_S_12   | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.795                           | 0.795 | 0.861 | 0.795 | 0.861 | 0.683                            | 0.683   | 0.721   | 0.683   | 0.721   | ns    |
| LVC MOS18_S_2    | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.861                           | 0.862 | 0.897 | 0.862 | 0.897 | 1.061                            | 1.076   | 1.098   | 1.076   | 1.098   | ns    |
| LVC MOS18_S_4    | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.716                           | 0.716 | 0.758 | 0.716 | 0.758 | 0.829                            | 0.829   | 0.872   | 0.829   | 0.872   | ns    |
| LVC MOS18_S_6    | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.682                           | 0.682 | 0.724 | 0.682 | 0.724 | 0.724                            | 0.724   | 0.762   | 0.724   | 0.762   | ns    |
| LVC MOS18_S_8    | 0.352                          | 0.418 | 0.445 | 0.418 | 0.445 | 0.707                           | 0.707 | 0.760 | 0.707 | 0.760 | 0.709                            | 0.709   | 0.745   | 0.709   | 0.745   | ns    |
| LVDCI_15_F       | 0.369                          | 0.425 | 0.462 | 0.425 | 0.462 | 0.407                           | 0.426 | 0.443 | 0.426 | 0.443 | 0.514                            | 0.548   | 0.581   | 0.548   | 0.581   | ns    |
| LVDCI_15_M       | 0.369                          | 0.425 | 0.462 | 0.425 | 0.462 | 0.549                           | 0.553 | 0.582 | 0.553 | 0.582 | 0.632                            | 0.645   | 0.685   | 0.645   | 0.685   | ns    |
| LVDCI_15_S       | 0.369                          | 0.425 | 0.462 | 0.425 | 0.462 | 0.749                           | 0.749 | 0.803 | 0.749 | 0.803 | 0.821                            | 0.821   | 0.890   | 0.821   | 0.890   | ns    |
| LVDCI_18_F       | 0.367                          | 0.414 | 0.447 | 0.414 | 0.447 | 0.422                           | 0.441 | 0.459 | 0.441 | 0.459 | 0.541                            | 0.560   | 0.589   | 0.560   | 0.589   | ns    |
| LVDCI_18_M       | 0.367                          | 0.414 | 0.447 | 0.414 | 0.447 | 0.546                           | 0.554 | 0.585 | 0.554 | 0.585 | 0.622                            | 0.644   | 0.683   | 0.644   | 0.683   | ns    |
| LVDCI_18_S       | 0.367                          | 0.414 | 0.447 | 0.414 | 0.447 | 0.760                           | 0.760 | 0.818 | 0.760 | 0.818 | 0.837                            | 0.837   | 0.899   | 0.837   | 0.899   | ns    |
| LVDS             | 0.508                          | 0.539 | 0.620 | 0.539 | 0.620 | 0.626                           | 0.626 | 0.662 | 0.626 | 0.662 | 960.447                          | 960.447 | 960.447 | 960.447 | 960.447 | ns    |
| MIPI_DPHY_DCI_HS | 0.305                          | 0.386 | 0.415 | 0.386 | 0.415 | 0.489                           | 0.502 | 0.522 | 0.502 | 0.522 | N/A                              | N/A     | N/A     | N/A     | N/A     | ns    |
| MIPI_DPHY_DCI_LP | 8.438                          | 8.438 | 8.792 | 8.438 | 8.792 | 0.895                           | 0.914 | 0.937 | 0.914 | 0.937 | N/A                              | N/A     | N/A     | N/A     | N/A     | ns    |
| POD10_DCI_F      | 0.336                          | 0.408 | 0.430 | 0.408 | 0.430 | 0.407                           | 0.425 | 0.444 | 0.425 | 0.444 | 0.512                            | 0.555   | 0.584   | 0.555   | 0.584   | ns    |
| POD10_DCI_M      | 0.336                          | 0.408 | 0.430 | 0.408 | 0.430 | 0.533                           | 0.542 | 0.571 | 0.542 | 0.571 | 0.618                            | 0.640   | 0.681   | 0.640   | 0.681   | ns    |
| POD10_DCI_S      | 0.336                          | 0.408 | 0.430 | 0.408 | 0.430 | 0.724                           | 0.754 | 0.815 | 0.754 | 0.815 | 0.815                            | 0.850   | 0.917   | 0.850   | 0.917   | ns    |
| POD10_F          | 0.336                          | 0.407 | 0.430 | 0.407 | 0.430 | 0.425                           | 0.438 | 0.459 | 0.438 | 0.459 | 0.531                            | 0.569   | 0.601   | 0.569   | 0.601   | ns    |
| POD10_M          | 0.336                          | 0.407 | 0.430 | 0.407 | 0.430 | 0.519                           | 0.538 | 0.568 | 0.538 | 0.568 | 0.589                            | 0.630   | 0.667   | 0.630   | 0.667   | ns    |
| POD10_S          | 0.336                          | 0.407 | 0.430 | 0.407 | 0.430 | 0.752                           | 0.766 | 0.821 | 0.766 | 0.821 | 0.821                            | 0.836   | 0.894   | 0.836   | 0.894   | ns    |
| POD12_DCI_F      | 0.336                          | 0.409 | 0.431 | 0.409 | 0.431 | 0.411                           | 0.425 | 0.443 | 0.425 | 0.443 | 0.519                            | 0.558   | 0.586   | 0.558   | 0.586   | ns    |
| POD12_DCI_M      | 0.336                          | 0.409 | 0.431 | 0.409 | 0.431 | 0.516                           | 0.543 | 0.572 | 0.543 | 0.572 | 0.602                            | 0.638   | 0.678   | 0.638   | 0.678   | ns    |
| POD12_DCI_S      | 0.336                          | 0.409 | 0.431 | 0.409 | 0.431 | 0.740                           | 0.772 | 0.822 | 0.772 | 0.822 | 0.833                            | 0.862   | 0.929   | 0.862   | 0.929   | ns    |
| POD12_F          | 0.336                          | 0.409 | 0.431 | 0.409 | 0.431 | 0.438                           | 0.455 | 0.476 | 0.455 | 0.476 | 0.549                            | 0.595   | 0.626   | 0.595   | 0.626   | ns    |
| POD12_M          | 0.336                          | 0.409 | 0.431 | 0.409 | 0.431 | 0.551                           | 0.551 | 0.582 | 0.551 | 0.582 | 0.632                            | 0.641   | 0.679   | 0.641   | 0.679   | ns    |
| POD12_S          | 0.336                          | 0.409 | 0.431 | 0.409 | 0.431 | 0.749                           | 0.767 | 0.817 | 0.767 | 0.817 | 0.818                            | 0.832   | 0.889   | 0.832   | 0.889   | ns    |
| SLVS_400_18      | 0.492                          | 0.539 | 0.620 | 0.539 | 0.620 | N/A                             | N/A   | N/A   | N/A   | N/A   | N/A                              | N/A     | N/A     | N/A     | N/A     | ns    |
| SSTL12_DCI_F     | 0.331                          | 0.381 | 0.399 | 0.381 | 0.399 | 0.411                           | 0.425 | 0.443 | 0.425 | 0.443 | 0.520                            | 0.558   | 0.586   | 0.558   | 0.586   | ns    |
| SSTL12_DCI_M     | 0.331                          | 0.381 | 0.399 | 0.381 | 0.399 | 0.549                           | 0.557 | 0.587 | 0.557 | 0.587 | 0.643                            | 0.654   | 0.694   | 0.654   | 0.694   | ns    |
| SSTL12_DCI_S     | 0.331                          | 0.381 | 0.399 | 0.381 | 0.399 | 0.754                           | 0.754 | 0.803 | 0.754 | 0.803 | 0.842                            | 0.842   | 0.908   | 0.842   | 0.908   | ns    |
| SSTL12_F         | 0.320                          | 0.403 | 0.403 | 0.403 | 0.403 | 0.394                           | 0.412 | 0.430 | 0.412 | 0.430 | 0.494                            | 0.538   | 0.566   | 0.538   | 0.566   | ns    |
| SSTL12_M         | 0.320                          | 0.403 | 0.403 | 0.403 | 0.403 | 0.550                           | 0.553 | 0.584 | 0.553 | 0.584 | 0.630                            | 0.641   | 0.676   | 0.641   | 0.676   | ns    |
| SSTL12_S         | 0.320                          | 0.403 | 0.403 | 0.403 | 0.403 | 0.758                           | 0.758 | 0.808 | 0.758 | 0.808 | 0.823                            | 0.823   | 0.879   | 0.823   | 0.879   | ns    |
| SSTL135_DCI_F    | 0.341                          | 0.366 | 0.399 | 0.366 | 0.399 | 0.392                           | 0.411 | 0.428 | 0.411 | 0.428 | 0.494                            | 0.537   | 0.565   | 0.537   | 0.565   | ns    |
| SSTL135_DCI_M    | 0.341                          | 0.366 | 0.399 | 0.366 | 0.399 | 0.551                           | 0.551 | 0.582 | 0.551 | 0.582 | 0.643                            | 0.645   | 0.685   | 0.645   | 0.685   | ns    |

Table 29: IOB High Performance (HP) Switching Characteristics (Cont'd)

| I/O Standards  | T <sub>INBUF_DELAY_PAD_I</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_O_PAD</sub> |       |       |       |       | T <sub>OUTBUF_DELAY_TD_PAD</sub> |         |         |         |         | Units |
|----------------|--------------------------------|-------|-------|-------|-------|---------------------------------|-------|-------|-------|-------|----------------------------------|---------|---------|---------|---------|-------|
|                | 0.90V                          |       | 0.85V |       | 0.72V | 0.90V                           |       | 0.85V |       | 0.72V | 0.90V                            |         | 0.85V   |         | 0.72V   |       |
|                | -3                             | -2    | -1    | -2    | -1    | -3                              | -2    | -1    | -2    | -1    | -3                               | -2      | -1      | -2      | -1      |       |
| SSTL135_DCI_S  | 0.341                          | 0.366 | 0.399 | 0.366 | 0.399 | 0.746                           | 0.746 | 0.799 | 0.746 | 0.799 | 0.829                            | 0.829   | 0.893   | 0.829   | 0.893   | ns    |
| SSTL135_F      | 0.321                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.393                           | 0.408 | 0.428 | 0.408 | 0.428 | 0.491                            | 0.528   | 0.561   | 0.528   | 0.561   | ns    |
| SSTL135_M      | 0.321                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.548                           | 0.555 | 0.585 | 0.555 | 0.585 | 0.621                            | 0.641   | 0.679   | 0.641   | 0.679   | ns    |
| SSTL135_S      | 0.321                          | 0.378 | 0.399 | 0.378 | 0.399 | 0.772                           | 0.772 | 0.823 | 0.772 | 0.823 | 0.827                            | 0.827   | 0.878   | 0.827   | 0.878   | ns    |
| SSTL15_DCI_F   | 0.319                          | 0.402 | 0.417 | 0.402 | 0.417 | 0.394                           | 0.412 | 0.429 | 0.412 | 0.429 | 0.497                            | 0.531   | 0.563   | 0.531   | 0.563   | ns    |
| SSTL15_DCI_M   | 0.319                          | 0.402 | 0.417 | 0.402 | 0.417 | 0.549                           | 0.553 | 0.583 | 0.553 | 0.583 | 0.632                            | 0.645   | 0.685   | 0.645   | 0.685   | ns    |
| SSTL15_DCI_S   | 0.319                          | 0.402 | 0.417 | 0.402 | 0.417 | 0.768                           | 0.768 | 0.822 | 0.768 | 0.822 | 0.847                            | 0.847   | 0.912   | 0.847   | 0.912   | ns    |
| SSTL15_F       | 0.320                          | 0.371 | 0.400 | 0.371 | 0.400 | 0.393                           | 0.408 | 0.428 | 0.408 | 0.428 | 0.494                            | 0.530   | 0.556   | 0.530   | 0.556   | ns    |
| SSTL15_M       | 0.320                          | 0.371 | 0.400 | 0.371 | 0.400 | 0.547                           | 0.554 | 0.585 | 0.554 | 0.585 | 0.624                            | 0.639   | 0.677   | 0.639   | 0.677   | ns    |
| SSTL15_S       | 0.320                          | 0.371 | 0.400 | 0.371 | 0.400 | 0.767                           | 0.767 | 0.817 | 0.767 | 0.817 | 0.813                            | 0.813   | 0.867   | 0.813   | 0.867   | ns    |
| SSTL18_I_DCI_F | 0.256                          | 0.329 | 0.336 | 0.329 | 0.336 | 0.422                           | 0.445 | 0.461 | 0.445 | 0.461 | 0.540                            | 0.566   | 0.595   | 0.566   | 0.595   | ns    |
| SSTL18_I_DCI_M | 0.256                          | 0.329 | 0.336 | 0.329 | 0.336 | 0.552                           | 0.554 | 0.585 | 0.554 | 0.585 | 0.629                            | 0.644   | 0.683   | 0.644   | 0.683   | ns    |
| SSTL18_I_DCI_S | 0.256                          | 0.329 | 0.336 | 0.329 | 0.336 | 0.762                           | 0.762 | 0.818 | 0.762 | 0.818 | 0.837                            | 0.837   | 0.899   | 0.837   | 0.899   | ns    |
| SSTL18_I_F     | 0.259                          | 0.316 | 0.337 | 0.316 | 0.337 | 0.439                           | 0.454 | 0.476 | 0.454 | 0.476 | 0.549                            | 0.578   | 0.608   | 0.578   | 0.608   | ns    |
| SSTL18_I_M     | 0.259                          | 0.316 | 0.337 | 0.316 | 0.337 | 0.567                           | 0.571 | 0.603 | 0.571 | 0.603 | 0.535                            | 0.652   | 0.692   | 0.652   | 0.692   | ns    |
| SSTL18_I_S     | 0.259                          | 0.316 | 0.337 | 0.316 | 0.337 | 0.782                           | 0.782 | 0.835 | 0.782 | 0.835 | 0.816                            | 0.816   | 0.870   | 0.816   | 0.870   | ns    |
| SUB_LVDS       | 0.508                          | 0.539 | 0.620 | 0.539 | 0.620 | 0.658                           | 0.660 | 0.692 | 0.660 | 0.692 | 906.048                          | 969.863 | 969.863 | 969.863 | 969.863 | ns    |

## IOB 3-state Output Switching Characteristics

Table 30 specifies the values of  $T_{\text{OUTBUF\_DELAY\_TE\_PAD}}$  and  $T_{\text{INBUF\_DELAY\_IBUFDIS\_O}}$ .

- $T_{\text{OUTBUF\_DELAY\_TE\_PAD}}$  is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).
- $T_{\text{INBUF\_DELAY\_IBUFDIS\_O}}$  is the IOB delay from IBUFDISABLE to O output.
- In HP I/O banks, the internal DCI termination turn-off time is always faster than  $T_{\text{OUTBUF\_DELAY\_TE\_PAD}}$  when the DCITERMDISABLE pin is used.
- In HD I/O banks, the internal IN\_TERM termination turn-off time is always faster than  $T_{\text{OUTBUF\_DELAY\_TE\_PAD}}$  when the INTERMDISABLE pin is used.

Table 30: IOB 3-state Output Switching Characteristics

| Symbol                             | Description                                                     | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |       |       |       | Units |
|------------------------------------|-----------------------------------------------------------------|----------------------------------------------------------|-------|-------|-------|-------|-------|
|                                    |                                                                 | 0.90V                                                    | 0.85V |       | 0.72V |       |       |
|                                    |                                                                 | -3                                                       | -2    | -1    | -2    | -1    |       |
| T <sub>OUTBUF_DELAY_TE_PAD</sub>   | T input to pad high-impedance for HD I/O banks                  | 6.318                                                    | 6.318 | 6.369 | 6.710 | 6.752 | ns    |
|                                    | T input to pad high-impedance for HP I/O banks                  | 5.330                                                    | 5.330 | 5.341 | 5.330 | 5.341 | ns    |
| T <sub>INBUF_DELAY_IBUFDIS_O</sub> | IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks | 2.266                                                    | 2.266 | 2.430 | 2.266 | 2.430 | ns    |
|                                    | IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks | 0.873                                                    | 0.936 | 1.037 | 0.936 | 1.037 | ns    |

## Input Delay Measurement Methodology

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: Input Delay Measurement Methodology

| Description                                        | I/O Standard Attribute          | $V_L^{(1)(2)}$           | $V_H^{(1)(2)}$           | $V_{\text{MEAS}}^{(1)(4)(6)}$ | $V_{\text{REF}}^{(1)(3)(5)}$ |
|----------------------------------------------------|---------------------------------|--------------------------|--------------------------|-------------------------------|------------------------------|
| LVC MOS, 1.2V                                      | LVC MOS12                       | 0.1                      | 1.1                      | 0.6                           | —                            |
| LVC MOS, LVDCI, HSLVDCI, 1.5V                      | LVC MOS15, LVDCI_15, HSLVDCI_15 | 0.1                      | 1.4                      | 0.75                          | —                            |
| LVC MOS, LVDCI, HSLVDCI, 1.8V                      | LVC MOS18, LVDCI_18, HSLVDCI_18 | 0.1                      | 1.7                      | 0.9                           | —                            |
| LVC MOS, 2.5V                                      | LVC MOS25                       | 0.1                      | 2.4                      | 1.25                          | —                            |
| LVC MOS, 3.3V                                      | LVC MOS33                       | 0.1                      | 3.2                      | 1.65                          | —                            |
| LV TTL, 3.3V                                       | LV TTL                          | 0.1                      | 3.2                      | 1.65                          | —                            |
| HSTL (high-speed transceiver logic), class I, 1.2V | HSTL_I_12                       | $V_{\text{REF}} - 0.25$  | $V_{\text{REF}} + 0.25$  | $V_{\text{REF}}$              | 0.6                          |
| HSTL, class I, 1.5V                                | HSTL_I                          | $V_{\text{REF}} - 0.325$ | $V_{\text{REF}} + 0.325$ | $V_{\text{REF}}$              | 0.75                         |

Table 31: Input Delay Measurement Methodology (Cont'd)

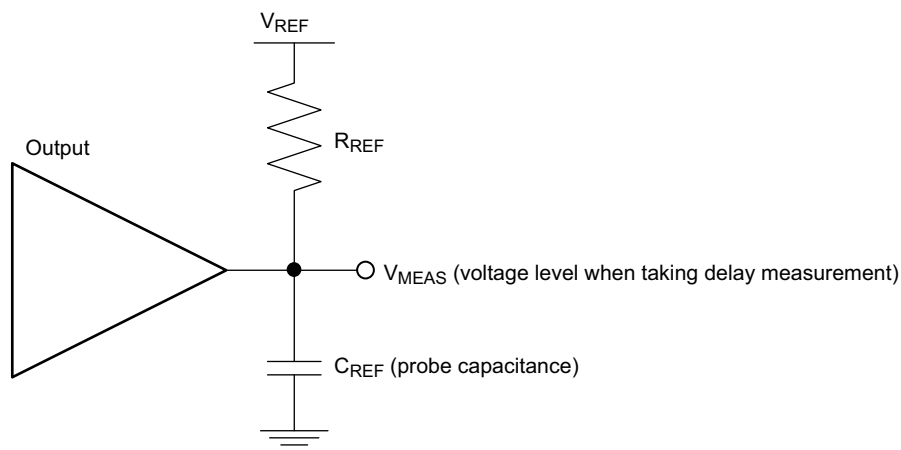
| Description                                     | I/O Standard Attribute        | $V_L^{(1)(2)}$     | $V_H^{(1)(2)}$     | $V_{MEAS}^{(1)(4)(6)}$ | $V_{REF}^{(1)(3)(5)}$ |
|-------------------------------------------------|-------------------------------|--------------------|--------------------|------------------------|-----------------------|
| HSTL, class I, 1.8V                             | HSTL_I_18                     | $V_{REF} - 0.4$    | $V_{REF} + 0.4$    | $V_{REF}$              | 0.9                   |
| HSUL (high-speed unterminated logic), 1.2V      | HSUL_12                       | $V_{REF} - 0.25$   | $V_{REF} + 0.25$   | $V_{REF}$              | 0.6                   |
| SSTL12 (stub series terminated logic), 1.2V     | SSTL12                        | $V_{REF} - 0.25$   | $V_{REF} + 0.25$   | $V_{REF}$              | 0.6                   |
| SSTL135 and SSTL135 class II, 1.35V             | SSTL135, SSTL135_II           | $V_{REF} - 0.2875$ | $V_{REF} + 0.2875$ | $V_{REF}$              | 0.675                 |
| SSTL15 and SSTL15 class II, 1.5V                | SSTL15, SSTL15_II             | $V_{REF} - 0.325$  | $V_{REF} + 0.325$  | $V_{REF}$              | 0.75                  |
| SSTL18, class I and II, 1.8V                    | SSTL18_I, SSTL18_II           | $V_{REF} - 0.4$    | $V_{REF} + 0.4$    | $V_{REF}$              | 0.9                   |
| POD10, 1.0V                                     | POD10                         | $V_{REF} - 0.2$    | $V_{REF} + 0.2$    | $V_{REF}$              | 0.7                   |
| POD12, 1.2V                                     | POD12                         | $V_{REF} - 0.24$   | $V_{REF} + 0.24$   | $V_{REF}$              | 0.84                  |
| DIFF_HSTL, class I, 1.2V                        | DIFF_HSTL_I_12                | $0.6 - 0.25$       | $0.6 + 0.25$       | 0 <sup>(6)</sup>       | –                     |
| DIFF_HSTL, class I, 1.5V                        | DIFF_HSTL_I                   | $0.75 - 0.325$     | $0.75 + 0.325$     | 0 <sup>(6)</sup>       | –                     |
| DIFF_HSTL, class I, 1.8V                        | DIFF_HSTL_I_18                | $0.9 - 0.4$        | $0.9 + 0.4$        | 0 <sup>(6)</sup>       | –                     |
| DIFF_HSUL, 1.2V                                 | DIFF_HSUL_12                  | $0.6 - 0.25$       | $0.6 + 0.25$       | 0 <sup>(6)</sup>       | –                     |
| DIFF_SSTL, 1.2V                                 | DIFF_SSTL12                   | $0.6 - 0.25$       | $0.6 + 0.25$       | 0 <sup>(6)</sup>       | –                     |
| DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V   | DIFF_SSTL135, DIFF_SSTL135_II | $0.675 - 0.2875$   | $0.675 + 0.2875$   | 0 <sup>(6)</sup>       | –                     |
| DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V      | DIFF_SSTL15, DIFF_SSTL15_II   | $0.75 - 0.325$     | $0.75 + 0.325$     | 0 <sup>(6)</sup>       | –                     |
| DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V             | DIFF_SSTL18_I, DIFF_SSTL18_II | $0.9 - 0.4$        | $0.9 + 0.4$        | 0 <sup>(6)</sup>       | –                     |
| DIFF_POD10, 1.0V                                | DIFF_POD10                    | $0.5 - 0.2$        | $0.5 + 0.2$        | 0 <sup>(6)</sup>       | –                     |
| DIFF_POD12, 1.2V                                | DIFF_POD12                    | $0.6 - 0.25$       | $0.6 + 0.25$       | 0 <sup>(6)</sup>       | –                     |
| LVDS (low-voltage differential signaling), 1.8V | LVDS                          | $0.9 - 0.125$      | $0.9 + 0.125$      | 0 <sup>(6)</sup>       | –                     |
| LVDS_25, 2.5V                                   | LVDS_25                       | $1.25 - 0.125$     | $1.25 + 0.125$     | 0 <sup>(6)</sup>       | –                     |
| SUB_LVDS, 1.8V                                  | SUB_LVDS                      | $0.9 - 0.125$      | $0.9 + 0.125$      | 0 <sup>(6)</sup>       | –                     |
| SLVS, 1.8V                                      | SLVS_400_18                   | $0.9 - 0.125$      | $0.9 + 0.125$      | 0 <sup>(6)</sup>       | –                     |
| SLVS, 2.5V                                      | SLVS_400_25                   | $1.25 - 0.125$     | $1.25 + 0.125$     | 0 <sup>(6)</sup>       | –                     |
| LVPECL, 2.5V                                    | LVPECL                        | $1.25 - 0.125$     | $1.25 + 0.125$     | 0 <sup>(6)</sup>       | –                     |
| MIPI D-PHY (high speed) 1.2V                    | MIPI_DPHY_DCI_HS              | $0.2 - 0.125$      | $0.2 + 0.125$      | 0 <sup>(6)</sup>       | –                     |
| MIPI D-PHY (low power) 1.2V                     | MIPI_DPHY_DCI_LP              | $0.715 - 0.2$      | $0.715 + 0.2$      | 0 <sup>(6)</sup>       | –                     |

**Notes:**

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVC MOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between  $V_L$  and  $V_H$ .
3. Measurements are made at typical, minimum, and maximum  $V_{REF}$  values. Reported delays reflect worst case of these measurements.  $V_{REF}$  values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the  $V_{REF}/V_{MEAS}$  parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

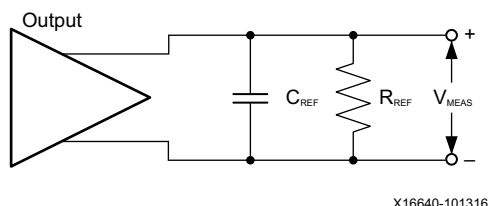
## Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



X16654-101316

Figure 1: Single-Ended Test Setup



X16640-101316

Figure 2: Differential Test Setup

Parameters  $V_{REF}$ ,  $R_{REF}$ ,  $C_{REF}$ , and  $V_{MEAS}$  fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 32](#).
2. Record the time to  $V_{MEAS}$ .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to  $V_{MEAS}$ .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: Output Delay Measurement Methodology

| Description                                        | I/O Standard Attribute           | R <sub>REF</sub><br>( $\Omega$ ) | C <sub>REF</sub> <sup>(1)</sup><br>(pF) | V <sub>MEAS</sub><br>(V) | V <sub>REF</sub><br>(V) |
|----------------------------------------------------|----------------------------------|----------------------------------|-----------------------------------------|--------------------------|-------------------------|
| LVC MOS, 1.2V                                      | LVC MOS12                        | 1M                               | 0                                       | 0.6                      | 0                       |
| LVC MOS, 1.5V                                      | LVC MOS15                        | 1M                               | 0                                       | 0.75                     | 0                       |
| LVC MOS, 1.8V                                      | LVC MOS18                        | 1M                               | 0                                       | 0.9                      | 0                       |
| LVC MOS, 2.5V                                      | LVC MOS25                        | 1M                               | 0                                       | 1.25                     | 0                       |
| LVC MOS, 3.3V                                      | LVC MOS33                        | 1M                               | 0                                       | 1.65                     | 0                       |
| LVTTL, 3.3V                                        | LVTTL                            | 1M                               | 0                                       | 1.65                     | 0                       |
| LVDCI, HSLVDCI, 1.5V                               | LVDCI_15, HSLVDCI_15             | 50                               | 0                                       | V <sub>REF</sub>         | 0.75                    |
| LVDCI, HSLVDCI, 1.8V                               | LVDCI_15, HSLVDCI_18             | 50                               | 0                                       | V <sub>REF</sub>         | 0.9                     |
| HSTL (high-speed transceiver logic), class I, 1.2V | HSTL_I_12                        | 50                               | 0                                       | V <sub>REF</sub>         | 0.6                     |
| HSTL, class I, 1.5V                                | HSTL_I                           | 50                               | 0                                       | V <sub>REF</sub>         | 0.75                    |
| HSTL, class I, 1.8V                                | HSTL_I_18                        | 50                               | 0                                       | V <sub>REF</sub>         | 0.9                     |
| HSUL (high-speed unterminated logic), 1.2V         | HSUL_12                          | 50                               | 0                                       | V <sub>REF</sub>         | 0.6                     |
| SSTL12 (stub series terminated logic), 1.2V        | SSTL12                           | 50                               | 0                                       | V <sub>REF</sub>         | 0.6                     |
| SSTL135 and SSTL135 class II, 1.35V                | SSTL135, SSTL135_II              | 50                               | 0                                       | V <sub>REF</sub>         | 0.675                   |
| SSTL15 and SSTL15 class II, 1.5V                   | SSTL15, SSTL15_II                | 50                               | 0                                       | V <sub>REF</sub>         | 0.75                    |
| SSTL18, class I and class II, 1.8V                 | SSTL18_I, SSTL18_II              | 50                               | 0                                       | V <sub>REF</sub>         | 0.9                     |
| POD10, 1.0V                                        | POD10                            | 50                               | 0                                       | V <sub>REF</sub>         | 1.0                     |
| POD12, 1.2V                                        | POD12                            | 50                               | 0                                       | V <sub>REF</sub>         | 1.2                     |
| DIFF_HSTL, class I, 1.2V                           | DIFF_HSTL_I_12                   | 50                               | 0                                       | V <sub>REF</sub>         | 0.6                     |
| DIFF_HSTL, class I, 1.5V                           | DIFF_HSTL_I                      | 50                               | 0                                       | V <sub>REF</sub>         | 0.75                    |
| DIFF_HSTL, class I, 1.8V                           | DIFF_HSTL_I_18                   | 50                               | 0                                       | V <sub>REF</sub>         | 0.9                     |
| DIFF_HSUL, 1.2V                                    | DIFF_HSUL_12                     | 50                               | 0                                       | V <sub>REF</sub>         | 0.6                     |
| DIFF_SSTL12, 1.2V                                  | DIFF_SSTL12                      | 50                               | 0                                       | V <sub>REF</sub>         | 0.6                     |
| DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V      | DIFF_SSTL135,<br>DIFF_SSTL135_II | 50                               | 0                                       | V <sub>REF</sub>         | 0.675                   |
| DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V         | DIFF_SSTL15,<br>DIFF_SSTL15_II   | 50                               | 0                                       | V <sub>REF</sub>         | 0.75                    |
| DIFF_SSTL18, class I and II, 1.8V                  | DIFF_SSTL18_I,<br>DIFF_SSTL18_II | 50                               | 0                                       | V <sub>REF</sub>         | 0.9                     |
| DIFF_POD10, 1.0V                                   | DIFF_POD10                       | 50                               | 0                                       | V <sub>REF</sub>         | 1.0                     |
| DIFF_POD12, 1.2V                                   | DIFF_POD12                       | 50                               | 0                                       | V <sub>REF</sub>         | 1.2                     |
| LVDS (low-voltage differential signaling), 1.8V    | LVDS                             | 100                              | 0                                       | 0 <sup>(2)</sup>         | 0                       |
| SUB_LVDS, 1.8V                                     | SUB_LVDS                         | 100                              | 0                                       | 0 <sup>(2)</sup>         | 0                       |
| MIPI D-PHY (high speed) 1.2V                       | MIPI_DPHY_DCI_HS                 | 100                              | 0                                       | 0 <sup>(2)</sup>         | 0                       |
| MIPI D-PHY (low power) 1.2V                        | MIPI_DPHY_DCI_LP                 | 1M                               | 0                                       | 0.6                      | 0                       |

**Notes:**

1. C<sub>REF</sub> is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

## Block RAM and FIFO Switching Characteristics

Table 33: Block RAM and FIFO Switching Characteristics

| Symbol                                 | Description                                                                                           | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |      |       |      | Units   |
|----------------------------------------|-------------------------------------------------------------------------------------------------------|----------------------------------------------------------|-------|------|-------|------|---------|
|                                        |                                                                                                       | 0.90V                                                    | 0.85V |      | 0.72V |      |         |
|                                        |                                                                                                       | -3                                                       | -2    | -1   | -2    | -1   |         |
| Maximum Frequency                      |                                                                                                       |                                                          |       |      |       |      |         |
| F <sub>MAX_WF_NC</sub>                 | Block RAM (WRITE_FIRST and NO_CHANGE modes).                                                          | 825                                                      | 738   | 645  | 585   | 516  | MHz     |
| F <sub>MAX_RF</sub>                    | Block RAM (READ_FIRST mode).                                                                          | 718                                                      | 637   | 575  | 510   | 460  | MHz     |
| F <sub>MAX_FIFO</sub>                  | FIFO in all modes without ECC.                                                                        | 825                                                      | 738   | 645  | 585   | 516  | MHz     |
| F <sub>MAX_ECC</sub>                   | Block RAM and FIFO in ECC configuration without PIPELINE.                                             | 718                                                      | 637   | 575  | 510   | 460  | MHz     |
|                                        | Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode. | 825                                                      | 738   | 645  | 585   | 516  | MHz     |
| T <sub>PW</sub> <sup>(1)</sup>         | Minimum pulse width.                                                                                  | 495                                                      | 542   | 543  | 577   | 578  | ps      |
| Block RAM and FIFO Clock-to-Out Delays |                                                                                                       |                                                          |       |      |       |      |         |
| T <sub>RCKO_DO</sub>                   | Clock CLK to DOUT output (without output register).                                                   | 0.91                                                     | 1.02  | 1.11 | 1.46  | 1.53 | ns, Max |
| T <sub>RCKO_DO_REG</sub>               | Clock CLK to DOUT output (with output register).                                                      | 0.27                                                     | 0.29  | 0.30 | 0.42  | 0.44 | ns, Max |

### Notes:

1. The MMCM and PLL DUTY\_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

## UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Kintex UltraScale+ FPGAs that include this memory.

Table 34: UltraRAM Switching Characteristics

| Symbol                          | Description                                                                   | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |     |       |     | Units |
|---------------------------------|-------------------------------------------------------------------------------|----------------------------------------------------------|-------|-----|-------|-----|-------|
|                                 |                                                                               | 0.90V                                                    | 0.85V |     | 0.72V |     |       |
|                                 |                                                                               | -3                                                       | -2    | -1  | -2    | -1  |       |
| Maximum Frequency               |                                                                               |                                                          |       |     |       |     |       |
| F <sub>MAX</sub>                | UltraRAM maximum frequency with<br>OREG_B = True.                             | 650                                                      | 600   | 575 | 500   | 481 | MHz   |
| F <sub>MAX_ECC_NOPIPELINE</sub> | UltraRAM maximum frequency with<br>OREG_B = False and<br>EN_ECC_RD_B = True.  | 435                                                      | 400   | 386 | 312   | 303 | MHz   |
| F <sub>MAX_NOPIPELINE</sub>     | UltraRAM maximum frequency with<br>OREG_B = False and<br>EN_ECC_RD_B = False. | 528                                                      | 500   | 478 | 404   | 389 | MHz   |
| T <sub>PW</sub> <sup>(1)</sup>  | Minimum pulse width.                                                          | 650                                                      | 700   | 730 | 800   | 832 | ps    |
| T <sub>RSTPW</sub>              | Asynchronous reset minimum pulse<br>width. One cycle required.                | 1 clock cycle                                            |       |     |       |     |       |

**Notes:**

1. The MMCM and PLL DUTY\_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

## Input/Output Delay Switching Characteristics

Table 35: Input/Output Delay Switching Characteristics

| Symbol                                                             | Description                                          | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |                |             |             |             | Units |
|--------------------------------------------------------------------|------------------------------------------------------|----------------------------------------------------------|----------------|-------------|-------------|-------------|-------|
|                                                                    |                                                      | 0.90V                                                    | 0.85V          |             | 0.72V       |             |       |
|                                                                    |                                                      | -3                                                       | -2             | -1          | -2          | -1          |       |
| F <sub>REFCLK</sub>                                                | REFCLK frequency for IDELAYCTRL (component mode).    | 300 to 800                                               |                |             |             |             | MHz   |
|                                                                    | REFCLK frequency for BITSlice_CONTROL (native mode). | 300 to 2666.67                                           | 300 to 2666.67 | 300 to 2400 | 300 to 2400 | 300 to 2133 | MHz   |
| T <sub>MINPER_CLK</sub>                                            | Minimum period for IODELAY clock.                    | 3.195                                                    | 3.195          | 3.195       | 3.195       | 3.195       | ns    |
| T <sub>MINPER_RST</sub>                                            | Minimum reset pulse width.                           | 52.00                                                    |                |             |             |             | ns    |
| T <sub>IDELAY_RESOLUTION</sub> /<br>T <sub>ODELAY_RESOLUTION</sub> | IDELAY/ODELAY chain resolution.                      | 2.1 to 12                                                |                |             |             |             | ps    |

**Notes:**

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY = VCO\_HALF, the minimum frequency is PLL\_FVCOMIN/2.

## DSP48 Slice Switching Characteristics

Table 36: DSP48 Slice Switching Characteristics

| Symbol                                | Description                                                   | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |     |                      |     | Units |
|---------------------------------------|---------------------------------------------------------------|----------------------------------------------------------|-------|-----|----------------------|-----|-------|
|                                       |                                                               | 0.90V                                                    | 0.85V |     | 0.72V <sup>(1)</sup> |     |       |
|                                       |                                                               | -3                                                       | -2    | -1  | -2                   | -1  |       |
| Maximum Frequency                     |                                                               |                                                          |       |     |                      |     |       |
| F <sub>MAX</sub>                      | With all registers used.                                      | 891                                                      | 775   | 645 | 644                  | 600 | MHz   |
| F <sub>MAX_PATDET</sub>               | With pattern detector.                                        | 794                                                      | 687   | 571 | 562                  | 524 | MHz   |
| F <sub>MAX_MULT_NOMREG</sub>          | Two register multiply without MREG.                           | 635                                                      | 544   | 456 | 440                  | 413 | MHz   |
| F <sub>MAX_MULT_NOMREG_PATDET</sub>   | Two register multiply without MREG with pattern detect.       | 577                                                      | 492   | 410 | 395                  | 371 | MHz   |
| F <sub>MAX_PREADD_NOADREG</sub>       | Without ADREG.                                                | 655                                                      | 565   | 468 | 453                  | 423 | MHz   |
| F <sub>MAX_NOPIPELINEREG</sub>        | Without pipeline registers (MREG, ADREG).                     | 483                                                      | 410   | 338 | 323                  | 304 | MHz   |
| F <sub>MAX_NOPIPELINEREG_PATDET</sub> | Without pipeline registers (MREG, ADREG) with pattern detect. | 448                                                      | 379   | 314 | 299                  | 280 | MHz   |

### Notes:

- For devices operating at the lower power V<sub>CCINT</sub> = 0.72V voltages, DSP cascades that cross clock region boundaries might operate below the specified F<sub>MAX</sub>.

## Clock Buffers and Networks

Table 37: Clock Buffers Switching Characteristics

| Symbol                                                                                | Description                                                                                                 | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |     |       |     | Units |
|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|-------|-----|-------|-----|-------|
|                                                                                       |                                                                                                             | 0.90V                                                    | 0.85V |     | 0.72V |     |       |
|                                                                                       |                                                                                                             | -3                                                       | -2    | -1  | -2    | -1  |       |
| Global Clock Switching Characteristics (Including BUFGCTRL)                           |                                                                                                             |                                                          |       |     |       |     |       |
| F <sub>MAX</sub>                                                                      | Maximum frequency of a global clock tree (BUFG).                                                            | 891                                                      | 775   | 667 | 725   | 667 | MHz   |
| Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)                         |                                                                                                             |                                                          |       |     |       |     |       |
| F <sub>MAX</sub>                                                                      | Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).                       | 891                                                      | 775   | 667 | 725   | 667 | MHz   |
| Global Clock Buffer with Clock Enable (BUFGCE)                                        |                                                                                                             |                                                          |       |     |       |     |       |
| F <sub>MAX</sub>                                                                      | Maximum frequency of a global clock buffer with clock enable (BUFGCE).                                      | 891                                                      | 775   | 667 | 725   | 667 | MHz   |
| Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)                                      |                                                                                                             |                                                          |       |     |       |     |       |
| F <sub>MAX</sub>                                                                      | Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).                                    | 891                                                      | 775   | 667 | 725   | 667 | MHz   |
| GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT) |                                                                                                             |                                                          |       |     |       |     |       |
| F <sub>MAX</sub>                                                                      | Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability. | 512                                                      | 512   | 512 | 512   | 512 | MHz   |

# MMCM Switching Characteristics

Table 38: MMCM Specification

| Symbol                          | Description                                             | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |      |       |      | Units |
|---------------------------------|---------------------------------------------------------|----------------------------------------------------------|-------|------|-------|------|-------|
|                                 |                                                         | 0.90V                                                    | 0.85V |      | 0.72V |      |       |
|                                 |                                                         | -3                                                       | -2    | -1   | -2    | -1   |       |
| MMCM_F <sub>INMAX</sub>         | Maximum input clock frequency.                          | 1066                                                     | 933   | 800  | 933   | 800  | MHz   |
| MMCM_F <sub>INMIN</sub>         | Minimum input clock frequency.                          | 10                                                       | 10    | 10   | 10    | 10   | MHz   |
| MMCM_F <sub>INJITTER</sub>      | Maximum input clock period jitter.                      | < 20% of clock input period or 1 ns Max                  |       |      |       |      |       |
| MMCM_F <sub>INDUTY</sub>        | Input duty cycle range: 10–49 MHz.                      | 25–75                                                    |       |      |       |      | %     |
|                                 | Input duty cycle range: 50–199 MHz.                     | 30–70                                                    |       |      |       |      | %     |
|                                 | Input duty cycle range: 200–399 MHz.                    | 35–65                                                    |       |      |       |      | %     |
|                                 | Input duty cycle range: 400–499 MHz.                    | 40–60                                                    |       |      |       |      | %     |
|                                 | Input duty cycle range: >500 MHz.                       | 45–55                                                    |       |      |       |      | %     |
| MMCM_F <sub>MIN_PSCLK</sub>     | Minimum dynamic phase shift clock frequency.            | 0.01                                                     | 0.01  | 0.01 | 0.01  | 0.01 | MHz   |
| MMCM_F <sub>MAX_PSCLK</sub>     | Maximum dynamic phase shift clock frequency.            | 550                                                      | 500   | 450  | 500   | 450  | MHz   |
| MMCM_F <sub>VCOMIN</sub>        | Minimum MMCM VCO frequency.                             | 800                                                      | 800   | 800  | 800   | 800  | MHz   |
| MMCM_F <sub>VCOMAX</sub>        | Maximum MMCM VCO frequency.                             | 1600                                                     | 1600  | 1600 | 1600  | 1600 | MHz   |
| MMCM_F <sub>BANDWIDTH</sub>     | Low MMCM bandwidth at typical. <sup>(1)</sup>           | 1.00                                                     | 1.00  | 1.00 | 1.00  | 1.00 | MHz   |
|                                 | High MMCM bandwidth at typical. <sup>(1)</sup>          | 4.00                                                     | 4.00  | 4.00 | 4.00  | 4.00 | MHz   |
| MMCM_T <sub>STATPHAOFFSET</sub> | Static phase offset of the MMCM outputs. <sup>(2)</sup> | 0.12                                                     | 0.12  | 0.12 | 0.12  | 0.12 | ns    |
| MMCM_T <sub>OUTJITTER</sub>     | MMCM output jitter.                                     | Note 3                                                   |       |      |       |      |       |
| MMCM_T <sub>OUTDUTY</sub>       | MMCM output clock duty cycle precision. <sup>(4)</sup>  | 0.165                                                    | 0.20  | 0.20 | 0.20  | 0.20 | ns    |
| MMCM_T <sub>LOCKMAX</sub>       | MMCM maximum lock time for MMCM_F <sub>PFDMIN</sub> .   | 100                                                      | 100   | 100  | 100   | 100  | μs    |
| MMCM_F <sub>OUTMAX</sub>        | MMCM maximum output frequency.                          | 891                                                      | 775   | 667  | 725   | 667  | MHz   |
| MMCM_F <sub>OUTMIN</sub>        | MMCM minimum output frequency. <sup>(4)(5)</sup>        | 6.25                                                     | 6.25  | 6.25 | 6.25  | 6.25 | MHz   |
| MMCM_T <sub>EXTFVAR</sub>       | External clock feedback variation.                      | < 20% of clock input period or 1 ns Max                  |       |      |       |      |       |
| MMCM_RST <sub>MINPULSE</sub>    | Minimum reset pulse width.                              | 5.00                                                     | 5.00  | 5.00 | 5.00  | 5.00 | ns    |
| MMCM_F <sub>PFDMAX</sub>        | Maximum frequency at the phase frequency detector.      | 550                                                      | 500   | 450  | 500   | 450  | MHz   |
| MMCM_F <sub>PFDMIN</sub>        | Minimum frequency at the phase frequency detector.      | 10                                                       | 10    | 10   | 10    | 10   | MHz   |
| MMCM_T <sub>FBDELAY</sub>       | Maximum delay in the feedback path.                     | 5 ns Max or one clock cycle                              |       |      |       |      |       |
| MMCM_F <sub>DPRCLK_MAX</sub>    | Maximum DRP clock frequency.                            | 250                                                      | 250   | 250  | 250   | 250  | MHz   |

## Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F<sub>VCO</sub>/128 assuming output duty cycle is 50%.

# PLL Switching Characteristics

Table 39: PLL Specification<sup>(1)</sup>

| Symbol                         | Description                                                                          | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages     |       |       |       |       | Units |
|--------------------------------|--------------------------------------------------------------------------------------|--------------------------------------------------------------|-------|-------|-------|-------|-------|
|                                |                                                                                      | 0.90V                                                        | 0.85V |       | 0.72V |       |       |
|                                |                                                                                      | -3                                                           | -2    | -1    | -2    | -1    |       |
| PLL_F <sub>INMAX</sub>         | Maximum input clock frequency.                                                       | 1066                                                         | 933   | 800   | 933   | 800   | MHz   |
| PLL_F <sub>INMIN</sub>         | Minimum input clock frequency.                                                       | 70                                                           | 70    | 70    | 70    | 70    | MHz   |
| PLL_F <sub>INJITTER</sub>      | Maximum input clock period jitter.                                                   | < 20% of clock input period or 1 ns Max                      |       |       |       |       |       |
| PLL_F <sub>INDUTY</sub>        | Input duty cycle range: 70–399 MHz.                                                  | 35–65                                                        |       |       |       |       | %     |
|                                | Input duty cycle range: 400–499 MHz.                                                 | 40–60                                                        |       |       |       |       | %     |
|                                | Input duty cycle range: >500 MHz.                                                    | 45–55                                                        |       |       |       |       | %     |
| PLL_F <sub>VCOMIN</sub>        | Minimum PLL VCO frequency.                                                           | 750                                                          | 750   | 750   | 750   | 750   | MHz   |
| PLL_F <sub>VCOMAX</sub>        | Maximum PLL VCO frequency.                                                           | 1500                                                         | 1500  | 1500  | 1500  | 1500  | MHz   |
| PLL_T <sub>STATPHAOFFSET</sub> | Static phase offset of the PLL outputs. <sup>(2)</sup>                               | 0.12                                                         | 0.12  | 0.12  | 0.12  | 0.12  | ns    |
| PLL_T <sub>OUTJITTER</sub>     | PLL output jitter.                                                                   | Note 3                                                       |       |       |       |       |       |
| PLL_T <sub>OUTDUTY</sub>       | PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision. <sup>(4)</sup>        | 0.165                                                        | 0.20  | 0.20  | 0.20  | 0.20  | ns    |
| PLL_T <sub>LOCKMAX</sub>       | PLL maximum lock time.                                                               | 100                                                          |       |       |       |       | μs    |
| PLL_F <sub>OUTMAX</sub>        | PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.                | 891                                                          | 775   | 667   | 725   | 667   | MHz   |
|                                | PLL maximum output frequency at CLKOUTPHY.                                           | 2667                                                         | 2667  | 2400  | 2400  | 2133  | MHz   |
| PLL_F <sub>OUTMIN</sub>        | PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B. <sup>(5)</sup> | 5.86                                                         | 5.86  | 5.86  | 5.86  | 5.86  | MHz   |
|                                | PLL minimum output frequency at CLKOUTPHY.                                           | 2 x VCO mode: 1500, 1 x VCO mode: 750<br>0.5 x VCO mode: 375 |       |       |       |       | MHz   |
| PLL_RST <sub>MINPULSE</sub>    | Minimum reset pulse width.                                                           | 5.00                                                         | 5.00  | 5.00  | 5.00  | 5.00  | ns    |
| PLL_F <sub>PFDMAX</sub>        | Maximum frequency at the phase frequency detector.                                   | 667.5                                                        | 667.5 | 667.5 | 667.5 | 667.5 | MHz   |
| PLL_F <sub>PFDMIN</sub>        | Minimum frequency at the phase frequency detector.                                   | 70                                                           | 70    | 70    | 70    | 70    | MHz   |
| PLL_F <sub>BANDWIDTH</sub>     | PLL bandwidth at typical.                                                            | 14                                                           | 14    | 14    | 14    | 14    | MHz   |
| PLL_F <sub>DP RCLK_MAX</sub>   | Maximum DRP clock frequency                                                          | 250                                                          | 250   | 250   | 250   | 250   | MHz   |

## Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F<sub>VCO</sub>/128 assuming output duty cycle is 50%.

## Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 40 through Table 42 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 40: Global Clock Input to Output Delay Without MMCM (Near Clock Region)

| Symbol                                                                                                 | Description                                                                      | Device  | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |      |       |      | Units |
|--------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|---------|----------------------------------------------------------|-------|------|-------|------|-------|
|                                                                                                        |                                                                                  |         | 0.90V                                                    | 0.85V |      | 0.72V |      |       |
|                                                                                                        |                                                                                  |         | -3                                                       | -2    | -1   | -2    | -1   |       |
| SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM. |                                                                                  |         |                                                          |       |      |       |      |       |
| T <sub>ICKOF</sub>                                                                                     | Global clock input and output flip-flop <i>without</i> MMCM (near clock region). | XCKU3P  | 4.30                                                     | 5.09  | 5.48 | 6.45  | 6.88 | ns    |
|                                                                                                        |                                                                                  | XCKU5P  | 4.30                                                     | 5.09  | 5.48 | 6.45  | 6.88 | ns    |
|                                                                                                        |                                                                                  | XCKU9P  | 5.00                                                     | 5.91  | 6.35 | 7.61  | 8.08 | ns    |
|                                                                                                        |                                                                                  | XCKU11P | 5.82                                                     | 6.96  | 7.61 | 8.01  | 9.35 | ns    |
|                                                                                                        |                                                                                  | XCKU13P | 5.15                                                     | 6.09  | 6.55 | 7.89  | 8.39 | ns    |
|                                                                                                        |                                                                                  | XCKU15P | 5.72                                                     | 6.90  | 7.40 | 8.82  | 9.37 | ns    |

### Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 41: Global Clock Input to Output Delay Without MMCM (Far Clock Region)

| Symbol                                                                                                 | Description                                                                     | Device  | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |      |       |       | Units |
|--------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|---------|----------------------------------------------------------|-------|------|-------|-------|-------|
|                                                                                                        |                                                                                 |         | 0.90V                                                    | 0.85V |      | 0.72V |       |       |
|                                                                                                        |                                                                                 |         | -3                                                       | -2    | -1   | -2    | -1    |       |
| SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM. |                                                                                 |         |                                                          |       |      |       |       |       |
| T <sub>ICKOF_FAR</sub>                                                                                 | Global clock input and output flip-flop <i>without</i> MMCM (far clock region). | XCKU3P  | 4.46                                                     | 5.30  | 5.70 | 6.74  | 7.19  | ns    |
|                                                                                                        |                                                                                 | XCKU5P  | 4.46                                                     | 5.30  | 5.70 | 6.74  | 7.19  | ns    |
|                                                                                                        |                                                                                 | XCKU9P  | 5.38                                                     | 6.49  | 6.97 | 8.29  | 8.81  | ns    |
|                                                                                                        |                                                                                 | XCKU11P | 6.18                                                     | 7.41  | 8.11 | 8.47  | 9.98  | ns    |
|                                                                                                        |                                                                                 | XCKU13P | 5.38                                                     | 6.49  | 6.96 | 8.30  | 8.83  | ns    |
|                                                                                                        |                                                                                 | XCKU15P | 6.21                                                     | 7.53  | 8.07 | 9.67  | 10.28 | ns    |

### Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 42: Global Clock Input to Output Delay With MMCM

| Symbol                                                                                       | Description                                               | Device  | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |      |       |      | Units |
|----------------------------------------------------------------------------------------------|-----------------------------------------------------------|---------|----------------------------------------------------------|-------|------|-------|------|-------|
|                                                                                              |                                                           |         | 0.90V                                                    | 0.85V |      | 0.72V |      |       |
|                                                                                              |                                                           |         | -3                                                       | -2    | -1   | -2    | -1   |       |
| SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM. |                                                           |         |                                                          |       |      |       |      |       |
| T <sub>ICKOFMMCMCC</sub>                                                                     | Global clock input and output flip-flop <i>with</i> MMCM. | XCKU3P  | 1.98                                                     | 1.98  | 2.17 | 2.67  | 2.81 | ns    |
|                                                                                              |                                                           | XCKU5P  | 1.98                                                     | 1.98  | 2.17 | 2.67  | 2.81 | ns    |
|                                                                                              |                                                           | XCKU9P  | 2.15                                                     | 2.15  | 2.36 | 2.89  | 3.04 | ns    |
|                                                                                              |                                                           | XCKU11P | 2.64                                                     | 2.64  | 2.96 | 3.31  | 3.71 | ns    |
|                                                                                              |                                                           | XCKU13P | 2.18                                                     | 2.18  | 2.38 | 2.93  | 3.08 | ns    |
|                                                                                              |                                                           | XCKU15P | 2.44                                                     | 2.44  | 2.66 | 3.26  | 3.41 | ns    |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

## Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in [Table 43](#) and [Table 44](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

**Table 43: Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM**

| Symbol                                                                                                      | Description                                                     | Device | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |       |       |       | Units |    |
|-------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|--------|----------------------------------------------------------|-------|-------|-------|-------|-------|----|
|                                                                                                             |                                                                 |        | 0.90V                                                    | 0.85V |       | 0.72V |       |       |    |
|                                                                                                             |                                                                 |        | -3                                                       | -2    | -1    | -2    | -1    |       |    |
| Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. <sup>(1)(2)(3)</sup> |                                                                 |        |                                                          |       |       |       |       |       |    |
| T <sub>PSFD_KU3P</sub>                                                                                      | Global clock input and input flip-flop (or latch) without MMCM. | Setup  | XCKU3P                                                   | 1.40  | 2.28  | 2.38  | 3.54  | 3.84  | ns |
| T <sub>PHFD_KU3P</sub>                                                                                      |                                                                 | Hold   |                                                          | −0.36 | −0.36 | −0.36 | −1.01 | −1.01 | ns |
| T <sub>PSFD_KU5P</sub>                                                                                      |                                                                 | Setup  | XCKU5P                                                   | 1.40  | 2.28  | 2.38  | 3.54  | 3.84  | ns |
| T <sub>PHFD_KU5P</sub>                                                                                      |                                                                 | Hold   |                                                          | −0.36 | −0.36 | −0.36 | −1.01 | −1.01 | ns |
| T <sub>PSFD_KU9P</sub>                                                                                      |                                                                 | Setup  | XCKU9P                                                   | 0.96  | 1.79  | 1.86  | 2.81  | 3.07  | ns |
| T <sub>PHFD_KU9P</sub>                                                                                      |                                                                 | Hold   |                                                          | −0.05 | −0.05 | −0.05 | −0.58 | −0.58 | ns |
| T <sub>PSFD_KU11P</sub>                                                                                     |                                                                 | Setup  | XCKU11P                                                  | 1.28  | 2.01  | 2.07  | 3.58  | 3.56  | ns |
| T <sub>PHFD_KU11P</sub>                                                                                     |                                                                 | Hold   |                                                          | −0.29 | −0.29 | −0.29 | −0.98 | −0.98 | ns |
| T <sub>PSFD_KU13P</sub>                                                                                     |                                                                 | Setup  | XCKU13P                                                  | 0.96  | 1.79  | 1.85  | 2.81  | 3.06  | ns |
| T <sub>PHFD_KU13P</sub>                                                                                     |                                                                 | Hold   |                                                          | −0.04 | −0.04 | −0.04 | −0.57 | −0.57 | ns |
| T <sub>PSFD_KU15P</sub>                                                                                     |                                                                 | Setup  | XCKU15P                                                  | 1.41  | 2.29  | 2.38  | 3.55  | 3.85  | ns |
| T <sub>PHFD_KU15P</sub>                                                                                     |                                                                 | Hold   |                                                          | −0.38 | −0.38 | −0.38 | −1.05 | −1.05 | ns |

### Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 44: Global Clock Input Setup and Hold With MMCM

| Symbol                                                                                                      | Description                                                  | Device | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |       |       |       | Units |    |
|-------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|--------|----------------------------------------------------------|-------|-------|-------|-------|-------|----|
|                                                                                                             |                                                              |        | 0.90V                                                    | 0.85V |       | 0.72V |       |       |    |
|                                                                                                             |                                                              |        | -3                                                       | -2    | -1    | -2    | -1    |       |    |
| Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. <sup>(1)(2)(3)</sup> |                                                              |        |                                                          |       |       |       |       |       |    |
| T <sub>PSMMCMCC_KU3P</sub>                                                                                  | Global clock input and input flip-flop (or latch) with MMCM. | Setup  | XCKU3P                                                   | 1.99  | 2.04  | 2.16  | 2.04  | 2.16  | ns |
| T <sub>PHMMCMCC_KU3P</sub>                                                                                  |                                                              | Hold   |                                                          | −0.17 | −0.17 | −0.17 | −0.17 | −0.17 | ns |
| T <sub>PSMMCMCC_KU5P</sub>                                                                                  |                                                              | Setup  | XCKU5P                                                   | 1.99  | 2.04  | 2.16  | 2.04  | 2.16  | ns |
| T <sub>PHMMCMCC_KU5P</sub>                                                                                  |                                                              | Hold   |                                                          | −0.17 | −0.17 | −0.17 | −0.17 | −0.17 | ns |
| T <sub>PSMMCMCC_KU9P</sub>                                                                                  |                                                              | Setup  | XCKU9P                                                   | 1.94  | 2.00  | 2.12  | 2.00  | 2.12  | ns |
| T <sub>PHMMCMCC_KU9P</sub>                                                                                  |                                                              | Hold   |                                                          | −0.11 | −0.11 | −0.11 | −0.11 | −0.11 | ns |
| T <sub>PSMMCMCC_KU11P</sub>                                                                                 |                                                              | Setup  | XCKU11P                                                  | 2.08  | 2.08  | 2.23  | 2.08  | 2.23  | ns |
| T <sub>PHMMCMCC_KU11P</sub>                                                                                 |                                                              | Hold   |                                                          | −0.05 | −0.05 | 0.04  | −0.18 | 0.14  | ns |
| T <sub>PSMMCMCC_KU13P</sub>                                                                                 |                                                              | Setup  | XCKU13P                                                  | 1.93  | 1.99  | 2.12  | 1.99  | 2.12  | ns |
| T <sub>PHMMCMCC_KU13P</sub>                                                                                 |                                                              | Hold   |                                                          | −0.10 | −0.10 | −0.10 | −0.20 | −0.20 | ns |
| T <sub>PSMMCMCC_KU15P</sub>                                                                                 |                                                              | Setup  | XCKU15P                                                  | 1.89  | 1.89  | 2.03  | 1.89  | 2.03  | ns |
| T <sub>PHMMCMCC_KU15P</sub>                                                                                 |                                                              | Hold   |                                                          | −0.16 | −0.16 | −0.16 | −0.19 | −0.24 | ns |

**Notes:**

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 45: Sampling Window

| Description                           | Speed Grade and V <sub>CCINT</sub> Operating Voltages |       |     |       |     | Units |
|---------------------------------------|-------------------------------------------------------|-------|-----|-------|-----|-------|
|                                       | 0.90V                                                 | 0.85V |     | 0.72V |     |       |
|                                       | -3                                                    | -2    | -1  | -2    | -1  |       |
| T <sub>SAMP_BUFG</sub> <sup>(1)</sup> | 510                                                   | 610   | 610 | 610   | 610 | ps    |
| T <sub>SAMP_NATIVE_DPA</sub>          | 100                                                   | 100   | 125 | 125   | 150 | ps    |
| T <sub>SAMP_NATIVE_BISC</sub>         | 60                                                    | 60    | 85  | 85    | 110 | ps    |

**Notes:**

- This parameter indicates the total sampling error of the Kintex UltraScale+ FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

## Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 46: Package Skew

| Symbol  | Description  | Device  | Package  | Value | Units |
|---------|--------------|---------|----------|-------|-------|
| PKGSKEW | Package Skew | XCKU3P  | SFVB784  | 75    | ps    |
|         |              |         | FFVA676  | 136   | ps    |
|         |              |         | FFVB676  | 69    | ps    |
|         |              |         | FFVD900  | 179   | ps    |
|         |              | XCKU5P  | SFVB784  | 75    | ps    |
|         |              |         | FFVA676  | 136   | ps    |
|         |              |         | FFVB676  | 69    | ps    |
|         |              |         | FFVD900  | 179   | ps    |
|         |              | XCKU9P  | FFVE900  | 212   | ps    |
|         |              | XCKU11P | FFVD900  |       | ps    |
|         |              |         | FFVA1156 |       | ps    |
|         |              |         | FFVE1517 |       | ps    |
|         |              | XCKU13P | FFVE900  | 197   | ps    |
|         |              | XCKU15P | FFVA1156 | 203   | ps    |
|         |              |         | FFVE1517 | 167   | ps    |
|         |              |         | FFVA1760 | 191   | ps    |
|         |              |         | FFVE1760 | 172   | ps    |

### Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

# GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Kintex UltraScale+ FPGAs that include the GTH transceivers.

## GTH Transceiver DC Input and Output Levels

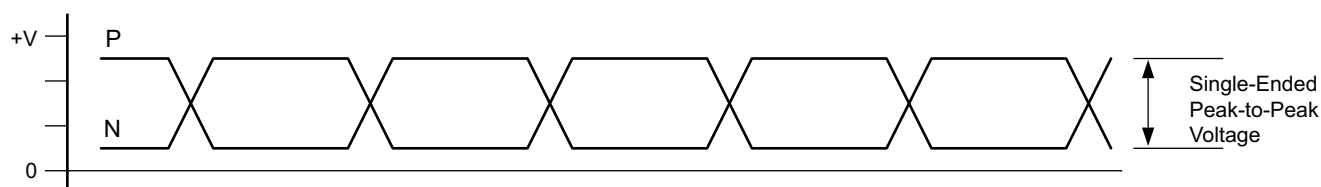
[Table 47](#) summarizes the DC specifications of the GTH transceivers in the Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further information.

**Table 47: GTH Transceiver DC Specifications**

| Symbol               | DC Parameter                                                               | Conditions                                                          | Min                                                                                        | Typ                      | Max                  | Units |
|----------------------|----------------------------------------------------------------------------|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------|--------------------------|----------------------|-------|
| DV <sub>PPIN</sub>   | Differential peak-to-peak input voltage (external AC coupled).             | > 10.3125 Gb/s                                                      | 150                                                                                        | –                        | 1250                 | mV    |
|                      |                                                                            | 6.6 Gb/s to 10.3125 Gb/s                                            | 150                                                                                        | –                        | 1250                 | mV    |
|                      |                                                                            | ≤ 6.6 Gb/s                                                          | 150                                                                                        | –                        | 2000                 | mV    |
| V <sub>IN</sub>      | Single-ended input voltage. Voltage measured at the pin referenced to GND. | DC coupled<br>V <sub>MGTAVTT</sub> = 1.2V                           | –400                                                                                       | –                        | V <sub>MGTAVTT</sub> | mV    |
| V <sub>CMIN</sub>    | Common mode input voltage.                                                 | DC coupled<br>V <sub>MGTAVTT</sub> = 1.2V                           | –                                                                                          | 2/3 V <sub>MGTAVTT</sub> | –                    | mV    |
| D <sub>VPPOUT</sub>  | Differential peak-to-peak output voltage. <sup>(1)</sup>                   | Transmitter output swing is set to 11111                            | 800                                                                                        | –                        | –                    | mV    |
| V <sub>CMOUTDC</sub> | Common mode output voltage: DC coupled (equation based).                   | When remote RX is terminated to GND                                 | $V_{MGTAVTT}/2 - D_{VPPOUT}/4$                                                             |                          |                      | mV    |
|                      |                                                                            | When remote RX termination is floating                              | $V_{MGTAVTT} - D_{VPPOUT}/2$                                                               |                          |                      | mV    |
|                      |                                                                            | When remote RX is terminated to V <sub>RX_TERM</sub> <sup>(2)</sup> | $V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left( \frac{V_{MGTAVTT} - V_{RX\_TERM}}{2} \right)$ |                          |                      | mV    |
| V <sub>CMOUTAC</sub> | Common mode output voltage: AC coupled (equation based).                   |                                                                     | $V_{MGTAVTT} - D_{VPPOUT}/2$                                                               |                          |                      | mV    |
| R <sub>IN</sub>      | Differential input resistance.                                             |                                                                     | –                                                                                          | 100                      | –                    | Ω     |
| R <sub>OUT</sub>     | Differential output resistance.                                            |                                                                     | –                                                                                          | 100                      | –                    | Ω     |
| T <sub>OSKEW</sub>   | Transmitter output pair (TXP and TXN) intra-pair skew (All packages).      |                                                                     | –                                                                                          | –                        | 10                   | ps    |
| C <sub>EXT</sub>     | Recommended external AC coupling capacitor. <sup>(3)</sup>                 |                                                                     | –                                                                                          | 100                      | –                    | nF    |

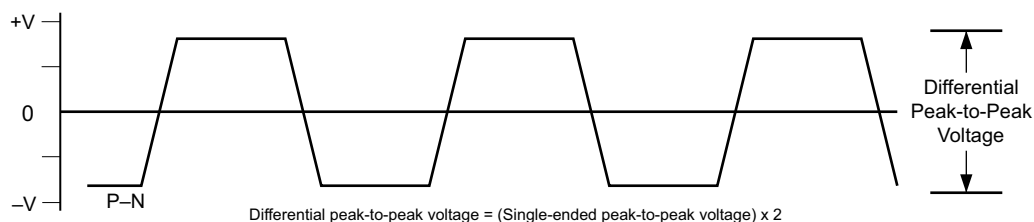
### Notes:

- The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)), and can result in values lower than reported in this table.
- V<sub>RX\_TERM</sub> is the remote RX termination voltage.
- Other values can be used as appropriate to conform to specific protocols and standards.



X16653-101316

Figure 3: Single-Ended Peak-to-Peak Voltage



X16639-101316

Figure 4: Differential Peak-to-Peak Voltage

Table 48 and Table 49 summarize the DC specifications of the GTH transceivers input and output clocks in Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further information.

Table 48: GTH Transceiver Clock DC Input Level Specification

| Symbol      | DC Parameter                             | Min | Typ | Max  | Units    |
|-------------|------------------------------------------|-----|-----|------|----------|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage. | 250 | –   | 2000 | mV       |
| $R_{IN}$    | Differential input resistance.           | –   | 100 | –    | $\Omega$ |
| $C_{EXT}$   | Required external AC coupling capacitor. | –   | 10  | –    | nF       |

Table 49: GTH Transceiver Clock Output Level Specification

| Symbol      | Description                                                        | Conditions                               | Min | Typ | Max | Units |
|-------------|--------------------------------------------------------------------|------------------------------------------|-----|-----|-----|-------|
| $V_{OL}$    | Output Low voltage for P and N.                                    | $R_T = 100\Omega$ across P and N signals | 100 | –   | 330 | mV    |
| $V_{OH}$    | Output High voltage for P and N.                                   | $R_T = 100\Omega$ across P and N signals | 500 | –   | 700 | mV    |
| $V_{DDOUT}$ | Differential output voltage.<br>(P–N), P = High<br>(N–P), N = High | $R_T = 100\Omega$ across P and N signals | 300 | –   | 430 | mV    |
| $V_{CMOUT}$ | Common mode voltage.                                               | $R_T = 100\Omega$ across P and N signals | 300 | –   | 500 | mV    |

# GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further information.

Table 50: GTH Transceiver Performance

| Symbol                   | Description                           | Output<br>Divider | Speed Grade and V <sub>CCINT</sub> Operating Voltages |        |        |        |        |        |        |        |         |         | Units |
|--------------------------|---------------------------------------|-------------------|-------------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|---------|---------|-------|
|                          |                                       |                   | 0.90V                                                 |        | 0.85V  |        |        |        | 0.72V  |        |         |         |       |
|                          |                                       |                   | -3                                                    |        | -2     |        | -1     |        | -2     |        | -1      |         |       |
| F <sub>GTHMAX</sub>      | GTH maximum line rate.                |                   | 16.375                                                |        | 16.375 |        | 12.5   |        | 12.5   |        | 10.3125 |         | Gb/s  |
| F <sub>GTHMIN</sub>      | GTH minimum line rate.                |                   | 0.5                                                   |        | 0.5    |        | 0.5    |        | 0.5    |        | 0.5     |         | Gb/s  |
|                          |                                       |                   | Min                                                   | Max    | Min    | Max    | Min    | Max    | Min    | Max    | Min     | Max     |       |
| F <sub>GTHCRANGE</sub>   | CPLL line rate range. <sup>(1)</sup>  | 1                 | 4                                                     | 12.5   | 4      | 12.5   | 4      | 8.5    | 4      | 8.5    | 4       | 8.5     | Gb/s  |
|                          |                                       | 2                 | 2                                                     | 6.25   | 2      | 6.25   | 2      | 4.25   | 2      | 4.25   | 2       | 4.25    | Gb/s  |
|                          |                                       | 4                 | 1                                                     | 3.125  | 1      | 3.125  | 1      | 2.125  | 1      | 2.125  | 1       | 2.125   | Gb/s  |
|                          |                                       | 8                 | 0.5                                                   | 1.5625 | 0.5    | 1.5625 | 0.5    | 1.0625 | 0.5    | 1.0625 | 0.5     | 1.0625  | Gb/s  |
|                          |                                       | 16                | N/A                                                   |        |        |        |        |        |        |        |         |         | Gb/s  |
|                          |                                       |                   | Min                                                   | Max    | Min    | Max    | Min    | Max    | Min    | Max    | Min     | Max     |       |
| F <sub>GTHQRANGE1</sub>  | QPLL0 line rate range. <sup>(2)</sup> | 1                 | 9.8                                                   | 16.375 | 9.8    | 16.375 | 9.8    | 12.5   | 9.8    | 12.5   | 9.8     | 10.3125 | Gb/s  |
|                          |                                       | 2                 | 4.9                                                   | 8.1875 | 4.9    | 8.1875 | 4.9    | 8.15   | 4.9    | 8.1875 | 4.9     | 8.15    | Gb/s  |
|                          |                                       | 4                 | 2.45                                                  | 4.0938 | 2.45   | 4.0938 | 2.45   | 4.075  | 2.45   | 4.0938 | 2.45    | 4.075   | Gb/s  |
|                          |                                       | 8                 | 1.225                                                 | 2.0469 | 1.225  | 2.0469 | 1.225  | 2.0375 | 1.225  | 2.0469 | 1.225   | 2.0375  | Gb/s  |
|                          |                                       | 16                | 0.6125                                                | 1.0234 | 0.6125 | 1.0234 | 0.6125 | 1.0188 | 0.6125 | 1.0234 | 0.6125  | 1.0188  | Gb/s  |
|                          |                                       |                   | Min                                                   | Max    | Min    | Max    | Min    | Max    | Min    | Max    | Min     | Max     |       |
| F <sub>GTHQRANGE2</sub>  | QPLL1 line rate range. <sup>(3)</sup> | 1                 | 8.0                                                   | 13     | 8.0    | 13     | 8.0    | 12.5   | 8.0    | 12.5   | 8.0     | 10.3125 | Gb/s  |
|                          |                                       | 2                 | 4.0                                                   | 6.5    | 4.0    | 6.5    | 4.0    | 6.5    | 4.0    | 6.5    | 4.0     | 6.5     | Gb/s  |
|                          |                                       | 4                 | 2.0                                                   | 3.25   | 2.0    | 3.25   | 2.0    | 3.25   | 2.0    | 3.25   | 2.0     | 3.25    | Gb/s  |
|                          |                                       | 8                 | 1.0                                                   | 1.625  | 1.0    | 1.625  | 1.0    | 1.625  | 1.0    | 1.625  | 1.0     | 1.625   | Gb/s  |
|                          |                                       | 16                | 0.5                                                   | 0.8125 | 0.5    | 0.8125 | 0.5    | 0.8125 | 0.5    | 0.8125 | 0.5     | 0.8125  | Gb/s  |
|                          |                                       |                   | Min                                                   | Max    | Min    | Max    | Min    | Max    | Min    | Max    | Min     | Max     |       |
| F <sub>CPLL</sub> RANGE  | CPLL frequency range.                 |                   | 2                                                     | 6.25   | 2      | 6.25   | 2      | 4.25   | 2      | 4.25   | 2       | 4.25    | GHz   |
| F <sub>QPLL0</sub> RANGE | QPLL0 frequency range.                |                   | 9.8                                                   | 16.375 | 9.8    | 16.375 | 9.8    | 16.375 | 9.8    | 16.375 | 9.8     | 16.375  | GHz   |
| F <sub>QPLL1</sub> RANGE | QPLL1 frequency range.                |                   | 8                                                     | 13     | 8      | 13     | 8      | 13     | 8      | 13     | 8       | 13      | GHz   |

## Notes:

- The values listed are the rounded results of the calculated equation  $(2 \times \text{CPLL\_Frequency}) / \text{Output\_Divider}$ .
- The values listed are the rounded results of the calculated equation  $(\text{QPLL0\_Frequency}) / \text{Output\_Divider}$ .
- The values listed are the rounded results of the calculated equation  $(\text{QPLL1\_Frequency}) / \text{Output\_Divider}$ .

Table 51: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol                 | Description                  | All Speed Grades | Units |
|------------------------|------------------------------|------------------|-------|
| F <sub>GTHDRPCLK</sub> | GTHDRPCLK maximum frequency. | 250              | MHz   |

Table 52: GTH Transceiver Reference Clock Switching Characteristics

| Symbol             | Description                      | Conditions           | All Speed Grades |     |     | Units |
|--------------------|----------------------------------|----------------------|------------------|-----|-----|-------|
|                    |                                  |                      | Min              | Typ | Max |       |
| F <sub>GCLK</sub>  | Reference clock frequency range. |                      | 60               | –   | 820 | MHz   |
| T <sub>RCLK</sub>  | Reference clock rise time.       | 20% – 80%            | –                | 200 | –   | ps    |
| T <sub>FCLK</sub>  | Reference clock fall time.       | 80% – 20%            | –                | 200 | –   | ps    |
| T <sub>DCREF</sub> | Reference clock duty cycle.      | Transceiver PLL only | 40               | 50  | 60  | %     |

Table 53: GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask

| Symbol                                       | Description                                                                          | Offset Frequency | Min | Typ | Max  | Units  |
|----------------------------------------------|--------------------------------------------------------------------------------------|------------------|-----|-----|------|--------|
| QPLL <sub>REFCLKMASK</sub> <sup>(1)(2)</sup> | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz. | 10 kHz           | –   | –   | –105 | dBc/Hz |
|                                              |                                                                                      | 100 kHz          | –   | –   | –124 |        |
|                                              |                                                                                      | 1 MHz            | –   | –   | –130 |        |
| CPLL <sub>REFCLKMASK</sub> <sup>(1)(2)</sup> | CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.        | 10 kHz           | –   | –   | –105 | dBc/Hz |
|                                              |                                                                                      | 100 kHz          | –   | –   | –124 |        |
|                                              |                                                                                      | 1 MHz            | –   | –   | –130 |        |
|                                              |                                                                                      | 50 MHz           | –   | –   | –140 |        |

**Notes:**

- For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by  $20 \times \log(N/312.5)$  where N is the new reference clock frequency in MHz.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 54: GTH Transceiver PLL/Lock Time Adaptation

| Symbol             | Description                                                                                             | Conditions                                                                                                                                        | All Speed Grades |        |                   | Units |
|--------------------|---------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------|-------------------|-------|
|                    |                                                                                                         |                                                                                                                                                   | Min              | Typ    | Max               |       |
| T <sub>LOCK</sub>  | Initial PLL lock.                                                                                       |                                                                                                                                                   | –                | –      | 1                 | ms    |
| T <sub>DLOCK</sub> | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).             | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | –                | 50,000 | $37 \times 10^6$  | UI    |
|                    | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled. |                                                                                                                                                   | –                | 50,000 | $2.3 \times 10^6$ | UI    |

Table 55: GTH Transceiver User Clock Switching Characteristics<sup>(1)</sup>

| Symbol                | Description                                        | Data Width Conditions (Bit) |                    | Speed Grade, Temperature Ranges, and V <sub>CCINT</sub> Operating Voltages |          |          |         |          | Units |
|-----------------------|----------------------------------------------------|-----------------------------|--------------------|----------------------------------------------------------------------------|----------|----------|---------|----------|-------|
|                       |                                                    |                             |                    | 0.90V                                                                      | 0.85V    |          | 0.72V   |          |       |
|                       |                                                    | Internal Logic              | Interconnect Logic | -3(2)                                                                      | -2(2)(3) | -1(4)(5) | -2(3)   | -1(3)(5) |       |
| F <sub>TXOUTPMA</sub> | TXOUTCLK maximum frequency sourced from OUTCLKPMA. |                             |                    | 511.719                                                                    | 511.719  | 390.625  | 390.625 | 322.266  | MHz   |
| F <sub>RXOUTPMA</sub> | RXOUTCLK maximum frequency sourced from OUTCLKPMA. |                             |                    | 511.719                                                                    | 511.719  | 390.625  | 390.625 | 322.266  | MHz   |

Table 55: GTH Transceiver User Clock Switching Characteristics<sup>(1)</sup> (Cont'd)

| Symbol                    | Description                                           | Data Width Conditions (Bit) |                    | Speed Grade, Temperature Ranges, and V <sub>CCINT</sub> Operating Voltages |                      |                      |                   |                      | Units |
|---------------------------|-------------------------------------------------------|-----------------------------|--------------------|----------------------------------------------------------------------------|----------------------|----------------------|-------------------|----------------------|-------|
|                           |                                                       |                             |                    | 0.90V                                                                      | 0.85V                |                      | 0.72V             |                      |       |
|                           |                                                       | Internal Logic              | Interconnect Logic | -3 <sup>(2)</sup>                                                          | -2 <sup>(2)(3)</sup> | -1 <sup>(4)(5)</sup> | -2 <sup>(3)</sup> | -1 <sup>(3)(5)</sup> |       |
| F <sub>TXOUTPROGDIV</sub> | TXOUTCLK maximum frequency sourced from TXPROGDIVCLK. |                             | 511.719            | 511.719                                                                    | 511.719              | 511.719              | 511.719           | MHz                  |       |
| F <sub>RXOUTPROGDIV</sub> | RXOUTCLK maximum frequency sourced from RXPROGDIVCLK. |                             | 511.719            | 511.719                                                                    | 511.719              | 511.719              | 511.719           | MHz                  |       |
| F <sub>TXIN</sub>         | TXUSRCLK <sup>(6)</sup> maximum frequency             | 16                          | 16, 32             | 511.719                                                                    | 511.719              | 390.625              | 390.625           | 322.266              | MHz   |
|                           |                                                       | 32                          | 32, 64             | 511.719                                                                    | 511.719              | 390.625              | 390.625           | 322.266              | MHz   |
|                           |                                                       | 20                          | 20, 40             | 409.375                                                                    | 409.375              | 312.500              | 312.500           | 257.813              | MHz   |
|                           |                                                       | 40                          | 40, 80             | 409.375                                                                    | 409.375              | 312.500              | 312.500           | 257.813              | MHz   |
| F <sub>RXIN</sub>         | RXUSRCLK <sup>(6)</sup> maximum frequency             | 16                          | 16, 32             | 511.719                                                                    | 511.719              | 390.625              | 390.625           | 322.266              | MHz   |
|                           |                                                       | 32                          | 32, 64             | 511.719                                                                    | 511.719              | 390.625              | 390.625           | 322.266              | MHz   |
|                           |                                                       | 20                          | 20, 40             | 409.375                                                                    | 409.375              | 312.500              | 312.500           | 257.813              | MHz   |
|                           |                                                       | 40                          | 40, 80             | 409.375                                                                    | 409.375              | 312.500              | 312.500           | 257.813              | MHz   |
| F <sub>TXIN2</sub>        | TXUSRCLK2 <sup>(6)</sup> maximum frequency            | 16                          | 16                 | 511.719                                                                    | 511.719              | 390.625              | 390.625           | 322.266              | MHz   |
|                           |                                                       | 16                          | 32                 | 255.859                                                                    | 255.859              | 195.313              | 195.313           | 161.133              | MHz   |
|                           |                                                       | 32                          | 32                 | 511.719                                                                    | 511.719              | 390.625              | 390.625           | 322.266              | MHz   |
|                           |                                                       | 32                          | 64                 | 255.859                                                                    | 255.859              | 195.313              | 195.313           | 161.133              | MHz   |
|                           |                                                       | 20                          | 20                 | 409.375                                                                    | 409.375              | 312.500              | 312.500           | 257.813              | MHz   |
|                           |                                                       | 20                          | 40                 | 204.688                                                                    | 204.688              | 156.250              | 156.250           | 128.906              | MHz   |
|                           |                                                       | 40                          | 40                 | 409.375                                                                    | 409.375              | 312.500              | 312.500           | 257.813              | MHz   |
|                           |                                                       | 40                          | 80                 | 204.688                                                                    | 204.688              | 156.250              | 156.250           | 128.906              | MHz   |
| F <sub>RXIN2</sub>        | RXUSRCLK2 <sup>(6)</sup> maximum frequency            | 16                          | 16                 | 511.719                                                                    | 511.719              | 390.625              | 390.625           | 322.266              | MHz   |
|                           |                                                       | 16                          | 32                 | 255.859                                                                    | 255.859              | 195.313              | 195.313           | 161.133              | MHz   |
|                           |                                                       | 32                          | 32                 | 511.719                                                                    | 511.719              | 390.625              | 390.625           | 322.266              | MHz   |
|                           |                                                       | 32                          | 64                 | 255.859                                                                    | 255.859              | 195.313              | 195.313           | 161.133              | MHz   |
|                           |                                                       | 20                          | 20                 | 409.375                                                                    | 409.375              | 312.500              | 312.500           | 257.813              | MHz   |
|                           |                                                       | 20                          | 40                 | 204.688                                                                    | 204.688              | 156.250              | 156.250           | 128.906              | MHz   |
|                           |                                                       | 40                          | 40                 | 409.375                                                                    | 409.375              | 312.500              | 312.500           | 257.813              | MHz   |
|                           |                                                       | 40                          | 80                 | 204.688                                                                    | 204.688              | 156.250              | 156.250           | 128.906              | MHz   |

#### Notes:

- Clocking must be implemented as described in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)).
- For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
- For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V<sub>CCINT</sub> = 0.85V or 6.25 Gb/s when V<sub>CCINT</sub> = 0.72V.
- For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
- For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V<sub>CCINT</sub> = 0.85V or 5.15625 Gb/s when V<sub>CCINT</sub> = 0.72V.
- When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)).

Table 56: GTH Transceiver Transmitter Switching Characteristics

| Symbol                     | Description                            | Condition                | Min   | Typ | Max                 | Units |
|----------------------------|----------------------------------------|--------------------------|-------|-----|---------------------|-------|
| F <sub>GTHTX</sub>         | Serial data rate range                 |                          | 0.500 | –   | F <sub>GTHMAX</sub> | Gb/s  |
| T <sub>RTX</sub>           | TX rise time                           | 20%–80%                  | –     | 21  | –                   | ps    |
| T <sub>FTX</sub>           | TX fall time                           | 80%–20%                  | –     | 21  | –                   | ps    |
| T <sub>LLSKEW</sub>        | TX lane-to-lane skew <sup>(1)</sup>    |                          | –     | –   | 500.00              | ps    |
| T <sub>J16.375</sub>       | Total jitter <sup>(2)(4)</sup>         | 16.375 Gb/s              | –     | –   | 0.28                | UI    |
| D <sub>J16.375</sub>       | Deterministic jitter <sup>(2)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J15.0</sub>         | Total jitter <sup>(2)(4)</sup>         | 15.0 Gb/s                | –     | –   | 0.28                | UI    |
| D <sub>J15.0</sub>         | Deterministic jitter <sup>(2)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J14.1</sub>         | Total jitter <sup>(2)(4)</sup>         | 14.1 Gb/s                | –     | –   | 0.28                | UI    |
| D <sub>J14.1</sub>         | Deterministic jitter <sup>(2)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J14.1</sub>         | Total jitter <sup>(2)(4)</sup>         | 14.025 Gb/s              | –     | –   | 0.28                | UI    |
| D <sub>J14.1</sub>         | Deterministic jitter <sup>(2)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J13.1</sub>         | Total jitter <sup>(2)(4)</sup>         | 13.1 Gb/s                | –     | –   | 0.28                | UI    |
| D <sub>J13.1</sub>         | Deterministic jitter <sup>(2)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J12.5_QPLL</sub>    | Total jitter <sup>(2)(4)</sup>         | 12.5 Gb/s                | –     | –   | 0.28                | UI    |
| D <sub>J12.5_QPLL</sub>    | Deterministic jitter <sup>(2)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J12.5_CPLL</sub>    | Total jitter <sup>(3)(4)</sup>         | 12.5 Gb/s                | –     | –   | 0.33                | UI    |
| D <sub>J12.5_CPLL</sub>    | Deterministic jitter <sup>(3)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J11.3_QPLL</sub>    | Total jitter <sup>(2)(4)</sup>         | 11.3 Gb/s                | –     | –   | 0.28                | UI    |
| D <sub>J11.3_QPLL</sub>    | Deterministic jitter <sup>(2)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J10.3125_QPLL</sub> | Total jitter <sup>(2)(4)</sup>         | 10.3125 Gb/s             | –     | –   | 0.28                | UI    |
| D <sub>J10.3125_QPLL</sub> | Deterministic jitter <sup>(2)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J10.3125_CPLL</sub> | Total jitter <sup>(3)(4)</sup>         | 10.3125 Gb/s             | –     | –   | 0.33                | UI    |
| D <sub>J10.3125_CPLL</sub> | Deterministic jitter <sup>(3)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J9.953_QPLL</sub>   | Total jitter <sup>(2)(4)</sup>         | 9.953 Gb/s               | –     | –   | 0.28                | UI    |
| D <sub>J9.953_QPLL</sub>   | Deterministic jitter <sup>(2)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J9.953_CPLL</sub>   | Total jitter <sup>(3)(4)</sup>         | 9.953 Gb/s               | –     | –   | 0.33                | UI    |
| D <sub>J9.953_CPLL</sub>   | Deterministic jitter <sup>(3)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J8.0</sub>          | Total jitter <sup>(3)(4)</sup>         | 8.0 Gb/s                 | –     | –   | 0.32                | UI    |
| D <sub>J8.0</sub>          | Deterministic jitter <sup>(3)(4)</sup> |                          | –     | –   | 0.17                | UI    |
| T <sub>J6.6</sub>          | Total jitter <sup>(3)(4)</sup>         | 6.6 Gb/s                 | –     | –   | 0.30                | UI    |
| D <sub>J6.6</sub>          | Deterministic jitter <sup>(3)(4)</sup> |                          | –     | –   | 0.15                | UI    |
| T <sub>J5.0</sub>          | Total jitter <sup>(3)(4)</sup>         | 5.0 Gb/s                 | –     | –   | 0.30                | UI    |
| D <sub>J5.0</sub>          | Deterministic jitter <sup>(3)(4)</sup> |                          | –     | –   | 0.15                | UI    |
| T <sub>J4.25</sub>         | Total jitter <sup>(3)(4)</sup>         | 4.25 Gb/s                | –     | –   | 0.30                | UI    |
| D <sub>J4.25</sub>         | Deterministic jitter <sup>(3)(4)</sup> |                          | –     | –   | 0.15                | UI    |
| T <sub>J4.0</sub>          | Total jitter <sup>(3)(4)</sup>         | 4.0 Gb/s                 | –     | –   | 0.32                | UI    |
| D <sub>J4.0</sub>          | Deterministic jitter <sup>(3)(4)</sup> |                          | –     | –   | 0.16                | UI    |
| T <sub>J3.20</sub>         | Total jitter <sup>(3)(4)</sup>         | 3.20 Gb/s <sup>(5)</sup> | –     | –   | 0.20                | UI    |
| D <sub>J3.20</sub>         | Deterministic jitter <sup>(3)(4)</sup> |                          | –     | –   | 0.10                | UI    |

Table 56: GTH Transceiver Transmitter Switching Characteristics (Cont'd)

| Symbol             | Description                            | Condition                | Min | Typ | Max  | Units |
|--------------------|----------------------------------------|--------------------------|-----|-----|------|-------|
| T <sub>J2.5</sub>  | Total jitter <sup>(3)(4)</sup>         | 2.5 Gb/s <sup>(6)</sup>  | –   | –   | 0.20 | UI    |
| D <sub>J2.5</sub>  | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.10 | UI    |
| T <sub>J1.25</sub> | Total jitter <sup>(3)(4)</sup>         | 1.25 Gb/s <sup>(7)</sup> | –   | –   | 0.15 | UI    |
| D <sub>J1.25</sub> | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.06 | UI    |
| T <sub>J500</sub>  | Total jitter <sup>(3)(4)</sup>         | 500 Mb/s <sup>(8)</sup>  | –   | –   | 0.10 | UI    |
| D <sub>J500</sub>  | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.03 | UI    |

**Notes:**

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at the maximum line rate.
- Using QPLL\_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL\_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10<sup>-12</sup>.
- CPLL frequency at 3.2 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT\_DIV = 8.

Table 57: GTH Transceiver Receiver Switching Characteristics

| Symbol                             | Description                                      | Condition                           | Min   | Typ | Max                 | Units |
|------------------------------------|--------------------------------------------------|-------------------------------------|-------|-----|---------------------|-------|
| F <sub>GTHRX</sub>                 | Serial data rate                                 |                                     | 0.500 | –   | F <sub>GTHMAX</sub> | Gb/s  |
| R <sub>XSSST</sub>                 | Receiver spread-spectrum tracking <sup>(1)</sup> | Modulated at 33 kHz                 | –5000 | –   | 0                   | ppm   |
| R <sub>XRL</sub>                   | Run length (CID)                                 |                                     | –     | –   | 256                 | UI    |
| R <sub>XPMTOL</sub>                | Data/REFCLK PPM offset tolerance                 | Bit rates ≤ 6.6 Gb/s                | –1250 | –   | 1250                | ppm   |
|                                    |                                                  | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700  | –   | 700                 | ppm   |
|                                    |                                                  | Bit rates > 8.0 Gb/s                | –200  | –   | 200                 | ppm   |
| SJ Jitter Tolerance <sup>(2)</sup> |                                                  |                                     |       |     |                     |       |
| J <sub>T_SJ16.375</sub>            | Sinusoidal jitter (QPLL) <sup>(3)</sup>          | 16.375 Gb/s                         | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ15.1</sub>              | Sinusoidal jitter (QPLL) <sup>(3)</sup>          | 15.1 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ14.1</sub>              | Sinusoidal jitter (QPLL) <sup>(3)</sup>          | 14.1 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ13.1</sub>              | Sinusoidal jitter (QPLL) <sup>(3)</sup>          | 13.1 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ12.5</sub>              | Sinusoidal jitter (QPLL) <sup>(3)</sup>          | 12.5 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ11.3</sub>              | Sinusoidal jitter (QPLL) <sup>(3)</sup>          | 11.3 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ10.32_QPLL</sub>        | Sinusoidal jitter (QPLL) <sup>(3)</sup>          | 10.32 Gb/s                          | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ10.32_CPLL</sub>        | Sinusoidal jitter (CPLL) <sup>(3)</sup>          | 10.32 Gb/s                          | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ9.953_QPLL</sub>        | Sinusoidal jitter (QPLL) <sup>(3)</sup>          | 9.953 Gb/s                          | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ9.953_CPLL</sub>        | Sinusoidal jitter (CPLL) <sup>(3)</sup>          | 9.953 Gb/s                          | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ8.0</sub>               | Sinusoidal jitter (QPLL) <sup>(3)</sup>          | 8.0 Gb/s                            | 0.42  | –   | –                   | UI    |
| J <sub>T_SJ6.6_CPLL</sub>          | Sinusoidal jitter (CPLL) <sup>(3)</sup>          | 6.6 Gb/s                            | 0.44  | –   | –                   | UI    |
| J <sub>T_SJ5.0</sub>               | Sinusoidal jitter (CPLL) <sup>(3)</sup>          | 5.0 Gb/s                            | 0.44  | –   | –                   | UI    |
| J <sub>T_SJ4.25</sub>              | Sinusoidal jitter (CPLL) <sup>(3)</sup>          | 4.25 Gb/s                           | 0.44  | –   | –                   | UI    |
| J <sub>T_SJ3.2</sub>               | Sinusoidal jitter (CPLL) <sup>(3)</sup>          | 3.2 Gb/s <sup>(4)</sup>             | 0.45  | –   | –                   | UI    |

Table 57: GTH Transceiver Receiver Switching Characteristics (Cont'd)

| Symbol                                                     | Description                                        | Condition                | Min  | Typ | Max | Units |
|------------------------------------------------------------|----------------------------------------------------|--------------------------|------|-----|-----|-------|
| J <sub>T_SJ2.5</sub>                                       | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 2.5 Gb/s <sup>(5)</sup>  | 0.30 | –   | –   | UI    |
| J <sub>T_SJ1.25</sub>                                      | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 1.25 Gb/s <sup>(6)</sup> | 0.30 | –   | –   | UI    |
| J <sub>T_SJ500</sub>                                       | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 500 Mb/s <sup>(7)</sup>  | 0.30 | –   | –   | UI    |
| <b>SJ Jitter Tolerance with Stressed Eye<sup>(2)</sup></b> |                                                    |                          |      |     |     |       |
| J <sub>T_TJSE3.2</sub>                                     | Total jitter with stressed eye <sup>(8)</sup>      | 3.2 Gb/s                 | 0.70 | –   | –   | UI    |
| J <sub>T_TJSE6.6</sub>                                     |                                                    | 6.6 Gb/s                 | 0.70 | –   | –   | UI    |
| J <sub>T_SJSE3.2</sub>                                     | Sinusoidal jitter with stressed eye <sup>(8)</sup> | 3.2 Gb/s                 | 0.10 | –   | –   | UI    |
| J <sub>T_SJSE6.6</sub>                                     |                                                    | 6.6 Gb/s                 | 0.10 | –   | –   | UI    |

**Notes:**

1. Using RXOUT\_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10<sup>-12</sup>.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT\_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT\_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT\_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT\_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

## GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 58](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 58: GTH Transceiver Protocol List

| Protocol                      | Specification                                    | Serial Rate (Gb/s) | Electrical Compliance |
|-------------------------------|--------------------------------------------------|--------------------|-----------------------|
| CAUI-10                       | IEEE 802.3-2012                                  | 10.3125            | Compliant             |
| nPPI                          | IEEE 802.3-2012                                  | 10.3125            | Compliant             |
| 10GBASE-KR <sup>(1)</sup>     | IEEE 802.3-2012                                  | 10.3125            | Compliant             |
| 40GBASE-KR                    | IEEE 802.3-2012                                  | 10.3125            | Compliant             |
| SFP+                          | SFF-8431 (SR and LR)                             | 9.95328–11.10      | Compliant             |
| XFP                           | INF-8077i, revision 4.5                          | 10.3125            | Compliant             |
| RXAUI                         | CEI-6G-SR                                        | 6.25               | Compliant             |
| XAUI                          | IEEE 802.3-2012                                  | 3.125              | Compliant             |
| 1000BASE-X                    | IEEE 802.3-2012                                  | 1.25               | Compliant             |
| 5.0G Ethernet                 | IEEE 802.3bx (PAR)                               | 5                  | Compliant             |
| 2.5G Ethernet                 | IEEE 802.3bx (PAR)                               | 2.5                | Compliant             |
| HiGig, HiGig+, HiGig2         | IEEE 802.3-2012                                  | 3.74, 6.6          | Compliant             |
| OTU2                          | ITU G.8251                                       | 10.709225          | Compliant             |
| OTU4 (OTL4.10)                | OIF-CEI-11G-SR                                   | 11.180997          | Compliant             |
| OC-3/12/48/192                | GR-253-CORE                                      | 0.1555–9.956       | Compliant             |
| TFI-5                         | OIF-TFI5-0.1.0                                   | 2.488              | Compliant             |
| Interlaken                    | OIF-CEI-6G, OIF-CEI-11G-SR                       | 4.25–12.5          | Compliant             |
| PCIe Gen1, 2, 3               | PCI Express base 3.0                             | 2.5, 5.0, and 8.0  | Compliant             |
| SDI <sup>(2)</sup>            | SMPTE 424M-2006                                  | 0.27–2.97          | Compliant             |
| UHD-SDI <sup>(2)</sup>        | SMPTE ST-2081 6G, SMPTE ST-2082 12G              | 6 and 12           | Compliant             |
| Hybrid memory cube (HMC)      | HMC-15G-SR                                       | 10, 12.5, and 15.0 | Compliant             |
| MoSys Bandwidth Engine        | CEI-11-SR and CEI-11-SR (overclocked)            | 10.3125, 15.5      | Compliant             |
| CPRI                          | CPRI_v_6_1_2014-07-01                            | 0.6144–12.165      | Compliant             |
| HDMI <sup>(2)</sup>           | HDMI 2.0                                         | All                | Compliant             |
| Passive optical network (PON) | 10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON | 0.155–10.3125      | Compliant             |
| JESD204a/b                    | OIF-CEI-6G, OIF-CEI-11G                          | 3.125–12.5         | Compliant             |
| Serial RapidIO                | RapidIO specification 3.1                        | 1.25–10.3125       | Compliant             |
| DisplayPort <sup>(2)</sup>    | DP 1.2B CTS                                      | 1.62–5.4           | Compliant             |
| Fibre channel                 | FC-PH-4                                          | 1.0625–14.025      | Compliant             |
| SATA Gen1, 2, 3               | Serial ATA revision 3.0 specification            | 1.5, 3.0, and 6.0  | Compliant             |
| SAS Gen1, 2, 3                | T10/BSR INCITS 519                               | 3.0, 6.0, and 12.0 | Compliant             |
| SFI-5                         | OIF-SFI5-01.0                                    | 0.625–12.5         | Compliant             |
| Aurora                        | CEI-6G, CEI-11G-LR                               | up to 11.180997    | Compliant             |

**Notes:**

1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

# GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Kintex UltraScale+ FPGAs that include the GTY transceivers.

## GTY Transceiver DC Input and Output Levels

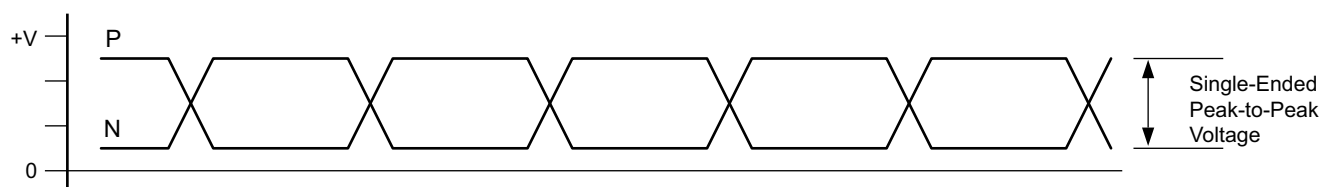
[Table 59](#) and [Table 60](#) summarize the DC specifications of the GTY transceivers in Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further information.

**Table 59: GTY Transceiver DC Specifications**

| Symbol               | DC Parameter                                                               | Conditions                                                          | Min                                                                                        | Typ                      | Max                  | Units |
|----------------------|----------------------------------------------------------------------------|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------|--------------------------|----------------------|-------|
| DV <sub>PPIN</sub>   | Differential peak-to-peak input voltage (external AC coupled)              | > 10.3125 Gb/s                                                      | 150                                                                                        | –                        | 1250                 | mV    |
|                      |                                                                            | 6.6 Gb/s to 10.3125 Gb/s                                            | 150                                                                                        | –                        | 1250                 | mV    |
|                      |                                                                            | ≤ 6.6 Gb/s                                                          | 150                                                                                        | –                        | 2000                 | mV    |
| V <sub>IN</sub>      | Single-ended input voltage. Voltage measured at the pin referenced to GND. | DC coupled<br>V <sub>MGTAVTT</sub> = 1.2V                           | –400                                                                                       | –                        | V <sub>MGTAVTT</sub> | mV    |
| V <sub>CMIN</sub>    | Common mode input voltage                                                  | DC coupled<br>V <sub>MGTAVTT</sub> = 1.2V                           | –                                                                                          | 2/3 V <sub>MGTAVTT</sub> | –                    | mV    |
| D <sub>VPPOUT</sub>  | Differential peak-to-peak output voltage <sup>(1)</sup>                    | Transmitter output swing is set to 11111                            | 800                                                                                        | –                        | –                    | mV    |
| V <sub>CMOUTDC</sub> | Common mode output voltage: DC coupled (equation based)                    | When remote RX is terminated to GND                                 | $V_{MGTAVTT}/2 - D_{VPPOUT}/4$                                                             |                          |                      | mV    |
|                      |                                                                            | When remote RX termination is floating                              | $V_{MGTAVTT} - D_{VPPOUT}/2$                                                               |                          |                      | mV    |
|                      |                                                                            | When remote RX is terminated to V <sub>RX_TERM</sub> <sup>(2)</sup> | $V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left( \frac{V_{MGTAVTT} - V_{RX\_TERM}}{2} \right)$ |                          |                      | mV    |
| V <sub>CMOUTAC</sub> | Common mode output voltage: AC coupled                                     | Equation based                                                      | $V_{MGTAVTT} - D_{VPPOUT}/2$                                                               |                          |                      | mV    |
| R <sub>IN</sub>      | Differential input resistance                                              |                                                                     | –                                                                                          | 100                      | –                    | Ω     |
| R <sub>OUT</sub>     | Differential output resistance                                             |                                                                     | –                                                                                          | 100                      | –                    | Ω     |
| T <sub>OSKEW</sub>   | Transmitter output pair (TXP and TXN) intra-pair skew                      |                                                                     | –                                                                                          | –                        | 10                   | ps    |
| C <sub>EXT</sub>     | Recommended external AC coupling capacitor <sup>(3)</sup>                  |                                                                     | –                                                                                          | 100                      | –                    | nF    |

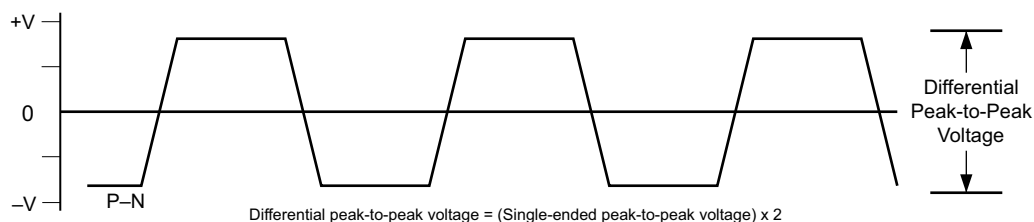
### Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) and can result in values lower than reported in this table.
2. V<sub>RX\_TERM</sub> is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.



X16653-101316

Figure 5: Single-Ended Peak-to-Peak Voltage



X16639-101316

Figure 6: Differential Peak-to-Peak Voltage

Table 60 and Table 61 summarize the DC specifications of the clock input of the GTY transceivers in Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further information.

Table 60: GTY Transceiver Clock DC Input Level Specification

| Symbol      | DC Parameter                            | Min | Typ | Max  | Units    |
|-------------|-----------------------------------------|-----|-----|------|----------|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 250 | –   | 2000 | mV       |
| $R_{IN}$    | Differential input resistance           | –   | 100 | –    | $\Omega$ |
| $C_{EXT}$   | Required external AC coupling capacitor | –   | 10  | –    | nF       |

Table 61: GTY Transceiver Clock Output Level Specification

| Symbol      | Description                                                 | Conditions                               | Min | Typ | Max | Units |
|-------------|-------------------------------------------------------------|------------------------------------------|-----|-----|-----|-------|
| $V_{OL}$    | Output Low voltage for P and N                              | $R_T = 100\Omega$ across P and N signals | 100 | –   | 330 | mV    |
| $V_{OH}$    | Output High voltage for P and N                             | $R_T = 100\Omega$ across P and N signals | 500 | –   | 700 | mV    |
| $V_{DDOUT}$ | Differential output voltage (P–N), P = High (N–P), N = High | $R_T = 100\Omega$ across P and N signals | 300 | –   | 430 | mV    |
| $V_{CMOUT}$ | Common mode voltage                                         | $R_T = 100\Omega$ across P and N signals | 300 | –   | 500 | mV    |

# GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further information.

Table 62: GTY Transceiver Performance

| Symbol                   | Description                          | Output<br>Divider | Speed Grade and V <sub>CCINT</sub> Operating Voltages |         |                      |         |         |         |                      |         |        |         | Units |
|--------------------------|--------------------------------------|-------------------|-------------------------------------------------------|---------|----------------------|---------|---------|---------|----------------------|---------|--------|---------|-------|
|                          |                                      |                   | 0.90V                                                 |         | 0.85V                |         |         |         | 0.72V                |         |        |         |       |
|                          |                                      |                   | -3                                                    |         | -2                   |         | -1      |         | -2                   |         | -1     |         |       |
| F <sub>GTYMAX</sub>      | GTY maximum line rate                |                   | 32.75 <sup>(1)</sup>                                  |         | 28.21 <sup>(1)</sup> |         | 25.7813 |         | 28.21 <sup>(1)</sup> |         | 12.5   |         | Gb/s  |
| F <sub>GTYMIN</sub>      | GTY minimum line rate                |                   | 0.5                                                   |         | 0.5                  |         | 0.5     |         | 0.5                  |         | 0.5    |         | Gb/s  |
|                          |                                      |                   | Min                                                   | Max     | Min                  | Max     | Min     | Max     | Min                  | Max     | Min    | Max     |       |
| F <sub>GTYCRANGE</sub>   | CPLL line rate range <sup>(2)</sup>  | 1                 | 4.0                                                   | 12.5    | 4.0                  | 12.5    | 4.0     | 8.5     | 4.0                  | 12.5    | 4.0    | 8.5     | Gb/s  |
|                          |                                      | 2                 | 2.0                                                   | 6.25    | 2.0                  | 6.25    | 2.0     | 4.25    | 2.0                  | 6.25    | 2.0    | 4.25    | Gb/s  |
|                          |                                      | 4                 | 1.0                                                   | 3.125   | 1.0                  | 3.125   | 1.0     | 2.125   | 1.0                  | 3.125   | 1.0    | 2.125   | Gb/s  |
|                          |                                      | 8                 | 0.5                                                   | 1.5625  | 0.5                  | 1.5625  | 0.5     | 1.0625  | 0.5                  | 1.5625  | 0.5    | 1.0625  | Gb/s  |
|                          |                                      | 16                | N/A                                                   |         |                      |         |         |         |                      |         |        |         | Gb/s  |
|                          |                                      | 32                | N/A                                                   |         |                      |         |         |         |                      |         |        |         | Gb/s  |
|                          |                                      |                   | Min                                                   | Max     | Min                  | Max     | Min     | Max     | Min                  | Max     | Min    | Max     |       |
| F <sub>GTYQRANGE1</sub>  | QPLL0 line rate range <sup>(3)</sup> | 1                 | 19.6                                                  | 32.75   | 19.6                 | 28.21   | 19.6    | 25.7813 | 19.6                 | 28.21   | N/A    |         | Gb/s  |
|                          |                                      | 1                 | 9.8                                                   | 16.375  | 9.8                  | 16.375  | 9.8     | 12.5    | 9.8                  | 16.375  | 9.8    | 12.5    | Gb/s  |
|                          |                                      | 2                 | 4.9                                                   | 8.1875  | 4.9                  | 8.1875  | 4.9     | 8.1875  | 4.9                  | 8.1875  | 4.9    | 8.1875  | Gb/s  |
|                          |                                      | 4                 | 2.45                                                  | 4.09375 | 2.45                 | 4.09375 | 2.45    | 4.09375 | 2.45                 | 4.09375 | 2.45   | 4.09375 | Gb/s  |
|                          |                                      | 8                 | 1.225                                                 | 2.04688 | 1.225                | 2.04688 | 1.225   | 2.04688 | 1.225                | 2.04688 | 1.225  | 2.04688 | Gb/s  |
|                          |                                      | 16                | 0.6125                                                | 1.02344 | 0.6125               | 1.02344 | 0.6125  | 1.02344 | 0.6125               | 1.02344 | 0.6125 | 1.02344 | Gb/s  |
|                          |                                      |                   | Min                                                   | Max     | Min                  | Max     | Min     | Max     | Min                  | Max     | Min    | Max     |       |
| F <sub>GTYQRANGE2</sub>  | QPLL1 line rate range <sup>(4)</sup> | 1                 | 16.0                                                  | 26.0    | 16.0                 | 26.0    | 19.6    | 25.7813 | 16.0                 | 26.0    | N/A    |         | Gb/s  |
|                          |                                      | 1                 | 8.0                                                   | 13.0    | 8.0                  | 13.0    | 8.0     | 12.5    | 8.0                  | 13.0    | 8.0    | 12.5    | Gb/s  |
|                          |                                      | 2                 | 4.0                                                   | 6.5     | 4.0                  | 6.5     | 4.0     | 6.5     | 4.0                  | 6.5     | 4.0    | 6.5     | Gb/s  |
|                          |                                      | 4                 | 2.0                                                   | 3.25    | 2.0                  | 3.25    | 2.0     | 3.25    | 2.0                  | 3.25    | 2.0    | 3.25    | Gb/s  |
|                          |                                      | 8                 | 1.0                                                   | 1.625   | 1.0                  | 1.625   | 1.0     | 1.625   | 1.0                  | 1.625   | 1.0    | 1.625   | Gb/s  |
|                          |                                      | 16                | 0.5                                                   | 0.8125  | 0.5                  | 0.8125  | 0.5     | 0.8125  | 0.5                  | 0.8125  | 0.5    | 0.8125  | Gb/s  |
|                          |                                      |                   | Min                                                   | Max     | Min                  | Max     | Min     | Max     | Min                  | Max     | Min    | Max     |       |
| F <sub>CPLL</sub> RANGE  | CPLL frequency range                 |                   | 2.0                                                   | 6.25    | 2.0                  | 6.25    | 2.0     | 4.25    | 2.0                  | 6.25    | 2.0    | 4.25    | GHz   |
| F <sub>QPLL0</sub> RANGE | QPLL0 frequency range                |                   | 9.8                                                   | 16.375  | 9.8                  | 16.375  | 9.8     | 16.375  | 9.8                  | 16.375  | 9.8    | 16.375  | GHz   |
| F <sub>QPLL1</sub> RANGE | QPLL1 frequency range                |                   | 8.0                                                   | 13.0    | 8.0                  | 13.0    | 8.0     | 13.0    | 8.0                  | 13.0    | 8.0    | 13.0    | GHz   |

## Notes:

- GTY transceiver line rates are package limited: SFVB784 to 12.5 Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3 Gb/s.
- The values listed are the rounded results of the calculated equation  $(2 \times \text{CPLL\_Frequency}) / \text{Output\_Divider}$ .
- The values listed are the rounded results of the calculated equation  $(2 \times \text{QPLL0\_Frequency}) / \text{Output\_Divider}$ .
- The values listed are the rounded results of the calculated equation  $(2 \times \text{QPLL1\_Frequency}) / \text{Output\_Divider}$ .

Table 63: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol                 | Description                  | All Speed Grades | Units |
|------------------------|------------------------------|------------------|-------|
| F <sub>GTYDRPCLK</sub> | GTYDRPCLK maximum frequency. | 250              | MHz   |

Table 64: GTY Transceiver Reference Clock Switching Characteristics

| Symbol             | Description                      | Conditions           | All Speed Grades |     |     | Units |
|--------------------|----------------------------------|----------------------|------------------|-----|-----|-------|
|                    |                                  |                      | Min              | Typ | Max |       |
| F <sub>GCLK</sub>  | Reference clock frequency range. |                      | 60               | –   | 820 | MHz   |
| T <sub>RCLK</sub>  | Reference clock rise time.       | 20% – 80%            | –                | 200 | –   | ps    |
| T <sub>FCLK</sub>  | Reference clock fall time.       | 80% – 20%            | –                | 200 | –   | ps    |
| T <sub>DCREF</sub> | Reference clock duty cycle.      | Transceiver PLL only | 40               | 50  | 60  | %     |

Table 65: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask<sup>(1)</sup>

| Symbol                     | Description                                                                           | Offset Frequency | Min | Typ | Max  | Units  |
|----------------------------|---------------------------------------------------------------------------------------|------------------|-----|-----|------|--------|
| QPLL <sub>REFCLKMASK</sub> | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz. | 10 kHz           | –   | –   | –112 | dBc/Hz |
|                            |                                                                                       | 100 kHz          | –   | –   | –128 |        |
|                            |                                                                                       | 1 MHz            | –   | –   | –145 |        |
|                            | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.  | 10 kHz           | –   | –   | –103 | dBc/Hz |
|                            |                                                                                       | 100 kHz          | –   | –   | –123 |        |
|                            |                                                                                       | 1 MHz            | –   | –   | –143 |        |
|                            | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz.    | 10 kHz           | –   | –   | –98  | dBc/Hz |
|                            |                                                                                       | 100 kHz          | –   | –   | –117 |        |
|                            |                                                                                       | 1 MHz            | –   | –   | –140 |        |
| CPLL <sub>REFCLKMASK</sub> | CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.        | 10 kHz           | –   | –   | –112 | dBc/Hz |
|                            |                                                                                       | 100 kHz          | –   | –   | –128 |        |
|                            |                                                                                       | 1 MHz            | –   | –   | –145 |        |
|                            |                                                                                       | 50 MHz           | –   | –   | –145 |        |
|                            | CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.         | 10 kHz           | –   | –   | –103 | dBc/Hz |
|                            |                                                                                       | 100 kHz          | –   | –   | –123 |        |
|                            |                                                                                       | 1 MHz            | –   | –   | –143 |        |
|                            |                                                                                       | 50 MHz           | –   | –   | –145 |        |
|                            | CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.           | 10 kHz           | –   | –   | –98  | dBc/Hz |
|                            |                                                                                       | 100 kHz          | –   | –   | –117 |        |
|                            |                                                                                       | 1 MHz            | –   | –   | –140 |        |
|                            |                                                                                       | 50 MHz           | –   | –   | –144 |        |

**Notes:**

- For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.

Table 66: GTY Transceiver PLL /Lock Time Adaptation

| Symbol             | Description                                                                                             | Conditions                                                                                                                                        | All Speed Grades |        |                       | Units |
|--------------------|---------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------|-----------------------|-------|
|                    |                                                                                                         |                                                                                                                                                   | Min              | Typ    | Max                   |       |
| T <sub>LOCK</sub>  | Initial PLL lock.                                                                                       |                                                                                                                                                   | –                | –      | 1                     | ms    |
| T <sub>DLOCK</sub> | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).             | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | –                | 50,000 | 37 x 10 <sup>6</sup>  | UI    |
|                    | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled. |                                                                                                                                                   | –                | 50,000 | 2.3 x 10 <sup>6</sup> | UI    |

Table 67: GTY Transceiver User Clock Switching Characteristics<sup>(1)</sup>

| Symbol                    | Description                                          | Data Width Conditions (Bit) |                    | Speed Grade and V <sub>CCINT</sub> Operating Voltages |                      |                      |                   |                   | Units |
|---------------------------|------------------------------------------------------|-----------------------------|--------------------|-------------------------------------------------------|----------------------|----------------------|-------------------|-------------------|-------|
|                           |                                                      |                             |                    | 0.90V                                                 | 0.85V                |                      | 0.72V             |                   |       |
|                           |                                                      | Internal Logic              | Interconnect Logic | -3 <sup>(2)</sup>                                     | -2 <sup>(2)(3)</sup> | -1 <sup>(4)(5)</sup> | -2 <sup>(3)</sup> | -1 <sup>(5)</sup> |       |
| F <sub>TXOUTPMA</sub>     | TXOUTCLK maximum frequency sourced from OUTCLKPMA    |                             | 511.719            | 511.719                                               | 402.832              | 402.832              | 322.266           | MHz               |       |
| F <sub>RXOUTPMA</sub>     | RXOUTCLK maximum frequency sourced from OUTCLKPMA    |                             | 511.719            | 511.719                                               | 402.832              | 402.832              | 322.266           | MHz               |       |
| F <sub>TXOUTPROGDIV</sub> | TXOUTCLK maximum frequency sourced from TXPROGDIVCLK |                             | 511.719            | 511.719                                               | 511.719              | 511.719              | 511.719           | MHz               |       |
| F <sub>RXOUTPROGDIV</sub> | RXOUTCLK maximum frequency sourced from RXPROGDIVCLK |                             | 511.719            | 511.719                                               | 511.719              | 511.719              | 511.719           | MHz               |       |
| F <sub>TXIN</sub>         | TXUSRCLK <sup>(6)</sup> maximum frequency            | 16                          | 16, 32             | 511.719                                               | 511.719              | 390.625              | 390.625           | 322.266           | MHz   |
|                           |                                                      | 32                          | 32, 64             | 511.719                                               | 511.719              | 390.625              | 390.625           | 322.266           | MHz   |
|                           |                                                      | 64                          | 64, 128            | 511.719                                               | 440.781              | 402.832              | 402.832           | 195.313           | MHz   |
|                           |                                                      | 20                          | 20, 40             | 409.375                                               | 409.375              | 312.500              | 312.500           | 257.813           | MHz   |
|                           |                                                      | 40                          | 40, 80             | 409.375                                               | 409.375              | 312.500              | 350.000           | 257.813           | MHz   |
|                           |                                                      | 80                          | 80, 160            | 409.375                                               | 352.625              | 322.266              | 352.625           | 156.250           | MHz   |
| F <sub>RXIN</sub>         | RXUSRCLK <sup>(6)</sup> maximum frequency            | 16                          | 16, 32             | 511.719                                               | 511.719              | 390.625              | 390.625           | 322.266           | MHz   |
|                           |                                                      | 32                          | 32, 64             | 511.719                                               | 511.719              | 390.625              | 390.625           | 322.266           | MHz   |
|                           |                                                      | 64                          | 64, 128            | 511.719                                               | 440.781              | 402.832              | 402.832           | 195.313           | MHz   |
|                           |                                                      | 20                          | 20, 40             | 409.375                                               | 409.375              | 312.500              | 312.500           | 257.813           | MHz   |
|                           |                                                      | 40                          | 40, 80             | 409.375                                               | 409.375              | 312.500              | 350.000           | 257.813           | MHz   |
|                           |                                                      | 80                          | 80, 160            | 409.375                                               | 352.625              | 322.266              | 352.625           | 156.250           | MHz   |

Table 67: GTY Transceiver User Clock Switching Characteristics<sup>(1)</sup> (Cont'd)

| Symbol             | Description                                      | Data Width Conditions<br>(Bit) |                       | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |                      |                      |                   |                   | Units |
|--------------------|--------------------------------------------------|--------------------------------|-----------------------|----------------------------------------------------------|----------------------|----------------------|-------------------|-------------------|-------|
|                    |                                                  |                                |                       | 0.90V                                                    | 0.85V                |                      | 0.72V             |                   |       |
|                    |                                                  | Internal<br>Logic              | Interconnect<br>Logic | -3 <sup>(2)</sup>                                        | -2 <sup>(2)(3)</sup> | -1 <sup>(4)(5)</sup> | -2 <sup>(3)</sup> | -1 <sup>(5)</sup> |       |
| F <sub>TXIN2</sub> | TXUSRCLK2 <sup>(6)</sup><br>maximum<br>frequency | 16                             | 16                    | 511.719                                                  | 511.719              | 390.625              | 390.625           | 322.266           | MHz   |
|                    |                                                  | 16                             | 32                    | 255.859                                                  | 255.859              | 195.313              | 195.313           | 161.133           | MHz   |
|                    |                                                  | 32                             | 32                    | 511.719                                                  | 511.719              | 390.625              | 390.625           | 322.266           | MHz   |
|                    |                                                  | 32                             | 64                    | 255.859                                                  | 255.859              | 195.313              | 195.313           | 161.133           | MHz   |
|                    |                                                  | 64                             | 64                    | 511.719                                                  | 440.781              | 402.832              | 402.832           | 195.313           | MHz   |
|                    |                                                  | 64                             | 128                   | 255.859                                                  | 220.391              | 201.416              | 201.416           | 97.656            | MHz   |
|                    |                                                  | 20                             | 20                    | 409.375                                                  | 409.375              | 312.500              | 312.500           | 257.813           | MHz   |
|                    |                                                  | 20                             | 40                    | 204.688                                                  | 204.688              | 156.250              | 156.250           | 128.906           | MHz   |
|                    |                                                  | 40                             | 40                    | 409.375                                                  | 409.375              | 312.500              | 350.000           | 257.813           | MHz   |
|                    |                                                  | 40                             | 80                    | 204.688                                                  | 204.688              | 156.250              | 175.000           | 128.906           | MHz   |
|                    |                                                  | 80                             | 80                    | 409.375                                                  | 352.625              | 322.266              | 352.625           | 156.250           | MHz   |
|                    |                                                  | 80                             | 160                   | 204.688                                                  | 176.313              | 161.133              | 176.313           | 78.125            | MHz   |
| F <sub>RXIN2</sub> | RXUSRCLK2 <sup>(6)</sup><br>maximum<br>frequency | 16                             | 16                    | 511.719                                                  | 511.719              | 390.625              | 390.625           | 322.266           | MHz   |
|                    |                                                  | 16                             | 32                    | 255.859                                                  | 255.859              | 195.313              | 195.313           | 161.133           | MHz   |
|                    |                                                  | 32                             | 32                    | 511.719                                                  | 511.719              | 390.625              | 390.625           | 322.266           | MHz   |
|                    |                                                  | 32                             | 64                    | 255.859                                                  | 255.859              | 195.313              | 195.313           | 161.133           | MHz   |
|                    |                                                  | 64                             | 64                    | 511.719                                                  | 440.781              | 402.832              | 402.832           | 195.313           | MHz   |
|                    |                                                  | 64                             | 128                   | 255.859                                                  | 220.391              | 201.416              | 201.416           | 97.656            | MHz   |
|                    |                                                  | 20                             | 20                    | 409.375                                                  | 409.375              | 312.500              | 312.500           | 257.813           | MHz   |
|                    |                                                  | 20                             | 40                    | 204.688                                                  | 204.688              | 156.250              | 156.250           | 128.906           | MHz   |
|                    |                                                  | 40                             | 40                    | 409.375                                                  | 409.375              | 312.500              | 350.000           | 257.813           | MHz   |
|                    |                                                  | 40                             | 80                    | 204.688                                                  | 204.688              | 156.250              | 175.000           | 128.906           | MHz   |
|                    |                                                  | 80                             | 80                    | 409.375                                                  | 352.625              | 322.266              | 352.625           | 156.250           | MHz   |
|                    |                                                  | 80                             | 160                   | 204.688                                                  | 176.313              | 161.133              | 176.313           | 78.125            | MHz   |

**Notes:**

- Clocking must be implemented as described in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
- For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
- For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V<sub>CCINT</sub> = 0.85V or 6.25 Gb/s when V<sub>CCINT</sub> = 0.72V.
- For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
- For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V<sub>CCINT</sub> = 0.85V or 5.15625 Gb/s when V<sub>CCINT</sub> = 0.72V.
- When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).

Table 68: GTY Transceiver Transmitter Switching Characteristics

| Symbol                     | Description                            | Condition    | Min   | Typ | Max                 | Units |
|----------------------------|----------------------------------------|--------------|-------|-----|---------------------|-------|
| F <sub>GTYTX</sub>         | Serial data rate range                 |              | 0.500 | –   | F <sub>GTYMAX</sub> | Gb/s  |
| T <sub>RTX</sub>           | TX rise time                           | 20%–80%      | –     | 21  | –                   | ps    |
| T <sub>FTX</sub>           | TX fall time                           | 80%–20%      | –     | 21  | –                   | ps    |
| T <sub>LLSKEW</sub>        | TX lane-to-lane skew <sup>(1)</sup>    |              | –     | –   | 500.00              | ps    |
| T <sub>J32.75</sub>        | Total jitter <sup>(2)(4)</sup>         | 32.75 Gb/s   | –     | –   | 0.35                | UI    |
| D <sub>J32.75</sub>        | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.19                | UI    |
| T <sub>J28.21</sub>        | Total jitter <sup>(2)(4)</sup>         | 28.21 Gb/s   | –     | –   | 0.28                | UI    |
| D <sub>J28.21</sub>        | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J16.375</sub>       | Total jitter <sup>(2)(4)</sup>         | 16.375 Gb/s  | –     | –   | 0.28                | UI    |
| D <sub>J16.375</sub>       | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J15.0</sub>         | Total jitter <sup>(2)(4)</sup>         | 15.0 Gb/s    | –     | –   | 0.28                | UI    |
| D <sub>J15.0</sub>         | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J14.1</sub>         | Total jitter <sup>(2)(4)</sup>         | 14.1 Gb/s    | –     | –   | 0.28                | UI    |
| D <sub>J14.1</sub>         | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J14.1</sub>         | Total jitter <sup>(2)(4)</sup>         | 14.025 Gb/s  | –     | –   | 0.28                | UI    |
| D <sub>J14.1</sub>         | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J13.1</sub>         | Total jitter <sup>(2)(4)</sup>         | 13.1 Gb/s    | –     | –   | 0.28                | UI    |
| D <sub>J13.1</sub>         | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J12.5_QPLL</sub>    | Total jitter <sup>(2)(4)</sup>         | 12.5 Gb/s    | –     | –   | 0.28                | UI    |
| D <sub>J12.5_QPLL</sub>    | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J12.5_CPLL</sub>    | Total jitter <sup>(2)(4)</sup>         | 12.5 Gb/s    | –     | –   | 0.33                | UI    |
| D <sub>J12.5_CPLL</sub>    | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J11.3_QPLL</sub>    | Total jitter <sup>(2)(4)</sup>         | 11.3 Gb/s    | –     | –   | 0.28                | UI    |
| D <sub>J11.3_QPLL</sub>    | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J10.3125_QPLL</sub> | Total jitter <sup>(2)(4)</sup>         | 10.3125 Gb/s | –     | –   | 0.28                | UI    |
| D <sub>J10.3125_QPLL</sub> | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J10.3125_CPLL</sub> | Total jitter <sup>(3)(4)</sup>         | 10.3125 Gb/s | –     | –   | 0.33                | UI    |
| D <sub>J10.3125_CPLL</sub> | Deterministic jitter <sup>(3)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J9.953_QPLL</sub>   | Total jitter <sup>(2)(4)</sup>         | 9.953 Gb/s   | –     | –   | 0.28                | UI    |
| D <sub>J9.953_QPLL</sub>   | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J9.953_CPLL</sub>   | Total jitter <sup>(3)(4)</sup>         | 9.953 Gb/s   | –     | –   | 0.33                | UI    |
| D <sub>J9.953_CPLL</sub>   | Deterministic jitter <sup>(3)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J8.0</sub>          | Total jitter <sup>(2)(4)</sup>         | 8.0 Gb/s     | –     | –   | 0.32                | UI    |
| D <sub>J8.0</sub>          | Deterministic jitter <sup>(2)(4)</sup> |              | –     | –   | 0.17                | UI    |
| T <sub>J6.6</sub>          | Total jitter <sup>(3)(4)</sup>         | 6.6 Gb/s     | –     | –   | 0.30                | UI    |
| D <sub>J6.6</sub>          | Deterministic jitter <sup>(3)(4)</sup> |              | –     | –   | 0.15                | UI    |
| T <sub>J5.0</sub>          | Total jitter <sup>(3)(4)</sup>         | 5.0 Gb/s     | –     | –   | 0.30                | UI    |
| D <sub>J5.0</sub>          | Deterministic jitter <sup>(3)(4)</sup> |              | –     | –   | 0.15                | UI    |
| T <sub>J4.25</sub>         | Total jitter <sup>(3)(4)</sup>         | 4.25 Gb/s    | –     | –   | 0.30                | UI    |
| D <sub>J4.25</sub>         | Deterministic jitter <sup>(3)(4)</sup> |              | –     | –   | 0.15                | UI    |

Table 68: GTY Transceiver Transmitter Switching Characteristics (Cont'd)

| Symbol             | Description                            | Condition                | Min | Typ | Max  | Units |
|--------------------|----------------------------------------|--------------------------|-----|-----|------|-------|
| T <sub>J3.20</sub> | Total jitter <sup>(3)(4)</sup>         | 3.20 Gb/s <sup>(5)</sup> | –   | –   | 0.20 | UI    |
| D <sub>J3.20</sub> | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.10 | UI    |
| T <sub>J2.5</sub>  | Total jitter <sup>(3)(4)</sup>         | 2.5 Gb/s <sup>(6)</sup>  | –   | –   | 0.20 | UI    |
| D <sub>J2.5</sub>  | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.10 | UI    |
| T <sub>J1.25</sub> | Total jitter <sup>(3)(4)</sup>         | 1.25 Gb/s <sup>(7)</sup> | –   | –   | 0.15 | UI    |
| D <sub>J1.25</sub> | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.06 | UI    |
| T <sub>J500</sub>  | Total jitter <sup>(3)(4)</sup>         | 500 Mb/s <sup>(8)</sup>  | –   | –   | 0.10 | UI    |
| D <sub>J500</sub>  | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.03 | UI    |

**Notes:**

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL\_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL\_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10<sup>-12</sup>.
5. CPLL frequency at 3.2 GHz and TXOUT\_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT\_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT\_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT\_DIV = 8.

Table 69: GTY Transceiver Receiver Switching Characteristics

| Symbol                                               | Description                                        | Condition                           | Min   | Typ | Max                 | Units |
|------------------------------------------------------|----------------------------------------------------|-------------------------------------|-------|-----|---------------------|-------|
| F <sub>GTYRX</sub>                                   | Serial data rate                                   |                                     | 0.500 | –   | F <sub>GTYMAX</sub> | Gb/s  |
| R <sub>XSSST</sub>                                   | Receiver spread-spectrum tracking <sup>(1)</sup>   | Modulated at 33 kHz                 | –5000 | –   | 0                   | ppm   |
| R <sub>XRL</sub>                                     | Run length (CID)                                   |                                     | –     | –   | 256                 | UI    |
| R <sub>XPPMTOL</sub>                                 | Data/REFCLK PPM offset tolerance                   | Bit rates ≤ 6.6 Gb/s                | –1250 | –   | 1250                | ppm   |
|                                                      |                                                    | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700  | –   | 700                 | ppm   |
|                                                      |                                                    | Bit rates > 8.0 Gb/s                | –200  | –   | 200                 | ppm   |
| SJ Jitter Tolerance <sup>(2)</sup>                   |                                                    |                                     |       |     |                     |       |
| J <sub>T_SJ32.75</sub>                               | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 32.75 Gb/s                          | 0.25  | –   | –                   | UI    |
| J <sub>T_SJ28.21</sub>                               | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 28.21 Gb/s                          | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ16.375</sub>                              | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 16.375 Gb/s                         | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ15.0</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 15.0 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ14.1</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 14.1 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ13.1</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 13.1 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ12.5</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 12.5 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ11.3</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 11.3 Gb/s                           | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ10.32_QPLL</sub>                          | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 10.32 Gb/s                          | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ10.32_CPLL</sub>                          | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 10.32 Gb/s                          | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ9.953_QPLL</sub>                          | Sinusoidal jitter (QPLL) <sup>(3)</sup>            | 9.953 Gb/s                          | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ9.953_CPLL</sub>                          | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 9.953 Gb/s                          | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ8.0</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 8.0 Gb/s                            | 0.42  | –   | –                   | UI    |
| J <sub>T_SJ6.6</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 6.6 Gb/s                            | 0.44  | –   | –                   | UI    |
| J <sub>T_SJ5.0</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 5.0 Gb/s                            | 0.44  | –   | –                   | UI    |
| J <sub>T_SJ4.25</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 4.25 Gb/s                           | 0.44  | –   | –                   | UI    |
| J <sub>T_SJ3.2</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 3.2 Gb/s <sup>(4)</sup>             | 0.45  | –   | –                   | UI    |
| J <sub>T_SJ2.5</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 2.5 Gb/s <sup>(5)</sup>             | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ1.25</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 1.25 Gb/s <sup>(6)</sup>            | 0.30  | –   | –                   | UI    |
| J <sub>T_SJ500</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>            | 500 Mb/s <sup>(7)</sup>             | 0.30  | –   | –                   | UI    |
| SJ Jitter Tolerance with Stressed Eye <sup>(2)</sup> |                                                    |                                     |       |     |                     |       |
| J <sub>T_TJSE3.2</sub>                               | Total jitter with stressed eye <sup>(8)</sup>      | 3.2 Gb/s                            | 0.70  | –   | –                   | UI    |
| J <sub>T_TJSE6.6</sub>                               |                                                    | 6.6 Gb/s                            | 0.70  | –   | –                   | UI    |
| J <sub>T_SJSE3.2</sub>                               | Sinusoidal jitter with stressed eye <sup>(8)</sup> | 3.2 Gb/s                            | 0.10  | –   | –                   | UI    |
| J <sub>T_SJSE6.6</sub>                               |                                                    | 6.6 Gb/s                            | 0.10  | –   | –                   | UI    |

**Notes:**

- Using RXOUT\_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10<sup>–12</sup>.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 4.
- CPLL frequency at 2.0 GHz and RXOUT\_DIV = 8.
- Composite jitter with RX equalizer enabled. DFE disabled.

## GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 70](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 70: GTY Transceiver Protocol List

| Protocol                      | Specification                                    | Serial Rate (Gb/s) | Electrical Compliance    |
|-------------------------------|--------------------------------------------------|--------------------|--------------------------|
| CAUI-4                        | IEEE 802.3-2012                                  | 25.78125           | Compliant                |
| 28 Gb/s backplane             | CEI-25G-LR                                       | 25–28.05           | Compliant                |
| Interlaken                    | OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR        | 4.25–25.78125      | Compliant                |
| 100GBASE-KR4                  | IEEE 802.3bj-2014, CEI-25G-LR                    | 25.78125           | Compliant <sup>(1)</sup> |
| 100GBASE-CR4                  | IEEE 802.3bj-2014, CEI-25G-LR                    | 25.78125           | Compliant <sup>(1)</sup> |
| 50GBASE-KR4                   | IEEE 802.3by-2014, CEI-25G-LR                    | 25.78125           | Compliant <sup>(1)</sup> |
| 50GBASE-CR4                   | IEEE 802.3by-2014, CEI-25G-LR                    | 25.78125           | Compliant <sup>(1)</sup> |
| 25GBASE-KR4                   | IEEE 802.3by-2014, CEI-25G-LR                    | 25.78125           | Compliant <sup>(1)</sup> |
| 25GBASE-CR4                   | IEEE 802.3by-2014, CEI-25G-LR                    | 25.78125           | Compliant <sup>(1)</sup> |
| OTU4 (OTL4.4) CFP2            | OIF-CEI-28G-VSR                                  | 27.952493–32.75    | Compliant                |
| OTU4 (OTL4.4) CFP             | OIF-CEI-11G-MR                                   | 11.18–13.1         | Compliant                |
| CAUI-10                       | IEEE 802.3-2012                                  | 10.3125            | Compliant                |
| nPPI                          | IEEE 802.3-2012                                  | 10.3125            | Compliant                |
| 10GBASE-KR <sup>(2)</sup>     | IEEE 802.3-2012                                  | 10.3125            | Compliant                |
| SFP+                          | SFF-8431 (SR and LR)                             | 9.95328–11.10      | Compliant                |
| XFP                           | INF-8077i, revision 4.5                          | 10.3125            | Compliant                |
| RXAUI                         | CEI-6G-SR                                        | 6.25               | Compliant                |
| XAUI                          | IEEE 802.3-2012                                  | 3.125              | Compliant                |
| 1000BASE-X                    | IEEE 802.3-2012                                  | 1.25               | Compliant                |
| 5.0G Ethernet                 | IEEE 802.3bx (PAR)                               | 5                  | Compliant                |
| 2.5G Ethernet                 | IEEE 802.3bx (PAR)                               | 2.5                | Compliant                |
| HiGig, HiGig+, HiGig2         | IEEE 802.3-2012                                  | 3.74, 6.6          | Compliant                |
| QSGMII                        | QSGMII v1.2 (Cisco System, ENG-46158)            | 5                  | Compliant                |
| OTU2                          | ITU G.8251                                       | 10.709225          | Compliant                |
| OTU4 (OTL4.10)                | OIF-CEI-11G-SR                                   | 11.180997          | Compliant                |
| OC-3/12/48/192                | GR-253-CORE                                      | 0.1555–9.956       | Compliant                |
| PCIe Gen1, 2, 3               | PCI Express base 3.0                             | 2.5, 5.0, and 8.0  | Compliant                |
| SDI <sup>(3)</sup>            | SMPTE 424M-2006                                  | 0.27–2.97          | Compliant                |
| UHD-SDI <sup>(3)</sup>        | SMPTE ST-2081 6G, SMPTE ST-2082 12G              | 6 and 12           | Compliant                |
| Hybrid memory cube (HMC)      | HMC-15G-SR                                       | 10, 12.5, and 15.0 | Compliant                |
| MoSys bandwidth engine        | CEI-11-SR and CEI-11-SR (overclocked)            | 10.3125, 15.5      | Compliant                |
| CPRI                          | CPRI_v_6_1_2014-07-01                            | 0.6144–12.165      | Compliant                |
| Passive optical network (PON) | 10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON | 0.155–10.3125      | Compliant                |
| JESD204a/b                    | OIF-CEI-6G, OIF-CEI-11G                          | 3.125–12.5         | Compliant                |

Table 70: GTY Transceiver Protocol List (Cont'd)

| Protocol        | Specification                         | Serial Rate (Gb/s) | Electrical Compliance    |
|-----------------|---------------------------------------|--------------------|--------------------------|
| Serial RapidIO  | RapidIO specification 3.1             | 1.25–10.3125       | Compliant                |
| DisplayPort     | DP 1.2B CTS                           | 1.62–5.4           | Compliant <sup>(3)</sup> |
| Fibre channel   | FC-PH-4                               | 1.0625–14.025      | Compliant                |
| SATA Gen1, 2, 3 | Serial ATA revision 3.0 specification | 1.5, 3.0, and 6.0  | Compliant                |
| SAS Gen1, 2, 3  | T10/BSR INCITS 519                    | 3.0, 6.0, and 12.0 | Compliant                |
| SFI-5           | OIF-SFI5-01.0                         | 0.625 - 12.5       | Compliant                |
| Aurora          | CEI-6G, CEI-11G-LR                    | All rates          | Compliant                |

**Notes:**

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

## Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at [UltraScale Interlaken](#). The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Kintex UltraScale+ FPGA. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode ([Table 71](#)).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode ([Table 72](#)).
- 12 x 25.78125 Gb/s lane logic only mode ([Table 73](#)).

Kintex UltraScale+ FPGAs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See [Table 62](#) for the  $F_{GTMAX}$  description.

**Table 71: Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

| Symbol                     | Description                                   | Speed Grade and V <sub>CCINT</sub> Operating Voltages |        |                    |        |                    |        |                    |        |                    |        | Units |
|----------------------------|-----------------------------------------------|-------------------------------------------------------|--------|--------------------|--------|--------------------|--------|--------------------|--------|--------------------|--------|-------|
|                            |                                               | 0.90V                                                 |        | 0.85V              |        |                    |        | 0.72V              |        |                    |        |       |
|                            |                                               | -3                                                    |        | -2                 |        | -1                 |        | -2                 |        | -1                 |        |       |
| F <sub>RX_SERDES_CLK</sub> | Receive serializer/<br>deserializer clock     | 195.32                                                |        | 195.32             |        | 195.32             |        | 195.32             |        | 195.32             |        | MHz   |
| F <sub>TX_SERDES_CLK</sub> | Transmit<br>serializer/<br>deserializer clock | 195.32                                                |        | 195.32             |        | 195.32             |        | 195.32             |        | 195.32             |        | MHz   |
| F <sub>DRP_CLK</sub>       | Dynamic<br>reconfiguration<br>port clock      | 250.00                                                |        | 250.00             |        | 250.00             |        | 250.00             |        | 250.00             |        | MHz   |
|                            |                                               | Min <sup>(1)</sup>                                    | Max    | Min <sup>(1)</sup> | Max    | Min <sup>(1)</sup> | Max    | Min <sup>(1)</sup> | Max    | Min <sup>(1)</sup> | Max    |       |
| F <sub>CORE_CLK</sub>      | Interlaken core<br>clock                      | 300.00                                                | 322.27 | 300.00             | 322.27 | 300.00             | 322.27 | 300.00             | 322.27 | 300.00             | 322.27 | MHz   |
| F <sub>LBUS_CLK</sub>      | Interlaken local<br>bus clock                 | 300.00                                                | 322.27 | 300.00             | 322.27 | 300.00             | 322.27 | 300.00             | 322.27 | 300.00             | 322.27 | MHz   |

**Notes:**

1. These are the minimum clock frequencies at the maximum lane performance.

**Table 72: Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

| Symbol                     | Description                                | Speed Grade and V <sub>CCINT</sub> Operating Voltages |                   |                       |        |     |        |                    |     |     |     | Units |
|----------------------------|--------------------------------------------|-------------------------------------------------------|-------------------|-----------------------|--------|-----|--------|--------------------|-----|-----|-----|-------|
|                            |                                            | 0.90V                                                 |                   | 0.85V                 |        |     | 0.72V  |                    |     |     |     |       |
|                            |                                            | -3 <sup>(1)</sup>                                     | -2 <sup>(1)</sup> | -1                    | -2     | -1  |        |                    |     |     |     |       |
| F <sub>RX_SERDES_CLK</sub> | Receive serializer/<br>deserializer clock  | 440.79                                                | 440.79            | N/A                   | 402.84 | N/A | MHz    |                    |     |     |     |       |
| F <sub>TX_SERDES_CLK</sub> | Transmit serializer/<br>deserializer clock | 440.79                                                | 440.79            | N/A                   | 402.84 | N/A | MHz    |                    |     |     |     |       |
| F <sub>DRP_CLK</sub>       | Dynamic reconfiguration<br>port clock      | 250.00                                                | 250.00            | N/A                   | 250.00 | N/A | MHz    |                    |     |     |     |       |
|                            |                                            | Min <sup>(2)</sup>                                    | Max               | Min <sup>(2)</sup>    | Max    | Min | Max    | Min <sup>(2)</sup> | Max | Min | Max |       |
| F <sub>CORE_CLK</sub>      | Interlaken core clock                      | 412.50 <sup>(3)</sup>                                 | 479.20            | 412.50 <sup>(3)</sup> | 479.20 | N/A | 412.50 | 429.69             | N/A | MHz |     |       |
| F <sub>LBUS_CLK</sub>      | Interlaken local bus clock                 | 300.00 <sup>(4)</sup>                                 | 349.52            | 300.00 <sup>(4)</sup> | 349.52 | N/A | 300.00 | 349.52             | N/A | MHz |     |       |

**Notes:**

- 6 x 28.21 mode is only supported in the -2 (V<sub>CCINT</sub>=0.85V) and -3 (V<sub>CCINT</sub>=0.90V) speed grades.
- These are the minimum clock frequencies at the maximum lane performance.
- The minimum value for CORE\_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
- The minimum value for LBUS\_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

**Table 73: Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

| Symbol                     | Description                                | Speed Grade and V <sub>CCINT</sub> Operating Voltages |        |     |       |     | Units |
|----------------------------|--------------------------------------------|-------------------------------------------------------|--------|-----|-------|-----|-------|
|                            |                                            | 0.90V                                                 | 0.85V  |     | 0.72V |     |       |
|                            |                                            | -3                                                    | -2     | -1  | -2    | -1  |       |
| F <sub>RX_SERDES_CLK</sub> | Receive serializer/<br>deserializer clock  | 402.84                                                | 402.84 | N/A | N/A   | N/A | MHz   |
| F <sub>TX_SERDES_CLK</sub> | Transmit serializer/<br>deserializer clock | 402.84                                                | 402.84 | N/A | N/A   | N/A | MHz   |
| F <sub>DRP_CLK</sub>       | Dynamic reconfiguration<br>port clock      | 250.00                                                | 250.00 | N/A | N/A   | N/A | MHz   |
| F <sub>CORE_CLK</sub>      | Interlaken core clock                      | 412.50                                                | 412.50 | N/A | N/A   | N/A | MHz   |
| F <sub>LBUS_CLK</sub>      | Interlaken local bus clock                 | 349.52                                                | 349.52 | N/A | N/A   | N/A | MHz   |

## Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at [UltraScale Integrated 100G Ethernet MAC/PCS](#). The *UltraScale Architecture and Product Overview* ([DS890](#)) lists how many blocks are in each Kintex UltraScale+ FPGA.

Table 74: Maximum Performance for 100G Ethernet Designs

| Symbol                     | Description                           | Speed Grade and V <sub>CCINT</sub> Operating Voltages |                   |         |         |                   | Units |
|----------------------------|---------------------------------------|-------------------------------------------------------|-------------------|---------|---------|-------------------|-------|
|                            |                                       | 0.90V                                                 | 0.85V             |         | 0.72V   |                   |       |
|                            |                                       | -3                                                    | -2 <sup>(1)</sup> | -1      | -2      | -1 <sup>(2)</sup> |       |
| F <sub>TX_CLK</sub>        | Transmit clock                        | 390.625                                               | 390.625           | 322.223 | 322.223 | 322.223           | MHz   |
| F <sub>RX_CLK</sub>        | Receive clock                         | 390.625                                               | 390.625           | 322.223 | 322.223 | 322.223           | MHz   |
| F <sub>RX_SERDES_CLK</sub> | Receive serializer/deserializer clock | 390.625                                               | 390.625           | 322.223 | 322.223 | 322.223           | MHz   |
| F <sub>DRP_CLK</sub>       | Dynamic reconfiguration port clock    | 250.00                                                | 250.00            | 250.00  | 250.00  | 250.00            | MHz   |

### Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.
2. The CAUI-4 interface is not supported by -1L speed grade devices where V<sub>CCINT</sub>=0.72V.

## Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at [PCI Express](#). The *UltraScale Architecture and Product Overview* ([DS890](#)) lists how many blocks are in each Kintex UltraScale+ FPGA.

Table 75: Maximum Performance for PCI Express Designs<sup>(1)(2)</sup>

| Symbol               | Description                   | Speed Grade and V <sub>CCINT</sub> Operating Voltages |        |        |                      |        | Units |
|----------------------|-------------------------------|-------------------------------------------------------|--------|--------|----------------------|--------|-------|
|                      |                               | 0.90V                                                 | 0.85V  |        | 0.72V <sup>(3)</sup> |        |       |
|                      |                               | -3                                                    | -2     | -1     | -2                   | -1     |       |
| F <sub>PIPECLK</sub> | Pipe clock maximum frequency. | 250.00                                                | 250.00 | 250.00 | 250.00               | 250.00 | MHz   |
| F <sub>CORECLK</sub> | Core clock maximum frequency. | 500.00                                                | 500.00 | 500.00 | 250.00               | 250.00 | MHz   |
| F <sub>DRPCLK</sub>  | DRP clock maximum frequency.  | 250.00                                                | 250.00 | 250.00 | 250.00               | 250.00 | MHz   |
| F <sub>MCAPCLK</sub> | MCAP clock maximum frequency. | 125.00                                                | 125.00 | 125.00 | 125.00               | 125.00 | MHz   |

### Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.
3. PCI Express Gen3 x16 operation is not supported when V<sub>CCINT</sub> = 0.72V.

# System Monitor Specifications

Table 76: System Monitor Specifications

| Parameter                                                                                                                                                                      | Symbol | Comments/Conditions                                                                            | Min  | Typ | Max         | Units       |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------|------|-----|-------------|-------------|
| $V_{CCADC} = 1.8V \pm 3\%$ , $V_{REFP} = 1.25V$ , $V_{REFN} = 0V$ , $ADCCLK = 5.2\text{ MHz}$ , $T_j = -40^{\circ}C$ to $100^{\circ}C$ , typical values at $T_j = 40^{\circ}C$ |        |                                                                                                |      |     |             |             |
| ADC Accuracy <sup>(1)</sup>                                                                                                                                                    |        |                                                                                                |      |     |             |             |
| Resolution                                                                                                                                                                     |        |                                                                                                | 10   | –   | –           | Bits        |
| Integral nonlinearity <sup>(2)</sup>                                                                                                                                           | INL    |                                                                                                | –    | –   | $\pm 1.5$   | LSBs        |
| Differential nonlinearity                                                                                                                                                      | DNL    | No missing codes, guaranteed monotonic                                                         | –    | –   | $\pm 1$     | LSBs        |
| Offset error                                                                                                                                                                   |        | Offset calibration enabled                                                                     | –    | –   | $\pm 2$     | LSBs        |
| Gain error                                                                                                                                                                     |        |                                                                                                | –    | –   | $\pm 0.4$   | %           |
| Sample rate                                                                                                                                                                    |        |                                                                                                | –    | –   | 0.2         | MS/s        |
| RMS code noise                                                                                                                                                                 |        | External 1.25V reference                                                                       | –    | –   | 1           | LSBs        |
|                                                                                                                                                                                |        | On-chip reference                                                                              | –    | 1   | –           | LSBs        |
| ADC Accuracy at Extended Temperatures                                                                                                                                          |        |                                                                                                |      |     |             |             |
| Resolution                                                                                                                                                                     |        | $T_j = -55^{\circ}C$ to $125^{\circ}C$                                                         | 10   | –   | –           | Bits        |
| Integral nonlinearity <sup>(2)</sup>                                                                                                                                           | INL    | $T_j = -55^{\circ}C$ to $125^{\circ}C$                                                         | –    | –   | $\pm 1.5$   | LSBs        |
| Differential nonlinearity                                                                                                                                                      | DNL    | No missing codes, guaranteed monotonic<br>$T_j = -55^{\circ}C$ to $125^{\circ}C$               | –    | –   | $\pm 1$     |             |
| Analog Inputs <sup>(2)</sup>                                                                                                                                                   |        |                                                                                                |      |     |             |             |
| ADC input ranges                                                                                                                                                               |        | Unipolar operation                                                                             | 0    | –   | 1           | V           |
|                                                                                                                                                                                |        | Bipolar operation                                                                              | –0.5 | –   | +0.5        | V           |
|                                                                                                                                                                                |        | Unipolar common mode range (FS input)                                                          | 0    | –   | +0.5        | V           |
|                                                                                                                                                                                |        | Bipolar common mode range (FS input)                                                           | +0.5 | –   | +0.6        | V           |
| Maximum external channel input ranges                                                                                                                                          |        | Adjacent channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | –   | $V_{CCADC}$ | V           |
| On-Chip Sensor Accuracy                                                                                                                                                        |        |                                                                                                |      |     |             |             |
| Temperature sensor error <sup>(1)(3)</sup>                                                                                                                                     |        | $T_j = -55^{\circ}C$ to $125^{\circ}C$ (with external REF)                                     | –    | –   | $\pm 3$     | $^{\circ}C$ |
|                                                                                                                                                                                |        | $T_j = -55^{\circ}C$ to $110^{\circ}C$ (with internal REF)                                     | –    | –   | $\pm 3.5$   | $^{\circ}C$ |
|                                                                                                                                                                                |        | $T_j = 110^{\circ}C$ to $125^{\circ}C$ (with internal REF)                                     | –    | –   | $\pm 5$     | $^{\circ}C$ |

Table 76: System Monitor Specifications (Cont'd)

| Parameter                             | Symbol            | Comments / Conditions                                                                                      | Min    | Typ  | Max       | Units  |
|---------------------------------------|-------------------|------------------------------------------------------------------------------------------------------------|--------|------|-----------|--------|
| Supply sensor error <sup>(4)</sup>    |                   | Supply voltages 0.72V to 1.2V,<br>$T_j = -40^{\circ}\text{C}$ to $100^{\circ}\text{C}$ (with external REF) | –      | –    | $\pm 0.5$ | %      |
|                                       |                   | Supply voltages 0.72V to 1.2V,<br>$T_j = -55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ (with external REF) | –      | –    | $\pm 1.0$ | %      |
|                                       |                   | All other supply voltages,<br>$T_j = -40^{\circ}\text{C}$ to $100^{\circ}\text{C}$ (with external REF)     | –      | –    | $\pm 1.0$ | %      |
|                                       |                   | All other supply voltages,<br>$T_j = -55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ (with external REF)     | –      | –    | $\pm 2.0$ | %      |
|                                       |                   | Supply voltages 0.72V to 1.2V,<br>$T_j = -40^{\circ}\text{C}$ to $100^{\circ}\text{C}$ (with internal REF) | –      | –    | $\pm 1.0$ | %      |
|                                       |                   | Supply voltages 0.72V to 1.2V,<br>$T_j = -55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ (with internal REF) | –      | –    | $\pm 2.0$ | %      |
|                                       |                   | All other supply voltages,<br>$T_j = -40^{\circ}\text{C}$ to $100^{\circ}\text{C}$ (with internal REF)     | –      | –    | $\pm 1.5$ | %      |
|                                       |                   | All other supply voltages,<br>$T_j = -55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ (with internal REF)     | –      | –    | $\pm 2.5$ | %      |
| <b>Conversion Rate<sup>(5)</sup></b>  |                   |                                                                                                            |        |      |           |        |
| Conversion time—continuous            | $t_{\text{CONV}}$ | Number of ADCCLK cycles                                                                                    | 26     | –    | 32        | Cycles |
| Conversion time—event                 | $t_{\text{CONV}}$ | Number of ADCCLK cycles                                                                                    | –      | –    | 21        | Cycles |
| DRP clock frequency                   | DCLK              | DRP clock frequency                                                                                        | 8      | –    | 250       | MHz    |
| ADC clock frequency                   | ADCCLK            | Derived from DCLK                                                                                          | 1      | –    | 5.2       | MHz    |
| DCLK duty cycle                       |                   |                                                                                                            | 40     | –    | 60        | %      |
| <b>SYSMON Reference<sup>(6)</sup></b> |                   |                                                                                                            |        |      |           |        |
| External reference                    | $V_{\text{REFP}}$ | Externally supplied reference voltage                                                                      | 1.20   | 1.25 | 1.30      | V      |
| On-chip reference                     |                   | Ground $V_{\text{REFP}}$ pin to AGND,<br>$T_j = -40^{\circ}\text{C}$ to $100^{\circ}\text{C}$              | 1.2375 | 1.25 | 1.2625    | V      |
|                                       |                   | Ground $V_{\text{REFP}}$ pin to AGND,<br>$T_j = -55^{\circ}\text{C}$ to $125^{\circ}\text{C}$              | 1.225  | 1.25 | 1.275     | V      |

**Notes:**

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a  $+4^{\circ}\text{C}$  offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of  $\pm 3^{\circ}\text{C}$  becomes  $+1^{\circ}\text{C}$  to  $+7^{\circ}\text{C}$  when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
6. Any variation in the reference voltage from the nominal  $V_{\text{REFP}} = 1.25\text{V}$  and  $V_{\text{REFN}} = 0\text{V}$  will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by  $\pm 4\%$  is permitted.

## SYSMON I2C/PMBus Interfaces

Table 77: SYSMON I2C Fast Mode Interface Switching Characteristics<sup>(1)</sup>

| Symbol       | Description             | Min | Max | Units   |
|--------------|-------------------------|-----|-----|---------|
| $T_{SMFCKL}$ | SCL Low time            | 1.3 | –   | $\mu$ s |
| $T_{SMFCKH}$ | SCL High time           | 0.6 | –   | $\mu$ s |
| $T_{SMFCKO}$ | SDAO clock-to-out delay | –   | 900 | ns      |
| $T_{SMFDCK}$ | SDAI setup time         | 100 | –   | ns      |
| $F_{SMFCLK}$ | SCL clock frequency     | –   | 400 | kHz     |

**Notes:**

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 78: SYSMON I2C Standard Mode Interface Switching Characteristics<sup>(1)</sup>

| Symbol       | Description             | Min | Max  | Units   |
|--------------|-------------------------|-----|------|---------|
| $T_{SMSCKL}$ | SCL Low time            | 4.7 | –    | $\mu$ s |
| $T_{SMSCKH}$ | SCL High time           | 4.0 | –    | $\mu$ s |
| $T_{SMSCKO}$ | SDAO clock-to-out delay | –   | 3450 | ns      |
| $T_{SMSDCK}$ | SDAI setup time         | 250 | –    | ns      |
| $F_{SMSCLK}$ | SCL clock frequency     | –   | 100  | kHz     |

**Notes:**

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

# Configuration Switching Characteristics

Table 79: Configuration Switching Characteristics

| Symbol                                  | Description                                                       | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |       |       |       |       | Units   |            |
|-----------------------------------------|-------------------------------------------------------------------|----------------------------------------------------------|-------|-------|-------|-------|---------|------------|
|                                         |                                                                   | 0.90V                                                    | 0.85V |       | 0.72V |       |         |            |
|                                         |                                                                   | -3                                                       | -2    | -1    | -2    | -1    |         |            |
| Power-up Timing Characteristics         |                                                                   |                                                          |       |       |       |       |         |            |
| T <sub>PL</sub>                         | Program latency.                                                  | 7.5                                                      | 7.5   | 7.5   | 7.5   | 7.5   | ms, Max |            |
| T <sub>POR</sub>                        | Power-on reset<br>(40 ms maximum ramp rate).                      | 65                                                       | 65    | 65    | 65    | 65    | ms, Max |            |
|                                         |                                                                   | 0                                                        | 0     | 0     | 0     | 0     | ms, Min |            |
|                                         | Power-on reset with POR override<br>(2 ms maximum ramp rate).     | 15                                                       | 15    | 15    | 15    | 15    | ms, Max |            |
|                                         |                                                                   | 5                                                        | 5     | 5     | 5     | 5     | ms, Min |            |
| T <sub>PROGRAM</sub>                    | Program pulse width.                                              | 250                                                      | 250   | 250   | 250   | 250   | ns, Min |            |
| CCLK Output (Master Mode)               |                                                                   |                                                          |       |       |       |       |         |            |
| T <sub>ICCK</sub>                       | Master CCLK output delay from INIT_B.                             |                                                          | 150   | 150   | 150   | 150   | 150     | ns, Min    |
| T <sub>MCCKL</sub> <sup>(1)</sup>       | Master CCLK clock Low time duty cycle.                            |                                                          | 40/60 | 40/60 | 40/60 | 40/60 | 40/60   | %, Min/Max |
| T <sub>MCCKH</sub>                      | Master CCLK clock High time duty cycle.                           |                                                          | 40/60 | 40/60 | 40/60 | 40/60 | 40/60   | %, Min/Max |
| F <sub>MCCK</sub>                       | Master SPI/BPI CCLK<br>frequency.                                 | XCKU3P, XCKU5P                                           | 125   | 125   | 125   | 60    | 60      | MHz, Max   |
|                                         |                                                                   | All other devices                                        | 150   | 150   | 150   | 125   | 125     |            |
| F <sub>MCCK_START</sub>                 | Master CCLK frequency at start of<br>configuration.               |                                                          | 2.70  | 2.70  | 2.70  | 2.70  | 2.70    | MHz, Typ   |
| F <sub>MCCKTOL</sub>                    | Frequency tolerance, master mode with<br>respect to nominal CCLK. |                                                          | ±15   | ±15   | ±15   | ±15   | ±15     | %, Max     |
| CCLK Input (Slave Mode)                 |                                                                   |                                                          |       |       |       |       |         |            |
| T <sub>SCCKL</sub>                      | Slave CCLK clock minimum Low time.                                |                                                          | 2.5   | 2.5   | 2.5   | 2.5   | 2.5     | ns, Min    |
| T <sub>SCCKH</sub>                      | Slave CCLK clock minimum High time.                               |                                                          | 2.5   | 2.5   | 2.5   | 2.5   | 2.5     | ns, Min    |
| F <sub>SCCK</sub>                       | Slave serial/<br>SelectMap CCLK<br>frequency.                     | XCKU3P, XCKU5P                                           | 125   | 125   | 125   | 60    | 60      | MHz, Max   |
|                                         |                                                                   | All other devices                                        | 125   | 125   | 125   | 125   | 125     |            |
| EMCCLK Input (Master Mode)              |                                                                   |                                                          |       |       |       |       |         |            |
| T <sub>EMCCKL</sub>                     | External master CCLK Low time.                                    |                                                          | 2.5   | 2.5   | 2.5   | 2.5   | 2.5     | ns, Min    |
| T <sub>EMCCKH</sub>                     | External master CCLK High time.                                   |                                                          | 2.5   | 2.5   | 2.5   | 2.5   | 2.5     | ns, Min    |
| F <sub>EMCCK</sub>                      | External master CCLK<br>frequency.                                | XCKU3P, XCKU5P                                           | 125   | 125   | 125   | 60    | 60      | MHz, Max   |
|                                         |                                                                   | All other devices                                        | 150   | 150   | 150   | 125   | 125     |            |
| Internal Configuration Access Port      |                                                                   |                                                          |       |       |       |       |         |            |
| F <sub>ICAPCK</sub>                     | Internal configuration access port<br>(ICAPE3).                   |                                                          | 200   | 200   | 200   | 150   | 150     | MHz, Max   |
| Slave Serial Mode Programming Switching |                                                                   |                                                          |       |       |       |       |         |            |
| T <sub>DCCK</sub> /T <sub>CCKD</sub>    | D <sub>IN</sub> setup/hold.                                       |                                                          | 3.0/0 | 3.0/0 | 3.0/0 | 4.0/0 | 4.0/0   | ns, Min    |
| T <sub>CCO</sub>                        | D <sub>OUT</sub> clock to out.                                    |                                                          | 8.0   | 8.0   | 8.0   | 9.0   | 9.0     | ns, Max    |

Table 79: Configuration Switching Characteristics (Cont'd)

| Symbol                                      | Description                                                 | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |               |               |               |                | Units          |             |
|---------------------------------------------|-------------------------------------------------------------|----------------------------------------------------------|---------------|---------------|---------------|----------------|----------------|-------------|
|                                             |                                                             | 0.90V                                                    | 0.85V         |               | 0.72V         |                |                |             |
|                                             |                                                             | -3                                                       | -2            | -1            | -2            | -1             |                |             |
| SelectMAP Mode Programming Switching        |                                                             |                                                          |               |               |               |                |                |             |
| T <sub>SMDCCCK</sub> /T <sub>SMCCKD</sub>   | D[31:00] setup/hold.                                        | XCKU3P, XCKU5P                                           | 4.5/0         | 4.5/0         | 4.5/0         | 8.0/0          | 8.0/0          | ns, Min     |
|                                             |                                                             | All other devices                                        | 3.5/0         | 3.5/0         | 3.5/0         | 4.5/0          | 4.5/0          |             |
| T <sub>SMCSCCK</sub> /T <sub>SMCCCKCS</sub> | CSI_B setup/hold.                                           | XCKU3P, XCKU5P                                           | 4.5/0         | 4.5/0         | 4.5/0         | 7.0/0          | 7.0/0          | ns, Min     |
|                                             |                                                             | All other devices                                        | 4.0/0         | 4.0/0         | 4.0/0         | 5.0/0          | 5.0/0          |             |
| T <sub>SMWCCK</sub> /T <sub>SMCCKW</sub>    | RDWR_B setup/hold.                                          | XCKU3P, XCKU5P                                           | 10.0/0        | 10.0/0        | 10.0/0        | 17.0/0         | 17.0/0         | ns, Min     |
|                                             |                                                             | All other devices                                        | 10.0/0        | 10.0/0        | 10.0/0        | 11.0/0         | 11.0/0         |             |
| T <sub>SMCKCSO</sub>                        | CSO_B clock to out (330Ω pull-up resistor required).        | XCKU3P, XCKU5P                                           | 7.0           | 7.0           | 7.0           | 10.0           | 10.0           | ns, Max     |
|                                             |                                                             | All other devices                                        | 7.0           | 7.0           | 7.0           | 7.0            | 7.0            |             |
| T <sub>SMCO</sub>                           | D[31:00] clock to out in readback.                          | XCKU3P, XCKU5P                                           | 8.0           | 8.0           | 8.0           | 10.0           | 10.0           | ns, Max     |
|                                             |                                                             | All other devices                                        | 8.0           | 8.0           | 8.0           | 8.0            | 8.0            |             |
| F <sub>RBCK</sub>                           | Readback frequency.                                         | XCKU3P, XCKU5P                                           | 125           | 125           | 125           | 60             | 60             | MHz, Max    |
|                                             |                                                             | All other devices                                        | 125           | 125           | 125           | 125            | 125            |             |
| Boundary-Scan Port Timing Specifications    |                                                             |                                                          |               |               |               |                |                |             |
| T <sub>TAPTCK</sub> /T <sub>TCKTAP</sub>    | TMS and TDI setup/hold.                                     |                                                          | 3.0/<br>2.0   | 3.0/<br>2.0   | 3.0/<br>2.0   | 3.0/<br>2.0    | 3.0/<br>2.0    | ns, Min     |
| T <sub>TCKTDO</sub>                         | TCK falling edge to TDO output.                             |                                                          | 7.0           | 7.0           | 7.0           | 7.0            | 7.0            | ns, Max     |
| F <sub>TCK</sub>                            | TCK frequency.                                              | XCKU15P                                                  | 66            | 66            | 66            | 50             | 50             | MHz, Max    |
|                                             |                                                             | All other devices                                        | 66            | 66            | 66            | 66             | 66             |             |
| BPI Master Flash Mode Programming Switching |                                                             |                                                          |               |               |               |                |                |             |
| T <sub>BPICCO</sub>                         | A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out. |                                                          | 10            | 10            | 10            | 10             | 10             | ns, Max     |
| T <sub>BPIDCC</sub> /T <sub>BPICCD</sub>    | D[15:00] setup/hold.                                        | XCKU3P, XCKU5P                                           | 4.5/0         | 4.5/0         | 4.5/0         | 8.0/0          | 8.0/0          | ns, Min     |
|                                             |                                                             | All other devices                                        | 3.5/0         | 3.5/0         | 3.5/0         | 4.5/0          | 4.5/0          |             |
| SPI Master Flash Mode Programming Switching |                                                             |                                                          |               |               |               |                |                |             |
| T <sub>SPIDCC</sub> /T <sub>SPICCD</sub>    | D[03:00] setup/hold.                                        |                                                          | 3.0/0         | 3.0/0         | 3.0/0         | 4.0/0          | 4.0/0          | ns, Min     |
| T <sub>SPIDCC</sub> /T <sub>SPICCD</sub>    | D[07:04] setup/hold.                                        | XCKU3P, XCKU5P                                           | 4.5/0         | 4.5/0         | 4.5/0         | 8.0/0          | 8.0/0          | ns, Min     |
|                                             |                                                             | All other devices                                        | 3.5/0         | 3.5/0         | 3.5/0         | 4.5/0          | 4.5/0          |             |
| T <sub>SPICCM</sub>                         | MOSI clock to out.                                          |                                                          | 8.0           | 8.0           | 8.0           | 8.0            | 8.0            | ns, Max     |
| T <sub>SPICCF</sub>                         | FCS_B clock to out.                                         |                                                          | 8.0           | 8.0           | 8.0           | 8.0            | 8.0            | ns, Max     |
| DNA Port Switching                          |                                                             |                                                          |               |               |               |                |                |             |
| F <sub>DNACK</sub>                          | DNA port frequency.                                         |                                                          | 200           | 200           | 200           | 175            | 175            | MHz, Max    |
| STARTUPE3 Ports                             |                                                             |                                                          |               |               |               |                |                |             |
| T <sub>USRCCLKO</sub>                       | STARTUPE3 USRCCLKO input port to CCLK pin output delay.     |                                                          | 0.25/<br>6.00 | 0.25/<br>6.50 | 0.25/<br>7.50 | 0.25/<br>9.00  | 0.25/<br>9.00  | ns, Min/Max |
| T <sub>DO</sub>                             | DO[3:0] ports to D03-D00 pins output delay.                 |                                                          | 0.25/<br>6.70 | 0.25/<br>7.70 | 0.25/<br>8.40 | 0.25/<br>10.00 | 0.25/<br>10.00 | ns, Min/Max |
| T <sub>DTS</sub>                            | DTS[3:0] ports to D03-D00 pins 3-state delays.              |                                                          | 0.25/<br>6.70 | 0.25/<br>7.70 | 0.25/<br>8.40 | 0.25/<br>10.00 | 0.25/<br>10.00 | ns, Min/Max |

Table 79: Configuration Switching Characteristics (Cont'd)

| Symbol                  | Description                                                                                                       | Speed Grade and<br>V <sub>CCINT</sub> Operating Voltages |               |                |                |                | Units       |
|-------------------------|-------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|---------------|----------------|----------------|----------------|-------------|
|                         |                                                                                                                   | 0.90V                                                    | 0.85V         |                | 0.72V          |                |             |
|                         |                                                                                                                   | -3                                                       | -2            | -1             | -2             | -1             |             |
| T <sub>FCSBO</sub>      | FCSBO port to FCS_B pin output delay.                                                                             | 0.25/<br>6.90                                            | 0.25/<br>7.50 | 0.25/<br>8.40  | 0.25/<br>9.80  | 0.25/<br>9.80  | ns, Min/Max |
| T <sub>FCSBTS</sub>     | FCSBTS port to FCS_B pin 3-state delay.                                                                           | 0.25/<br>6.90                                            | 0.25/<br>7.50 | 0.25/<br>8.40  | 0.25/<br>9.80  | 0.25/<br>9.80  | ns, Min/Max |
| T <sub>USRDONEO</sub>   | USRDONEO port to DONE pin output delay.                                                                           | 0.25/<br>8.60                                            | 0.25/<br>9.40 | 0.25/<br>10.50 | 0.25/<br>12.10 | 0.25/<br>12.10 | ns, Min/Max |
| T <sub>USRDONETS</sub>  | USRDONETS port to DONE pin 3-state delay.                                                                         | 0.25/<br>8.60                                            | 0.25/<br>9.40 | 0.25/<br>10.50 | 0.25/<br>12.10 | 0.25/<br>12.10 | ns, Min/Max |
| T <sub>DI</sub>         | D03-D00 pins to DI[3:0] ports input delay.                                                                        | 0.5/<br>2.6                                              | 0.5/<br>3.1   | 0.5/<br>3.5    | 0.5/<br>4.0    | 0.5/<br>4.0    | ns, Min/Max |
| F <sub>CFGMCLK</sub>    | STARTUPE3 CFGMCLK output frequency.                                                                               | 50                                                       | 50            | 50             | 50             | 50             | MHz, Typ    |
| F <sub>CFGMCLKTOL</sub> | STARTUPE3 CFGMCLK output frequency tolerance.                                                                     | ±15                                                      | ±15           | ±15            | ±15            | ±15            | %, Max      |
| T <sub>DCI_MATCH</sub>  | Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted. | 4                                                        | 4             | 4              | 4              | 4              | ms, Max     |

**Notes:**

1. When the CCLK is sourced from the EMCCLK pin with a divide-by-one setting, the external EMCCLK must meet this duty-cycle requirement.

## Revision History

The following table shows the revision history for this document.

| Date       | Version | Description of Revisions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 06/26/2017 | 1.4     | Updated <a href="#">Table 20</a> , <a href="#">Table 21</a> , and <a href="#">Table 22</a> to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.2.<br>XCKU13P: -2E, -2I, -1E, -1I<br>Updated <a href="#">Note 11</a> in <a href="#">Table 2</a> for clarity. Revised the -3E and -1LI/-2LE (V <sub>CCINT</sub> = 0.72V) speed files in <a href="#">Table 28</a> , <a href="#">Table 29</a> , <a href="#">Table 30</a> , <a href="#">Table 40</a> , <a href="#">Table 41</a> , <a href="#">Table 42</a> , <a href="#">Table 43</a> , <a href="#">Table 44</a> . Updated the F <sub>MAX</sub> symbol names and values in <a href="#">Table 34</a> . Added <a href="#">Note 1</a> to <a href="#">Table 36</a> . Added <a href="#">Note 3</a> to <a href="#">Table 75</a> . |
| 05/08/2017 | 1.3     | Updated <a href="#">Table 21</a> and <a href="#">Table 22</a> to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1.<br>XCKU9P: -2E, -2I, -1E, -1I<br>Removed the MIPI_DPHY_DCI_LP standard from <a href="#">Table 9</a> (HD I/O banks never supported DCI). Revised the minimum 32.75 Gb/s sinusoidal jitter in <a href="#">Table 69</a> .                                                                                                                                                                                                                                                                                                                                                                                                                            |

| Date       | Version | Description of Revisions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 04/11/2017 | 1.2     | <p>Updated the <a href="#">Summary</a> description. In <a href="#">Table 1</a>, updated and added data, and updated <a href="#">Note 7</a>, added <a href="#">Note 8</a>, <a href="#">Note 9</a>, and <a href="#">Note 10</a>. Updated and added data to <a href="#">Table 2</a>, revised <a href="#">Note 11</a> and added <a href="#">Note 12</a> and <a href="#">Note 13</a>. Updated <a href="#">Table 3</a> and added <a href="#">Note 6</a>. Added specifications to <a href="#">Table 4</a> through <a href="#">Table 6</a>. Updated maximum <math>V_{ICM}</math> and <a href="#">Note 1</a> in <a href="#">Table 18</a>. Updated the maximum <math>V_{ODIFF}</math> in <a href="#">Table 19</a>.</p> <p>Updated <a href="#">Table 20</a>, <a href="#">Table 21</a>, and <a href="#">Table 22</a> to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1.</p> <p>XCKU3P: -2E, -2I, -1E, -1I</p> <p>XCKU5P: -2E, -2I, -1E, -1I</p> <p>Added <a href="#">Note 1</a> to <a href="#">Table 21</a>. Updated <a href="#">Table 23</a>. Updated <a href="#">Table 24</a> and added <a href="#">Note 2</a>. Added <a href="#">Table 25</a>. Updated <a href="#">Table 27</a> and added <a href="#">Note 3</a>. Many revisions to the speed specifications in <a href="#">Table 28</a>, <a href="#">Table 29</a>, <a href="#">Table 30</a>, <a href="#">Table 33</a>, <a href="#">Table 34</a>, <a href="#">Table 35</a>, <a href="#">Table 40</a>, <a href="#">Table 41</a>, <a href="#">Table 42</a>, <a href="#">Table 43</a>, <a href="#">Table 44</a>, and <a href="#">Table 45</a>. Updated <math>V_L</math> and <math>V_H</math> values in <a href="#">Table 31</a>. In <a href="#">Table 35</a>, added <math>T_{MINPER\_CLK}</math> and <a href="#">Note 1</a>, and revised <math>F_{REFCLK}</math>. Added <math>MMCM\_F_{DPRCLK\_MAX}</math> to <a href="#">Table 38</a> and <math>PLL\_F_{DPRCLK\_MAX}</math> to <a href="#">Table 39</a>. Updated <a href="#">Table 46</a>. Revised the <a href="#">GTH Transceiver Specifications</a> and <a href="#">GTH Transceiver Specifications</a> sections. Revised the <a href="#">Integrated Interface Block for Interlaken</a> and <a href="#">Integrated Interface Block for 100G Ethernet MAC and PCS</a> sections. Updated the <a href="#">System Monitor Specifications</a> section including <a href="#">On-Chip Sensor Accuracy</a> and adding <a href="#">Note 3</a> to <a href="#">Table 76</a>. Removed timing diagrams from the <a href="#">SYSMON I2C/PMBus Interfaces</a> section. Updated the <a href="#">Configuration Switching Characteristics</a> section. Removed the <a href="#">eFUSE Programming Conditions</a> table and added the specifications to <a href="#">Table 2</a> and <a href="#">Table 3</a>. Updated <a href="#">Table 79</a>. Updated the <a href="#">Automotive Applications Disclaimer</a>.</p> |
| 05/09/2016 | 1.1     | <p>In <a href="#">Table 1</a> revised <math>V_{IN}</math> for HP I/O banks. Updated <a href="#">Note 5</a> in <a href="#">Table 3</a>. Added values to <a href="#">Table 7</a>. Added MIPI_DPHY_DCI to <a href="#">Table 9</a>, <a href="#">Table 10</a>, and <a href="#">Table 12</a>. Updated and added notes in <a href="#">Table 18</a> and <a href="#">Table 19</a>. Updated <a href="#">Table 20</a> speed specifications for Vivado Design Suite 2016.1. Removed <a href="#">Table 23</a>, <a href="#">Video Codec Unit Performance</a>. Updated <a href="#">Table 24</a>. Expanded and updated <a href="#">Table 27</a>. Updated <a href="#">Table 28</a> and <a href="#">Table 29</a>. Updated <a href="#">Table 31</a> and <a href="#">Table 32</a> with MIPI D-PHY values. Updated <a href="#">Table 31</a> and <a href="#">Table 32</a>. In <a href="#">Table 33</a>, added the <a href="#">Block RAM and FIFO Clock-to-Out Delays</a> section. Updated <a href="#">Table 40</a> to <a href="#">Table 44</a>. Revised the symbol names in <a href="#">Table 43</a>. Revised typical values in <a href="#">Table 48</a>. Updated the -2 (0.72V) and -1 (0.72V) values in <a href="#">Table 50</a>. Added <a href="#">Table 53</a> and <a href="#">Table 65</a>. Added <a href="#">Note 2</a> to <a href="#">Table 59</a>. Revised <a href="#">Table 67</a>. Revised data and added notes to <a href="#">Table 62</a>, <a href="#">Table 71</a>, and <a href="#">Table 74</a>. Revised INL in <a href="#">Table 76</a>. Added notes to <a href="#">Table 77</a> and <a href="#">Table 78</a>. Many revised sections in <a href="#">Table 79</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 11/24/2015 | 1.0     | Initial Xilinx release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

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