Vishay Electro-Films

Thin Film Single Value Chip and Wire Capacitors
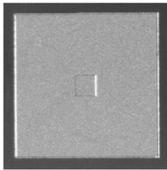
Product may not be to scale

FEATURES

- Small size: 0.020 to 0.060 inches square

- Substrate: silicon with gold backing

- Dielectric: silicon dioxide/silicon nitride

- Capacitance range: 0.5pF to 1000pF

The NC series of thin film capacitors has the advantage of increased performance and smaller size when compared with its thick film counterparts. These chips are available in sizes down to 20 mil square and in capacitances up to 1000pF.
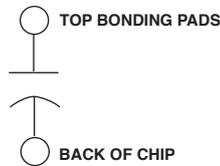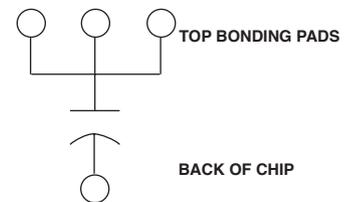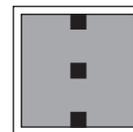
Parts require epoxy or eutectic die attach to substrate and one wire bond.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The NC's are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

The NC series of capacitor chips are designed for assembly in hybrid circuits using conventional wire-bonding techniques. They provide excellent stability and performance, and their small size gives the hybrid designer greater layout flexibility.

They are available as MNOS or MOS capacitors. The MOS version is to be preferred when low dielectric absorption is required.

ELECTRICAL SCHEMATIC
NCA/NCB/NCC

TOP BONDING PADS

BACK OF CHIP

ELECTRICAL SCHEMATIC
NCD/NCE

TOP BONDING PADS

BACK OF CHIP

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Peak voltage at + 25°C	1.5 x working voltage
Dissipation factor, 1kHz, $1V_{rms}$, + 25°C	0.05% MNOS 0.1% MOS
Q at 1mHz, $50mV_{rms}$, + 25°C	1000 minimum
TCC, - 55°C to + 150°C	+ 45 ± 25ppm/°C MNOS + 15 ± 25ppm/°C MOS
Insulation resistance at working voltage, + 25°C	10^9 minimum
Operating temperature range	- 55°C to + 125°C
Thermal shock	± 0.25% + 0.25pF maximum ΔC/C
Moisture resistance, MIL-STD-202, Method 106	± 1.0% + 0.25pF maximum ΔC/C
Short time overload, + 25°C, 5 seconds, 1.5 x working voltage	± 0.25% + 0.25pF maximum
High temperature exposure, 100 hours at 150°C ambient	± 0.25% + 0.25pF maximum ΔC/C
Life, MIL-STD-202, Method 108 Condition D, + 125°C ambient, 100 hours at working voltage	± 0.25% + 0.25pF maximum ΔC/C

DC WORKING VOLTAGES VALUES AND TOLERANCES

NCA 0.020 Inches Square

NA = NOT AVAILABLE
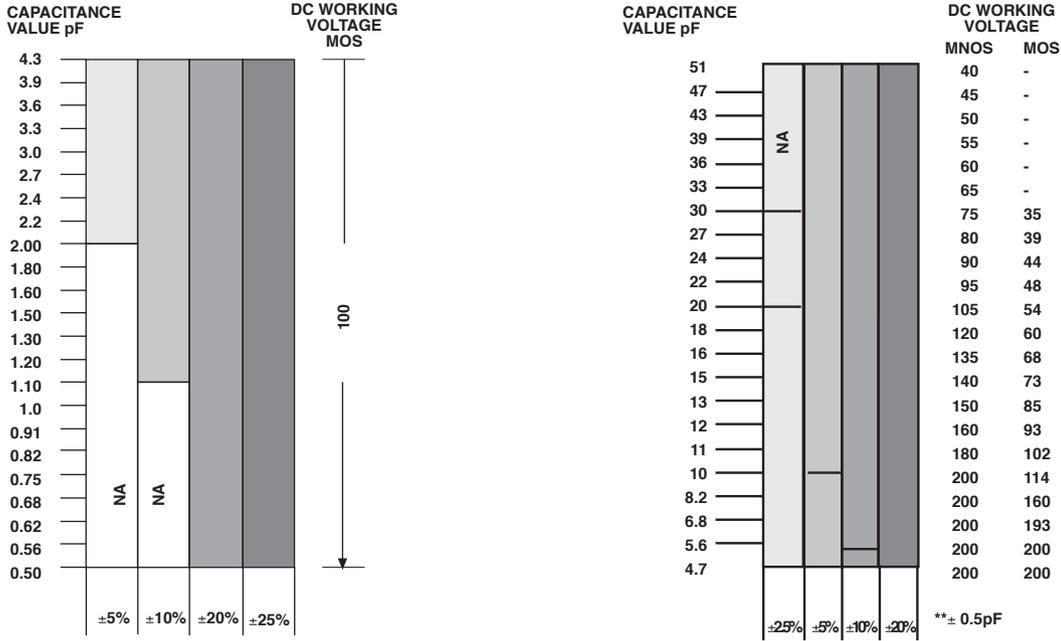
**** ± 0.5pF

NCB 0.030 inches square   NCC 0.040 inches square   NCD 0.055 inches square / NCE 0.060 inches square

CHIP CAPACITORS
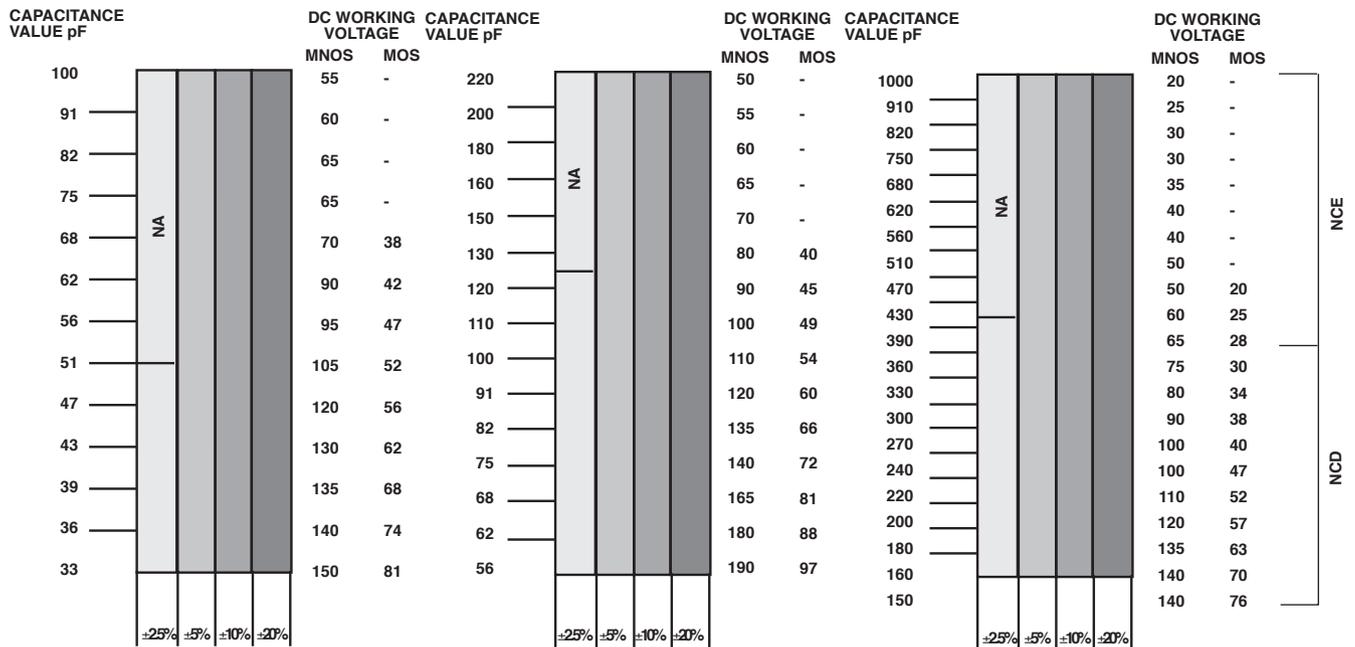
DIMENSIONS

0.5pF - 1.3pF	1.4pF - 3.9pF	4pF - 9.1pF	10pF - 51pF

NCA
0.020 ± 0.003 inches square

33pF - 100pF	56pF - 220pF	150pF - 510pF	360pF - 1000pF

CHIP CAPACITORS
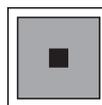
NCB	**NCC**	**NCD**	**NCE**
0.030 ± 0.003 inches square	0.040 ± 0.003 inches square	0.055 ± 0.003 inches square	0.060 ± 0.003 inches square
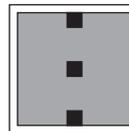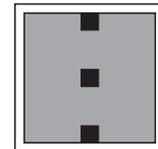
MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	Per Diagrams
Chip thickness	0.010 ± 0.002 (0.25 ± 0.05mm)
Chip substrate material	Semiconductor silicon
Dielectric	Silicon dioxide/Silicon nitride
Bond pad	0.005 x 0.005 minimum, 10kÅ aluminum
Backing	3kÅ minimum gold

OPTIONS: Gold bond pads 15kÅ
Lower profile version is available, Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 2pF, ± 5%, 20 mil MOS capacitor, Aluminum Pads, Class H visual inspection

W	NCA	017	2000	C	J
INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	CAPACITANCE VALUE (pF)	MULTIPLIER CODE	TOLERANCE CODE
W = 100% visually inspected parts in matrix trays per MIL-STD-883	NCA	**017** = MOS Aluminum	Use first 4 digits significant digits of capacitance	**C** = 0.001	**D** = ± 0.5pF
	NCB	**000** = MNOS Aluminum		**B** = 0.01	**H** = ± 2.5%*
	NCC			**A** = 0.1	**J** = ± 5.0%
X = Sample, commercial visually inspected loaded in matrix trays (4% AQL)	NCD			**0** = 1	**K** = ± 10%
	NCE				**M** = ± 20%
					L = ± 25%
					N = ± 50%
					* MOS only