XRT7298

DS3/STS-1, E3
Integrated Line Transmitter

April 2000-2

FEATURES

- Fully Integrated Transmit Interface for DS3/STS-1 or E3
- Integrated Pulse Shaping Circuit
- Compliance with Compatibility Bulletin 119
- Compliance with CCITT Recommendations G.703 & G.824
- Compliance with Bellcore TR-NWT-000499
- Compliance with ANSI T1.404
- Built-in B3ZS/HDB3 Encoder and Decoder
- Remote and Local Loopback Functions
- Single 5V Power Supply
- Contains Transmit Clock Duty Cycle Correction Circuit on Chip

APPLICATIONS

- Interface for SONET, DS-3 and E3 Network Equipment
- Digital Cross-Connect Systems
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals

GENERAL DESCRIPTION

The XRT7298 is a fully integrated PCM Line Driver IC intended for DS3 (44.736Mbps) or E3 (34.368Mbps) applications. It can also be used for transmitting SONET STS-1 (51.84Mbps) signals over coaxial cable. The IC is designed to complement either XRT7295 DS3/SONET STS-1 or XRT7295E E3 Integrated Line Receivers. The XRT7298 converts input clock and dual-rail unipolar data into AMI pulses according to AT&T Technical Advisory No. 34 or CCITT G.703 recommendations.

The device provides B3ZS (DS3) or HDB3 (E3) encoding functions for data to be transmitted to the line. A complimentary decoder circuit is also included in the chip for decoding received signals from an external line receiver. Both encoder and decoder functions can be disabled independently through external control pins. In the receive direction, coding errors and bipolar violations are detected and flagged at an output pin.

On-chip pulse shaper circuitry eliminates normally required external components for line equalization to meet the cross-connect template. For system level trouble-shooting and testing, both local and remote loop-backs are possible with the built-in loop-back circuit.

The XRT7298 device contains an “on-chip” Transmit Clock Duty Cycle Correction circuit. This circuit guarantees that the XRT7298 device will generate pulses, that will meet the various “pulse-template” requirements (e.g., ITU-T G.703 for E3, ANSI T1.404 and Bellcore TR-NWT-000499 for DS3); provided the user supplies a “transmit clock” signal, to the TCLK input pin (pin 9); that has duty cycle ranging from 30% to 70%. This feature eliminates the need for the user to provide a transmit clock signal (to TCLK), with a duty cycle ranging from 47% to 53% (for E3) and 45% to 55% (for DS3).

The XRT7298 is manufactured using BiCMOS technology and is packaged in a 28-pin PDIP or SOJ packages. The device requires a single 5V power supply and consumes a maximum power of 700mW. (Line current feed + device dissipation).

ORDERING INFORMATION

Part No.	Package	Operating TemperatureRange
XRT7298IP	28 Lead 600 Mil PDIP	-40°C to + 85°C
XRT7298IW	28 J Lead 300 Mil JEDEC SOJ	-40°C to + 85°C

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BLOCK DIAGRAM

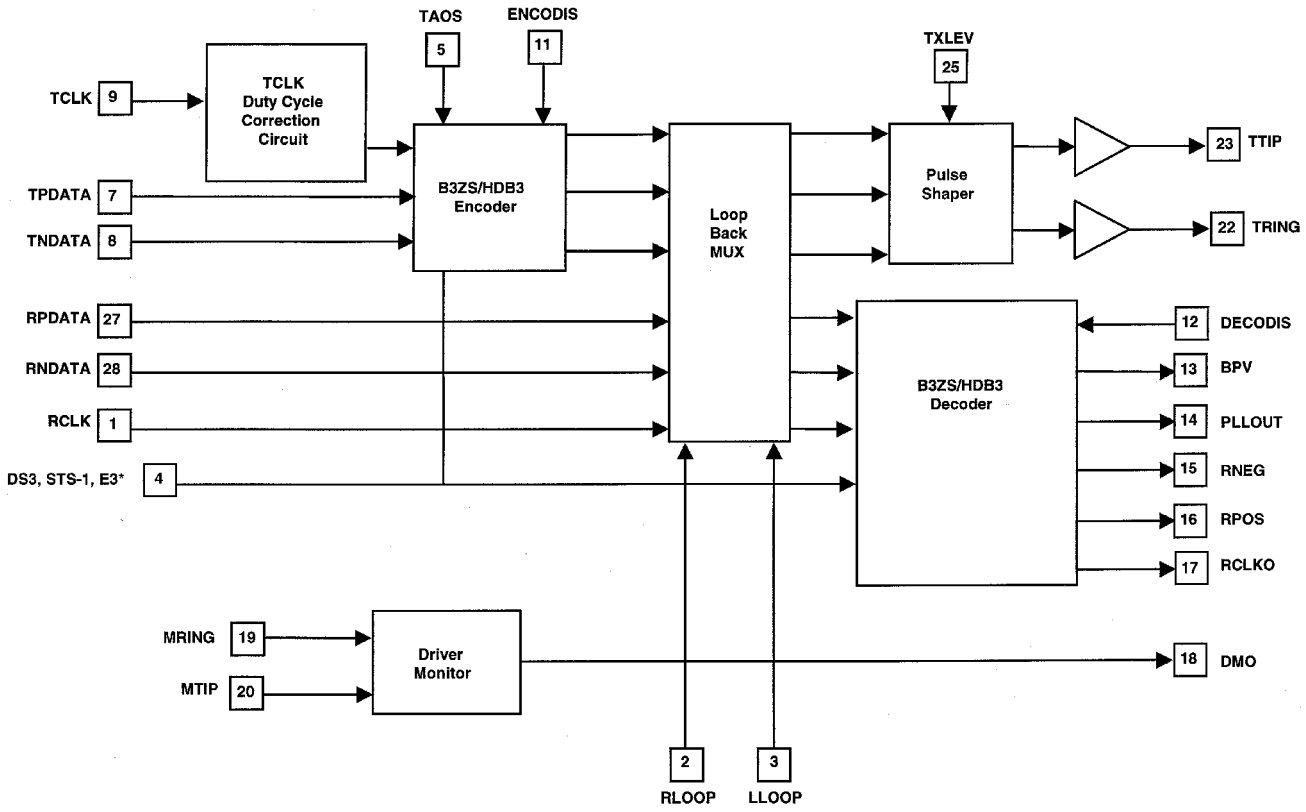
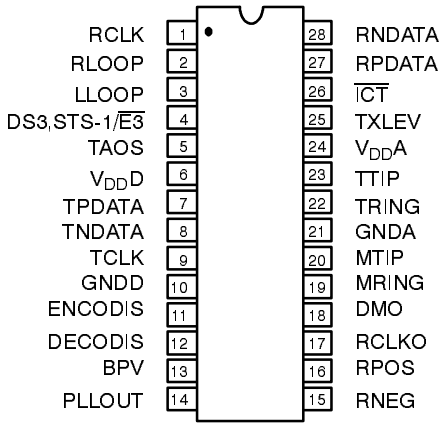
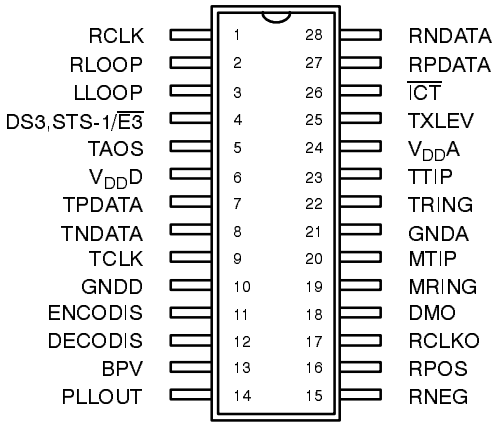


Figure 1. XRT7298 Block Diagram

PIN CONFIGURATION



28 Lead PDIP (0.600")



28 Lead SOJ (Jedec,0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	RCLK	I	**Receive Clock Input.** Input sampling clock for RPDATA and RNDATA.
2	RLOOP	I	**Remote Loop Back.** A high on this pin causes RPDATA and RNDATA to transmitted to the line using RCLK. Setting RLOOP and LLOOP high simultaneously is not permitted.
3	LLOOP	I	**Local Loop Back.** A high on this pin causes TPDATA and TNDATA to pass through the encoder and output at RPOS and RNEG respectively. Setting LLOOP and RLOOP high simultaneously is not permitted.
4	DS3,STS-1/ $\overline{E3}$	I	**DS3, STS-1 or $\overline{E3}$ Select Pin** . A high on this pin selects DS3 or STS-1 operation and sets the encoder and decoder in B3ZS mode. A low selects E3 and sets the encoder and decoder in HDB3 mode.
5	TAOS	I	**Transmit All Ones Select**. A high on this pin causes a continuous AMI all 1's pattern to be transmitted to the line. The frequency is determined by TCLK.
6	$V_{DD}D$		**5 V Digital Supply** (± 5%) for all logic circuitry.
7	TPDATA	I	**Transmit Positive Data**. TPDATA is sampled on the falling edge of TCLK. Pin 7 and pin 8 can be tied together for binary input signals.
8	TNDATA	I	**Transmit Negative Data.** TNDATA is sampled on the falling edge of TCLK. Pin 7 and pin 8 can be tied together for binary input signals.
9	TCLK	I	**Transmit Clock** for TPDATA and TNDATA.
10	GNDD		**Digital Ground** for all logic circuitry.
11	ENCODIS	I	**Encoder Disable.** A high on this pin disables B3ZS or HDB3 encoding functions, unless overridden by TAOS request. This pin must be set high if TPDATA and TNDATA are already encoded.
12	DECODIS	I	**Decoder Disable**. A high on this pin disables B3ZS or HDB3 decoding functions.

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Type	Description
13	BPV	O	**Bipolar Violation Output**. This pin goes high for one bit period when a bipolar violation not corresponding to the appropriate coding rule or coding error is detected in the RPDATA/ RNDATA signals.
14	PLLOUT	O	**PLL Clock Output.** Clock output synchronized to TCLK.
15	RNEG	O	**Receive Negative Data.** This signal is the decoded version of RNDATA.[1]
16	RPOS	O	**Receive Positive Data**. This signal is the decoded version of RPDATA.[1]
17	RCLKO	O	**Receive Clock Output**. This signal is the inverted version of RCLK.
18	DMO	O	**Driver Monitor Output.** If no transmitted AMI signal is present on MTIP and MRING for 128 ± 32 TCLK clock periods. DMO goes high until the next AMI signal is detected.
19	MRING	I	**Monitor Ring Input**. AMI signal from TRING can be connected to this pin for line driver failure detection. Internally pulled high.
20	MTIP	I	**Monitor Tip Input**. AMI signal from TTIP can be connected to this pin for line driver failure detection. Internally pulled high.
21	GNDA		**Analog Ground** for analog circuitry.
22	TRING	O	**Transmit Ring Output**. Transmit AMI signal is driven to the line via a 1:1 transformer from this pin.
23	TTIP	O	**Transmit Tip Output.** Transmit AMI signal is driven to the line via a 1:1 transformer from this pin.
24	$V_{DD}A$	-	**5V Analog Supply (± 5%)** for analog circuitry.
25	TXLEV	I	**Transmit Level Select.** The output signal amplitude at TTIP and TRING can be varied by setting this pin high or low. When the cable length is greater than 225 ft. TXLEV should be set high. When it is below 225 ft, it should be set low. This pin is active only with pin 4 set to DS3 or STS-1 mode.
26	ICT	I	**In-circuit Testing.** A low at this pin causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. Internally pulled high.
27	RPDATA	I	**Receive Positive Data**. NRZ input data to the decoder block. Sampled on the falling edge of RCLK.
28	RNDATA	I	**Receive Negative Data**. NRZ input data of the decoder block. Sampled on falling edge of RCLK.

Note:
[1] If a bipolar violation occurs, RPOS and RNEG can correspond to the decoded versions of RNDATA and RPDATA respectively. If DECODIS is high, RPOS and RNEG always track RPDATA and RNDATA respectively.

ELECTRICAL CHARACTERISTICS ***(See Figure 8)***

Test Conditions: V_{DD} = 5V ± 5%, T_A = -40°C to +85°C, unless otherwise specified. All timing characteristics are measured with 10pF loading.

Symbol	Parameter	Min.	Typ.	Max.	Units
AC Electrical Characteristics					
	TCLK Clock Duty Cycle (DS3 / STS-1)	30	50	70	%
	TCLK Clock Duty Cycle (E3)	30	50	70	%
tR	TCLK Clock Rise Time (10% to 90%)			4.0	ns
tF	TCLK Clock Fall Time (10% to 90%)			4.0	ns
tTSU	TPDATA/TNDATA to TCLK Falling Set Up Time	4.0			ns
tTHO	TPDATA/TNDATA to TCLK Falling Hold Time	5.0			ns
tTDY	TTIP/TRING to TCLK Rising Propagation Delay [1]	0.6		14	ns
	RCLK Clock Duty Cycle	45	50	55	%
tR	RCLK Clock Rise Time (10% to 90%)			4.0	ns
tF	RCLK Clock Fall Time (10% to 90%)			4.0	ns
tRSU	RPDATA/RNDATA to RCLK Falling Set Up Time	4.0			ns
tRHO	RPDATA/RNDATA to RCLK Falling Hold Time	5.0			ns
tR	RCLKO Clock Rise Time (10% to 90%)			4.0	ns
tF	RCLKO Clock Fall Time (10% to 90%)			4.0	ns
tRDY	RPOS/RNEG/RNRZ to RCLKO Rising Propagation Delay [2]			4.0	ns
DC Electrical Characteristics					
$V_{DD}D$, $V_{DD}A$	DC Supply Voltage	4.75	5	5.25	V
	Supply Current [3]			133	mA
V_{IL}	Input Low Voltage	0		0.5	V
V_{IH}	Input High Voltage	V_{DD}* 0.7		$V_{DD}D$	V
V_{OL}	Output Low Voltage I_{OUT}=-4.0mA	GNDD		0.4	V
V_{OH}	Output High Voltage I_{OUT}=3.0mA	$V_{DD}D$ - 0.5		$V_{DD}D$	V
I_L	Input Leakage Current [4]			± 10	µA
	Pin 19/20/26 (Input=0V)	-50		-150	µA
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

Notes:

[1] When the encoder is enabled a handling delay of six TCLK clock cycles for B3ZS and seven clock cycles for HDB3 always exists between TPDATA/TNDATA and TTIP/TRING. The handling delay is reduced to three and a half cycles when the encoder is disabled.

[2] When the decoder is enabled a handling delay of six and a half RCLK clock cycles will always exist between RPDATA/RNDATA and RPOS/RNEG. The handling delay is reduced to one and half RCLK clock cycles when the decoder is disabled.

[3] Supply current is measured with transmitter sending all ones AMI signal and with Transmit Level (TXLEV) set to high.

[4] All inputs except pin 19, 20 and pin 26.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply ..... -0.5 to +6.5V

Storage Temperature ..... -65°C to 150°C

Voltage At Any Pin ..... -0.5V to V_{DD} +0.5V

Power Dissipation SOJ Pkg. 725mW

Power Dissipation DIP Pkg. 1W

Input Voltage (Any Pin) ..... -0.5V to V_{DD} + 0.5V

Input Current (Any Pin) 10mA

SYSTEM DESCRIPTION

B3ZS/HDB3 ENCODER

Data to be transmitted is input to the encoder block to be encoded either in B3ZS or HDB3 as determined by the state of the DS3,STS-1/$\overline{E3}$ pin. Input data format can be unipolar or binary. For binary signals, TPDATA and TNDATA need to be connected together externally. The line code used for DS3 is B3ZS. In this mode, each block of three consecutive zeros is removed and replaced by one of two codes which contain bipolar violation. These replacement codes are B0V and 00V; where B indicates a pulse conforming with the bipolar rule and V represents a pulse violating the rule. The choice of these codes is made such that an odd number of B pulses will be transmitted between consecutive bipolar violation (V) pulses. For E3 format, the line code is HDB3. The encoding rule of HDB3 is similar to B3ZS except the number of consecutive zeros is increased to four before a code replacement can take place. The replacement codes in this case are 000V and B00V.

STS-1 operation is achieved by placing the part in the DS3 mode and using 51.84 MHz clocks. Logic operation for STS-1 is the same for DS3.

TRANSMIT ALL ONE SELECT

Setting TAOS high causes continuous AMI encoded 1s to be transmitted to the line. In this mode, input TPDATA and TNDATA are ignored. If remote loop back (RLOOP) is set high, TAOS request is ignored.

REMOTE LOOP-BACK

Setting RLOOP high causes receive RPDATA and RNDATA to be transmitted to the line through TTIP and TRING. The data rate is determined by RCLK. In this mode, TPDATA and TNDATA are ignored.

LOCAL LOOPBACK

Setting LLOOP high causes TPDATA and TNDATA to go through both the encoder and the decoder. In this mode, the transmit signal RCLKO, RPOS and RNEG corresponds to TCLK, TPDATA and TNDATA respectively. Unless overriden by TAOS request, TPDATA and TNDATA will still be transmitted to the line. Setting RLOOP and LLOOP high simultaneously is not permitted.

B3ZS/HDB3 DECODER

The decoder block is included to perform B3ZS or HDB3 decoding as determined by the state of the DS3, STS-1/$\overline{E3}$ pin. In the B3ZS format, the decoder detects both B0V and 00V pulses and replaces them with 000 data. If HDB3 decoding is selected by setting the DS3, STS-1/$\overline{E3}$ pin low, B00V and 000V pulses will be detected and replaced with 0000 code. In both cases, bipolar violation and coding errors which do not conform to the coding scheme are detected and indicated at the BPV output pin.

DECODER DISABLE

For testing purposes and in applications where the decoder needs to be bypassed, the decoder can be disabled by setting DECODIS high. In this mode all bipolar violation pulses are indicated at the BPV pin.

BIPOLAR VIOLATION

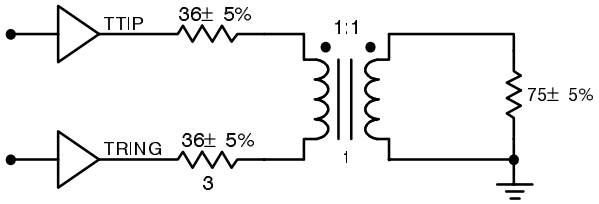
The BPV pin will go high for one bit period when a bipolar violation not corresponding to the appropriate coding rule or a code error is detected on the RPDATA/RNDATA. The violation pulse is always removed from the decoder output RPOS / RNEG when DECODIS is set low.

PULSE SHAPER

The pulse shaper circuit uses a combination of filters and slew rate control techniques to pre-shape the pulse going out to the line. The amplitude of the transmit pulse can be adjusted using the TXLEV (Transmit Level) pin. When the distance to the cross-connect exceeds 225 ft, TXLEV should be set high. When the distance is less than 225 ft. TXLEV should be set low. Setting TXLEV high enables the transmitter to send out a nominal voltage of 1.0V peak, and 850mV peak when low. The state of TXLEV pin has no effect on E3 operation.

DRIVER MONITOR

Using TTIP and TRING as input, the driver monitor detects driver failure by monitoring the activities at MTIP and MRING. If no signal is detected on these pins for 128 TCLK cycles ± 32 cycles, DMO will be set high until the next AMI signal is detected.



Note:
1 Transformer= Pulse EngineeringPE 65966, PE 65967 Surface Mount,Same Transformerfor DS3, STS-1 and E3.

Figure 2. Transmit Pulse Amplitude Test Circuit

Parameter	Value
Turn Ratio	1:1
Primary Inductance	40μH
Isolation Voltage	1500Vrms
Leakage Inductance	0.6μH

Table1. Transmit Transformer Characteristics

DS3 SIGNAL REQUIREMENTS AT THE DSX

For DS3 operation, pulse characteristics are specified at the DSX-3, which is an interconnection and test point referred to as the crossconnect. The crossconnect exists at the point where the transmitted signal reaches the distribution frame jack. The DSX-3 interconnection specification tables list the signal requirements (*Table1)*. The XRT7298 can transmit through 450 feet of 782A cable to the DSX-3 in DS3 mode.

Currently, two isolated pulse template requirements exist: the ANSI T1.404 pulse template (*See Table3 and Figure 3*) and the Bellcore TR-NWT-000499 pulse template. The pulse transmitted by the XRT7298 meets these templates.

Parameter	Specification
Line Rate	44.736Mbps ± 20 ppm
Line Code	Bipolar with three-0 substitution (B3ZS)
Test Load	75 Ω ±5%
Pulse Shape	An isolated pulse must fit the template in *Figure 3* or *Figure 4*.[1] The pulse amplitude may be scaled by a constant factor to fit the template. The pulse amplitude must be between 0.36Vpk and 0.85Vpk, measured at the center of the pulse.
Power Levels	For an all 1s transmitted pattern, the power at 22.368 ± 0.002MHz must be -1.8 to +5.7dBm, and the power at 44.736 ± .002MHz must be -21.8dBm to -14.3dBm.[2, 3]

Notes:

[1] The pulse template proposed by G.703 standards is shown in Figure 4 and specified in Table4 The proposed G.703 standards further state that the voltage in a timeslot containing a 0 must not exceed ±5% of the peak pulse amplitude, except for the residue of preceding pulses.

[2] The power levels specified by the proposed G.703 standards are identical except that the power is to be measured in 3kHz bands.

[3] The all 1s pattern must be a pure all 1s signal, without framing or other control bits.

Table2. DSX•3 Interconnection Specification

Lower Curve		Upper Curve	
Time	**Equation**	**Time**	**Equation**
$T \leq -0.36$	-0.03	$T \leq -0.68$	+0.03
$-0.36 \leq T \leq +0.36$	$0.5\,[1 + \sin^{\pi/2}\,[1 + T/0.18\,]] - 0.03$	$-0.68 \leq T \leq +0.36$	$0.5[\,1 + \sin^{\pi/2}\,[1 + T/0.34]] + 0.03$
$+0.36 \leq T$	-0.03	+0.36	$0.05 + 0.407e^{-1.84(T-0.36)}$

Table3. DSX-3 Pulse Template Boundaries for ANSI T1.404 Standards (See *Figure 3.*)

Lower Curve		Upper Curve	
Time	**Equation**	**Time**	**Equation**
$-0.85 \leq T \leq -0.36$	-0.03	$-0.85 \leq T \leq -0.68$	+0.03
$-0.36 \leq T \leq +0.36$	$0.5\,[1 + \sin^{\pi/2}\,[1 + T/0.18]] - 0.03$	$-0.68 \leq T \leq +0.36$	$0.5[\,1 + \sin^{\pi/2}\,[1 + T/0.34]] + 0.03$
$+0.36 \leq T \leq +1.4$	-0.03	$-0.68 \leq T \leq 0.36$	$0.08 + 0.407e^{-1.84(T-0.36)}$

Table4. DSX-3 Pulse Template Boundaries for Bellcore TR-NWT -000499 Standards (See *Figure 4*)

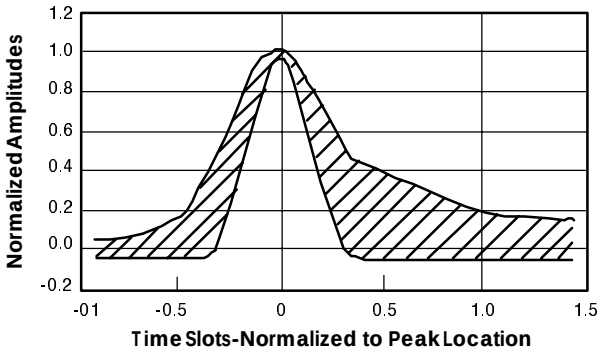


Figure 3. DSX-3 Isolated Pulse Templatefor ANSI T1.404 Standards

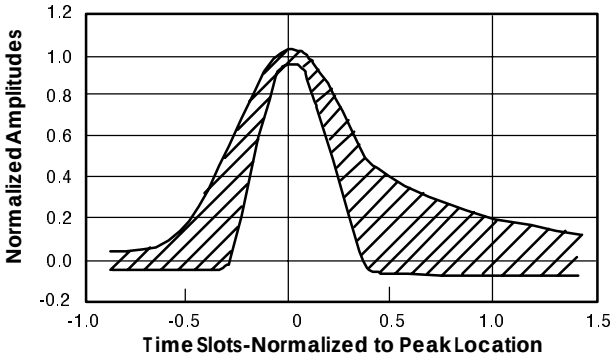


Figure 4. DSX-3 Isolated Pulse Templatefor Bellcore TR-NWT -000499

STS-1 SIGNAL REQUIREMENTS

For STS-1 operation, the cross-connect is referred at the STSX-1. *Table5* lists the signal requirements at the STSX-1. Instead of the DS3 isolated pulse template, an eye diagram mask is specified for STS-1 operation (TA-TSY-000253). (See *Figure 5*).

Parameter	Specification
Line Rate	51.84Mbps
Line Code	Bipolar with three-0 substitution (B3ZS)
Test Load	75 Ω ± 5%
Power Levels	A wide-band power level measurement at the STSX-1 interface using a low-pass filter with a 3dB cutoff frequency of at least 200MHz is within -2.7dBm and 4.7dBm.

Table5. STSX-1 InterconnectionSpecification

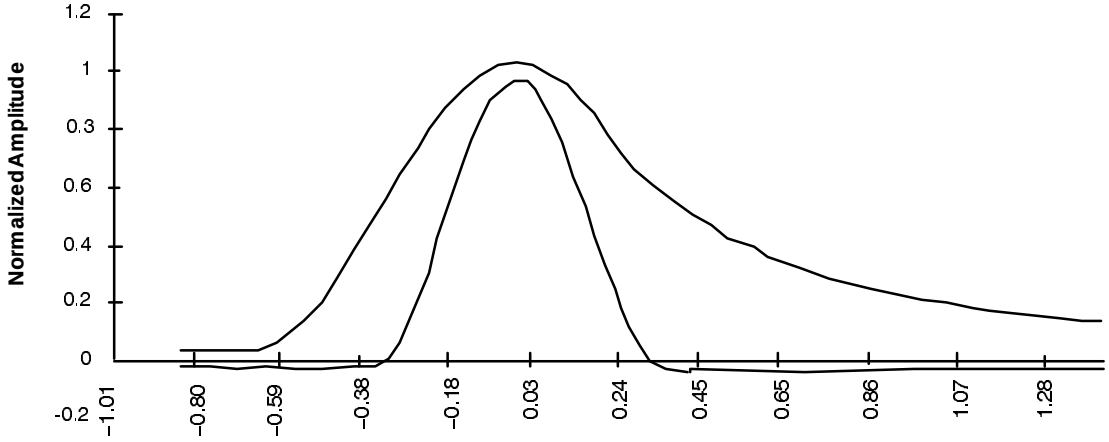


Figure 5. STSX-1 Isolated Pulse Templatefor Bellcore TA-TSY -000253

E3 SIGNAL REQUIREMENTS

The T7298 is designed to transmit pulses that conform to CCITT recommendation G.703. *Figure 6* shows the E3 pulse mask requirement recommended in G.703, and *Table6* shows the pulse specifications.

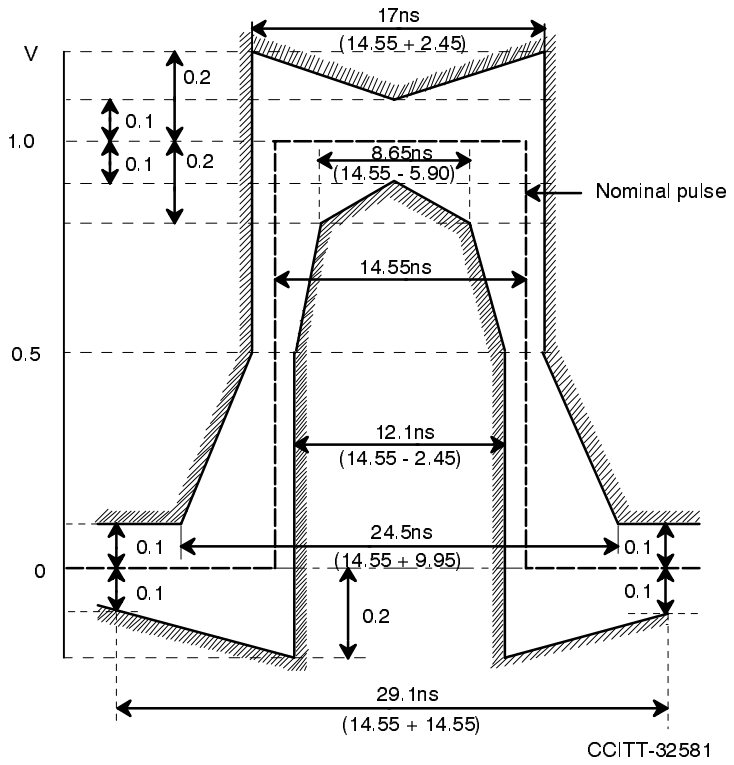


Figure 6. CCITT G.703 Pulse Mark at the 34,368-kbit/sInterface

Parameter	Value
Pulse Shape (Nominally Rectangular)	All marks of a valid signal must conform with the mask (*see Figure 6*), irrespective of the sign
Pair(s) In Each Direction	One coaxial pair
Test Load Impedance	75Ω resistive
Nominal Peak Voltage of a Mark (Pulse)	1.0V
Peak Voltage of a Space (No Pulse)	0V ± 0.1V
Nominal Pulse Width	14.55ns
Ratio of the Amplitudes of Positive and Negative Pulses at the Center of a Pulse Interval	0.95 to 1.05
Ratio of the Widths of Positive and Negative Pulses at the Nominal Half Amplitude	0.95 to 1.05

Table6. E3 Pulse Specifications

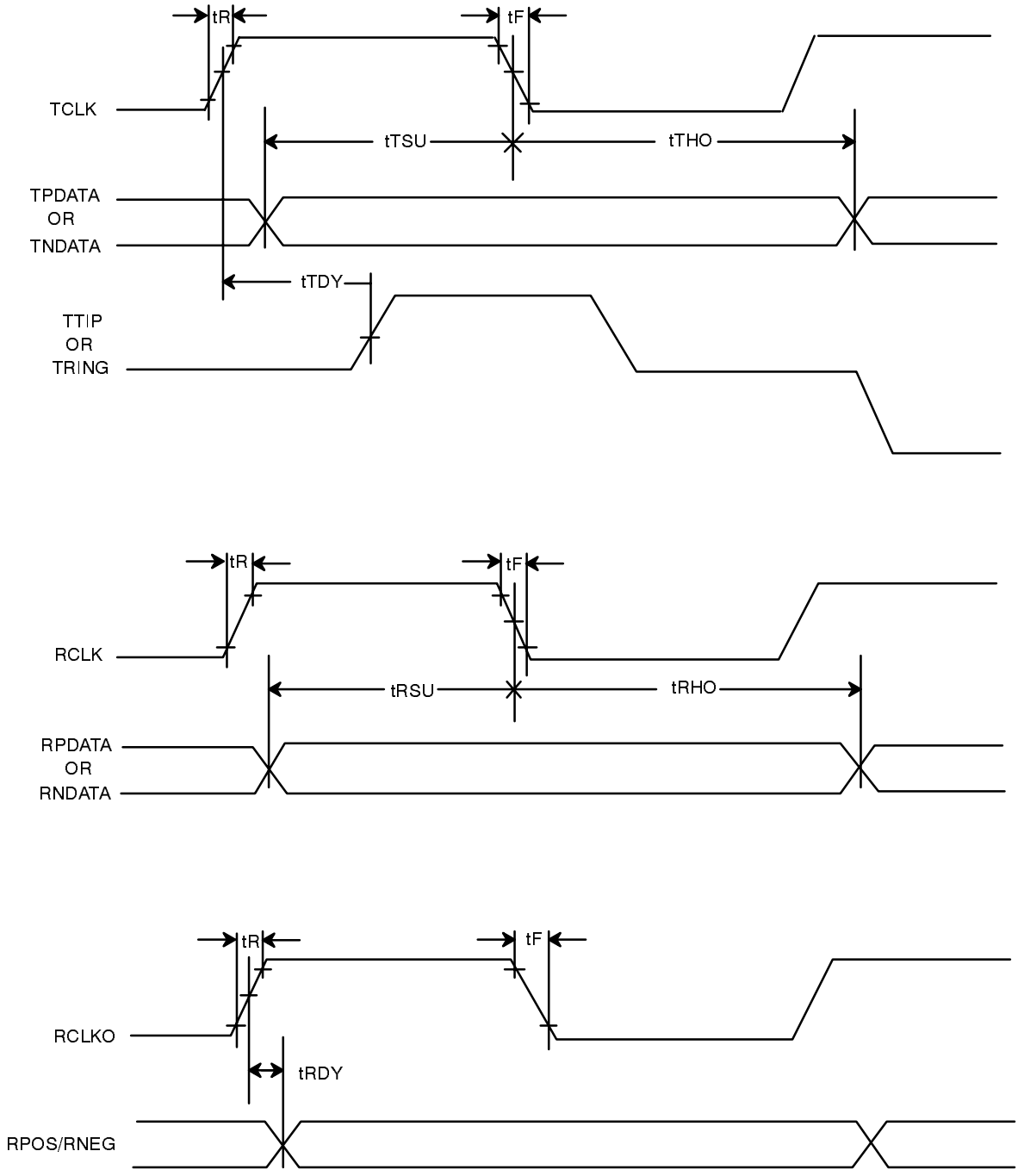
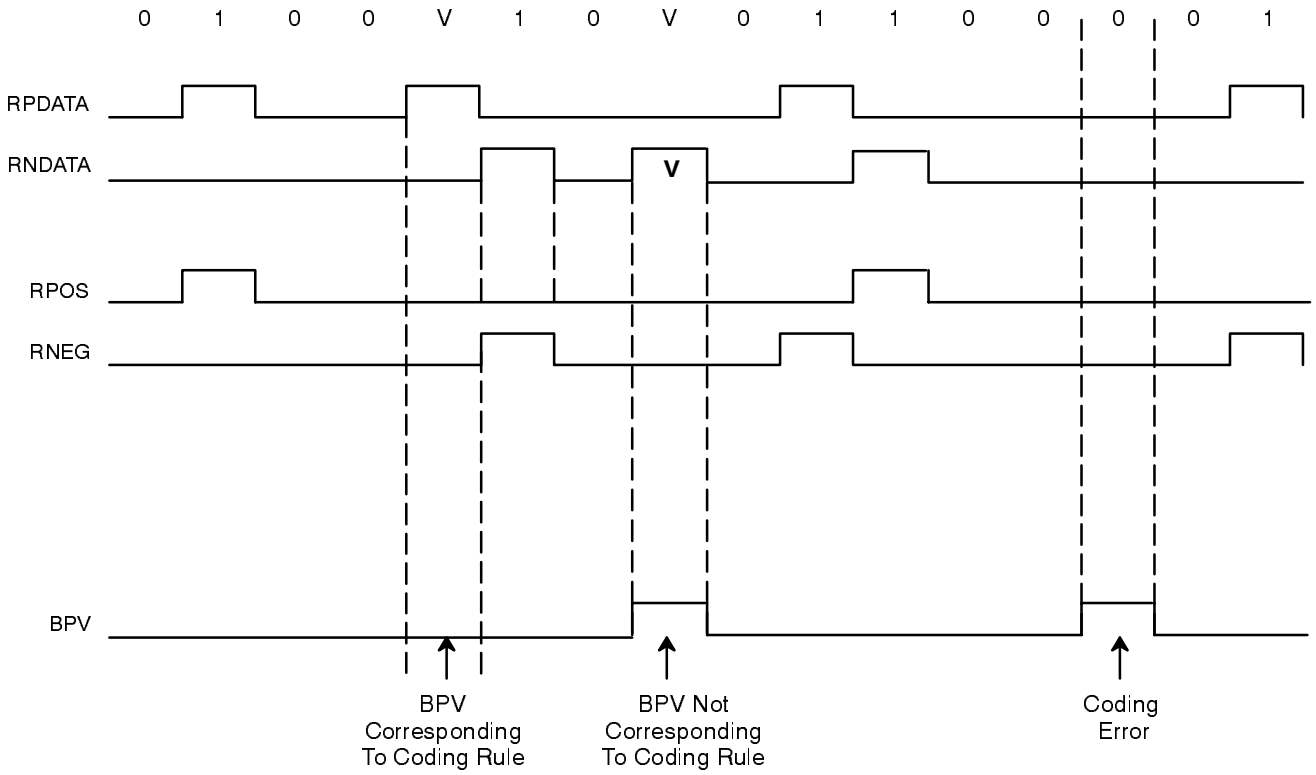


Figure 7. Timing Diagrams for System Interface



Note:
The delay from RPDATA/RNDATA to RPOS/RNEG/RNRZ is not shown here.

Figure 8. Bipolar Violation Example for B3ZS Mode

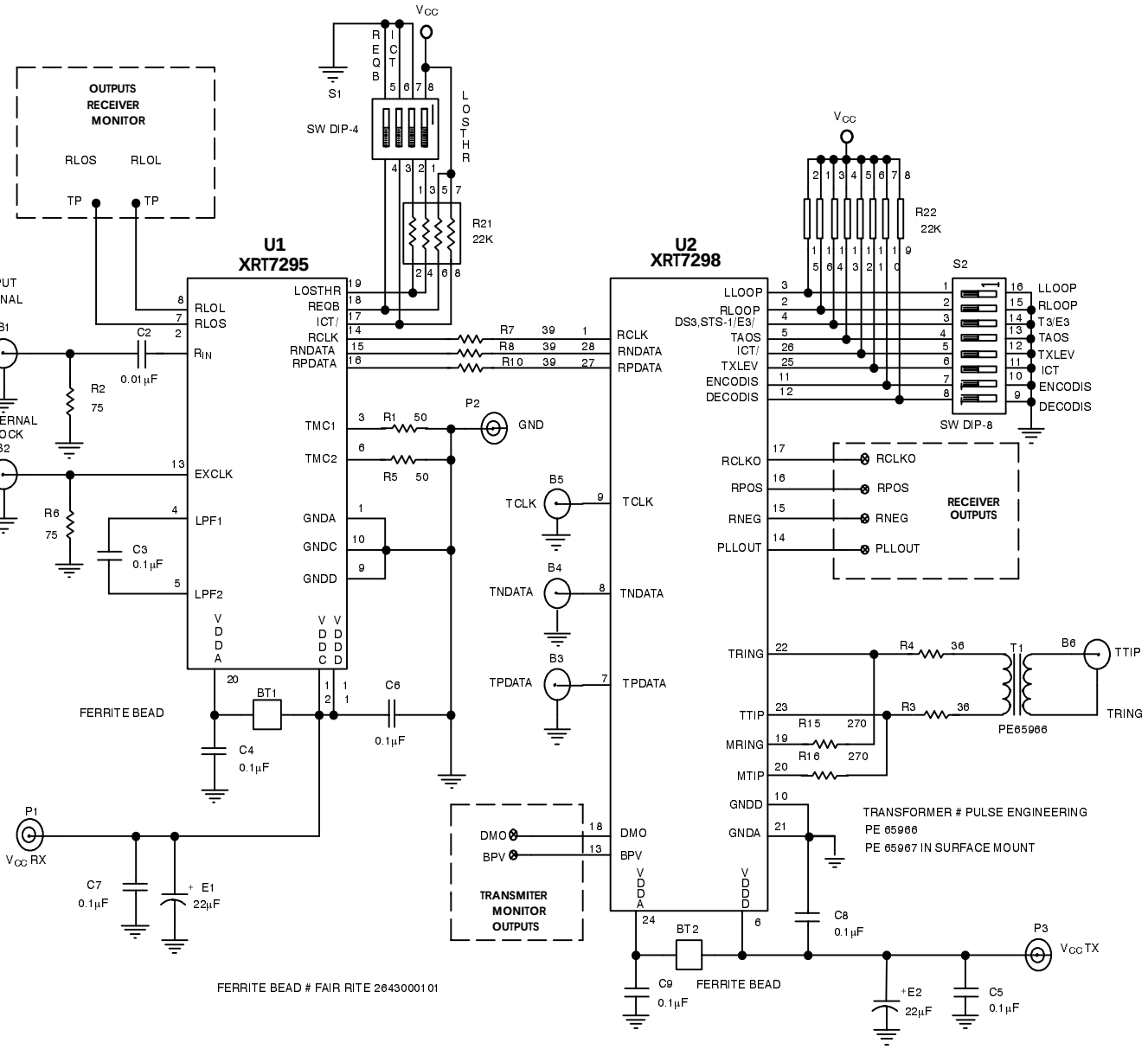
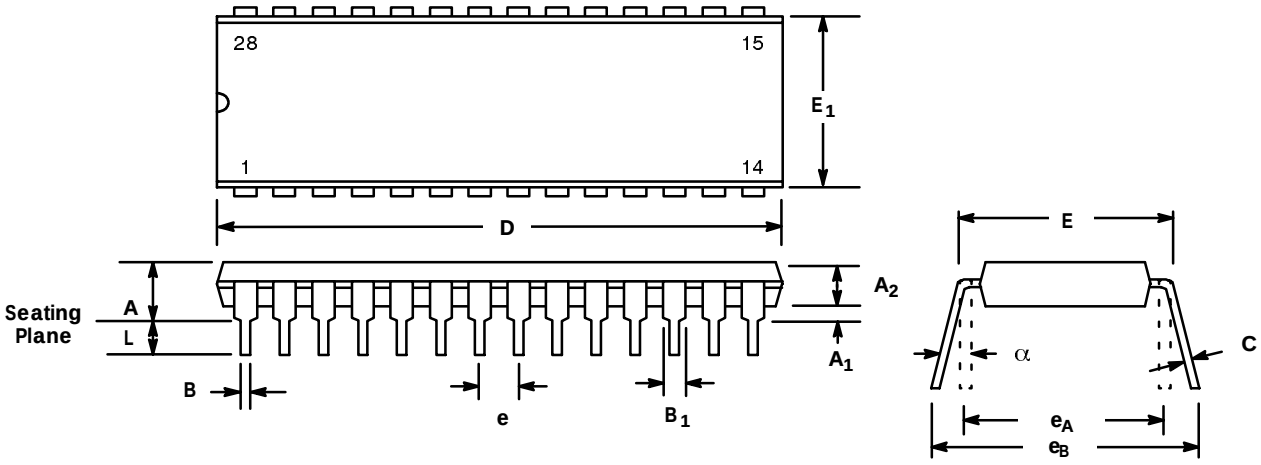


Figure 9. Evaluation System Schematic

28 LEAD PLASTIC DUAL-IN-LINE (600 MIL PDIP)

Rev. 1.00

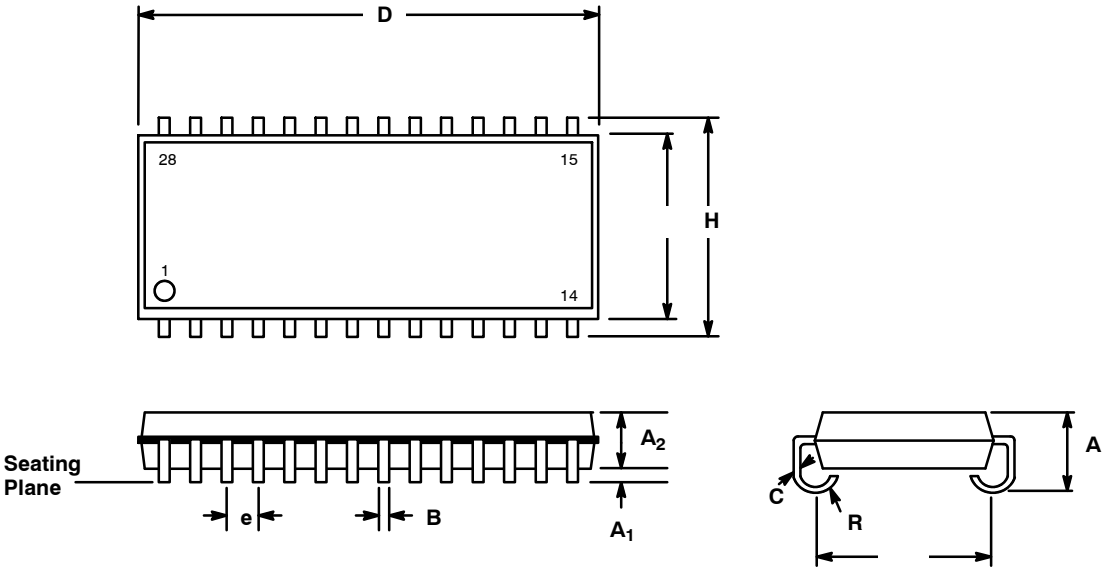


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.250	4.06	6.35
A_1	0.015	0.070	0.38	1.78
A_2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.380	1.565	35.05	39.75
E	0.600	0.625	15.24	15.88
E_1	0.485	0.580	12.32	14.73
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	0.600	0.700	15.24	17.78
L	0.115	0.200	2.92	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

28 LEAD SMALL OUTLINE J LEAD (300 MIL JEDEC SOJ)

Rev. 3.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.120	0.140	3.05	3.56
A_1	0.025	---	0.64	---
A_2	0.090	0.115	2.29	2.92
B	0.014	0.020	0.36	0.51
C	0.008	0.013	0.20	0.30
D	0.697	0.712	17.70	18.08
E	0.292	0.300	7.42	7.62
E_1	0.262	0.272	6.65	6.91
e	0.050 BSC		1.27 BSC	
H	0.335	0.347	8.51	8.81
R	0.030	0.040	0.76	1.02

Note: The control dimension is the inch column

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Datasheet April 2000