SINGLE CHANNEL DS3/E3 FRAMER IC WITH HDLC CONTROLLER

OCTOBER 2003 *REV. 1.2.1*

GENERAL DESCRIPTION

The XRT72L50, single Channel DS3/E3 Framer IC is designed to accept user data from the Terminal Equipment and insert this data into the payload bit-fields within an outbound DS3/E3 Data Stream. Further, the Framer IC is also designed to receive an inbound DS3/E3 Data Stream from the Remote Terminal Equipment and extract out the user data.

The XRT72L50 DS3/E3 Framer device is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

The XRT72L50 DS3/E3 Framer IC consists of a Transmit section, Receiver section, Performance Monitor Section and a Microprocessor interface.

The Transmit Section includes a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Section consists of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer IC in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of Reset-upon-Read and Read-Only registers that contain cumulative and one-second statistics that reflect the performance/health of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 1 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 100 Pin PQFP package
- 3.3V Power Supply with 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

FIGURE 1. BLOCK DIAGRAM OF THE XRT72L50

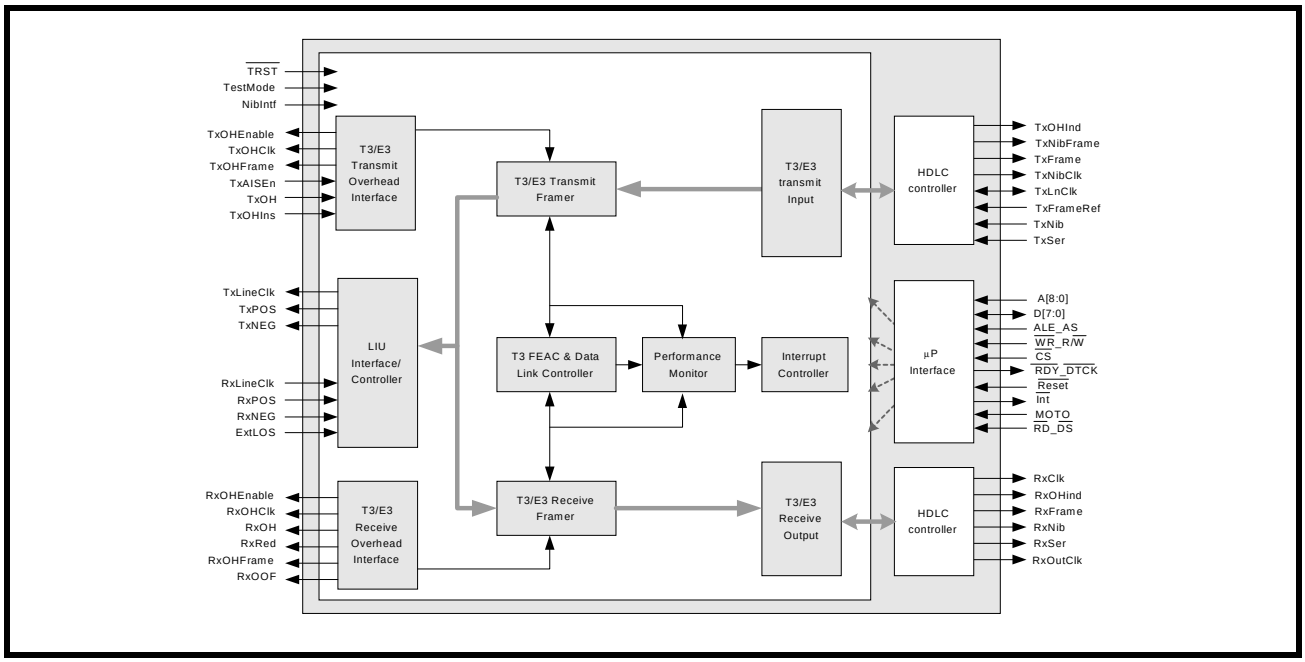
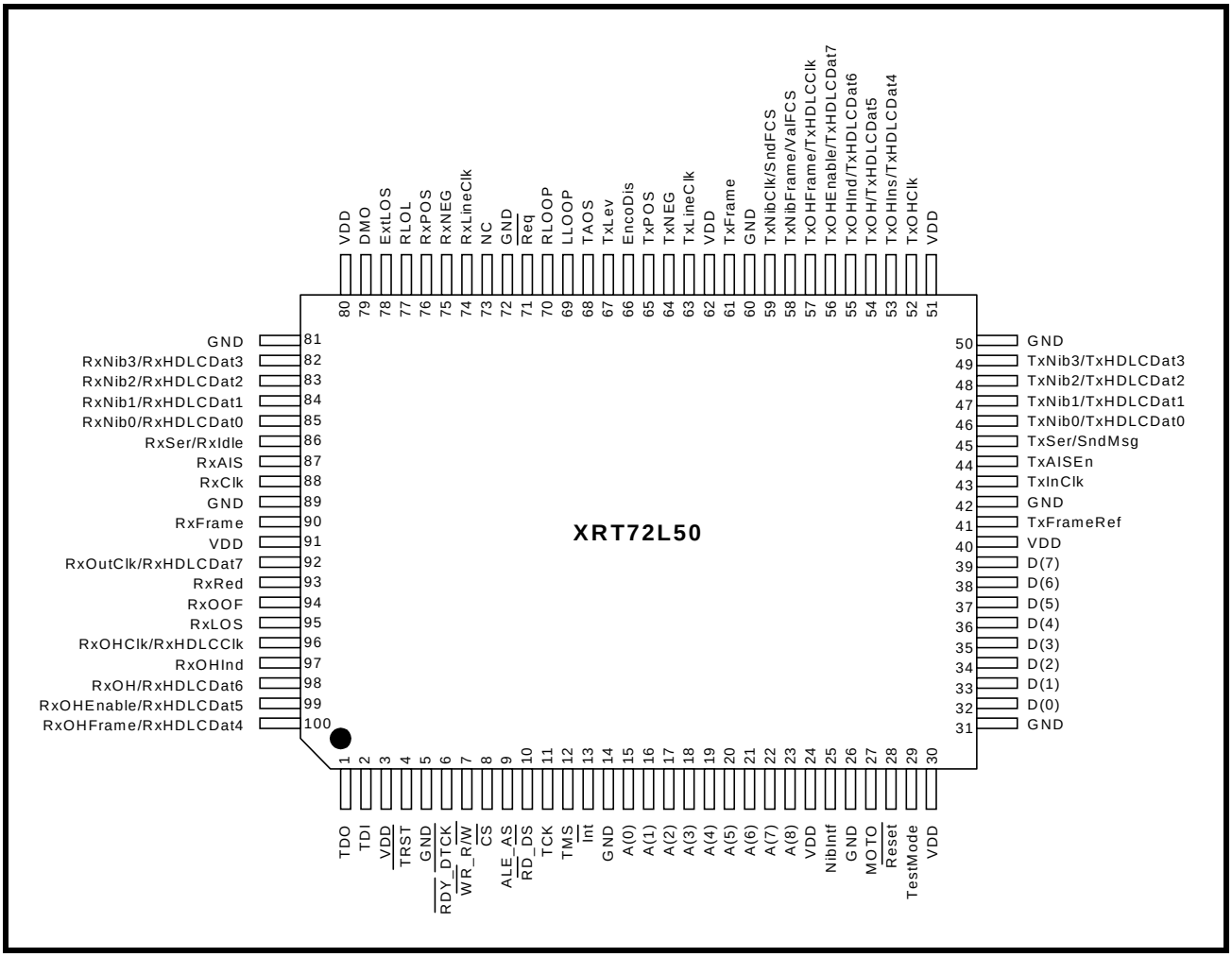


FIGURE 2. PIN OUT OF THE XRT72L50



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT72L50IQ	14x20mm, 100 Lead Plastic QFP	-40°C to +85°C

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PIN DESCRIPTIONS

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
1	TDO	O	**Test Data Out:** Boundary Scan test data output.
2	TDI	I	**Test Data In:** Boundary Scan Test data input.
3	VDD	****	**Power Supply 3.3V ± 5%**
4	$\overline{\text{TRST}}$	I	**JTAG Reset Pin:** Resets Boundary Scan Logic.
5	GND	****	**Ground**
6	$\overline{\text{RDY}}$_$\overline{\text{DTCK}}$	O	**READY or DTACK:** This active-low output pin will function as the READY output, when the microprocessor interface is running in the Intel Mode; and will function as the DTACK output, when the microprocessor interface is running in the Motorola Mode. **Intel Mode - READY Output:** When the Framer negates this output pin (e.g., toggles it "Low"), it indicates (to the µP) that the current READ or WRITE cycle is completed. **Motorola Mode - DTACK (Data Transfer Acknowledge) Output:** The Framer device will assert this pin in order to inform the local microprocessor that the present READ or WRITE cycle is nearly complete. If the Framer device requires that the current READ or WRITE cycle be extended, then the Framer will delay its assertion of this signal. The 68000 family of µPs requires this signal from its peripheral devices, in order to quickly and properly complete a READ or WRITE cycle.
7	$\overline{\text{WR}}$_R/$\overline{\text{W}}$	I	**Write Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this active-low input pin functions as the $\overline{\text{WR}}$ (Write Strobe) input signal from the µP. Once this active-low signal is asserted, then the Framer will latch the contents of the µP Data Bus, into the addressed register (or RAM location) within the Framer IC. In the Intel Mode, data gets latched on the rising edge of $\overline{\text{WR}}$ **R/W Input Pin (Motorola Mode):** When the Microprocessor Interface is operating in the Motorola Mode, this pin is functionally equivalent to the R/$\overline{\text{W}}$ pin. In the Motorola Mode, a READ operation occurs if this pin is at a logic "1". Similarly, a WRITE operation occurs if this pin is at a logic "0".
8	$\overline{\text{CS}}$	I	**Chip Select Input:** This active-low input signal selects the Microprocessor Interface Section of the Framer device and enables READ/WRITE operations between the Local Microprocessor and the Framer on-chip registers and RAM locations.
9	ALE_AS	I	**Address Latch Enable/Address Strobe:** This input is used to latch the address (present at the Microprocessor Interface Address Bus, A(8:0)) into the Framer Microprocessor Interface circuitry and to indicate the start of a READ/WRITE cycle. This input is active-high in the Intel Mode (MOTO = "Low") and active-low in the Motorola Mode (MOTO = "High").

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
10	$\overline{RD}_\overline{DS}$	I	**Read Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this input will function as the $\overline{RD}$ (READ STROBE) input signal from the local µP. Once this active-low signal is asserted, then the Framer will place the contents of the addressed registers (within the Framer) on the Microprocessor Data Bus (D(7:0)). When this signal is negated, the Data Bus will be tri-stated. **Data Strobe (Motorola Mode):** If the microprocessor interface is operating in the Motorola mode, then this pin will function as the active-low Data Strobe signal.
11	TCK	I	**Test Clock:** Boundary Scan clock input.
12	TMS	I	**Test Mode Select:** Boundary Scan Mode Select input.
13	$\overline{Int}$	O	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Framer device is requesting interrupt service from the local microprocessor. This output pin should typically be connected to the Interrupt Request input of the local microprocessor.
14	GND	****	**Ground**
15	A(0)	I	**Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit):** (Please see description for A(8) pin 23)
16	A(1)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
17	A(2)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
18	A(3)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
19	A(4)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
20	A(5)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
21	A(6)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
22	A(7)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
23	A(8)	I	**Address Bus Input (Microprocessor Interface) - MSB (Most Significant Bit):** This input pin, along with inputs A0 - A7 are used to select the on-chip Framer register and RAM space for READ/WRITE operations with the local microprocessor.
24	VDD	****	**Power Supply 3.3V ± 5%**

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
25	NibIntf	I	**Nibble Interface Select Input Pin:** This input pin allows the user to configure the Transmit Payload Data Input Interface and the Receive Payload Data Output Interface to operate in either the Serial-Mode or the Nibble/Parallel-Mode. Setting this input pin "High" configures the Transmit and Receive Terminal Interfaces to operate in the Nibble/Parallel-Mode. In this mode, the Transmit Payload Data Input Interface block will accept the outbound payload data (from the Terminal Equipment) in a nibble-parallel manner via the TxNib[3:0] input pins. Further, the Receive Payload Data Output Interface block will output the inbound payload data (to the Terminal Equipment) in a nibble-parallel manner via the RxNib[3:0] output pin. HDLC mode of operation requires Nibble/Parallel mode setup. Setting this input pin "Low" configures the Transmit and Receive Terminal Interfaces to operate in the Serial Mode. In this mode, the Transmit Payload Data Input Interface block will accept the outbound payload data (from the Terminal Equipment) in a serial manner via the TxSer input pin. Further, the Receive Payload Data Output Interface block will output the inbound payload data (to the Terminal Equipment) in a serial manner via the RxSer output pin.
26	GND	****	**Ground**
27	MOTO	I	**Motorola/Intel Processor Interface Select Mode:** This input pin allows the user to configure the Microprocessor Interface to interface with either a Motorola-type or Intel-type microprocessor/microcontroller. Tying this input pin to VCC, configures the microprocessor interface to operate in the Motorola mode (e.g., the Framer device can be readily interfaced to a Motorola type local microprocessor). Tying this input pin to GND configures the Microprocessor Interface to operate in the Intel Mode (e.g., the Framer device can be readily interfaced to a Intel type local microprocessor).
28	$\overline{\text{Reset}}$	I	**Reset Input:** When this active-low signal is asserted, the Framer device will be asynchronously reset. Additionally, all outputs will be tri-stated, and all on-chip registers will be reset to their default values.
29	TestMode	***	**Factory Test Pin:** The user should tie this pin to Ground.
30	VDD	****	**Power Supply 3.3V ± 5%**
31	GND	****	**Ground**
32	D(0)	I/O	**Bit 0 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
33	D(1)	I/O	**Bit 1 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
34	D(2)	I/O	**Bit 2 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
35	D(3)	I/O	**Bit 3 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
36	D(4)	I/O	**Bit 4 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
37	D(5)	I/O	**Bit 5 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
38	D(6)	I/O	**Bit 6 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
39	D(7)	I/O	**MSB of Bi-Directional Data Bus (Microprocessor Interface Section):** This pin, along with pins D0 - D6, function as the Microprocessor Interface bi-directional data bus, and is intended to be interfaced to the local microprocessor.
40	VDD	****	**Power Supply 3.3V ± 5%**
41	TxFrameRef	I	**Transmit Framer Reference Input:** This input pin functions as the Transmit Frame Generation reference signal, if the XRT72L50 has been configured to operate in the Local-Time/Frame Slave Mode. If the XRT72L50 has been configured to operate in the Local-Time/Frame-Slave Mode, then the user's terminal equipment is expected to apply a pulse (to this input pin) once every 106.4 microseconds (for DS3 applications); once every 125 microseconds (for E3, ITU-T G.832 applications) or once every 44.7 microseconds (for E3, ITU-T G.751 applications). In the Local-Time/Frame-Slave Mode, the Transmit Section of the XRT72L50 Framer IC will initiate its generation of a new outbound DS3 or E3 frame, upon the rising edge of this signal. ***NOTE:*** *The user can configure the XRT72L50 Framer IC to operate in the Local Time/Frame Slave Mode by writing xxxx xx01 into the Framer Operating Mode Register (Address = 0x00).*
42	GND	****	**Ground**
43	TxInClk	I	**Transmit Framer Reference Clock Input:** This input pin functions as the Timing Reference for the Transmit Section of the XRT72L50 Framer IC; if the device has been configured to operate in the Local-Time Mode. Further, if the XRT72L50 Framer IC has been configured to operate in the Local-Time Mode, the Transmit Payload Data Input Interface will sample the data at the TxSer input pin, upon the rising edge of TxInClk. For E3 applications, the user should apply a 34.368MHz clock signal. For DS3 applications, the user should apply a 44.736MHz clock signal. The user can configure the XRT72L50 Framer IC to operate in the Local-Time mode by writing xxxx xx01 or xxxx xx1x into the Framer Operating Mode register (Address = 0x00)
44	TxAISEn	I	**Transmit AIS Command Input:** Setting this input pin "High" configures the Transmit Section to generate and transmit an AIS Pattern. Setting this input pin "Low" configures the Transmit Section to generate E3 or DS3 traffic in a normal manner.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
45	TxSer/	I	**Transmit Serial Payload Data Input Pin:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound E3 or DS3 frame. If the XRT72L50 Framer IC has been configured to operate in the Local Time Mode, then it will sample the data (on this pin) upon the rising edge of TxInClk. If the XRT72L50 Framer IC has been configured to operate in the Loop-Time Mode, then it will sample the data (on this pin) upon the rising edge of RxOutClk. ***NOTE:*** *This input pin is active only if the Serial Mode has been selected.* **Send Message:** This input is to remain "High" during the entire duration of the HDLC packet (including FCS bytes) to be transmitted, when the HDLC controller is turned on.
	SndMsg		
46	TxNib0/	I	**Transmit Nibble-Parallel Payload Data Input -0:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin (along with TxNib1, TxNib2, and TxNib3), and insert it into an outbound E3 or DS3 frame. The XRT72L50 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **Transmit HDLC Data Input - 0:** This pin accepts bit 0 TxHDLC data when the HDLC controller is turned on.
	TxHDLCDat0		
47	TxNib1/	I	**Transmit Nibble-Parallel Payload Data Input -1:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound E3 or DS3 frame. The XRT72L50 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **Transmit HDLC Data Input - 1:** This pin accepts bit 1 TxHDLC data when the HDLC controller is turned on.
	TxHDLCDat1		
48	TxNib2/	I	**Transmit Nibble-Parallel Payload Data Input -2:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound E3 or DS3 frame. The XRT72L50 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **Transmit HDLC Data Input - 2:** This pin accepts bit 2 TxHDLC data when the HDLC controller is turned on.
	TxHDLCDat2		

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
49	TxNib3/	I	**Transmit Nibble-Parallel Payload Data Input -3:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin (along with TxNib1, TxNib2, and TxNib3), and insert it into an outbound E3 or DS3 frame. The XRT72L50 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* TxHDLCDat3 **Transmit HDLC Data Input - 3:** This pin accepts bit 3 TxHDLC data when the HDLC controller is turned on.
50	GND	****	**Ground**
51	VDD	****	**Power Supply 3.3V ± 5%**
52	TxOHClk	O	**Transmit Overhead Clock:** This output signal serves two purposes: 1. The Transmit Overhead Data Input Interface block will provide a rising clock edge on this signal, one bit-period prior to the start to the instant that the Transmit Overhead Data Input Interface block is processing an overhead bit. 2. The Transmit Overhead Data Input Interface will sample the data at the TxOH input pin, on the falling edge of this clock signal (provided that the TxOHIns input pin is "High"). ***NOTE:*** *The Transmit Overhead Data Input Interface block will supply a clock edge for all overhead bits within the DS3 or E3 frame (via the TxOHClk output signal). This includes those overhead bits that the Transmit Overhead Data Input Interface will not accept from the Terminal Equipment.*
53	TxOHIns/	I	**Transmit Overhead Data Insert Input:** Asserting this input signal (e.g., setting it "High") enables the Transmit Overhead Data Input Interface to accept overhead data from the Terminal Equipment. In other words, while this input pin is "High", the Transmit Overhead Data Input Interface will sample the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. Conversely, setting this pin "Low" configures the Transmit Overhead Data Input Interface to NOT sample (e.g., ignore) the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. ***NOTE:*** *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the Transmit Overhead Data Input Interface (e.g., if the Terminal Equipment asserts the TxOHIns signal, at a time when one of these non-insertable overhead bits are being processed); that particular insertion effort will be ignored.* TxHDLCDat4 **Transmit HDLC Data Input - 4:** This pin accepts bit 4 TxHDLC data when the HDLC controller is turned on.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
54	TxOH/	I	**Transmit Overhead Input Pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the overhead bit position within the very next outbound DS3 or E3 frame. If the TxOHIns pin is pulled "High", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the TxOHClk output pin. Conversely, if the TxOHIns pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.
	TxHDLCDat5		**Transmit HDLC Data Input - 5:** This pin accepts bit 5 TxHDLC data when the HDLC controller is turned on.
55	TxOHInd/	O	**Transmit Overhead Data Indicator:** This output pin will pulse "High" one-bit period prior to the time that the Transmit Section of the XRT72L50 will be processing an Overhead bit. The purpose of this output pin is to warn the Terminal Equipment that, during the very next bit-period, the XRT72L50 is going to be processing an Overhead bit and will be ignoring any data that is applied to the TxSer input pin. ***NOTE:*** *For DS3 applications, this output pin is only active if the XRT72L50 is operating in the Serial Mode. This output pin will be pulled "Low" if the device is operating in the Nibble-Parallel Mode.*
	TxHDLCDat6	I	**Transmit HDLC Data Input - 6:** This pin accepts bit 6 TxHDLC data when the HDLC controller is turned on.
56	TxOHEnable/	O	**Transmit Overhead Input Enable:** The XRT72L50 will assert this signal, for one TxInClk period, just prior to the instant that the Transmit Overhead Data Input Interface will be sampling and processing an overhead bit. If the Terminal Equipment intends to insert its own value for an overhead bit, into the outbound DS3 or E3 frame, it is expected to sample the state of this signal, upon the falling edge of TxInClk. Upon sampling the TxOHEnable "High", the Terminal Equipment should (1) place the desired value of the overhead bit, onto the TxOH input pin and (2) assert the TxOHIns input pin. The Transmit Overhead Data Input Interface" block will sample and latch the data on the TxOH signal, upon the rising edge of the very next TxInClk input signal.
	TxHDLCDat7	I	**Transmit HDLC Data Input - 7:** This pin accepts bit 7 TxHDLC data when the HDLC controller is turned on.
57	TxOHFrame/	O	**Transmit Overhead Framing Pulse:** This output pin pulses "High" when the Transmit Overhead Data Input Interface block is expecting the first Overhead bit, within a DS3 or E3 frame to be applied to the TxOH input pin. This pin is "High" for one clock period of TxOHClk.
	TxHDLCClk		**Transmit HDLC Output Clock:** When the HDLC controller is on, TxHDLCDat is updated by the 72L53 by this clock signal.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
58	TxNibFrame/	O	**Transmit Frame Boundary Indicator - Nibble/Parallel Interface:** This output pin pulses "High" when the last nibble of a given DS3 or E3 frame is expected at the TxNib[3:0] input pins. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame to the XRT72L50.
	ValFCS		**Valid Frame Check Sequence:** When the HDLC is on, this pin will go "High" at the end of a valid Frame Check Sequence.
59	TxNibClk/	O	**Transmit Nibble Clock Signal:** If the user opts to operate the XRT72L50 in the Nibble-Parallel mode, then the XRT72L50 will derive this clock signal from either the TxInClk or the RxLineClk signal (depending upon which signal is selected as the timing reference). The user is advised to configure the Terminal Equipment to output the outbound payload data (to the XRT72L50 Framer IC) onto the TxNib[3:0] input pins, upon the rising edge of this clock signal. ***NOTES:*** *1. For DS3 applications, the XRT72L50 Framer IC will output 1176 clock edges (to the Terminal Equipment) for each outbound DS3 frame.* *2. For E3, ITU-T G.832 applications, the XRT72L50 Framer IC will output 1074 clock edges (to the Terminal Equipment) for each outbound E3 frame.* *3. For E3, ITU-T G.751 applications, the XRT72L50 Framer IC will output 384 clock edges (fo the Terminal Equipment) for each outbound E3 frame.*
	SndFCS	I	**Send Frame Check Sequence:** When the HDLC controller is turned on, this pin is driven "High" during the time when FCS bytes are being sent after a valid HDLC message.
60	GND	****	**Ground**
61	TxFrame	O	**Transmit End of DS3 or E3 Frame Indicator:** The Transmit Section of the XRT72l50 will pulse this output pin "High" (for one bit-period), when the Transmit Payload Data Input Interface is processing the last bit of a given DS3 or E3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame to the XRT72l50 (e.g., to permit the XRT72l50 to maintain Transmit DS3/E3 framing alignment control over the Terminal Equipment).
62	VDD	****	**Power Supply 3.3V ± 5%**
63	TxLineClk	O	**Transmit Line Interface Clock:** This clock signal is output to the Line Interface Framer, along with the TxPOS and TxNEG signals. The purpose of this output clock signal is to provide the LIU with timing information that it can use to generate the AMI pulses and deliver them over the transmission medium to the Far-End Receiver. The user can configure the source of this clock to be either the RxLineClk (from the Receiver portion of the Framer) or the TxInClk input. The nominal frequency of this clock signal is 34.368 MHz.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
64	TxNEG	O	**Transmit Negative Polarity Pulse:** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output signal pulses "High" for one bit period, at the end of each outbound DS3 or E3 frame. This output signal is at a logic "Low" for all of the remaining bit-periods of the outbound DS3 or E3 frames **Bipolar Mode:** This output pin functions as one of the two dual-rail output signals that commands the sequence of pulses to be driven on the line. TxPOS is the other output pin. This input is typically connected to the TNDATA input of the external DS3/E3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a negative polarity pulse on the line.
65	TxPOS	O	**Transmit Positive Polarity Pulse:** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. Unipolar Mode: This output pin functions as the Single-Rail output signal for the outbound DS3 or E3 data stream. The signal, at this output pin, will be updated on the user-selected edge of the TxLineClk signal. Bipolar Mode: This output pin functions as one of the two dual rail output signals that commands the sequence of pulses to be driven on the line. TxNEG is the other output pin. This input is typically connected to the TPDATA input of the external DS3 or E3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a positive polarity pulse on the line
66	ENCODIS	O	**Encoder (HDB3) Disable Output pin (intended to be connected to the XRT73L00 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the ENDECDIS input pin of the XRT73L00 DS3/E3 Line Interface Unit IC when the device is being used in Hardware mode. The user can control the state of this output pin by writing a "0" or "1" to Bit 3 (Encodis) within the Line Interface Driver Register (Address = 0x80). If the user commands this signal to toggle "High" then it will disable the B3ZS/HDB3 encoder circuitry within the XRT73L00 IC. Conversely, if the user commands this output signal to toggle "Low", then the B3ZS/HDB3 Encoder circuitry, within the XRT73L00 IC will be enabled. The user is advised to disable the B3ZS/HDB3 encoder (within the XRT73L00 IC) if the XRT72L50 Framer IC has been configured to operate in the B3ZS/HDB3 line code. ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
67	TxLEV	O	**Transmit Line Build-Out Enable/Disable Select Output (to be connected to the XRT73L00 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the TxLev input pin of the XRT73L00 DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a "0" or a "1" to Bit 2 (TxLev) within the Line Interface Driver Register (Address = 0x80). **For DS3 Application:** If the user commands this signal to toggle "High" then the Transmit Line Build-Out circuit (within the XRT73L00) will be disabled. In this mode, the XRT73L00 will output unshaped (e.g., square) pulses onto the line (via the TTIP and TRING output pins). Conversely, if the user commands this signal to toggle "Low" then the Transmit Line Build-Out circuit (within the XRT73L00) will be disabled. In this mode, the XRT73L00 will output shaped (e.g., more rounded) pulses onto the line (via the TTIP and TRING output pins). In order to comply with the DSX-3 Isolated Pulse Template Requirement (per Bellcore GR-499-CORE), the user is advised to command this output pin to be "High" if the cable length (between the transmit output of the XRT73L00 and the DSX-3 Cross-Connect System) is greater than 225 feet. Conversely, the user is advised to command this output pin to be "Low" if the cable length (between the transmit output of the XRT73L00 and the DSX-3Cross Connect System) is less than 225 feet. **For E3 Applications:** This pin can be used as a General Purpose Output pin. The Transmit Line Build-Out circuitry (within the XRT73L00) is not active for E3 applications. ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*
68	TAOS	O	**Transmit All Ones Signal (TAOS) Command (for the XRT73L00 Line Interface Unit IC):** This output pin is intended to be connected to the TAOS input pin of the XRT73L00 DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 4 (TAOS) of the Line Interface Drive Register (Address = 0x80). If the user commands this signal to toggle "High" then it will force the XRT73L00 Line Interface Unit IC to transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "Low" then the XRT73L00 DS3/E3 Line Interface Unit IC will proceed to transmit data based upon the pattern that it receives via the TxPOS and TxNEG output pins. ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*
69	LLOOP	O	**Local Loopback Output Pin (to the XRT73L00 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the LLOOP input pin of the XRT73L00 LIU IC. The user can command this signal to toggle "High" and, in turn, force the LIU into the Local Loop-back mode. (For a detailed description of the XRT73L00 DS3/E3 Line Interface Unit IC's operation during Local Loopback, please see the XRT73L00 DS3/STS-1/E3 Line Interface Unit IC's Data Sheet). ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
70	RLOOP	O	**Remote Loopback Output Pin (to the XRT73L00 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the RLOOP input pin of the XRT73L00 DS3/E3 Line Interface Unit IC. The user can command this signal to toggle "High" and, in turn, force the XRT73L00 DS3/E3 Line Interface Unit IC into the Remote Loop-back mode. Conversely, the user can command this signal to toggle "Low" and allow the XRT73L00 to operate in the normal mode. (For a detailed description of the XRT73L00 DS3/E3 Line Interface Unit IC's operation during Remote Loopback, please see the XRT73L00 DS3/STS-1/ E3 Line Interface Unit IC's Data Sheet). ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.* ***NOTE:***
71	$\overline{\text{Req}}$	O	**Receive Equalization Enable/Disable Select output pin - (to be connected to the XRT73L00 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the $\overline{\text{REQ}}$ input pin of the XRT73L00 DS3/E3 ($\overline{\text{REQDIS}}$ or $\overline{\text{REQEN}}$ of the XRT73L03 or XRT 73L04) Line Interface Unit IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 5 ($\overline{\text{REQ}}$) within the Line Interface Driver Register (Address = 0x80). If the user commands this signal to toggle "High" then the internal Receive Equalizer (within the XRT73L00) will be disabled. Conversely, if the user commands this output signal to toggle "Low", then the internal Receive Equalizer (within the XRT73L00) will be enabled. For information on the criteria that should be used when deciding whether to bypass the equalization circuitry or not, please consult the XRT73L00 DS3/E3 Line Interface Unit data sheet. ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*
72	GND	****	**Ground**
73	NC		**No Connection**
74	RxLineClk	I	**Receiver LIU (Recovered) Clock:** This input signal serves three purposes: 1. The Receive Framer uses it to sample and latch the signals at the RxPOS and RxNEG input pins (into the Receive Framer circuitry). 2. This input signal functions as the timing reference for the Receive Framer block. 3. The Transmit Framer block can be configured to use this input signal as its timing reference. This signal is the recovered clock from the external DS3/E3 LIU (Line Interface Unit) IC, which is derived from the incoming DS3/E3 data.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
75	RxNEG	I	**Receive Negative Data Input:** The exact role of this input pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin is inactive, and should be pulled ("Low" or "High") when the Framer is operating in the Unipolar Mode. **Bipolar Mode:** This input pin functions as one of the dual rail inputs for the incoming AMI/HDB3 encoded DS3 or E3 data that has been received from an external Line Interface Unit (LIU) IC. RxPOS functions as the other dual rail input for the Framer. When this input pin is asserted, it means that the LIU has received a negative polarity pulse from the line.
76	RxPOS	I	**Receive Positive Data Input:** The exact role of this input pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin functions as the Single-Rail input for the incoming E3 data stream. The signal at this input pin will be sampled and latched (into the Receive DS3/E3 Framer) on the user-selected edge of the RxLineClk signal. **Bipolar Mode:** This input functions as one of the dual rail inputs for the incoming AMI/HDB3 encoded DS3 or E3 data that has been received from an external Line Interface Unit (LIU) IC. RxNEG functions as the other dual rail input for the Framer. When this input pin is asserted, it means that the LIU has received a positive polarity pulse from the line.
77	RLOL	I	**Receive Loss of Lock Indicator - from the XRT73L00 DS3/E3 Line Interface Unit IC:** This input pin is intended to be connected to the RLOL (Receive Loss of Lock) output pin of the XRT73L00 Line Interface Unit IC. The user can monitor the state of this pin by reading the state of Bit 1 (RLOL) within the Line Interface Scan Register (Address = 0x81). If this input pin is "Low", then it means that the clock recovery phase-locked-loop circuitry, within the XRT73L00 is properly locked onto the incoming DS3 E3 data-stream; and is properly recovering clock and data from this DS3/E3 data-stream. However, if this input pin is "High", then it means that the phase-locked-loop circuitry, within the XRT73L00 has lost lock with the incoming DS3 or E3 data-stream, and is not properly recovering clock and data. For more information on the operation of the XRT73L00 DS3/E3 Line Interface Unit IC, please consult the XRT73L00 DS3/E3 Line Interface Unit data sheet. ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
78	ExtLOS	I	**Receive LOS (Loss of Signal) Indicator Input (from XRT73L00 LIU IC):** This input pin is intended to be connected to the RLOS (Receive Loss of Signal) output pin of the XRT73L00 Line Interface Unit IC. The user can monitor the state of this pin by reading the state of Bit 0 (RLOS) within the Line Interface Scan Register (Address = 0x81). If this input pin is "Low", then it means that the XRT73L00 is currently NOT declaring an LOS (Loss of Signal) condition. However, if this input pin is "High", then it means that the XRT73L00 is currently declaring an LOS (Loss of Signal) condition. For more information on the operation of the XRT73L00 DS3/E3 Line Receiver IC, please consult the XRT73L00 DS3/STS-1/E3 Line Interface Unit IC data sheet. Asserting the RLOS input pin will cause the XRT72L50 DS3/E3 Framer device to declare an LOS (Loss of Signal) condition. Therefore, this input pin should not be used as a general purpose input pin.
79	DMO	I	**Drive Monitor Output Input (from the XRT73L00 DS3/E3 Line Interface Unit IC):** This input pin is intended to be connected to the DMO output pin of the XRT73L00 DS3/E3 Line Interface Unit IC. The user can determine the state of this input pin by reading Bit 2 (DMO) within the Line Interface Scan Register (Address = 0x81). If this input signal is "High", then it means that the drive monitor circuitry (within the XRT73L00 DS3/E3 Line Interface Unit IC) has not detected any bipolar signals at the MTIP and MRING inputs within the last 128 (32 bit-periods. If this input signal is "Low", then it means that bipolar signals are being detected at the MTIP and MRING input pins of the XRT73L00. If this customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then he/she can use this input pin for a variety of other purposes.
80	VDD	****	**Power Supply 3.3V ± 5%**
81	GND	****	**Ground**
82	RxNib3/ RxHDLCDat3	O	**Receive Nibble Output - 3:** The Framer IC will output Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0, RxNib1 and RxNib2. The data at this pin is updated on the rising edge of the RxClk output signal. ***NOTE:*** *This output pin is active only if the Nibble-Parallel Mode has been selected.* **Receive HDLC Data Output - 3:** This pin contains bit 3 RxHDLC data when the HDLC controller is on.
83	RxNib2/ RxHDLCDat2	O	**Receive Nibble Output - 2:** The Framer IC will output Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0, RxNib1 and RxNib2. The data at this pin is updated on the rising edge of the RxClk output signal. ***NOTE:*** *This output pin is active only if the Nibble-Parallel Mode has been selected.* **Receive HDLC Data Output - 2:** This pin contains bit 2 RxHDLC data when the HDLC controller is on.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
84	RxNib1/ RxHDLCDat1	O	**Receive Nibble Output - 1:** The Framer IC will output Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0, RxNib2 and RxNib3. The data at this pin is updated on the rising edge of the RxClk output signal. ***NOTE:*** *This output pin is active only if the Nibble-Parallel Mode has been selected.* **Receive HDLC Data Output - 1:** This pin contains bit 1 RxHDLC data when the HDLC controller is on.
85	RxNib0/ RxHDLCDat0	O	**Receive Nibble Output - 0:** The Framer IC will output Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib1, RxNib2 and RxNib3. The data at this pin is updated on the rising edge of the RxClk output signal. ***NOTE:*** *This output pin is active only if the Nibble-Parallel Mode has been selected.* **Receive HDLC Data Output - 0:** This pin contains bit 0 RxHDLC data when the HDLC controller is on.
86	RxSer/ RxIdle	O	**Receive Serial Output:** If the user opts to operate the XRT72L50 in the serial mode, then the chip will output the payload data, of the incoming DS3 or E3 frames, via this pin. The XRT72L50 will output this data upon the rising edge of RxClk. The user is advised to design the Terminal Equipment such that it will sample this data on the falling edge of RxClk. ***NOTE:*** *This signal is only active if the NibIntf input pin is pulled "Low".* **Receive Idle:** This pin will go "High" indicating the idle period of sent HDLC data packets. Also, in combination with ValFCS it can indicate error conditions.
87	RxAIS	O	**Receive Alarm Indication Signal Output pin:** The Framer will assert this pin to indicate that the Alarm Indication Signal (AIS) has been identified in the Receive DS3 or E3 data stream. **For DS3 Applications:** The Framer will assert this pin to indicate that the Alarm Indication Signal (AIS) has been identified in the Receive DS3 data stream. An AIS is detected if the payload consists of the recurring pattern of 1010... and this pattern persists for 63 M-frames. An additional requirement for AIS indication is that the C-bits are set to 0, and the X-bits are set to 1. This pin will be negated when a sufficient number of frames, not exhibiting the 1010... pattern in the payload has been detected. **For E3 Applications:** The Receive Section will declare an AIS condition, if it detects two consecutive E3 frames, each containing 7 or less "0s".

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
88	RxClk	O	**Receive Clock Output Signal for Serial and Nibble/Parallel Data Interface:** The exact behavior of this signal depends upon whether the XRT72L50 is operating in the Serial or in the Nibble-Parallel-Mode. **Serial Mode Operation:** In the serial mode, this signal is a 44.736MHz clock output signal (for DS3 applications) or 34.368MHz clock output signal (for E3 applications). The Receive Payload Data Output Interface will update the data via the RxSer output pin, upon the rising edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxSer pin, upon the falling edge of this clock signal. **Nibble-Parallel Mode Operation:** In this Nibble-Parallel Mode, the XRT72L50 will derive this clock signal, from the RxLineClk signal. The XRT72L50 will pulse this clock signal 1176 times for each inbound DS3 frame (or 1074 times for each inbound E3/ITU-T G.832 frame, or 384 times for each inbound E3/ITU-T G.751 frame). The Receive Payload Data Output interface will update the data, on the RxNib[3:0] output pins upon the falling edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxNib[3:0] output pins, upon the rising edge of this clock signal
89	GND	****	**Ground**
90	RxFrame	O	**Receive Boundary of DS3 or E3 Frame Output Indicator:** The exact functionality of this output pin depends upon whether the XRT72L50 Framer IC is operating in the Serial or Nibble-Parallel Mode. **Serial Mode Operation:** The Receive Section of the XRT72L50 will pulse this output pin "High" (for one bit-period) when the Receive Payload Data Output Interface block is driving the very first bit of a given DS3 or E3 frame, onto the RxSer output pin. **Nibble-Parallel Operation:** The Receive Section of the XRT72L50 will pulse this output pin "High" (for one nibble-period), when the Receive Payload Data Output Interface block is driving the very first nibble of a given DS3 or E3 frame, onto the RxNib[3:0] output pins.
91	VDD	****	**Power Supply 3.3V ± 5%**
92	RxOutClk/ RxHDLCDat7	O	**Receive Out Clock - Transmit Terminal Interface Clock for Loop-Timing:** This clock signal functions as the Terminal Interface clock source, if the XRT72L50 Framer IC is operating in the loop-timing mode. In this mode, the Transmitting Terminal Equipment is expected to input data to the Framer IC, via the TxSer input pin, upon the rising edge of this clock signal. The XRT72L50 will use the rising edge of this clock signal to sample the data at the TxSer input. This clock signal is a buffered version of the RxLineClk signal. **Receive HDLC Data Output - 7:** This pin contains bit 7 RxHDLC data when the HDLC controller is on.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
93	RxRed	O	**Receiver Red Alarm Indicator - Receive Framer:** The Framer asserts this output pin to denote that one of the following events has been detected by the Receive Framer: LOS - Loss of Signal Condition OOF - Out of Frame Condition AIS - Alarm Indication Signal Detection
94	RxOOF	O	**Receiver Out of Frame Indicator:** The Receive Section of the XRT72L50 Framer IC will assert this output signal whenever it has declared an Out of Frame (OOF) condition with the incoming DS3 or E3 frames. This signal is negated when the framer correctly locates the framing alignment bits or bytes and correctly aligns itself with the incoming DS3 or E3 frames.
95	RxLOS	O	**Receive Section - Loss of Signal Output Indicator:** This pin is asserted when the Receive Section encounters a string of 180 consecutive 0's (for DS3 operation) or 32 consecutive 0's (for E3 operation) via the RxPOS and RxNEG pins. This pin will be negated once the Receive Section has detected at least 60 pulses within 180 bit-periods (for DS3 operation); or the Receive Section has detected a string of 32 consecutive bits, that does not contain a string of 4 consecutive "0s" (for E3 operation).
96	RxOHClk/ RxHDLCClk	O	**Receive Overhead Output Clock Signal:** The XRT72L50 will output the Overhead bits (within the incoming DS3 or E3 frames), via the RxOH output pin, upon the falling edge of this clock signal. As a consequence, the user's data link equipment should use the rising edge of this clock signal to sample the data on both the RxOH and RxOHFrame output pins. ***NOTE:*** *This clock signal is always active.* **Receive HDLC Output Clock:** When the HDLC controller is on, RxHDLCDat is updated by the 72L53 on this clock signal.
97	RxOHInd	O	**Receive Overhead Bit Indicator:** The exact functionality of this output pin depends upon whether the XRT72L50 Framer IC is operating in the Serial or Nibble-Parallel Mode. **Serial Mode Operation:** This output pin pulses "High" (for one bit-period) whenever an overhead bit is being output via the RxSer output pin, by the Receive Payload Data Output Interface block. **Nibble-Parallel Mode Operation:** This output pin pulses "High" (for one nibble-period) whenever an overhead nibble is being output via the RxNib[3:0] output pins, by the Receive Payload Data Output Interface block. ***NOTE:*** *The purpose of this output pin is to alert the Receive Terminal Equipment that an overhead bit is being output via the RxSer output pin, and that this data should be ignored.*

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
98	RxOH/ RxHDLCDat6	O	**Receive Overhead Output Port:** All overhead bits, which are received via the Receive Section of the Framer IC; will be output via this output pin, upon the rising edge of RxOHClk. **Receive HDLC Data Output - 6:** This pin contains bit 6 RxHDLC data when the HDLC controller is on.
99	RxOHEnable/ RxHDLCDat5	O	**Receive Overhead Enable Indicator:** The XRT72L50 will assert this output signal for one RxOutClk period when it is safe for the Terminal Equipment to sample the data on the RxOH output pin. **Receive HDLC Data Output - 5:** This pin contains bit 5 RxHDLC data when the HDLC controller is on.
100	RxOHFrame/ RxHDLCDat4	O	**Receive Overhead Frame Boundary Indicator:** This output pin pulses "High" whenever the Receive Overhead Data Output Interface" block outputs the first overhead bit (or nibble) of a new DS3 or E3 frame. **Receive HDLC Data Output - 4:** This pin contains bit 4 RxHDLC data when the HDLC controller is on.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUMS

Power Supply..... -0.3V to +3.6V		Power Dissipation PQFP Package..... 1.2W
Storage Temperature .....-55°C to 150°C		Input Voltage (Any Pin) .....-0.3V to VDD + 0.3V
Voltage at Any Pin ..... -0.3V to VDD + 0.3V		Input Current (Any Pin) ..... ± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{CC}	Power Supply Current		120		mA	All Channels on
V_{IL}	Input Low Voltage			0.3*VDD	V	
V_{IH}	Input High Voltage	0.7*VDD			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = -1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 40µA
I_{IH}	Input High Voltage Current	-10		10	µA	V_{IH} = VDD
I_{IL}	Input Low Voltage Current	-1		1	µA	V_{IL} = GND

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Transmit Payload Data Input Interface - Loop-Timed/Serial Mode (See Figure 3)						
t_1	Payload data (TxSer) set-up time to rising edge of RxOutClk	12			ns	
t_2	Payload data (TxSer) hold time, from rising edge of RxOutClk	0			ns	
t_3	RxOutClk to TxFrame output delay			5	ns	
t_4	RxOutClk to TxOHInd output delay			6	ns	
Transmit Payload Data Input Interface - Local Timed/Serial Mode (See Figure 4)						
t_5	Payload data (TxSer) set-up time to rising edge of TxInClk	4			ns	
t_6	Payload data (TxSer) hold time, from rising edge of TxInClk	0			ns	
t_7	TxFrameRef set-up time to rising edge of TxInClk	2			ns	Framer IC is Frame Slave
t_8	TxFrameRef hold-time, from rising edge of TxInClk	0			ns	Frame IC is Frame Slave

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_9	TxInClk to TxOHInd output delay			15	ns	
t_{10}	TxInClk to TxFrame output delay			13	ns	
Transmit Payload Data Input Interface - Looped-Timed/Nibble Mode (See Figure 5)						
t_{11}	TxNib set-up time to third rising edge of RxOutClk	30			ns	
t_{12}	Payload Nibble hold time, from latching edge of RxOutClk	30			ns	
t_{13}	TxNibClk to TxNibFrame output delay			25 31	ns ns	DS3 Applications E3 Applications
t_{13A}	Max Delay of Rising Edge of TxNibClk to Data Valid on TxNib[3:0]			20 27	ns ns	DS3 Applications E3 Applications
Transmit Payload Data Input Interface - Local-Timed/Nibble Mode (See Figure 6)						
t_{14}	TxNib set-up time to third rising edge of TxInClk			20 27	ns ns	DS3 Applications E3 Applications
t_{15}	Payload Nibble hold time, from latching edge of TxInClk	0			ns	
t_{16}	TxFrameRef set-up time, to latching edge of TxInClk			20 27	ns ns	DS3 Applications E3 Applications Framer IC is Frame Slave
t_{17}	TxFrameRef hold time, from latching edge of TxNibClk	0			ns	Framer IC is Frame Slave
t_{18}	TxNibClk to TxNibFrame output delay time	20		25 31	ns ns	DS3 Applications E3 Applications

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Transmit Overhead Input Interface Timing - Method 1 (Figure 7)						
t_{21}	TxOHClk to TxOHFrame output delay			111	ns	DS3 Applications
				0	ns	E3, ITU-T G.832 Applications
				0	ns	E3, ITU-T G.751 Applications
t_{22}	TxOHIns set-up time, to falling edge of TxOHClk	194			ns	DS3 Applications
		305			ns	E3, ITU-T G.832 Applications
		17			ns	E3, ITU-T G.751 Applications
t_{23}	TxOHIns hold time, from falling edge of TxOHClk	48			ns	DS3 Applications
		110			ns	E3, ITU-T G.832 Applications
		7			ns	E3, ITU-T G.751 Applications
t_{24}	TxOH data set-up time, to falling edge of TxOHClk	194			ns	DS3 Applications
		305			ns	E3, ITU-T G.832 Applications
		17			ns	E3, ITU-T G.751 Applications
t_{25}	TxOH data hold time, from falling edge of TxOHClk	48			ns	DS3 Applications
		110			ns	E3, ITU-T G.832 Applications
		7			ns	E3, ITU-T G.751 Applications
Transmit Overhead Data Input Interface - Method 2 (Figure 8)						
t_{26}	TXOHIns to TxInClk (rising edge) set-up Time	254			ns	DS3 Applications
		72			ns	E3, ITU-T G.832 Applications
		15			ns	E3, ITU-T G.751 Applications

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{27}	TxInClk clock (rising edge) to TxOHIns hold-time	0			ns	DS3 Applications
		0			ns	E3, ITU-T G.832 Applications
		0			ns	E3, ITU-T G.751 Applications
t_{28}	TXOH to TxInClk (rising edge) set-up Time	254			ns	DS3 Applications
		72			ns	E3, ITU-T G.832 Applications
		15			ns	E3, ITU-T G.751 Applications
t_{29}	TxInClk clock (rising edge) to TxOH hold-time	0			ns	DS3 Applications
		0			ns	E3, ITU-T G.832 Applications
		0			ns	E3, ITU-T G.751 Applications
t_{29A}	TxOHEnable to TxOHIns/TxOH Delay	1			ns	
Transmit LIU Interface Timing (see Figure 9 and Figure 10)						
t_{31}	Rising or falling edge of TxLineClk to rising edge of TxPOS or TxNEG			2.4	ns	
t_{32}	Period of TxLineClk		22.36		ns	DS3 Applications
			29.10		ns	E3 Applications
t_{33}	RxPOS, RxNEG hold time from rising edge of TxLnClk	3			ns	
Receive LIU Interface Timing (see Figure 11 and Figure 12)						
t_{38}	RxPOS or RxNEG set-up time to rising edge or falling edge of RxLineClk.	0			ns	
t_{39}	RxPOS or RxNEG hold time, from rising edge or falling edge of RxLineClk (Framer is configured to sample data on RxPOS and RxNEG input pins on the rising edge of RxLineClk)	4			ns	
t_{42}	Period of RxLineClk		22.36		ns	DS3 Applications
			29.10		ns	E3 Applications
Receive Payload Data Output Interface Timing - Serial Mode Operation (See Figure 13)						
t_{50}	Rising edge of RxClk to Payload Data (RxSer) output delay			13	ns	DS3 Applications
				16	ns	E3 Applications

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{51}	Rising edge of RxClk to RxFrame output delay			13	ns	DS3 Applications
				16	ns	E3 Applications
t_{52}	Rising edge of RxClk to RxOHInd output delay.			13	ns	DS3 Applications
				16	ns	E3 Applications
Receive Payload Data Output Interface Timing - Nibble Mode Operation (see Figure 14)						
t_{53}	Falling edge of RxClk to rising edge of RxFrame output delay			2.1	ns	
t_{54}	Falling edge of RxClk to rising edge of RxNib[3:0] output delay			2	ns	
Receive Overhead Data Output Interface Timing - Method 1 - Using RxOHClk (see Figure 15)						
t_{59A}	Falling edge of RxOHClk to RxOHFrame output	20		23	ns	DS3 Applications
		25		0	ns	E3 Applications
t_{59B}	Falling edge of RxOHClk to RxOH output delay	20		23	ns	DS3 Applications
		25		0	ns	E3 Applications
Receive Overhead Data Output Interface Timing - Method 2 - Using RxOHEnable (see Figure 16)						
t_{60}	Rising edge of RxOutClk to rising edge of RxOHEnable delay.	2		9.4	ns	
t_{60A}	Rising edge of RxOHFrame to rising edge of RxOHEnable delay			88	ns	DS3 Applications
				224	ns	E3, ITU-T G.832 Applications
				28	ns	E3, ITU-T G.751 Applications
t_{60B}	RxOH Data Valid to rising edge of RxOHEnable delay			88	ns	DS3 Applications
				85	ns	E3, ITU-T G.832 Applications
				28	ns	E3, ITU-T G.751 Applications
Microprocessor Interface - Intel (See Figure 17)						
t_{64}	$\overline{CS}$ Setup Time to ALE_AS Low	0			ns	
t_{65}	$\overline{CS}$ Hold Time from ALE_AS Low.	1			ns	
t_{66}	$\overline{RD}$_$\overline{DS}$, $\overline{WR}$_R/$\overline{W}$ Pulse Width	87			ns	
Intel Type Read Operations (See Figure 17)						
t_{67}	Data Valid from $\overline{RD}$_$\overline{DS}$ Low.	32			ns	
t_{68}	Data Bus Floating from $\overline{RD}$_$\overline{DS}$ High	9			ns	
t_{69}	$\overline{CS}$ to $\overline{RD}$ read or write Time	3			ns	

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_{701}	$\overline{RD}$ Time to NOT READY (e.g., $\overline{RDY}$_$\overline{DTCK}$ toggling Low)			16	ns	
t_{70}	$\overline{RD}$ to READY Time (e.g., $\overline{RDY}$_$\overline{DTCK}$ toggling high)			80	ns	
Intel Type Write Operations (Figure 18)						
t_{71}	Data Setup Time to $\overline{WR}$_R/$\overline{W}$ High	0			ns	
t_{72}	Data Hold Time from $\overline{WR}$_R/$\overline{W}$ High	3			ns	
t_{73}	High Time between Reads and/or Writes	33			ns	
t_{74}	ALE to $\overline{WR}$ Time	3			ns	
Microprocessor Interface - Motorola (See Figure 19)						
t_{78}	A[8:0] Setup Time to falling edge of ALE_AS	0			ns	
Motorola Type Read Operations (See Figure 19)						
t_{79}	Rising edge of $\overline{RD}$_$\overline{DS}$ to rising edge of $\overline{RDY}$_$\overline{DTCK}$ delay			16	ns	
t_{80}	Rising edge of $\overline{RDY}$_$\overline{DTCK}$ to tri-state of D[7:0]			0	ns	
Motorola Type Write Operations (See Figure 20)						
t_{81}	D[7:0] Set-up time to falling edge of $\overline{RD}$_$\overline{DS}$	0			ns	
t_{82}	Rising edge of $\overline{RD}$_$\overline{DS}$ to rising edge of $\overline{RDY}$_$\overline{DTCK}$ delay			13	ns	
Reset Pulse Width - Both Motorola and Intel Operations (See Figure 21)						
t_{90}	$\overline{Reset}$ pulse width	200			ns	

1.0 TIMING DIAGRAMS

FIGURE 3. TIMING DIAGRAM FOR TRANSMIT PAYLOAD INPUT INTERFACE, WHEN THE XRT72L50 DEVICE IS OPERATING IN BOTH THE DS3 AND LOOP-TIMING MODES

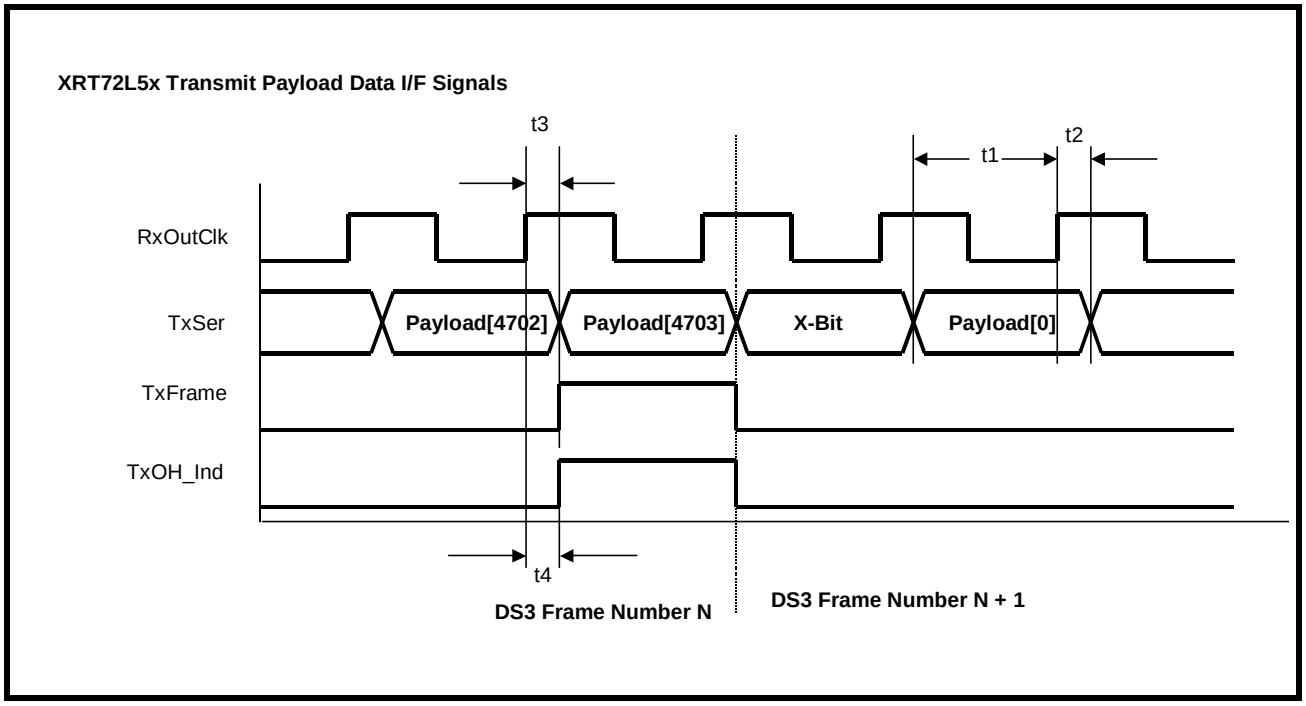


FIGURE 4. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD INPUT INTERFACE, WHEN THE XRT72L50 DEVICE IS OPERATING IN BOTH THE DS3 AND LOCAL-TIMING MODES

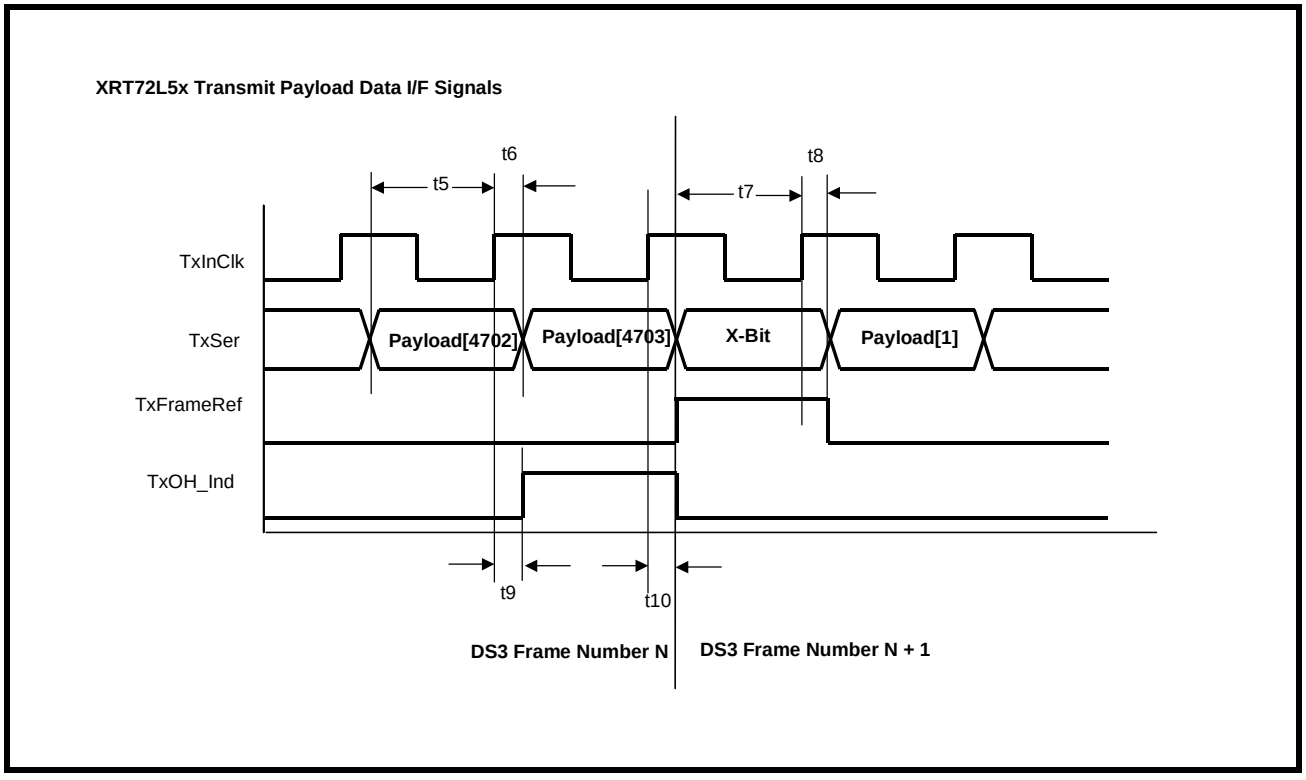


FIGURE 5. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE, WHEN THE XRT72L50 DEVICE IS OPERATING IN BOTH THE DS3/NIBBLE AND LOOPED-TIMING MODES

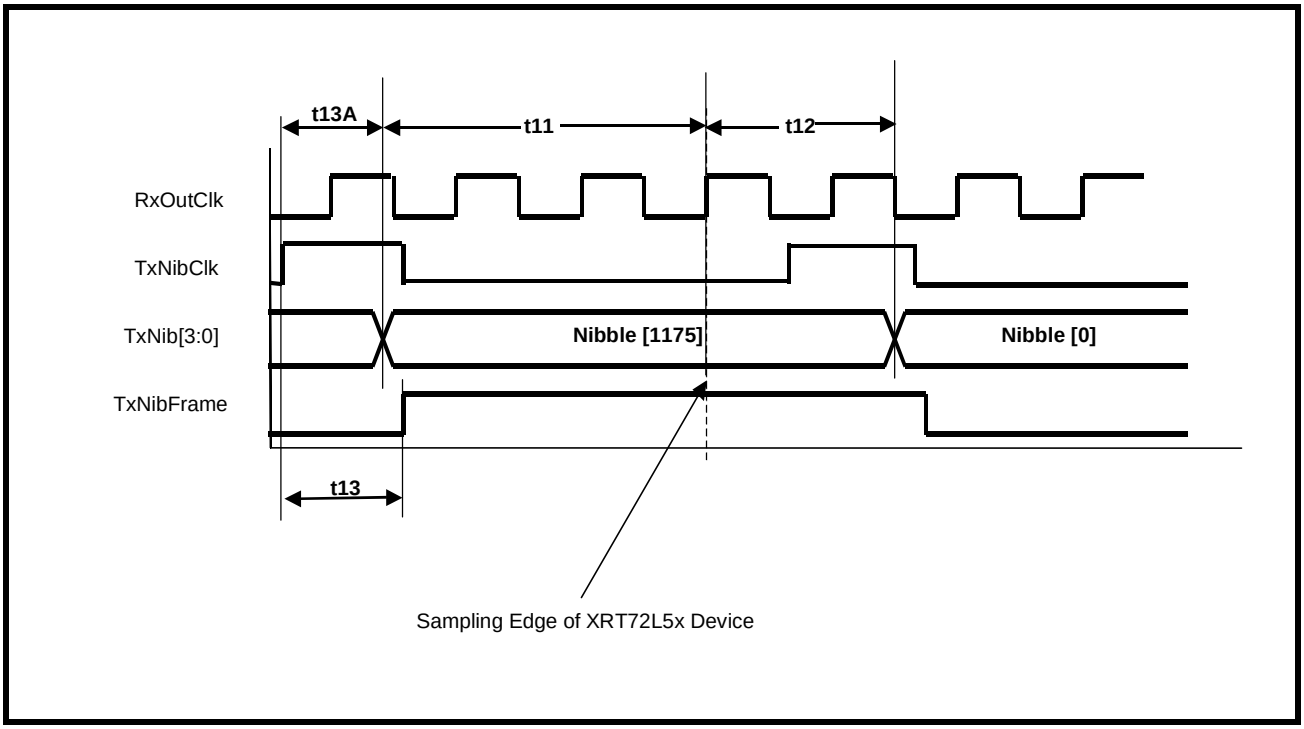


FIGURE 6. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE, WHEN THE XRT72L50 DEVICE IS OPERATING IN THE DS3/NIBBLE AND LOCAL-TIMING MODES

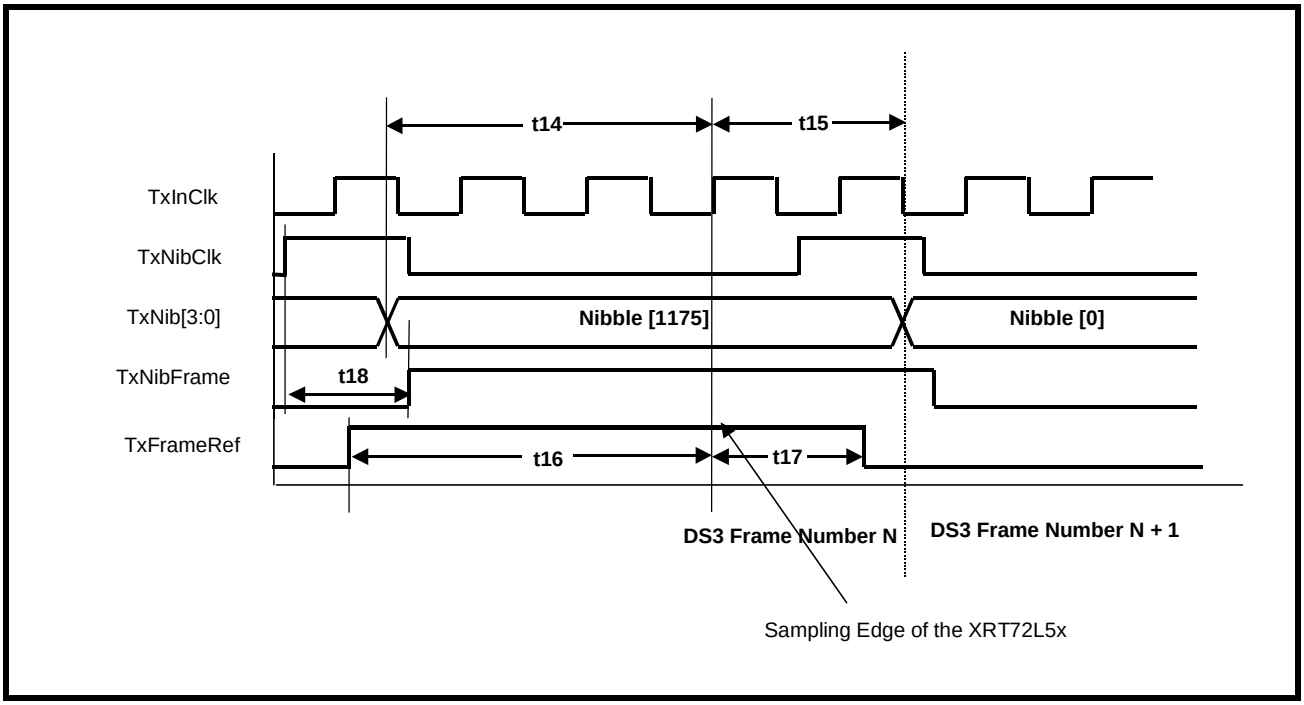


FIGURE 7. TIMING DIAGRAM FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 1 ACCESS)

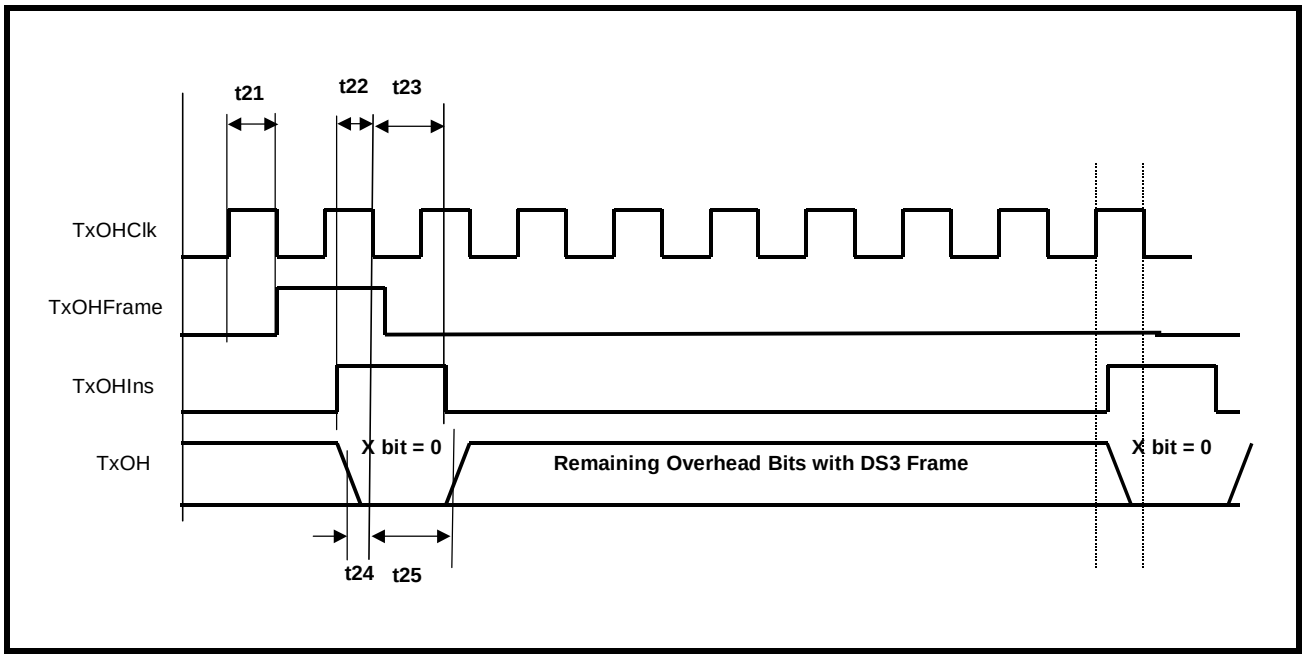


FIGURE 8. TIMING DIAGRAM FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 2 ACCESS)

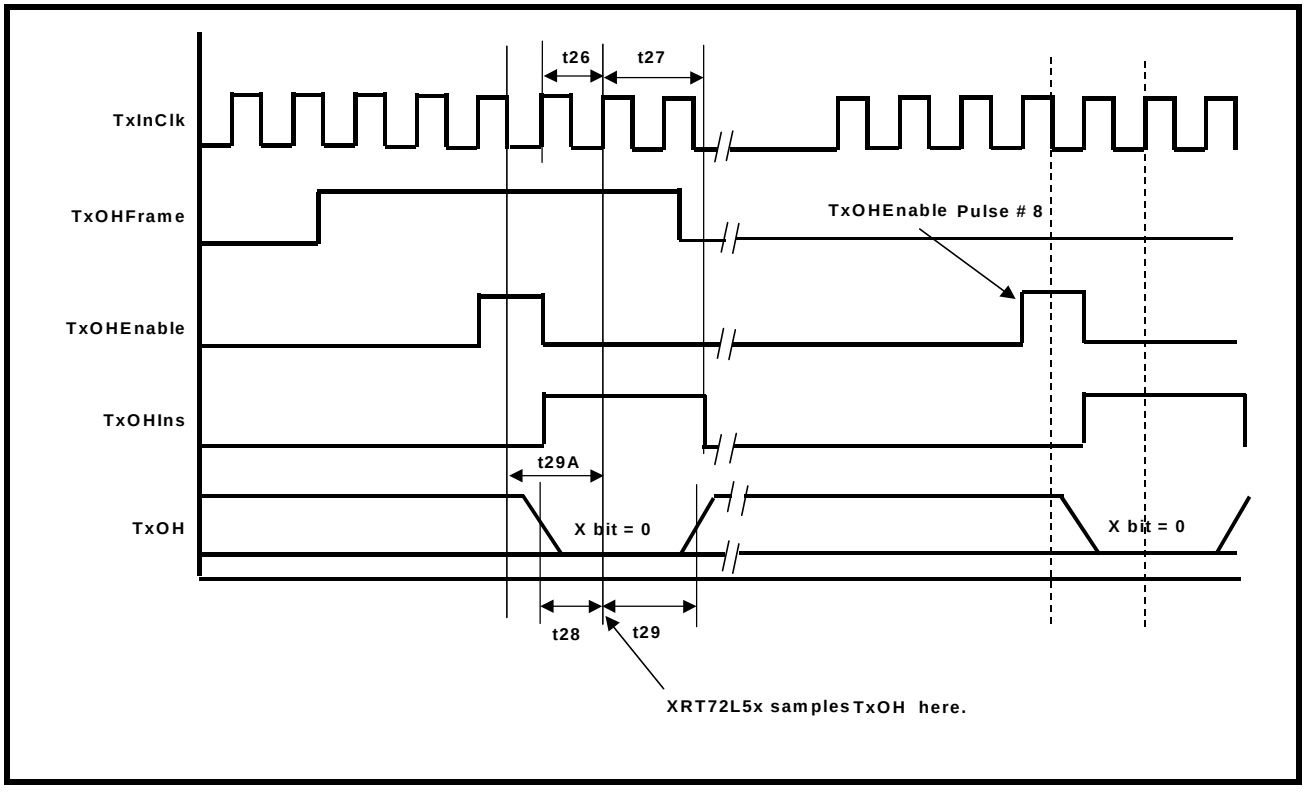


FIGURE 9. TRANSMIT LIU INTERFACE TIMING - TXPOS AND TXNEG ARE UPDATED ON THE RISING EDGE OF TXLINECLK

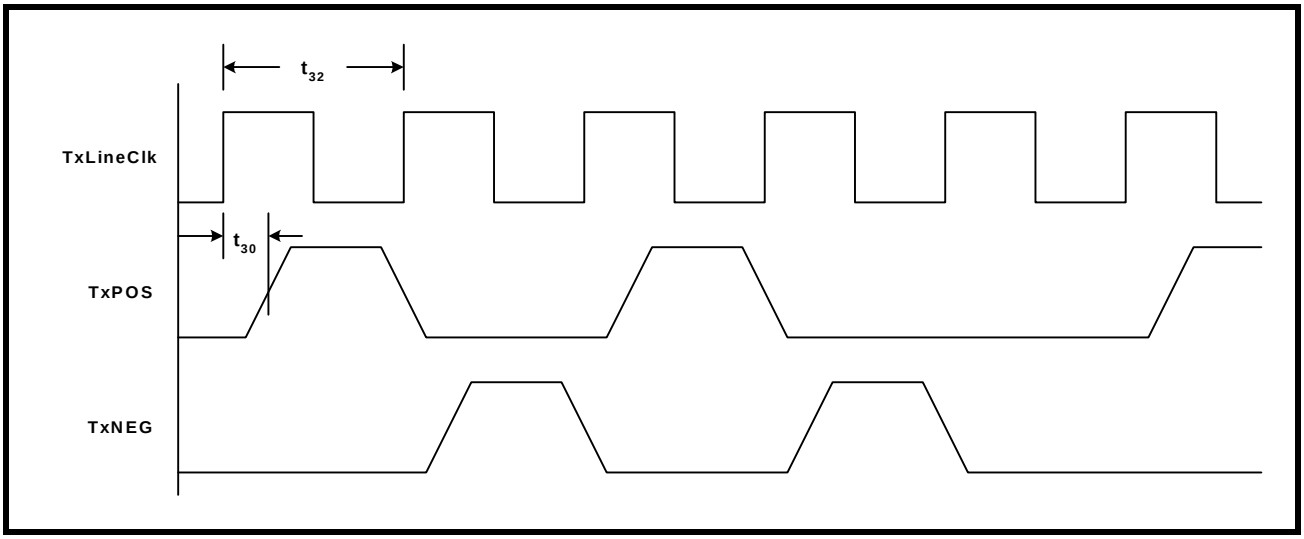


FIGURE 10. TRANSMIT LIU INTERFACE TIMING - TXPOS AND TXNEG ARE UPDATED ON THE FALLING EDGE OF TXLINECLK

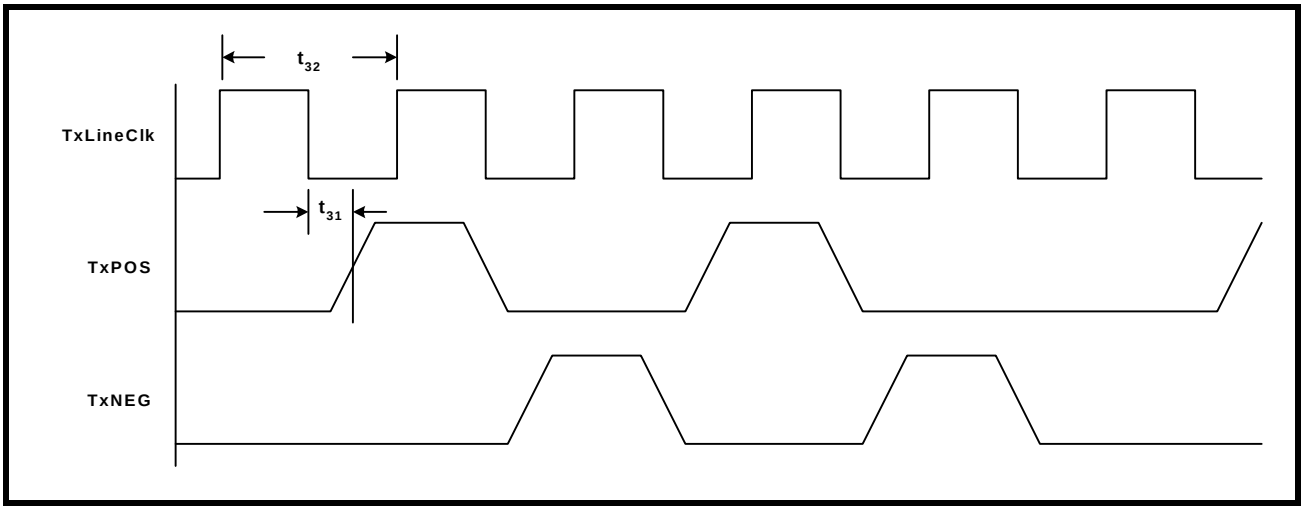


FIGURE 11. RECEIVE LIU INTERFACE TIMING - RXPOS AND RXNEG ARE SAMPLED ON RISING EDGE OF RXLINECLK

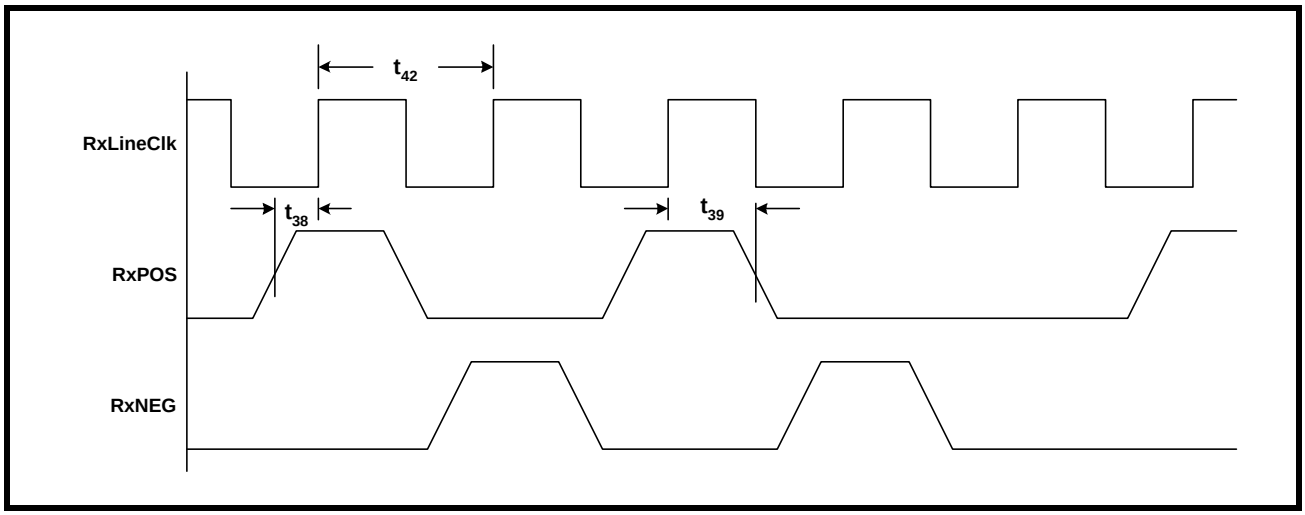


FIGURE 12. RECEIVE LIU INTERFACE TIMING - RXPOS AND RXNEG ARE SAMPLED ON FALLING EDGE OF RXLINECLK

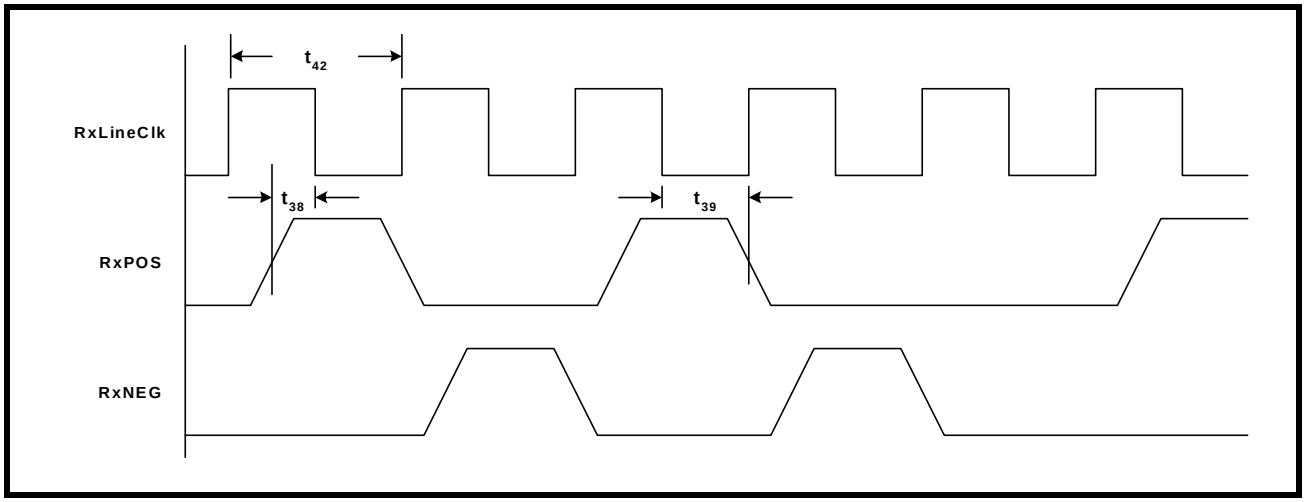


FIGURE 13. RECEIVE PAYLOAD DATA OUTPUT INTERFACE TIMING

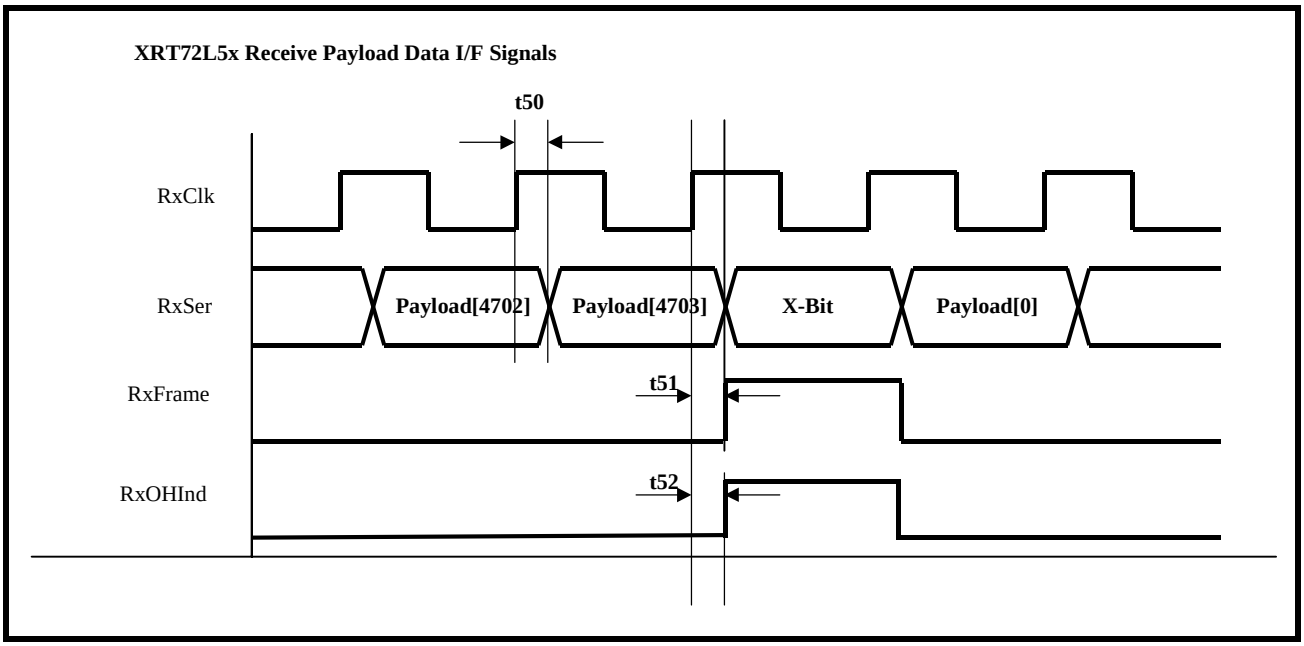


FIGURE 14. RECEIVE PAYLOAD DATA OUTPUT INTERFACE TIMING (NIBBLE MODE OPERATION)

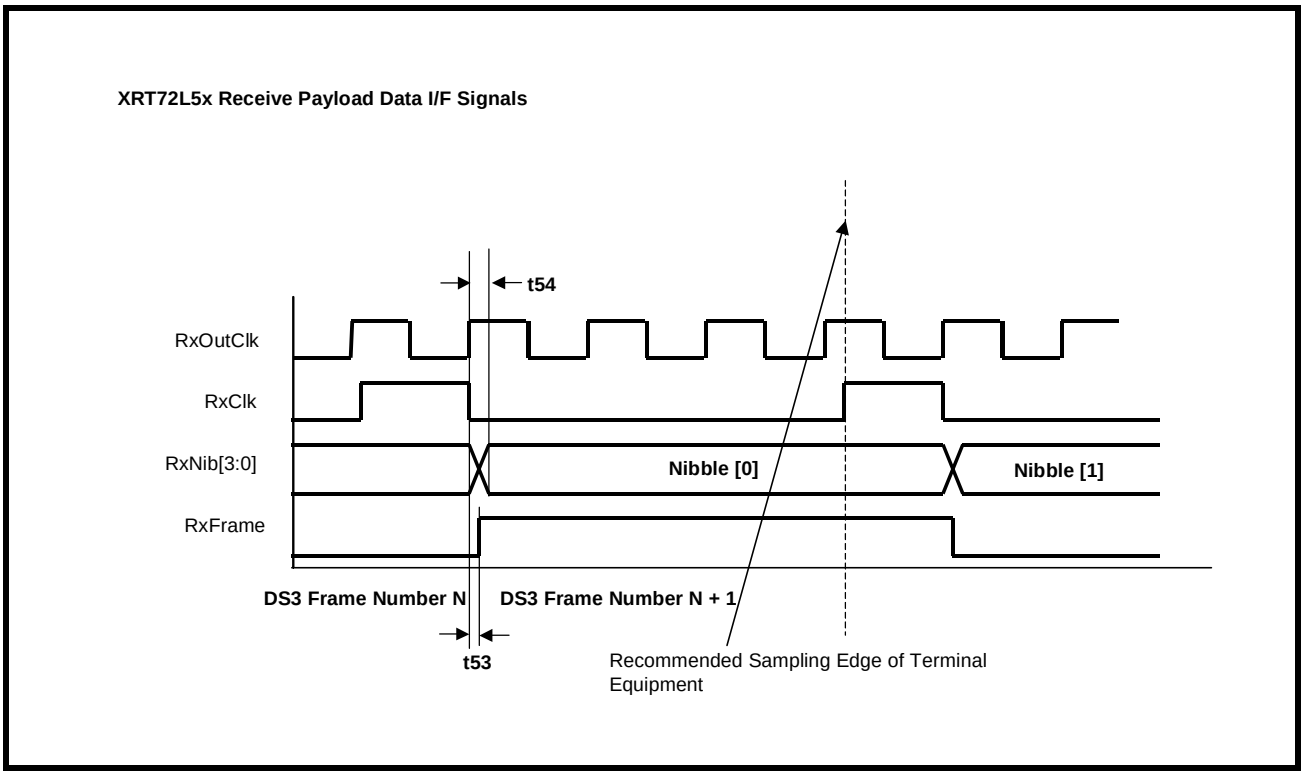


FIGURE 15. RECEIVE OVERHEAD DATA OUTPUT INTERFACE TIMING (METHOD 1 - USING RXOHCLK)

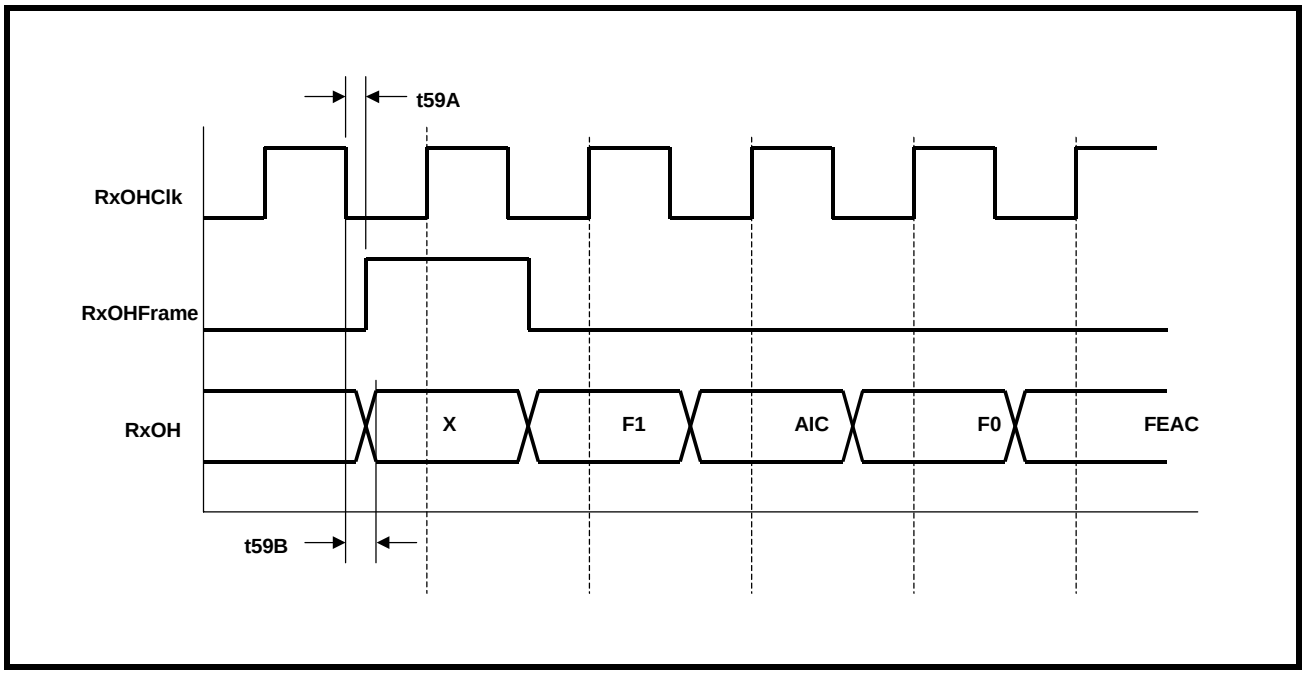


FIGURE 16. RECEIVE OVERHEAD DATA OUTPUT INTERFACE TIMING (METHOD 2 - USING RXOHENABLE)

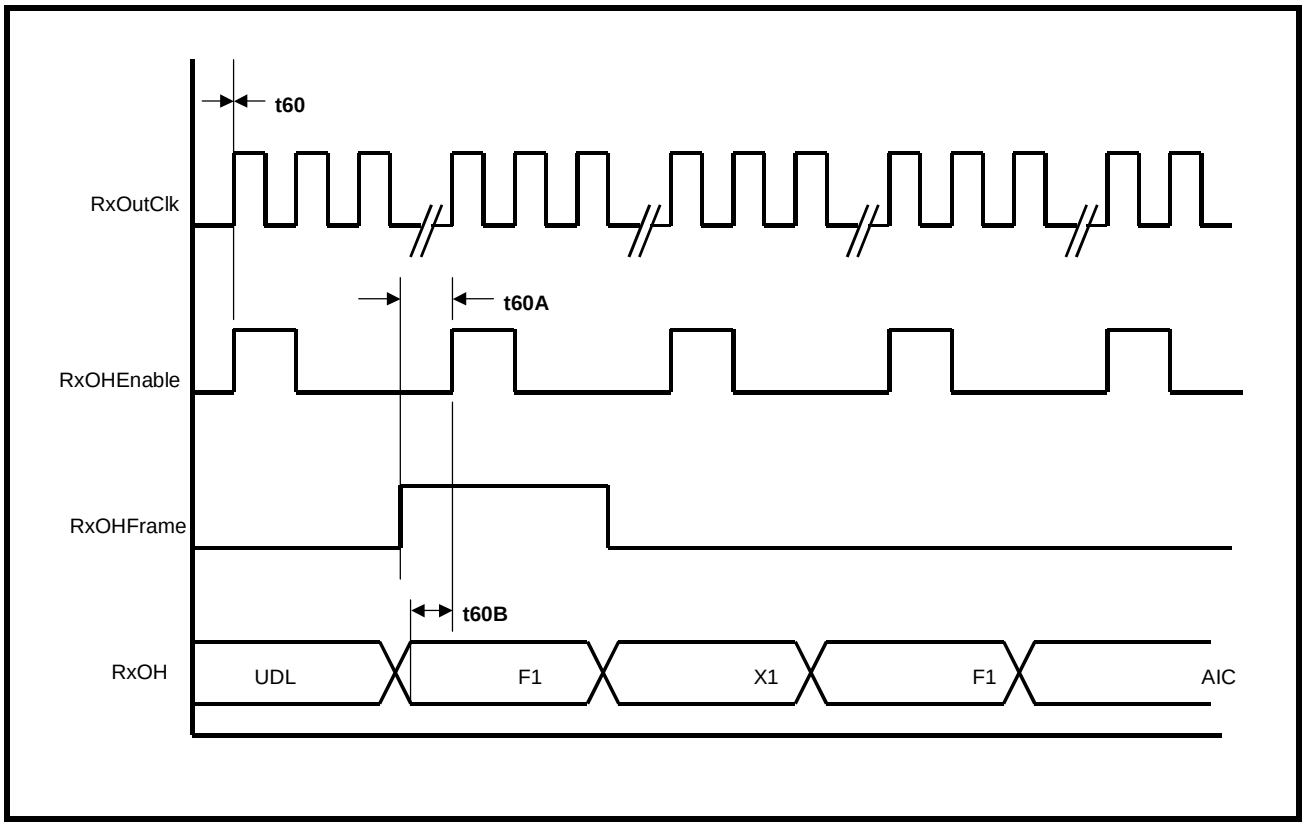


FIGURE 17. MICROPROCESSOR INTERFACE TIMING - INTEL-TYPE PROGRAMMED I/O READ OPERATION

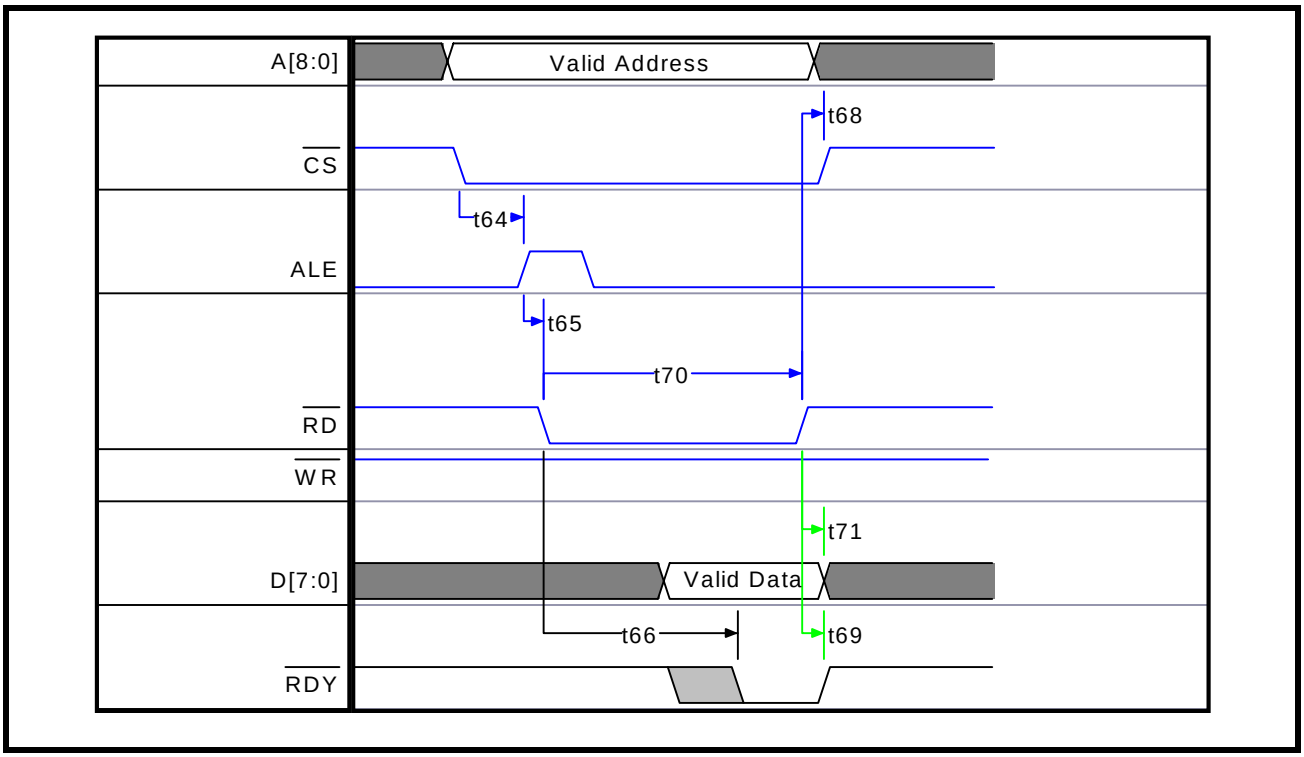


FIGURE 18. MICROPROCESSOR INTERFACE TIMING - INTEL-TYPE PROGRAMMED I/O WRITE OPERATION

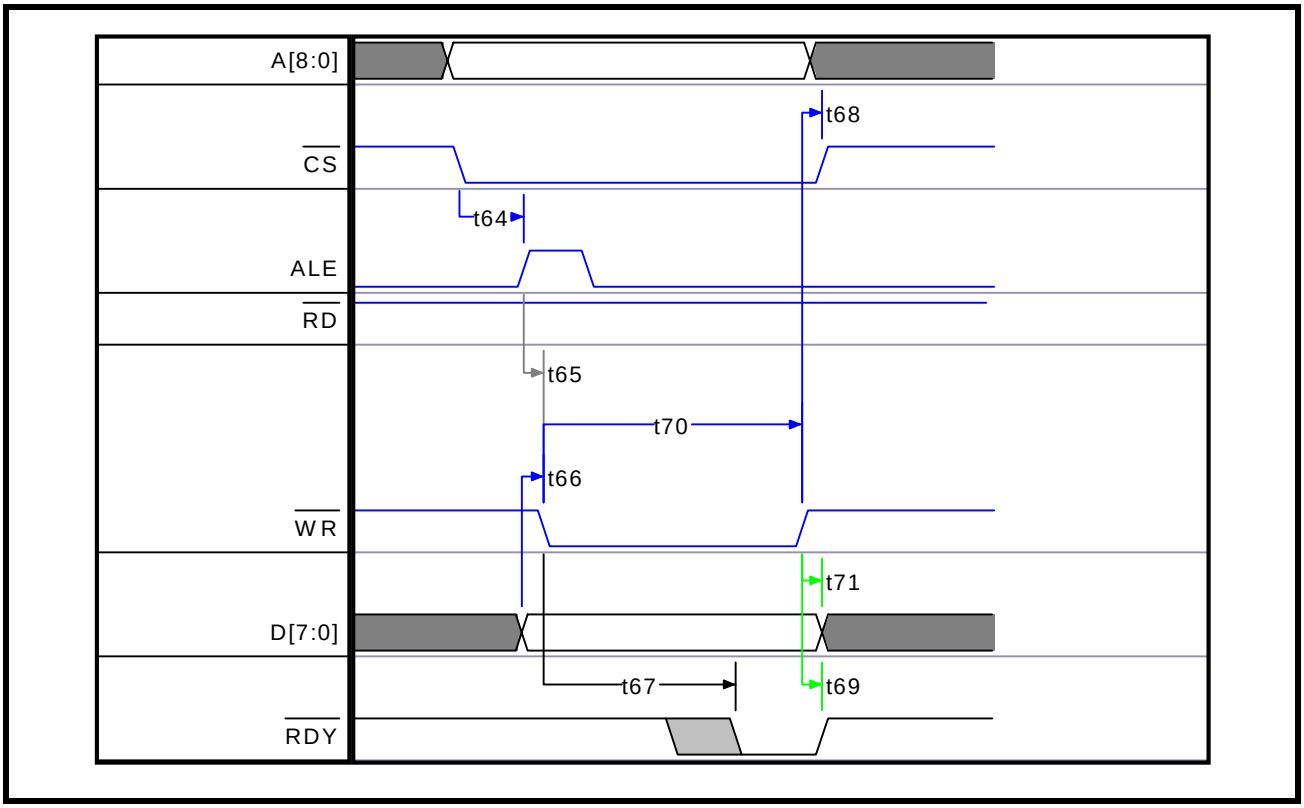


FIGURE 19. MICROPROCESSOR INTERFACE TIMING - MOTOROLA-TYPE PROGRAMMED I/O READ OPERATION

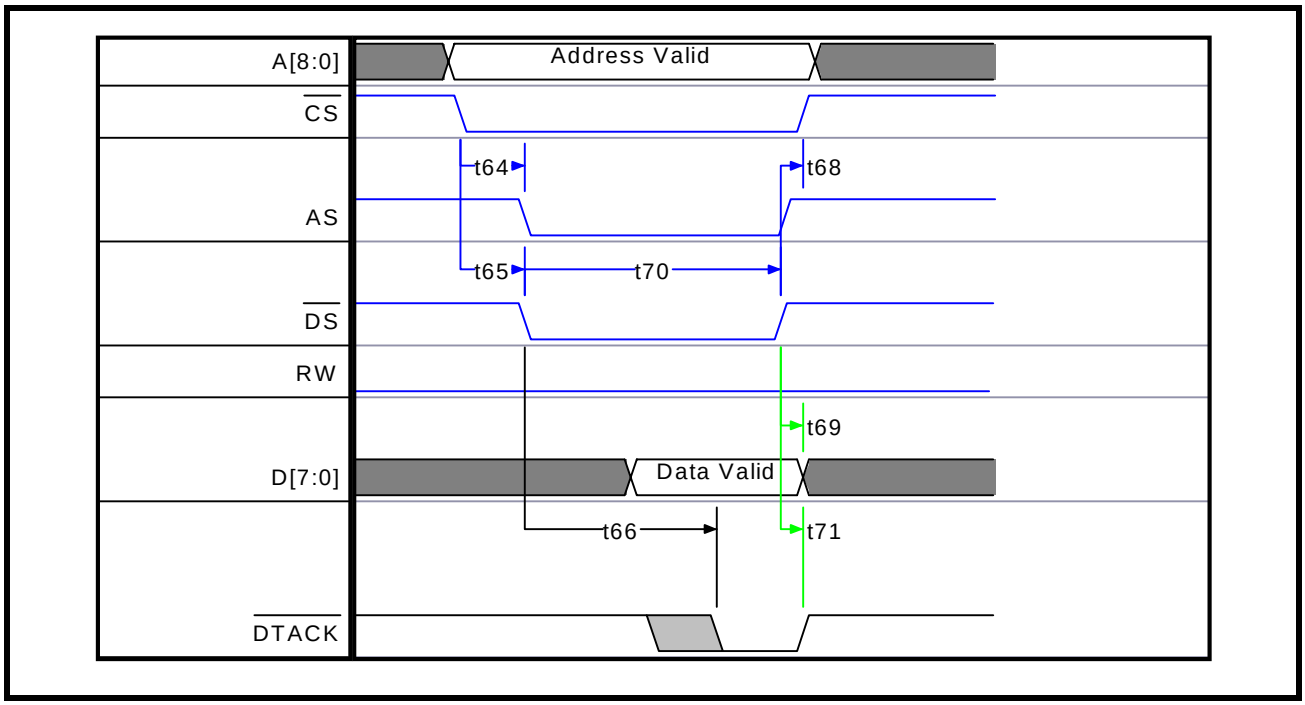


FIGURE 20. MICROPROCESSOR INTERFACE TIMING - MOTOROLA-TYPE PROGRAMMED I/O WRITE OPERATION

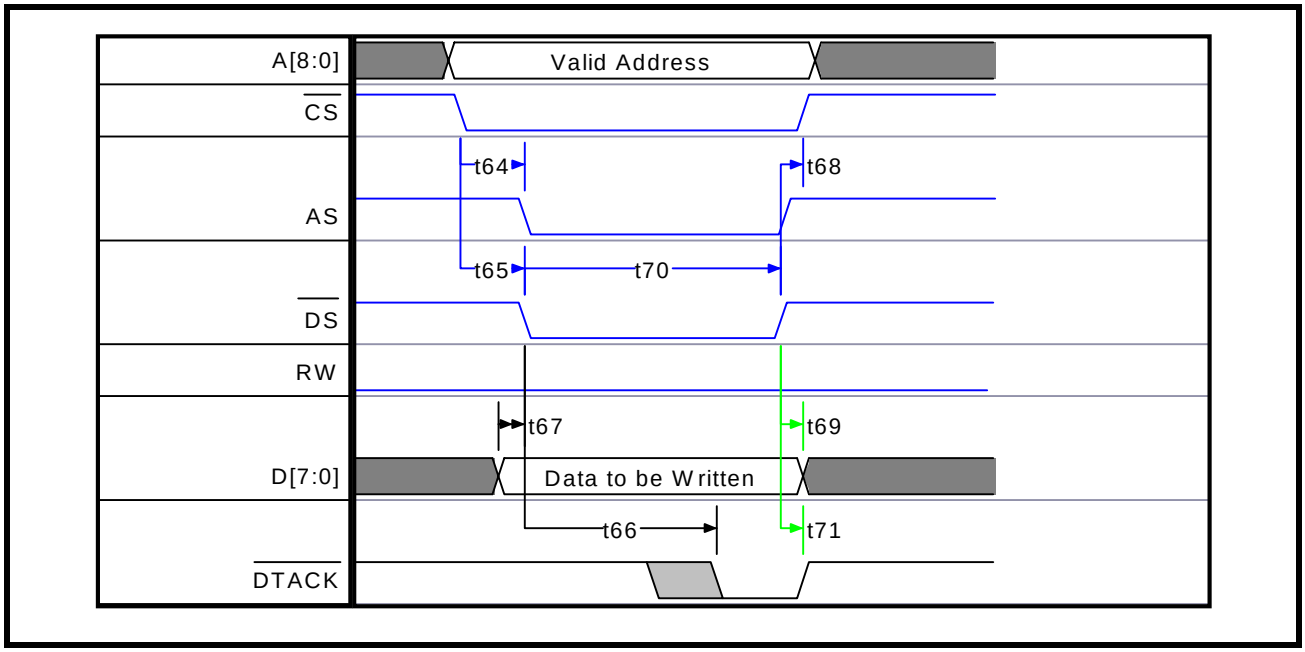
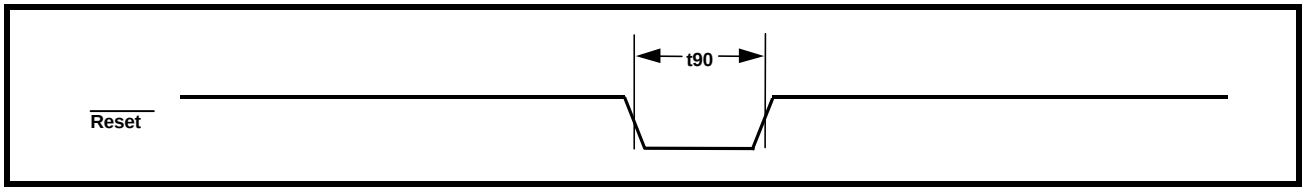


FIGURE 21. MICROPROCESSOR INTERFACE TIMING - $\overline{\text{RESET}}$ PULSE WIDTH



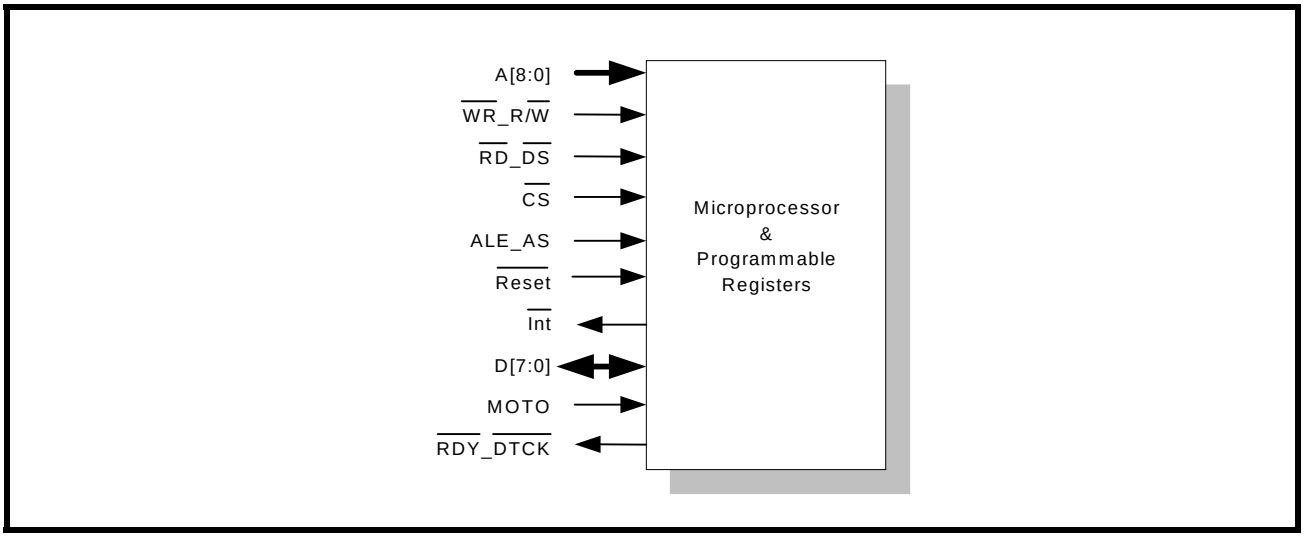
2.0 THE MICROPROCESSOR INTERFACE BLOCK

The Microprocessor Interface section supports the following operations for communication between the local Microprocessor (µP) and the Framer IC:

- The writing of configuration data into the Framer on-chip addressable registers.
- The writing of an outbound PMDL (Path Maintenance Data Link) message into the Transmit LAPD Message buffer.
- The Framer IC's generation of an Interrupt Request to the Microprocessor.
- The Microprocessor's servicing of the interrupt request from the Framer IC.
- The monitoring of the system's health by periodically reading the on-chip Performance Monitor registers.
- The reading of an inbound PMDL Message from the Receive LAPD Message Buffer.
- Receiving and sending FEAC Codes

Figure 22 is a simple block diagram of the Microprocessor Interface Section within the Framer..

FIGURE 22. BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



2.1 *The Microprocessor Interface Block Signasl*

The Framer IC may be configured into a wide variety of different operating modes and have its performance monitored by software through a standard microprocessor interface using data, address and control signals.

The local Microprocessor configures the Framer IC into a desired operating mode by writing data into specific addressables, on-chip Read/Write registers, or on-chip RAM. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The Microprocessor Interface also supports polled and interrupt driven environments. These interface signals are described below in Table 1, Table 2, and Table 3. The microprocessor interface can be configured to operate in the Motorola Mode or in the Intel mode. In the Motorola mode, the control signals function as required by the Motorola 68000 family of microprocessors. Likewise, in the Intel Mode, these control signals function as required by the Intel family of microprocessors.

TABLE 1: DESCRIPTION OF MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH THE INTEL AND MOTOROLA MODES

PIN NAME	TYPE	DESCRIPTION
MOTO	I	**Selection input for Intel/Motorola Microprocessor Interface.** Setting this pin to a logic "High" configures the Microprocessor Interface to operate in the Motorola mode. Setting this pin to a logic "Low" configures the Microprocessor Interface to operate in the Intel Mode.
D[7:0]	I/O	**Bi-Directional Data Bus for register read or write operations**
A[8:0]	I	**Nine Bit Address Bus input:** This Nine bit Address Bus is provided to allow the user to select an on-chip register or on-chip RAM location and select the desired Framer Channel to address.
$\overline{CS}$	I	**Chip Select input.** This active-low signal selects the Microprocessor Interface of the framer and enables read/write operations with the on-chip registers/on-chip RAM.
$\overline{Int}$	O	**Interrupt Request Output:** This open-drain/active-low output signal informs the local Microprocessor that the Framer has an interrupt condition that needs servicing.
$\overline{RESET}$	I	**Master Reset Input:** Setting this input “Low” resets the internal logic to power-on default settings. This input should be return to “High” for normal operation.

TABLE 2: DESCRIPTION OF MICROPROCESSOR INTERFACE SIGNALS - OPERATING IN THE INTEL MODE

PIN NAME	EQUIVALENT PIN IN INTEL ENVIRONMENT	TYPE	DESCRIPTION
ALE_AS	ALE	I	**Address-Latch Enable:** This active-high signal is used to latch the contents on the address bus, A[8:0]. The contents of the Address Bus are latched into the A[8:0] inputs on the falling edge of ALE_AS.
$\overline{RD}$_$\overline{DS}$	$\overline{RD}$	I	**Read Signal:** This active-low input functions as the read signal from the local µP. When this signal goes "Low", the framer places the contents of the addressed register on the Data Bus pins (D[7:0]). The Data Bus is tri-stated once this input signal returns "High".
$\overline{WR}$_R/$\overline{W}$	$\overline{WR}$	I	**Write Signal:** This active-low input functions as the write signal from the local µP. The contents of the Data Bus (D[7:0]) is written into the addressed register via A[8:0] on the rising edge of this signal.
$\overline{RDY}$_$\overline{DTCK}$	$\overline{READY}$	O	**Ready Output:** This active-low signal is provided by the Framer and indicates that the current read or write cycle is to be extended until this signal is asserted. The local µP typically inserts WAIT states until this signal is asserted. This output toggles "Low" when the current read or write cycle is complete.

TABLE 3: DESCRIPTION OF THE MICROPROCESSOR INTERFACE SIGNALS - OPERATING IN THE MOTOROLA MODE

PIN NAME	EQUIVALENT PIN IN MOTOROLA ENVIRONMENT	TYPE	DESCRIPTION
ALE_AS	$\overline{AS}$	I	**Address Strobe:** This active-low signal is used to latch the contents on the address bus input pins A[8:0] into the Microprocessor Interface circuitry. The contents of the Address Bus are latched into the Framer on the rising edge of the ALE_AS signal.
$\overline{RD}$_$\overline{DS}$	$\overline{DS}$	I	**Data Strobe:** This signal latches the contents of the bi-directional data bus pins into the Addressed Register during a Write Cycle.
$\overline{WR}$_R/$\overline{W}$	R/$\overline{W}$	I	**Read/$\overline{\text{Write}}$ Input:** When this pin is "High" it indicates a Read Cycle. When this pin is "Low" it indicates a Write cycle.
$\overline{RDY}$_$\overline{DTCK}$	$\overline{DTACK}$	O	**Data Transfer Acknowledge:** The Framer asserts $\overline{DTACK}$ in order to inform the CPU that the present READ or WRITE cycle is complete. The 68000 family of CPUs requires this signal from its peripheral devices in order to quickly and properly complete a READ or WRITE cycle.

2.2 *Interfacing the XRT72L50 DS3/E3 Framer to the Local µC/µP via the Microprocessor Interface Block*

The Microprocessor Interface block within the Framer is very flexible and provides the following options to the user.

- To interface the Framer to a µC/µP over an 8-bit wide bi-directional data bus.
- To interface the Framer to an Intel-type or Motorola-type µC/µP.
- To transfer data between the Framer IC and the µC/µP via the Programmed I/O or Burst Mode

2.2.1 Interfacing the XRT72L50 DS3/E3 Framer to the Microprocessor over an 8 bit wide bi-directional Data Bus

In general, interfacing the Framer to an 8-bit µC/µP is straight-forward because all of the registers except the PMON registers (as described below) within the Framer are 8-bits wide. Further, in this mode the µC/µP can read or write data into both even and odd numbered addresses within the Framer address space.

Performance Monitor (PMON) Registers

The XRT72L50 DS3/E3 Framer consists of the following PMON Registers.

- PMON LCV Event Count Register
- PMON Framing Error Event Count Register
- PMON Received FEBE Event Count Register
- PMON Parity Error Event Count Register

Unlike most of the registers, the PMON registers are 16-bits wide. Table 4 lists each of these PMON registers as consisting of two 8-bit registers. One of these 8-bit register is labeled MSB (Most Significant Byte) and the other register is labeled LSB (Least Significant Byte). An 8-bit PMON MSB Register reading, concatenated with its companion 8-bit LSB PMON Register, yields the full 16-bit expression within that PMON Register.

An 8-bit µC/µP has to perform two consecutive read operations in order to read in the full 16-bit expression contained within a given PMON register. These PMON Registers are Reset-Upon-Read registers. The entire 16-bit contents within a given PMON Register is reset as soon as an 8-bit µC/µP reads in either byte of this two-byte (e.g., 16 bit) expression. The unread companion byte is placed in the PMON Holding register as detailed below.

For example, consider that an 8-bit µC/µP needs to read in the PMON LCV Event Count Register. In order to accomplish this task, the 8-bit µC/µP is going to have to read in the contents of PMON LCV Event Count Register - MSB (located at Address = 0x50) and the contents of the PMON LCV Event Count Register - LSB

(located at Address = 0x51). These two eight-bit registers, when concatenated together, make up the PMON LCV Event Count Register.

If the 8-bit µC/µP reads in the PMON LCV Event Count-LSB register first, then the entire PMON LCV Event Count register will be reset to 0x0000. And if the 8-bit µC/µP attempts to read in the PMON LCV Event Count-MSB register in the very next read cycle, it will read in the value 0x00.

PMON Holding Register

To resolve this Reset-Upon-Read problem, the XRT72L50 DS3/E3 Framer includes a special register which permits an 8-bit µC/µP to read in the full 16-bit contents of these PMON registers. This register is called the PMON Holding Register and is located at 0x6c within the Framer Address space.

Whenever an 8-bit µC/µP reads in one of the bytes of the 2-byte PMON register, the contents of the unread byte will be stored in the PMON Holding Register. The 8-bit µC/µP must then read in the contents of the PMON Holding Register in the very next read operation.

Whenever an 8-bit µC/µP needs to read a PMON Register, it must execute the following steps.

Step 1: Read in the contents of a given 8-bit PMON Register. It does not matter whether the µC/µP reads in the MSB or the LSB register.

Step 2: Read in the contents of the PMON Holding Register (located at Address = 0x6c). This register will contain the contents of the other byte.

2.2.2 Data Access Modes

The Microprocessor Interface block supports data transfer between the Framer and the µC/µP (e.g., Read and Write operations) via two modes: the Programmed I/O and the Burst Modes.

2.2.2.1 *Data Access using Programmed I/O*

Programmed I/O is the conventional manner in which a microprocessor exchanges data with a peripheral device. It is also the slowest method of data exchange between the Framer and the µC/µP.

2.2.2.1.1 Programmed I/O Access in the Intel Mode

If the XRT72L50 DS3/E3 Framer is interfaced to an Intel-type µC/µP, then it should be configured to operate in the Intel mode by tying the MOTO pin to ground.

The Intel Mode Read Cycle

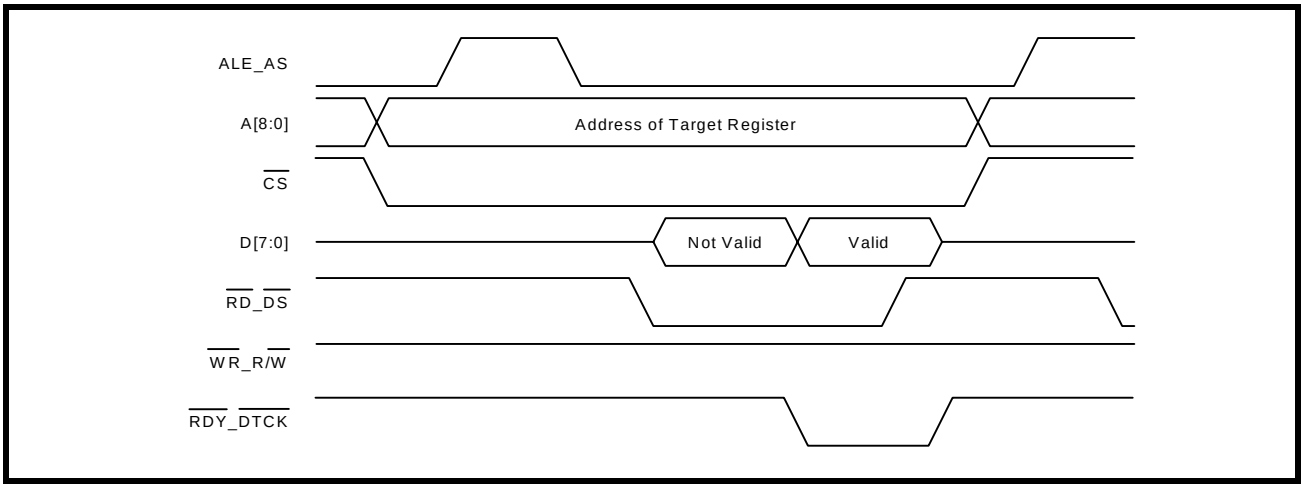
Whenever an Intel-type µC/µP wishes to read the contents of a register or some location within the Receive LAPD Message buffer, it should do the following.

1. Place the address of the target register or buffer location on the Address Bus input pins A[8:0].
2. While the µC/µP is placing this address value on the Address Bus, the Address Decoding circuitry (within the user's system) should assert the $\overline{CS}$ (Chip Select) pin of the Framer, by toggling it "Low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.
3. Toggle the ALE_AS (Address Latch Enable) input pin "High". This step enables the Address Bus input drivers, within the Microprocessor Interface block of the Framer.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate Address Data Setup time), the µC/µP should toggle the ALE_AS pin "Low". This step causes the Framer to latch the contents of the Address Bus into its internal circuitry. At this point, the address of the register or buffer locations has now been selected.
5. Next, the µC/µP should indicate that this current bus cycle is a Read Operation by toggling the $\overline{RD}_\overline{DS}$ (Read Strobe) input pin "Low". This action also enables the bi-directional data bus output drivers of the Framer. At this point, the bi-directional data bus output drivers will proceed to drive the contents of the latched addressed register or buffer location onto the bi-directional data bus, D[7:0].
6. After the µC/µP toggles the Read Strobe signal "Low", the Framer will keep the $\overline{RDY}_\overline{DTCK}$ output pin "High" in order to inform the µC/µP that the data to be read from the data bus is NOT READY to be latched into the µC/µP.

7. After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The XRT72L50 DS3/E3 Framer will indicate that this data can be read by toggling the $\overline{\text{RDY}}$_$\overline{\text{DTCK}}$ (READY) signal "Low".
8. After the µC/µP detects the $\overline{\text{RDY}}$_$\overline{\text{DTCK}}$ signal, it can then terminate the Read Cycle by toggling the $\overline{\text{RD}}$_$\overline{\text{DS}}$ (Read Strobe) input pin "High".

Figure 23 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals during an Intel-type Programmed I/O Read Operation.

FIGURE 23. MICROPROCESSOR INTERFACE TIMING - INTEL-TYPE PROGRAMMED I/O READ OPERATION

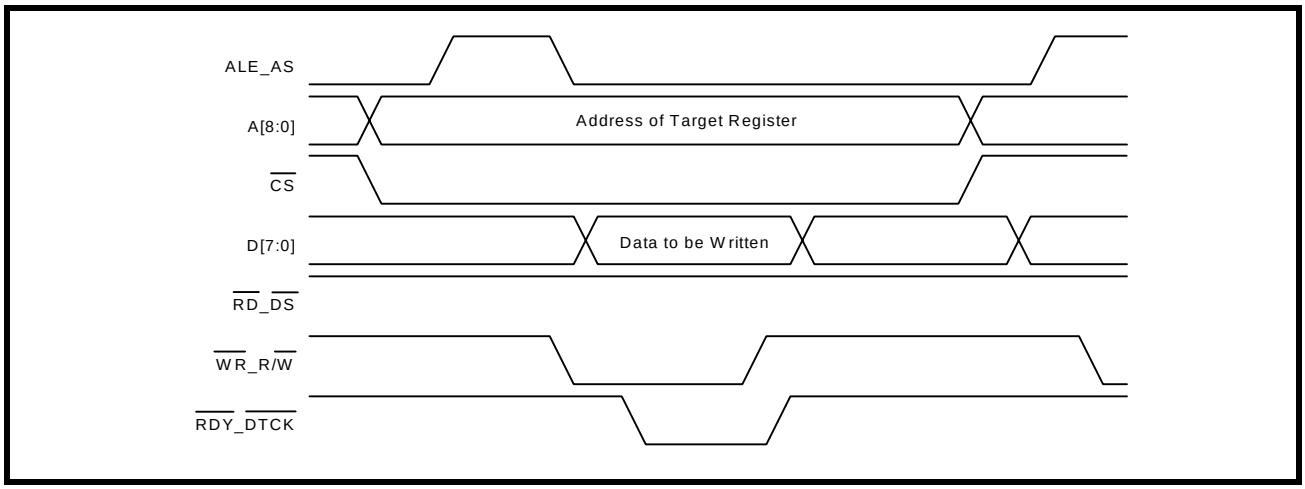


The Intel Mode Write Cycle

Whenever an Intel-type µC/µP wishes to write a byte or word of data into a register or buffer location, it should do the following.

1. Place the address of the target register or buffer location on the Address Bus input pins, A[8:0].
2. While the µC/µP is placing this address value onto the Address Bus, the Address Decoding circuitry (within the user's system) should assert the $\overline{\text{CS}}$ input pin of the Framer by toggling it "Low". This enables further communication between the µC/µP and the Framer Microprocessor Interface block.
3. Assert the ALE_AS input pin by toggling it "High". When the µC/µP asserts the ALE_AS input pin, it enables the Address Bus Input Drivers within the Framer chip.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate Address Setup time), the µC/µP should toggle the ALE_AS input pin "Low". This step causes the Framer to latch the contents of the Address Bus into its internal circuitry. At this point, the address of the register or buffer location has now been selected.
5. The µC/µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus, D[7:0].
6. Next, the µC/µP should indicate that this current bus cycle is a Write Operation by toggling the $\overline{\text{WR}}$_R/$\overline{\text{W}}$ (Write Strobe) input pin "Low". This action also enables the bi-directional data bus input drivers of the Framer.
7. After some amount of time when the data on the bi-directional data bus to settles, the $\overline{\text{RDY}}$ will go “low indicating that data has been written to its destination, the µC/µP will toggle the $\overline{\text{WR}}$_R/$\overline{\text{W}}$ (Write Strobe) input pin "High", which terminates the write cycle.
8. Figure 24 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals during an Intel-type Programmed I/O Write Operation.

FIGURE 24. MICROPROCESSOR INTERFACE TIMING - INTEL-TYPE PROGRAMMED I/O WRITE OPERATION



2.2.2.1.2 Programmed I/O Access in the Motorola Mode

If the XRT72L50 DS3/E3 Framer is interfaced to a Motorola-type µC/µP (e.g., the MC680X0 family, etc.), it should be configured to operate in the Motorola mode by tying the MOTO pin to “High”.

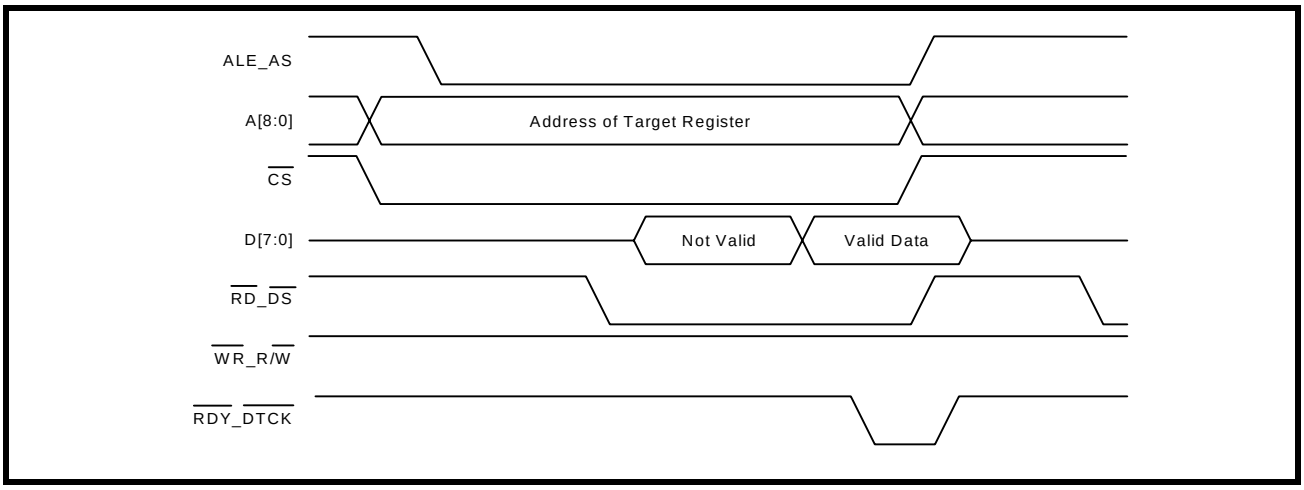
The Motorola Mode Read Cycle

Whenever a Motorola-type µC/µP wishes to read the contents of a register or some location within the Receive LAPD Message.

1. Place the address of the target register or buffer location on the Address Bus input pins, A[8:0].
2. At the same time, the Address Decoding circuitry (within the user's system) should assert the $\overline{CS}$ (Chip Select) input pin of the Framer, by toggling it "Low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.
3. Assert the ALE_AS (Address-Strobe) input pin by toggling it “Low”. This step enables the Address Bus input drivers within the Microprocessor Interface Block of the Framer IC.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate Address Setup time), the µC/µP should toggle the ALE_AS input pin "High". This step causes the Framer to latch the contents of the Address Bus into its internal circuitry. At this point, the address of the register or buffer location has now been selected.
5. The µC/µP should indicate that this cycle is a Read cycle by setting the $\overline{WR}$_R/$\overline{W}$ (R/$\overline{W}$) input pin "High".
6. Next the µC/µP should initiate the current bus cycle by toggling the $\overline{RD}$_$\overline{DS}$ (Data Strobe) input pin "Low". This step enables the bi-directional data bus output drivers within the XRT72L50 DS3/E3 Framer. At this point, the bi-directional data bus output drivers will proceed to drive the contents of the Address register onto the bi-directional data bus, D[7:0].
7. After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The XRT72L50 DS3/E3 Framer will indicate that this data can be read by asserting the $\overline{RDY}$_$\overline{DTCK}$ (DTACK) signal.
8. After the µC/µP detects the $\overline{RDY}$_$\overline{DTCK}$ signal, it terminates the Read Cycle by toggling the $\overline{RD}$_$\overline{DS}$ input pin "High".

Figure 25 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals during a Motorola-type Programmed I/O Read Operation.

FIGURE 25. MICROPROCESSOR INTERFACE TIMING - MOTOROLA-TYPE PROGRAMMED I/O READ OPERATION



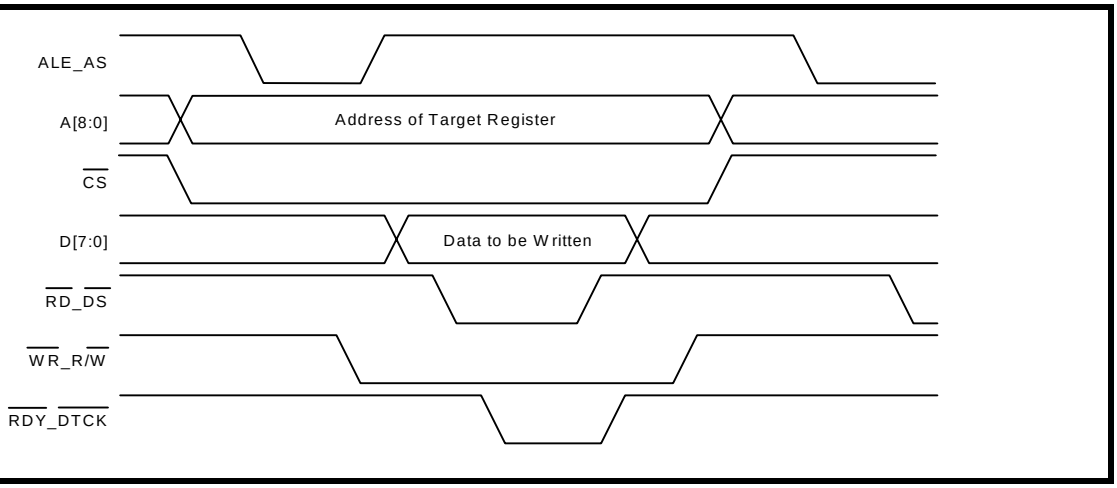
The Motorola Mode Write Cycle

Whenever a Motorola-type µC/µP wishes to write a byte or word of data into a register or buffer location, it should do the following.

1. Assert the ALE_AS input pin by toggling it "Low". This step enables the Address Bus input drivers.
2. Place the address of the target register or buffer location on the Address Bus input pins, A[8:0].
3. While the µC/µP is placing this address value onto the Address Bus, the Address-Decoding circuitry (within the user's system) should assert the $\overline{CS}$ input pins of the Framer by toggling it "Low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate Address Setup time), the µC/µP should toggle the ALE_AS input pin "High". This step causes the Framer to latch the contents of the Address Bus into its own circuitry. At this point, the Address of the register or buffer location has now been selected.
5. Further, the µC/µP should indicate that this current bus cycle is a Write operation by toggling the $\overline{WR}$_R/$\overline{W}$ (R/$\overline{W}$) input pin "Low".
6. The µC/µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus, D[7:0].
7. Next, the µC/µP should initiate the bus cycle by toggling the $\overline{RD}$_$\overline{DS}$ input pin "Low". When the XRT72L50 DS3/E3 Framer senses that the $\overline{WR}$_R/$\overline{W}$ (R/$\overline{W}$) input pin is "High" and the $\overline{RD}$_$\overline{DS}$ input pin has toggled "Low", it will enable the input drivers of the bi-directional data bus, D[7:0].
8. After waiting the appropriate time for this newly placed data to settle on the bi-directional data bus (e.g., the Data Setup time) the Framer will assert the $\overline{RDY}$_$\overline{DTCK}$ output signal.
9. After the µC/µP detects the $\overline{RDY}$_$\overline{DTCK}$ signal, the µC/µP should toggle the $\overline{RD}$_$\overline{DS}$ input pin "High" and terminates the Write cycle.

Figure 26 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during a Motorola-type Programmed I/O Write Operation.

FIGURE 26. MICROPROCESSOR INTERFACE TIMING - MOTOROLA-TYPE PROGRAMMED I/O WRITE OPERATION



2.3 *On-Chip Register Organization*

The Microprocessor Interface section allows the user to do the following.

- Configure the Framer into a wide variety of operating modes
- Employ various features of the Framer
- Perform status monitoring
- Enable/Disable and service Interrupt Conditions

All of these things are accomplished by reading from and writing to the many on-chip registers. Table 4 lists each of these registers and their corresponding address locations within the Framer Address space.

2.3.1 Framer Register Addressing

The array of on-chip registers consists of a variety of register types. These registers are denoted in Table 4, as follows.

RO - Read Only Registers.

R/W - Read/Write Registers

RUR - Reset-upon-Read Registers

Some of these registers consists of both RO and R/W bit-fields. The bit-format and definitions for each of these registers are presented in Section 2.3.2.

TABLE 4: REGISTER ADDRESSING OF THE FRAMER PROGRAMMER REGISTERS

ADDRESS	REGISTER NAME	POWER UP DEFAULT VALUE	HEX DEFAULT VALUE	REGISTER TYPE
0x00	Operating Mode register (E3 G.751 is default)	b00101011	0x2B	R/W
0x01	I/O Control Register	b10100000	0xA0	R/W, RO
0x02	Part Number Register (XRT72L50)	b00000111	0x07	RO
0x03	Version Number Register (Device Dpenent)	b00000001	0x01	RO
0x04	Block Interrupt Enable Register	b00000000	0x00	R/W
0x05	Block Interrupt Status Register	b00000001	0x01	RO
0x06-0x0B	Reserved			

TABLE 4: REGISTER ADDRESSING OF THE FRAMER PROGRAMMER REGISTERS

ADDRESS	REGISTER NAME	POWER UP DEFAULT VALUE	HEX DEFAULT VALUE	REGISTER TYPE
0x0C	Test Register	b00000000	0x00	R/W, RO
0x0D-0x0F	Reserved			
0x10	RxDS3 Configuration & Status Register RxE3 Configuration & Status Register 1 - G.832 RxE3 Configuration & Status Register 1 - G.751	b00000010	0x02	R/W, RO
0x11	RxDS3 Status Register RxE3 Configuration & Status Register 2 - G.832 RxE3 Configuration & Status Register 2 - G.751	b00000010	0x02	R/W, RO
0x12	RxDS3 Interrupt Enable Register RxE3 Interrupt Enable Registers -1 G.832 RxE3 Interrupt Enable Registers - 1 G.751	b00000000	0x00	R/W, RO
0x13	RxDS3 Interrupt Status Register RxE3 Interrupt Enable Register -2 G.832 RxE3 Interrupt Enable Register - 2 G.751	b00000000	0x00	R/W, RO
0x14	RxDS3 Sync Detect Enable Register RxE3 Interrupt Status Register 1 - G.832 RxE3 Interrupt Status Register 1 - G.751	b00000000	0x00	RUR, RO
0x15	RxE3 Interrupt Status Register 2 - G.832 RxE3 Interrupt Status Register 2 - G.751	b00000000	0x00	RUR, RO
0x16	RxDS3 FEAC Register	b00000000	0x00	RO
0x17	RxDS3 FEAC Interrupt Enable/Status Register	b00000000	0x00	RO
0x18	RxDS3 LAPD Control Register RxE3 LAPD Control Register	b00000000	0x00	R/W, RUR
0x19	RxDS3 LAPD Status Register RxE3 LAPD Status Register	b00000000	0x00	RO
0x1A	RxE3 NR Byte Register - G.832 RxE3 Service Bit Register G.751	b00000000	0x00	RO
0x1B	RxE3 GC Byte Register - G.832	b00000000	0x00	RO
0x1C	RxE3 TTB-0 Register - G.832	b00000000	0x00	RO
0x1D	RxE3 TTB-1 Register - G.832	b00000000	0x00	RO
0x1E	RxE3 TTB-2 Register - G.832	b00000000	0x00	RO
0x1F	RxE3 TTB-3 Register - G.832	b00000000	0x00	RO
0x20	RxE3 TTB-4 Register - G.832	b00000000	0x00	RO
0x21	RxE3 TTB-5 Register - G.832	b00000000	0x00	RO
0x22	RxE3 TTB-6 Register - G.832	b00000000	0x00	RO
0x23	RxE3 TTB-7 Register - G.832	b00000000	0x00	RO
0x24	RxE3 TTB-8 Register - G.832	b00000000	0x00	RO

TABLE 4: REGISTER ADDRESSING OF THE FRAMER PROGRAMMER REGISTERS

ADDRESS	REGISTER NAME	POWER UP DEFAULT VALUE	HEX DEFAULT VALUE	REGISTER TYPE
0x25	RxE3 TTB-9 Register - G.832	b00000000	0x00	RO
0x26	RxE3 TTB-10 Register - G.832	b00000000	0x00	RO
0x27	RxE3 TTB-11 Register - G.832	b00000000	0x00	RO
0x28	RxE3 TTB-12 Register - G.832	b00000000	0x00	RO
0x29	RxE3 TTB-13 Register - G.832	b00000000	0x00	RO
0x2A	RxE3 TTB-14 Register - G.832	b00000000	0x00	RO
0x2B	RxE3 TTB-15 Register - G.832	b00000000	0x00	RO
0x2C	RxE3 SSM Register - G.832	b00000000	0x00	R/W, RO
0x2D - 0x2F	Reserved			
0x30	TxDS3 Configuration Register TxE3 Configuration Register - G.832 TxE3 Configuration Register - G.751	b00000000	0x00	R/W
0x31	TxDS3 FEAC Configuration and Status Register	b00000000	0x00	RO, R/W, RUR
0x32	TxDS3 FEAC Register	b00000000	0x00	R/W
0x33	TxDS3 LAPD Configuration Register TxE3 LAPD Configuration Register	b00001000	0x08	R/W
0x34	TxDS3 LAPD Status/Interrupt Register TxE3 LAPD Status/Interrupt Register	b00000000	0x00	R/W, RO, RUR
0x35	TxDS3 M-Bit Mask Register TxE3 GC Byte Register - G.832 TxE3 Service Bits Register - G.751	b00000000	0x00	R/W
0x36	TxDS3 F-Bit Mask Register 1 TxE3 MA Byte Register - G.832	b00010000	0x10	R/W
0x37	TxDS3 F-Bit Mask Register 2 TxE3 NR Byte Register - G.832	b00000000	0x00	R/W
0x38	TxDS3 F-Bit Mask Register 3 TxE3 TTB-0 Register - G.832	b10000000	0x80	R/W
0x39	TxDS3 F-Bit Mask Register 4 TxE3 TTB-1 Register - G.832	b00000000	0x00	R/W
0x3A	TxE3 TTB-2 Register - G.832	b00000000	0x00	R/W
0x3B	TxE3 TTB-3 Register - G.832	b00000000	0x00	R/W
0x3C	TxE3 TTB-4 Register - G.832	b00000000	0x00	R/W
0x3D	TxE3 TTB-5 Register - G.832	b00000000	0x00	R/W
0x3E	TxE3 TTB-6 Register - G.832	b00000000	0x00	R/W
0x3F	TxE3 TTB-7 Register - G.832	b00000000	0x00	R/W

TABLE 4: REGISTER ADDRESSING OF THE FRAMER PROGRAMMER REGISTERS

ADDRESS	REGISTER NAME	POWER UP DEFAULT VALUE	HEX DEFAULT VALUE	REGISTER TYPE
0x40	TxE3 TTB-8 Register - G.832	b00000000	0x00	R/W
0x41	TxE3 TTB-9 Register - G.832	b00000000	0x00	R/W
0x42	TxE3 TTB-10 Register - G.832	b00000000	0x00	R/W
0x43	TxE3 TTB-11 Register - G.832	b00000000	0x00	R/W
0x44	TxE3 TTB-12 Register - G.832	b00000000	0x00	R/W
0x45	TxE3 TTB-13 Register - G.832	b00000000	0x00	R/W
0x46	TxE3 TTB-14 Register - G.832	b00000000	0x00	R/W
0x47	TxE3 TTB-15 Register - G.832	b00000000	0x00	R/W
0x48	TxE3 FA1 Error Mask Register - G.832 TxE3 FAS Error Mask Upper Register-0 - G.751	b00000000	0x00	R/W
0x49	TxE3 FA2 Error Mask Register - G.832 TxE3 FAS Error Mask Lower Register-1 - G.751	b00000000	0x00	R/W
0x4A	TxE3 BIP-8 Mask Register - G.832 TxE3 BIP-4 Mask Register - G.751	b00000000	0x00	R/W
0x4B	TxSSM Register - G.832	b00000000	0x00	R/W
0x4C-0x4F	Reserved			
0x50	PMON LCV Event Count Register - MSB	b00000000	0x00	RUR
0x51	PMON LCV Event Count Register - LSB	b00000000	0x00	RUR
0x52	PMON Framing Bit Error Event Count Register - MSB	b00000000	0x00	RUR
0x53	PMON Framing Bit Error Event Count Register - LSB	b00000000	0x00	RUR
0x54	PMON Parity Error Event Count Register - MSB	b00000000	0x00	RUR
0x55	PMON Parity Error Event Count Register - LSB	b00000000	0x00	RUR
0x56	PMON FEBE Event Count Register - MSB	b00000000	0x00	RUR
0x57	PMON FEBE Event Count Register - LSB	b00000000	0x00	RUR
0x58	PMON CP Bit Error Event Count Register - MSB	b00000000	0x00	RUR
0x59	PMON CP Bit Error Event Count Register - LSB	b00000000	0x00	RUR
0x5A - 0x67	Reserved			
0x68	PRBS Bit Error Counter - MSB	b00000000	0x00	RUR
0x69	PRBS Bit Error Counter - LSB	b00000000	0x00	RUR
0x6A-0x6B	Reserved			
0x6C	PMON Holding Register	b00000000	0x00	RUR
0x6D	One-Second Error Status Register	b00000000	0x00	RO

TABLE 4: REGISTER ADDRESSING OF THE FRAMER PROGRAMMER REGISTERS

ADDRESS	REGISTER NAME	POWER UP DEFAULT VALUE	HEX DEFAULT VALUE	REGISTER TYPE
0x6E	LCV One-Second Accumulator Register - MSB	b00000000	0x00	RO
0x6F	LCV One-Second Accumulator Register - LSB	b00000000	0x00	RO
0x70	Frame Parity Error One-Second Accumulator Register - MSB (BIP-8 in G.832)	b00000000	0x00	RO
0x71	Frame Parity Error One-Second Accumulator Register - LSB (BIP-8 in G.832)	b00000000	0x00	RO
0x72	Frame CP Bit Error - One-Second Accumulator Register - MSB	b00000000	0x00	RO
0x73	Frame CP Bit Error - One-Second Accumulator Register - LSB	b00000000	0x00	RO
0x74 - 0x7F	Reserved			
0x80	Line Interface Drive Register (XRT72L50)	b00000000	0x00	R/W
0x81	Line Interface Scan Register	b00000000	0x00	RO
0x82	HDLC Control Register	b00000100	0x04	R/W
0x83 - 0x85	Reserved			
0x86 - 0xDD	Transmit LAPD Message Buffer (RAM)	bxxxxxxx		R/W
0xDE - 0x135	Receive LAPD Message Buffer (RAM)	bxxxxxxx		R/W

2.3.2 Framer Register Description

2.3.2.1 *Operating Mode Register*

Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	1

Bit 7 - Local Loop-back Mode

This Read/Write bit-field permits the user to command the Framer chip to operate in the Local Loopback Mode.

Setting this bit-field to "0", configures the Framer chip to operate in the Normal Mode. Setting this bit-field to "1", configures the Framer chip to operate in the Local-Loopback Mode.

NOTE: *For more information of the Local Loop-back Mode, refer to* Section 7.0*.*

Bit 6 - DS3/$\overline{E3}$ select

This Read/Write bit-field permits the user to command the Framer chip to operate in either the DS3 Mode or the E3 Mode.

Setting this bit-field to "0", configures the Framer chip to operate in the E3 Mode. Setting this bit-field to "1", configures the Framer chip to operate in the DS3 Mode.

Bit 5 - Internal LOS Enable Select

This Read/Write bit-field permits the user to configure the Framer chip to either declare an LOS condition, based upon the Internal Circuit's criteria or not.

Setting this bit-field to "0", configures the Framer chip to NOT declare an LOS condition, based upon its own internal criteria.

Setting this bit-field to "1", configures the Framer chip to declare an LOS condition based upon its own internal criteria.

The XRT72L50 Framer Chip declares an LOS condition anytime the ExtLOS pin (pin 78) is set "High" independent of the setting of this bit-field.

NOTE: *For more information on the device's internal criteria for Loss of Signal, refer to* Section 4.3.2.5.1.

Bit 4 - RESET:

This Read/Write bit-field permits the user to command the Framer chip in the Software Reset state. If the XRT72L50 Framer is commanded into this state, then each of the internal state machines which control Framing Alignment, will be reset.

This type of Reset is different from the Hardware Reset (achieved by pulsing the Reset input pin "Low"). The Software Reset will NOT reset the contents of the registers back to their default values.

The Software Reset Command routine should be written to toggle this bit-field from “0” to “1” and back to “0”, to permit the chip to exit the Software Reset state.

Bit 3 - Interrupt Enable Reset

This Read/Write bit-field permits the user to configure the Framer chip to automatically disable all Interrupts that are activated. The purpose of this feature is to diagnose a fault condition that continuously generates an interrupt condition from recursively generating interrupts. This can hang up the Microprocessor by forcing it to continuously operate in the Interrupt Service Routine.

By invoking this feature the system is protected from these recursive interrupts. Once a given interrupt is generated and the Microprocessor executes its Interrupt Service Routine (e.g. by reading out the states of the various Interrupt Status Registers, etc.), that particular interrupt will automatically be disabled and will not be generated again until the Microprocessor goes back and enables this particular interrupt again.

Setting this bit-field to "0" configures the XRT72L50 Framer chip to **NOT** disable the Interrupt Enable Status, of any interrupts, following their activation. This is the default setting.

Setting this bit to "1" configures the XRT72L50 Framer chip to automatically disable any interrupt that is activated. This feature is typically used for diagnostic puposes only.

Bit 2 - Frame Format Select

This Read/Write bit-field, along with the DS3/E3 select bit-field (bit 6 in this register) permits the user to select the Framing Format that the XRT72L50 will operate in. The following table relates the states of this bit-field and that of bit 6 to the selected framing format for this chip.

BIT 6 - DS3/$\overline{E3}$ SELECT	BIT 2 - FRAME FORMAT SELECT	SELECTED FRAMING FORMAT
0	0	E3, ITU-T G.751
0	1	E3, ITU-T G.832
1	0	DS3, C-bit Parity
1	1	DS3, M13

Bits 1 & 0 - TimRefSel[1:0] - Timing Reference Select

These two Read/Write bit-fields permits the user to select both a Framing Reference and Timing Reference for the Transmit Section of the XRT72L50. The following table relates the states of these two bit-fields to the selected Framing and Timing references.

TIMREFSEL[1:0]	FRAMING REFERENCE	TIMING REFERENCE
00	Asynchronous	RxLineClk Input Signal
01	TxFrameRef	TxInClk Input Signal
10	Asynchronous	TxInClk Input Signal
11	Asynchronous	TxInClk Input Signal

NOTE: *For more information on Framing and Timing References, refer to* Section 4.2.

2.3.2.2 *I/O Control Register*

NOTE: *Data can be transmitted in;*

- **a.** *Unipolar*
- **b.** *Bipolar with AMI, or*
- **c.** *Bipolar with AMI and B3ZS (for DS3)/HDB3 (for E3)*

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ $\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine Clk Invert	RxLine Clk Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Bit 7 - DisableTxLOC

This Read/Write bit-field permits the user to enable or disable the Transmit Loss of Clock feature.

Setting this bit-field to "0" enables the Transmit Loss of Clock feature. Conversely, setting this bit-field to "1" disables the Transmit Loss of Clock feature.

NOTE: *For more details into the Transmit Loss of Clock feature, refer to* Section 2.4.

Bit 6 - LOC (Loss of Clock) Status

This Read-Only bit-field reflects the Loss of Clock status for the XRT72L50. The XRT72L50 will set this bit-field to "0" under normal operation conditions. Conversely, if the XRT72L50 experiences a Loss of Clock event, then it will set this bit-field to "1".

NOTE: *For more details into the Loss of Clock status, refer to Section 2.4.*

Bit 5 - DisableRxLOC

This Read/Write bit-field permits the user to enable or disable the Receive Loss of Clock feature.

Setting this bit-field to "0" enables the Receive Loss of Clock feature. Conversely, setting this bit-field to "1" disables the Receive Loss of Clock feature.

NOTE: *For more details into the Receive Loss of Clock feature, refer to* Section 2.4.

Bit 4 - AMI/$\overline{\text{ZeroSup}}$

This Read/Write bit-field permits the user to configure the XRT72L50 to transmit and receive data via the AMI (Alternate Mark Inversion) line code or via a Zero-Suppression (e.g, B3ZS/HDB3) line code.

Setting this bit-field to "0" configures the XRT72L50 to transmit and receive data via a Zero-Suppression line code.

Setting this bit-field to "1" configures the XRT72L50 to transmit and receive data via the Alternate Mark Inversion line code.

If the XRT72L50 is configured to transmit and receive data using a Zero-Suppression code while operating in the DS3 Mode, then the chip will transmit and receive data using the B3ZS Line Code.

If the XRT72L50 is configured to transmit and receive data using a Zero-Suppression code while operating in the E3 Mode, then the chip will transmit and receive data using the HDB3 Line Code.

This bit-field will be ignored if bit 3 (Unipolar/$\overline{\text{Bipolar}}$) of this Register is set to "1" (Unipolar Mode).

Bit 3 - Unipolar/$\overline{\text{Bipolar}}$

This Read/Write bit-field permits the user to configure the XRT72L50 to transmit and receive data from an LIU IC, in either the Single-Rail or Dual-Rail format.

Setting this bit-field to "0" configures the XRT72L50 to operate in the Bipolar or Dual-Rail Format. In this mode, the Transmit Section of the XRT72L50 will output data to the LIU via both the TxPOS and TxNEG output pins. The Receive Section of the device will receive data from the LIU via both the RxPOS and RxNEG output pins.

Setting this bit-field to "1" configures the XRT72L50 to operate in the Unipolar or Single-Rail Format. In this mode, the Transmit Section of the XRT72L50 will output data to the LIU in a binary data stream manner via the TxPOS output pin. The Receive Section of the device will receive data from the LIU in a binary data stream manner via the RxPOS input pin.

NOTE: *For more information on the transmission and reception of data in the Single-Rail or Dual-Rail format, refer to* Section 4.2.5.

Bit 2 - TxLineClk Invert

This Read/Write bit-field permits the user to configure the XRT72L50 to output data via the TxPOS and TxNEG output pins on the rising or falling edge of TxLineClk.

Setting this bit-field to "0" configures the XRT72L50 to output data, via the TxPOS and TxNEG output pins, on the rising edge of TxLineClk.

Setting this bit-field to "1" configures the XRT72L50 to output data, via the TxPOS and TxNEG output pins, on the falling edge of TxLineClk.

Bit 1 - RxLineClk Invert

This Read/Write bit-field permits the user to configure the XRT72L50 to latch data on the RxPOS and RxNEG input pins on the rising or falling edge of RxLineClk.

Setting this bit-field to "0" configures the XRT72L50 to latch the data on the RxPOS and RxNEG input pins, into the device, on the rising edge of RxLineClk.

Setting this bit-field to "1" configures the XRT72L50 to latch the data on the RxPOS and RxNEG input pins, into the device, data, on the falling edge of RxLineClk.

Bit 0 - Reframe

This Read/Write bit-field permits the user to configure the Receive Section of the XRT72L50 to start a new frame search. A "0" to "1" transition in this bit-field will force the device to start a new frame search. The bit should be reset to “0” after the transistion to prevent a continous forced reframing condition.

2.3.2.3 *Part Number Register*

Part Number Register (Address = 0x02)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Part Number Value							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	1	1	1

The Part Number register can be used by System-level software to identify this particular device as the XRT72L50 Single Channel DS3/E3 Framer IC. The value of the Part Number register is 0x07.

2.3.2.4 *Version Number Register*

The Version Number register permits the user's software to identify the revision number of the part. The very first revision of the part will contain the value 0x01.

Version Number Register (Address = 0x03)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Version Number Value							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	1

2.3.2.5 *Block Interrupt Enable Register*

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One-Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - RxDS3/E3 Interrupt Enable

This Read/Write bit-field permits the user to enable or disable all Receive Section related interrupts at the Block Level.

Setting this bit-field to "0" disables all Receive Section related Interrupts within the XRT72L50.

Setting this bit-field to "1" enables the Receive Section related Interrupts (within the XRT72L50) at the block level.

NOTE: *Setting this bit-field to "1" does not enable all Receive Section related Interrupts. Each of these interrupts can still be disabled at the Source Level. However, setting this bit-field to "0" does disable all Receive Section related Interrupts.*

Bit 1 - TxDS3/E3 Interrupt Enable

This Read/Write bit-field permits the user to enable or disable all Transmit Section related interrupt at the Block Level.

Setting this bit-field to "0" disables all Transmit Section related Interrupts within the XRT72L50.

Setting this bit-field to "1" enables the Transmit Section related Interrupts (within the XRT72L50) at the block level.

NOTE: *Setting this bit-field to "1" does not enable all Transmit Section related Interrupts. Each of these interrupts can still be disabled at the Source Level. However, setting this bit-field to "0" does disable all Transmit Section related Interrupts.*

Bit 0 - One-Second Interrupt Enable

This Read/Write bit-field permits the user to enable or disable the One-Second Interrupt. If this interrupt is enabled, then the XRT72L50 generate interrupts to the µC/µP at one-second intervals.

Setting this bit-field to "0" disables the One-Second Interrupt. Conversely, setting this bit-field to "1" enables the One-Second Interrupt.

2.3.2.6 *Block Interrupt Status Register*

Block Interrupt Status Register (Address = 0x05)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Status	Not Used					TxDS3/E3 Interrupt Status	One-Second Interrupt Status
RO	RO	RO	RO	RO	RO	RO	RUR
0	0	0	0	0	0	0	1

Bit 7 - RxDS3/E3 Interrupt Status Indicator

This Read-Only bit-field indicates whether or not a Receive-Section related interrupt has been requested and is awaiting service.

If this bit-field is set to "0", then there are no Receive-Section related interrupts awaiting service. Conversely, if this bit-field is set to "1", then there is at least one Receive Section related interrupt, awaiting service.

If this bit-field is set to "1", then the µC/µP must read the Source-Level Interrupt Status register in order to clear this bit-field.

Bit 1 - TxDS3/E3 Interrupt Status Indicator

This Read-Only bit-field indicates whether or not a Transmit-Section related interrupt has been requested and is awaiting service.

If this bit-field is set to "0", then there are no Transmit-Section related interrupts awaiting service. Conversely, if this bit-field is set to "1", then there is at least one Transmit Section related interrupt, awaiting service.

If this bit-field is set to "1", then the µC/µP must read the Source-Level Interrupt Status register in order to clear this bit-field.

Bit 0 - One-Second Interrupt Status

This Reset-upon-Read bit field indicates whether or not a One-Second interrupt has been requested and is awaiting service.

If this bit-field is set to "0", then the One-Second interrupt is not awaiting service. Conversely, if this bit-field is set to "1", then the One-Second interrupt is awaiting service.

This bit-field will be cleared immediately after the µC/µP has read this register.

2.3.2.7 *Test Register*

TEST Register (Address = 0x0C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxOH Source Select	Rx Payload Clock Enable	Tx Payload Clock Enable	Rx PRBS Lock	Rx PRBS Enable	Tx PRBS Enable	Reserved	
R/W	R/W	R/W	RO	R/W	R/W	RO	RUR
0	0	0	0	0	0	0	0

Bit 7 - TxOH Source Select

This Read/Write bit-field permits the user to configure the Transmit Section of the channel to accept overhead bits/bytes via the TxSer[n]or TxNib[3:0][n] input pins.

Setting this bit-field to “1” configures the Transmit Section of the channel to accept overhead bits/bytes via either the TxSer[n] or TxNib[3:0][n]input pins.

Setting this bit-field to “0” configures the Transmit Section of the channel to either internally generate or accept the overhead bits/bytes via the TxOH[n] input pin.

Bit 6 - Rx Payload Clock Enable

This Read/Write bit-field permits the user to configure the Receive Payload Data Output Interface block to output the receive data in a gapped-clock manner. The Receive Payload Data Output Interface will only generate a clock edge via the RxClk[n] output pin whenever a payload bit is being output via the RxSer[n] output pin. The Receive Payload Data Output Interface will not generate a clock edge via the RxClk[n] output pin whenever an overhead bit is being output via the RxSer[n]output pin.

If the user does not select this option then the Receive Payload Data Output Interface block will generate a clock edge for all bits (payload and overhead); as they are output via the RxSer[n] output pin. However, the Receive Payload Data Output Interface will also pulse the RxOHInd[n] output pin "High" each time an overhead bit is being output via the RxSer[n] output pin.

Setting this bit-field to “1” enables this feature. Setting this bit-field to “0” disables this feature.

Bit 5 - Tx Payload Clock Enable

This Read/Write bit-field permits the user to configure the TxOHInd[n] output pin to function as either of the following roles.

1. The Transmit Overhead Data Output Indicator
2. The Transmit Payload Data Clock Output signal.

If the TxOHInd[n] output pin is configured to function as the Transmit Overhead Data Output signal, then this output pin will pulse "High" one bit-period prior to the instant that the Transmit Section of the channel (within the XRT72L50) is processing an overhead bit.

If the TxOHInd[n] output pin is configured to function as the Transmit Payload Data Clock output signal, then the Transmit Payload Data Output interface block will generate a clock edge via the TxOHInd[n] output pin. The Local Terminal equipment is expected to output outbound payload data to the Transmit Payload Data Input Interface block (via the TxSer[n] input pin) upon the falling edge of this clock signal.

NOTE: *In this mode, the TxOHInd output pin will not generate a clock edge, whenever the Transmit Section of the XRT72L50 is about to process an overhead bit.*

Setting this bit-field to “0” configures the TxOHInd[n] output pin to function as the Transmit Overhead Data Output signal. Setting this bit-field to “1” configures the TxOHInd[n] output pin to function as the Transmit Payload Data Clock output signal.

Bit 4 - Rx PRBS Lock

This Read-Only bit-field indicates whether or not the PRBS Receiver has acquired PRBS Lock (or Pattern Sync) with the data generated by the PRBS Generator.

If this bit-field is set to “1”, then the PRBS Receiver has acquired PRBS lock with the data generated by the PRBS Generator. If this bit-field is set to “0”, then the PRBS Receiver has NOT acquired PRBS Lock with the data generated by the PRBS Generator.

This bit-field is only valid if both the RxPRBS Enable and Tx PRBS Enable bit-fields are both set to “1”.

Bit 3 - Rx PRBS Enable

This Read/Write bit-field permits the user to enable the PRBS Receiver within the channel.

Setting this bit-field to “1” enables the PRBS Receiver. Setting this bit-field to “0” disables the PRBS Receiver.

Bit 2 - Tx PRBS Enable

This Read/Write bit-field permits the user to enable the PRBS Generator within the channel.

Setting this bit-field to “1” enables the PRBS Generator. Setting this bit-field to “0” disables the PRBS Generator.

Receive DS3 Framer Configuration Registers

NOTE: *The default register values shown below are after the operating mode is set to DS3-CBit mode. These are different from the power-up default values. For DS3-M13 mode, default values for all registers are the same as DS3-C execpt for Register 0x13 is 0x00 and Register 0x51 is 0x6E or b11100110*

2.3.2.8 *Receive DS3 Configuration & Status Register*

RxDS3 Configuration & Status Register (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
0	0	0	0	X	0	0	0

Bit 7 - RxAIS (Receive AIS Pattern) Indicator

This Read-Only bit-field indicates whether or not the Receive Section of the channel is currently receiving an AIS pattern.

The channel will set this bit-field to "0" if it is not currently detecting an AIS pattern in the incoming data stream. The channel will set this bit-field to "1" if it is currently receiving an AIS pattern in the incoming data stream.

NOTE: *For a more detailed discussion on the AIS pattern for DS3 applications, refer to* Section 4.3.2.5.2

Bit 6 - RxLOS (Receive LOS Condition) Indicator

This Read-Only bit-field indicates whether or not the Receive Section of the channel is currently declaring an LOS condition of the incoming DS3 or E3 data stream.

If this bit-field is set to "0", then the Receive Section is currently not declaring an LOS condition.

If this bit-field is set to "1", then the Receive Section is currently declaring an LOS condition.

NOTE: *For more information on the LOS Declaration criteria, for DS3 or E3 applications, refer to* Section 4.3.2.5.1.

Bit 5 - RxIdle (Receive Idle Pattern) Indicator

This Read-Only bit-field indicates whether or not the Receive Section of the channel is currently detecting the Idle-pattern in the incoming DS3 data stream. This bit-field is relevant for DS3 applications only.

If this bit-field is set to "0" then the Receive Section is currently not detecting the Idle-pattern in the incoming DS3 data stream.

If this bit-field is set to "1" then the Receive Section is currently detecting the Idle pattern in the incoming DS3 data stream.

NOTE: *For more information on the Idle Pattern, refer to* Section 4.3.2.5.3

Bit 4 - RxOOF (Receive Out-of-Frame) Indicator

This Read-Only bit-field indicates whether or not the Receive Section of the channel is currently declaring an OOF condition.

If this bit-field is set to "0", then the Receive Section is currently not declaring the OOF condition.

If this bit-field is set to "1", then the Receive Section is currently declaring the OOF condition.

NOTE: *For more information on the OOF Declaration criteria, for DS3 applications, refer to* Section 4.3.2.2.

Bit 3 - Reserved

Bit 2 - Framing On Parity ON/OFF Select

This Read/Write bit field allows the user to require that the Receive DS3/E3 Framer block include Parity (P-bit) verification as a condition for declaring itself In-Frame during Frame Acquisition. This requirement will be imposed in addition to those criteria selected via Bits 0 and 1 of this register.

This feature also imposes an additional Frame Maintenance requirement on the Receive DS3/E3 Framer block, in addition to the requirements specified in the user's selection of Bits 0 and 1 of this register. In particular, if this additional requirement is implemented, the Receive DS3/E3 Framer block will perform a frame search if it detects P-bit errors in at least 2 out of 5 DS3 Frames. Writing a "1" to this bit-field imposes these additional requirements. Whereas, writing a '0' causes the Receive DS3/E3 Framer block to waive this requirement.

NOTE: *For more information on Framing with Parity, refer to* Section 4.3.2.2.

Bit 1 - F Sync Algo(rithim Select)

This Read/Write bit-field, in conjunction with Bits 0 and 2 of this register, allows the user to completely define the Frame Maintenance Criteria of the Receive DS3/E3 Framer block. This particular bit-field allows the user to define the Frame Maintenance Criteria as it applies to F-bits.

If the user writes a "1" to this bit-field, then the Receive DS3/E3 Framer block will declare an Out of Frame (OOF) condition if 3 out of 16 F-Bits are in Error. If the user writes a "0" to this bit-field, then the Receive DS3/E3 Framer block will declare an Out of Frame (OOF) condition if 6 out of 16 F-bits are in error.

NOTE: *For more information on the use of this bit, and the Framing Maintenance operation of the Receive DS3/E3 Framer block, refer to* Section 4.3.2.2.

Bit 0 - M Sync Algo(rithm Select)

This Read/Write bit-field in conjunction with Bits 1 and 2 of this register, allows the user to completely define the Frame Maintenance Criteria of the Receive DS3/E3 Framer block. This particular bit-field allows the user to define the Frame Maintenance criteria, as it applies to M-bits.

If the user writes a "1" to this bit-field, then the Receive DS3/E3 Framer block will declare an Out of Frame (OOF) condition if 3 out of 4 M-bits are in error. If the user writes a "0" to this bit-field, then the Receive DS3/E3 Framer block will ignore the occurrence of M-bit errors while operating in the Frame Maintenance mode.

NOTE: *For more information on the use of this bit-field, and the Framing Maintenance operation of the Receive DS3/E3 Framer block, refer to* Section 4.3.2.2.

2.3.2.9 *Receive DS3 Status Register*

RxDS3 Status Register (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			RxFERF	RxAIC	RxFEBE[2:0]		
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	1	0	0	0	0

Bit 4 - RxFERF Indicator

This Read Only bit-field indicates whether or not the Receive Section of the channel is declaring a FERF (Far-End-Receive Failure) condition.

If this bit-field is set to "0", then the Receive Section (of the channel) is currently not declaring an FERF condition.

If this bit-field is set to "1", then the Receive Section (of the chip) is currently declaring an FERF condition.

NOTE: *For more information on how the Receive Section of the channel declares the FERF condition, refer to* Section 4.3.2.5.4.

Bit 3 - RxAIC

This Read Only bit-field reflects the value of the AIC bit-field, within the incoming DS3 Frames, as detected by the Receive DS3/E3 Framer block (within the channel). This bit-field is set to "1" if the incoming frame is determined to be in the C-bit Parity Format (AIC bit = 1) for at least 63 consecutive frames. This bit-field is set to "0" if two (2) or more M-frames, out of the last 15 M-frames, contain a "0" in the AIC bit position.

Bits 2:0 - RxFEBE[2:0]

These Read-Only bit-fields reflect the FEBE value within the most recently received DS3 frame.

If these bit-fields are set to "111", then it indicates that the Remote Receiving Terminal is receiving DS3 frames in an un-erred manner.

If these bit-fields are set to "011", then it indicates that the Remote Receiving Terminal has detected Framing or Parity bit errors in the DS3 frames that it is receiving.

NOTE: *For more information on FEBE (Far-End-Block Error), refer to* Section 4.3.2.5.5.

2.3.2.10 *Receive DS3 Interrupt Enable Register*

RxDS3 Interrupt Enable Register (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - CP Bit Error Interrupt Enable

This Read/Write bit-field is used to enable or disable the Detection of CP-Bit Error Interrupt. Setting this bit-field to “1’ enables this interrupt. Setting this bit-field to “0” disables this interrupt.

NOTES:

1. *For more information on the CP-Bit Error Checking/Detection, refer to* Section 4.3.2.6.2.
2. *This bit-field is only valid if the Channel has been configured to operate in the DS3, C-Bit Parity Framing format.*

Bit 6 - LOS Interrupt Enable

This Read/Write bit-field is used to enable or disable the Change in LOS condition interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the LOS Condition, refer to* Section 4.3.2.5.1.

Bit 5 - AIS Interrupt Enable

This Read/Write bit-field is used to enable or disable the Change in AIS condition interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the AIS Condition, refer to* Section 4.3.2.5.2.

Bit 4 - Idle Interrupt Enable

This Read/Write bit-field is used to enable or disable the Change in Idle condition interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the Idle Condition, refer to* Section 4.3.2.5.3.

Bit 3 - FERF Interrupt Enable

This Read/Write bit-field is used to enable or disable the Change in FERF (Far End Receive Failure) Status interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on Far-End Receive Failures (or Yellow Alarms), refer to* Section 4.3.2.5.4.

Bit 2 - AIC Interrupt Enable

This Read/Write bit field allows the user to enable or disable the Change in AIC value interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on this interrupt condition, refer to* Section 4.3.2.5.6.

Bit 1 - OOF Interrupt Enable

This Read/Write bit field is used to enable or disable the Change in Out-of-Frame (OOF) status interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the OOF Condition, refer to* Section 4.3.2.2.

Bit 0 - P-Bit Error Interrupt Enable

This Read/Write bit-field is used to enable or disable the Detection of P-Bit Error interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the P-Bit Error Checking/Detection, refer to* Section 4.3.2.6.1.

2.3.2.11 *Receive DS3 Interrupt Status Register*

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	1	0	0	0	0	0	0

Bit 7 - CP Bit Error Interrupt Status

This Reset-upon-Read bit-field indicates whether or not the Detection of CP Bit Error Interrupt has occurred since the last read of this register. This bit-field will be “0” if the Detection of CP-Bit Error Interrupt has not occurred since the last read of this register. Conversely, this bit-field will be set to “1” if this interrupt has occurred since the last read of this register. The Detection of CP Bit Error Interrupt will occur if the Receive DS3/E3 Framer block detects a CP bit-error in the incoming DS3 frame.

NOTE: *This bit-field is only valid if the channel has been configured to operate in the DS3, C-bit Parity Framing format.*

Bit 6 - LOS Interrupt Status

This Reset Upon Read bit will be set to "1", if the Receive DS3/E3 Framer block has detected a Change in the LOS Status condition, since the last time this register was read. This bit-field will be asserted under either of the following conditions:

For DS3 Applications

1. When the Receive DS3/E3 Framer block detects the occurrence of an LOS Condition (e.g., the occurrence of 180 consecutive spaces in the incoming DS3 data stream), and
2. When the Receive DS3/E3 Framer block detects the end of an LOS Condition (e.g., when the Receive DS3 Framer detects 60 mark pulses in the last 180 bit periods).

NOTE: *For more information in the LOS of Signal (LOS) Alarm, refer to* Section 4.3.2.5.1.

Bit 5 - AIS Interrupt Status

This Reset Upon Read bit field will be set to "1", if the Receive DS3/E3 Framer block has detected a Change in the AIS condition, since the last time this register was read. This bit-field will be asserted under either of the following two conditions:

1. When the Receive DS3/E3 Framer block first detects an AIS Condition in the incoming DS3 data stream, and
2. When the Receive DS3/E3 Framer block has detected the end of an AIS Condition.

The local µP can determine the current state of the AIS condition by reading bit 7 of the Rx DS3 Configuration and Status Register (Address = 0x10).

NOTE: *For more information on the AIS Condition, refer to* Section 4.3.2.5.2*.*

Bit 4 - Idle Interrupt Status

This Reset Upon Read bit-field is set to "1" when the Receive DS3/E3 Framer block detects a Change in the Idle Condition in the incoming DS3 data stream. Specifically, the Receive DS3/E3 Framer block will assert this bit-field under either of the following two conditions:

1. When the Receive DS3/E3 Framer block detects the onset of the Idle Condition and
2. When the Receive DS3/E3 Framer block detects the end of the Idle Condition.

The local µP can determine the current state of the Idle condition by reading bit 5 of the Rx DS3 Configuration and Status Register (Address = 0x10).

NOTE: *For more information into the Idle Condition, refer to* Section 4.3.2.5.3*.*

Bit 3 - FERF Interrupt Status

This Reset Upon Read bit will be set to '1' if the Receive DS3/E3 Framer block has detected a Change in the Rx FERF Condition, since the last time this register was read.

This bit-field will be asserted under either of the following two conditions.

1. When the Receive DS3/E3 Framer block first detects the occurrence of an Rx FERF Condition (all X-bits are set to '0').
2. When the Receive DS3/E3 Framer block detects the end of the Rx FERF Condition (all X-bits are set to '1').

The local microprocessor can determine the current state of the FERF Condition by reading bit 4, within the Rx DS3 Status Register (Address = 0x11).

NOTE: *For more information on the Rx FERF (Yellow Alarm) condition, refer to* Section 4.3.2.5.4*.*

Bit 2 - (Change in) AIC Interrupt Status

This Reset Upon Read bit-field is set to "1" if the AIC bit-field, within the incoming DS3 frames, has changed state since the last read of this register.

NOTE: *For more information on this interrupt condition, refer to* Section 4.3.2.5.6*.*

Bit 1 - OOF Interrupt Status

This Reset Upon Read bit-field is set to "1" if the Receive DS3/E3 Framer block has detected a Change in the Out-of-Frame (OOF) Condition, since the last time this register was read. Therefore, this bit-field will be asserted under either of the following two conditions:

1. When the Receive DS3/E3 Framer block has detected the appropriate conditions to declare an OOF Condition.
2. When the Receive DS3/E3 Framer block has transitioned from the OOF Condition (Frame Acquisition Mode) into the In-Frame Condition (Frame Maintenance mode).

NOTE: *For more information of the OOF Condition, refer to* Section 4.3.2.2*.*

Bit 0 - P-Bit Error Interrupt Status

This Reset Upon Read bit-field indicates whether or not the Detection of P-bit error interrupt has occurred since the last read of this register. This bit-field will be "0" if the Detection of P-bit error interrupt has NOT occurred since the last read of this register. This bit-field will be set to "1", if this interrupt has occurred since the last read of this register. The Detection of P-bit Error interrupt will occur if the Receive DS3/E3 Framer Block detects a P-bit error in the incoming DS3 frame.

NOTE: *For more information into the role of P-bits, refer to* Section 4.3.2.6.1*.*

2.3.2.12 *Receive DS3 Sync Detect Enable Register*

RxDS3 SYNC Detect Enable Register (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			Enable F[4]	Enable F[3]	Enable F[2]	Enable F[1]	Enable F[0]
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	1	1	1	1	1

Bits 4 - 0 Enable5 F(4)- F(0)

These Read/Write bit-fields allows the user to enable or disable the 5 parallel searches for valid M and F-bit, while the Receive DS3 Framer is operating in the Frame Acquisition mode. For proper operation, the user is highly encouraged to ensure that all of these bit-fields are set to "1".

2.3.2.13 *Receive DS3 FEAC Register*

RxDS3 FEAC Register (Address = 0x16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxFEAC[5:0]						Not Used
RO	RO	RO	RO	RO	RO	RO	RO
0	1	1	1	1	1	1	0

This Read/Write register contains the latest 6-bit FEAC code that has been received and validated by the Receive FEAC Processor. The contents of this register will be cleared if the previously validated code has been removed by the FEAC Processor.

NOTES:

1. *For more information on the operation of the Receive FEAC Processor, refer to* Section 4.3.3.1.
2. *This register is only valid if the Channel has been configured to operate in the DS3, C-bit Parity Framing format.*

2.3.2.14 *Receive DS3 FEAC Interrupt Enable/Status Register*

RxDS3 FEAC Interrupt Enable/Status Register (Address = 0x17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
0	0	0	0	0	0	0	0

Bit 4 - FEAC Valid

This Read Only bit is set to "1" when an incoming FEAC Message Code has been validated by the Receive DS3/E3 Framer block. This bit is cleared to "0" when the FEAC code is removed.

NOTE: *For more information on the role of this bit-field and the Receive FEAC Processor, refer to* Section 4.3.3.1.

Bit 3 - RxFEAC Remove Interrupt Enable

This Read/Write bit-field permits the user to enable/disable the RxFEAC Removal interrupt. Writing a "1" to this bit enables this interrupt. Likewise, writing a "0" to this bit-field disables this interrupt.

NOTE: *For more information on the role of this bit-field and the Receive FEAC Processor, refer to* Section 4.3.3.1.

Bit 2 - RxFEAC Remove Interrupt Status

A "1" in this Reset-upon-Read bit-field indicates that the most recently received and validated FEAC Message has now been removed by the Receive FEAC Processor. The Receive FEAC Processor will remove a validated FEAC message if 3 out of the last 10 received FEAC messages differ from the latest valid FEAC Message.

NOTE: *For more information on this bit-field and the Receive FEAC Processor, refer to* Section 4.3.3.1.

Bit 1 - RxFEAC Valid Interrupt Enable

This Read/Write bit-field permits the user to enable or disable the Rx FEAC Valid interrupt. Writing a "1" to this bit-field enables this interrupt. Whereas, writing a "0" disables this interrupt. The value of this bit-field is "0" following power up or reset.

NOTE: *For more information on this bit-field and the Receive FEAC Processor, refer to* Section 4.3.3.1.

Bit 0 - RxFEAC Valid Interrupt Status

A "1" in this Reset-upon-Read bit-field indicates that a newly received FEAC Message has been validated by the Receive FEAC Processor.

The Receive FEAC Processor will validate a new FEAC message, once that message has been received in 8 out of 10 most recently received FEAC Messages.

NOTE: *For more information on this bit-field and the Receive FEAC Processor, refer to* Section 4.3.3.1.

2.3.2.15 *Receive DS3 LAPD Control Register*

RxDS3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	0	0

Bit 2 RxLAPD Enable

This Read/Write bit-field permits the user to enable or disable the LAPD Receiver. The LAPD Receiver MUST be enabled before it can begin to receive and process any LAPD Message frames from the incoming DS3 data stream.

Writing a "0" to this bit-field disables the LAPD Receiver (the default condition). Writing a "1" to this bit-field enables the LAPD Receiver.

Bit 1 RxLAPD (Message Frame Reception Complete) Interrupt Enable

This Read/Write bit-field permits the user to enable or disable the LAPD Message Frame Reception Complete interrupt. If this interrupt is enabled, then the channel generates this interrupt to the local µP, once the last bit of a LAPD Message frame has been received and the PMDL message has been extracted and written into the Receive LAPD Message buffer.

Writing a "0" to this bit-field disables this interrupt (the default condition). Writing a "1" to this bit-field enables this interrupt.

Bit 0 RxLAPD (Message Reception Complete) Interrupt Status

This Reset-upon-Read bit-field indicates whether or not the LAPD Message Reception Complete interrupt has occurred since the last read of this register. The LAPD Message Reception Complete interrupt will occur once the LAPD Receiver has received the last bit of a complete LAPD Message frame, extracted the PMDL message from this LAPD Message frame and has written this (PMDL) message frame into the Receive LAPD Message buffer. The purpose of this interrupt is to notify the local µP that the Receive LAPD Message buffer contains a new PMDL message, that needs to be read and/or processed.

A "0" in this bit-field indicates that the LAPD Message Reception Complete interrupt has NOT occurred since the last read of this register. A "1" in this bit-field indicates that the LAPD Message Reception Complete interrupt has occurred since the last read of this register.

NOTE: *For more information on the LAPD Receiver, refer to* Section 4.3.3.2.

2.3.2.16 *Receive DS3 LAPD Status Register*

RxDS3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxAbort	RxLAPDType[1:0}		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 6 - RxAbort (Receive Abort Sequence)

This Read-Only bit-field indicates whether or not the LAPD Receiver has detected the occurrence of an Abort Sequence (e.g., a string of seven or more consecutive "1's") from the remote LAPD Transmitter. A "0" in this bit-field indicates that no Abort-Sequence has been detected. A "1" in this bit-field indicates that the Abort-Sequence has been detected.

NOTE: *For more information on the LAPD Receiver, refer to* Section 4.3.3.2.

Bits, 5 and 4 - RxLAPDType[1:0]

These two Read Only bit-fields combine to indicate the type of LAPD Message frame that has been received by the LAPD Receiver. The relationship between these two bit-fields and the LAPD Message Type follows:

RXLAPDTYPE[1:0]		MESSAGE TYPE	MESSAGE LENGTH
BIT 5	BIT4		
0	0	CL Path Identification	76 Bytes
0	1	Idle Signal Identification	76 Bytes
1	0	Test Signal Identification	76 Bytes
1	1	ITU-T Path Identification	82 Bytes

Bit 3 - RxCR (Command/Response) Type

This Read Only bit field indicates the value of the C/R (Command/Response) bit-field of the latest received LAPD Message.

Bit 2 - Rx FCS (Frame Check Sequence) Error

This Read-Only bit-field indicates whether or not the LAPD Receiver has detected a Frame Check Sequence (FCS) error in the most recently received LAPD Message Frame. A "0" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is correct. A "1" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is incorrect.

NOTE: *For more information on the LAPD Receiver, refer to* Section 4.3.3.2.

Bit 1 - End Of Message

This Read-Only bit-field indicates whether or not the LAPD Receiver has completed its reception of the latest incoming LAPD Message frame. The local µP can poll the progress of the LAPD Receiver by periodically reading this bit-field.

The LAPD Receiver will assert this read-only bit-field, when it has received a complete LAPD Message frame. This bit-field, along with the Receipt of New LAPD Message frame interrupt, serves to inform the local µP that the Receive LAPD Message buffer contains a new PMDL message that needs to be read and processed.

This bit-field is cleared (to "0") when the LAPD receiver starts receiving a new LAPD frame. (The EOM bit goes “Low” once a valid header is received.).

A "0" in this bit-field indicates that the LAPD Receiver is still receiving the latest message from the remote LAPD Transmitter. A "1" in this bit-field indicates that the LAPD Receiver has finished receiving the complete LAPD Message Frame.

Bit 0 - Flag Present

This Read-Only bit-field indicates whether or not the LAPD Receiver has detected the occurrence of the Flag Sequence byte (0x7E) within the inbound LAPD channel (e.g., the DL bits in DS3 applications). A "0" in this bit-field indicates that the LAPD Receiver does not detect the occurrence of the Flag Sequence byte. A "1" in this bit-field indicates that the LAPD Receiver does detect the occurrence of the Flag Sequence byte.

NOTE: *For more information on the LAPD Receiver, refer to* Section 4.3.3.2.

2.3.3 Receive E3 Framer Configuration Registers (ITU-T G.832)

NOTE: *The default register values shown below are after the operating mode is set to G.832 Bit mode. These are different from the power-up default values.*

2.3.3.1 *Receive E3 Configuration & Status Register 1 (E3, ITU-T G.832)*

RxE3 Configuration & Status Register 1 (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxPLDType[2:0]			RxFERF Algo	RxTMark Algo	RxPLDExp[2:0]		
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	0

Bit 7 - 5 - RxPLDType[2:0] (Received Payload Type[2:0])

These three Read-Only bit-fields contain the Payload Type value within the MA byte of the most recently received E3 frame.

NOTES:

1. *The Payload Type Mismatch interrupt will be generated if the contents of these bit-fields differ from that of the Expected Payload Types in Bits 2 through 0 within this Register.*
2. *These bit-fields are ignored is the channel is configured to support the October 1998 version of the ITU-T G.832 framing format for E3.*

Bit 4 - RxFERF Algo

This Read/Write bit-field allows the user to select one of the two RxFERF Declaration Algorithms:

Writing a "0" to this bit-field selects the following RxFERF Declaration algorithm:

- The Receive DS3/E3 Framer declares a Far End Receive Failure (FERF) if the FERF bit-field, within the MA byte is set to "1" for 3 consecutive incoming E3 Frames. Likewise, the Receive DS3/E3 Framer block will negate the Far End Receive Failure condition if the FERF bit-field, within the MA byte is set to "0" for 3 consecutive incoming E3 Frames.

Writing a "1" to this bit-field selects the following RxFERF Declaration algorithm:

- The Receive DS3/E3 Framer block declares a Far End Receive Failure (FERF) if the FERF bit-field, within the MA byte is set to "1" for 5 consecutive E3 Frames. Likewise, the Receive E3/DS3 Framer block will negate the Far End Receive Failure condition if the FERF bit-field, within the MA byte is set to "0" for 5 consecutive incoming E3 Frames.

Bit 3 - RxTMark Algorithm

This Read/Write bit-field allows the user to select the number of consecutive incoming E3 frames, that the Timing Marker bit-field (within the MA byte-field) must be of a given logic state, before it is validated by the Receive DS3/E3 Framer block. Once the Receive DS3/E3 Framer block has validated the state of the Timing

Marker bit-field, then it will write this logic state into Bit 1 (RxTMark) within the Rx E3 Configuration & Status Register 2 (Address = 0x11)

Writing a "0" into this bit-field causes the Receive DS3/E3 Framer block to validate the Timing Marker value after receiving 3 consecutive incoming E3 frames, with the Timing Marker bit-field of a given value. Writing a "1" into this bit-field causes the Receive DS3/E3 Framer block to validate the Timing Marker value after receiving 5 consecutive incoming E3 frames, with the Timing Marker bit-field of a given value.

NOTE: *This bit-field is ignored if the channel is configured to support the October 1998 version of the ITU-T G.832 framing format for E3.*

Bits 2 - 0: RxPLDExp[2:0]

This Read/Write bit-field allows the user to specify the Payload Type that is expected in the MA bytes, of each incoming E3 frame.

If the Receive DS3/E3 Framer detects a Payload Type that differs from the values within these bit-fields, then the Framer will generate the Payload Type Mismatch interrupt.

2.3.3.2 *Receive E3 Configuration & Status Register 2 (E3, ITU-T G.832)*

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	RxTMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	1	0	0	1	0

Bit 7 - RxLOF Algo (Loss of Frame Declaration Algorithm)

This Read/Write bit-field allows the user to select the LOF (Loss of Frame) Declaration criteria, that will be used by the Receive DS3/E3 Framer. Writing a "0" to this bit-field configures the Receive DS3/E3 Framer to declare an LOF condition, after it has been in the OOF condition for 24 frame periods (3 ms). Writing a "1" to this bit-field configures the Receive DS3/E3 Framer to declare an LOF condition, after it has been in the OOF condition for 8 frame periods (1 ms).

Bit 6 - RxLOF (Loss of Frame Declaration)

This Read-Only bit-field indicates whether or not the Receive DS3/E3 Framer block is currently in the Loss of Frame (LOF) condition. If this bit-field is set to "1", then the Receive DS3/E3 Framer block is currently in the LOF condition. Conversely, if this bit-field is set to "0", then the Receive DS3/E3 Framer block is currently not in the LOF condition.

Bit 5 - RxOOF (Out of Frame Declaration)

This Read-Only bit field indicates whether or not the Receive DS3/E3 Framer block is currently experiencing an Out of Frame (OOF) condition. The Receive DS3/E3 Framer block will declare an OOF condition if it has detected errors in the frame alignment bytes (FA1 and FA2) in four consecutive frames. If this bit-field is set to "1", then the Receive DS3/E3 Framer block has declared, and is continuing to experience an OOF condition. If this bit-field is set to "0", then the Receive DS3/E3 Framer block is currently not experiencing an OOF condition.

Bit 4 - RxLOS (Loss of Signal Declaration)

This Read-Only bit-field indicates whether or not the Receive DS3/E3 Framer block is currently experiencing a Loss of Signal (LOS) condition. The Receive DS3/E3 Framer block will declare an LOS condition if it has detected a string of 32 consecutive "0's", via the RxPOS and RxNEG input pins. If this bit-field is set to "1", then the Receive DS3/E3 Framer block has declared, and is continuing to experience an LOS condition. If this bit-field is set to "0", then the Receive DS3/E3 Framer block is currently not experiencing an LOS condition.

Bit 3 - RxAIS (Alarm Indication Status Declaration)

This Read-Only bit-field indicates whether or not the Receive DS3/E3 Framer block is currently experiencing an AIS condition. The Receive DS3/E3 Framer block will declare an AIS condition if it has detected two

consecutive E3 frames, that each contain less than seven (7) "0's" . If this bit-field is set to "1", then the Receive DS3/E3 Framer block has declared, and is continuing to experience an AIS condition. If this bit-field is set to "0", then the Receive DS3/E3 Framer block is currently not experiencing an AIS condition.

Bit 2 - RxPLDType UnStab

This Read-Only bit-field indicates whether or not the Receive DS3/E3 Framer block has been receiving a consistent Payload Type value (within the MA Byte-Field) in the last 5 consecutive incoming E3 frames.

If the Receive DS3/E3 Framer block has detected a change in the Payload Type value, within the last 5 incoming E3 frames, then it will set this bit-field to "1". If the Payload Type value has been consistent in the last 5 E3 frames, then the Receive DS3/E3 Framer block will set this bit-field to "0".

Bit 1 - Rx TMark

This Read-Only bit-field reflects the most recently validated Timing Marker value. The Receive DS3/E3 Framer block will validate the Timing Marker state, after it has detected a user-selectable number of consecutive incoming E3 frames with a consistent Timing Marker value. The user makes this selection by writing the appropriate value to Bit 3 (RxTMarkAlgo) within the Rx E3 Configuration/Status Register 1 (Address = 0x10).

Bit 0 - RxFERF (Far End Receive Failure)

This Read-Only bit-field indicates whether or not the Receive DS3/E3 Framer block is experiencing an FERF (Far-End-Receive-Failure) condition. The Receive DS3/E3 Framer block will declare a FERF condition, if it has received a user-selectable number of consecutive E3 frames, with the FERF bit-field (within the MA byte) set to "1". This user-selectable number is either 3 or 5 E3 frames. Conversely, the Receive E3 Framer will negate the FERF declaration, if it has received this user-selectable number of consecutive E3 frames, with the FERF bit-field set to "0".

If this bit-field is set to "1", then the Receive DS3/E3 Framer block has declared an FERF condition. If this bit-field is set to "0", then the Receive DS3/E3 Framer block has not declared an FERF condition.

NOTE: *See* Section 6.1.1.4*, for a more detailed discussion on the meaning of the FERF bit-field, within the E3 frame.*

2.3.3.3 *Receive E3 Interrupt Enable Register 1 (E3, ITU-T G.832)*

RxE3 Interrupt Enable Register 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	SSM MSG Interrupt Enable	SSM OOS Interrupt Enable	COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - SSM Message Interrupt Enable

This Read/Write bit-field permits the user to enable or disable the Change in Synchronous Status Message (SSM) interrupt. Setting this bit-field to “1” enables this interrupt. Setting this bit-field to “0” disables this interrupt.

NOTE: *This bit-field is ignored if the Channel is configured to support the November 1995 revision of the ITU-T G.832 Framing format for E3. (See* Section 2.3.3.27*.)*

Bit 5 - SSM OOS (Out of Sequence) Interrupt Enable

This Read/Write bit-field permits the user to enable or disable the Change in SSM Out of Sequence State interrupt. Setting this bit-field to “1” enables this interrupt. Setting this bit-field to “0” disables this interrupt.

NOTE: *This bit-field is ignored if the Channel is configured to support the November 1995 revision of the ITU-T G.832 Framing format for E3. (See* Section 2.3.3.27*)*

Bit 4 - Change of Frame Alignment (COFA) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change of Frame Alignment interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

Bit 3 - OOF (Out of Frame) Interrupt Enable

This Read/Write bit field allows the user to enable or disable the Change in Out-of-Frame (OOF) status interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the OOF Condition, refer to* Section 6.3.2.1.

Bit 2 - LOF (Loss of Frame) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change in Loss-of-Frame (LOF) status interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the LOF Condition see* Section 6.3.2.1.

Bit 1 - LOS (Loss of Signal) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change in LOS condition interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the LOS Condition see* Section 6.3.2.6.

Bit 0 - AIS Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change in AIS condition interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the AIS Condition see* Section 6.3.2.6.2.

2.3.3.4 *Receive E3 Interrupt Enable Register 2 (E3, ITU-T G.832)*

RxE3 Interrupt Enable Register 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Enable	Not Used	FEBE Interrupt Enable	FERF Interrupt Enable	BIP-8 Error Interrupt Enable	Framing Byte Error Interrupt Enable	RxPld Mis Interrupt Enable
RO	R/W	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - TTB Change Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change in Trail Trace Buffer Message interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on Trail Trace Buffer messages see* Section 6.3.2.9.

Bit 4 - FEBE (Far-End Block Error) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Far-End-Block Error (FEBE) interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the FEBE Interrupt condition see* Section 6.3.6.2.8.

Bit 3 - FERF (Far-End Receive Failure) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change in FERF Condition interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the Change in FERF Condition interrupt see* Section 6.3.6.2.7.

Bit 2 - BIP-8 Error Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the BIP-8 interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on this interrupt see* Section 6.3.6.2.9.

Bit 1 - Framing Byte Error Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Framing Byte Error interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: For more information on this interrupt, refer to Section 6.3.6.2.10.

Bit 0 - Receive Payload Type Mismatch Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Receive Payload Type Mismatch interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: For more information on this interrupt, refer to Section 6.3.6.2.11.

2.3.3.5 *Receive E3 Interrupt Status Register 1 (E3, ITU-T G.832)*

RxE3 Interrupt Status Register 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	SSM MSG Interrupt Status	SSM OOS Interrupt Status	COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 6 - SSM Message Interrupt Status

This Reset-upon-Read bit-field indicates whether or not a Change of Synchronization Status Message (SSM) Interrupt has occurred since the last read of this register. This interrupt will occur whenever a change in the contents of the SSM (within the inbound E3 data stream) has been detected.

If this bit-field has been set to “1”, then the Change of SSM Interrupt has occurred since the last read of this register. Conversely, if this bit-field has been set to “0”, then the Change of SSM Interrupt has not occurred since the last read of this register.

NOTE: This bit-field is invalid if the channel has been configured to support the November 1995 revision of the ITU-T G.832 Framing format for E3.

Bit 5 - SSM Out of Sequence Interrupt Status

This Reset-upon-Read bit-field indicates whether or not the Change in SSM Out of Sequence State interrupt has occurred since the last read of this register. This interrupt will occur in response to either of the following conditions.

1. The Receive Section losses sequence synchronization with the SSM data.
2. The Receive Section re-acquires sequence synchronization with the SSM data.

NOTE: This bit-field is invalid if the Channel has been configured to support the November 1995 revision of the ITU-T G.832 Framing format for E3.

Bit 4 - COFA (Change of Frame Alignment) Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the Change of Frame Alignment interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate the Change of Frame Alignment interrupt if it has detected a change in frame alignment in the incoming E3 frames.

Bit 3 - OOF (Receive E3 Framer) Interrupt Status

This Reset Upon Read bit-field is set to "1" if the Receive DS3/E3 Framer block has detected a Change in the Out-of-Frame (OOF) Condition, since the last time this register was read. Therefore, this bit-field will be asserted under either of the following two conditions:

1. When the Receive DS3/E3 Framer block has detected the appropriate conditions to declare an OOF Condition.
2. When the Receive DS3/E3 Framer block has transitioned from the OOF Condition (Frame Acquisition Mode) into the In-Frame Condition (Frame Maintenance mode).

NOTE: For more information of the OOF Condition, refer to Section 6.3.2.1.

Bit 2 - LOF (Loss of Frame) Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if a Change in LOF Condition interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate the Change in LOF Condition interrupt in response to either of the following two occurrences.

1. Whenever the Receive DS3/E3 Framer block transitions from the OOF Condition state into the LOF Condition state, within the E3 Framing Acquisition/Maintenance algorithm (per Figure 182).
2. Whenever the Receive DS3/E3 Framer block transitions from the FA1, FA2 Octet Verification state to the In-frame state, within the E3 Framing Acquisition/Maintenance algorithm (per Figure 182).

Bit 1 - LOS (Loss of Signal) Interrupt Status

This Reset Upon Read bit will be set to "1", if the Receive DS3/E3 Framer block has detected a

Change in the LOS Status condition, since the last time this register was read. This bit-field will be asserted under either of the following two conditions:

1. When the Receive DS3/E3 Framer block detects the occurrence of an LOS Condition (e.g., the occurrence of 32 consecutive spaces in the incoming E3 data stream), and
2. When the Receive DS3/E3 Framer block detects the end of an LOS Condition (e.g., when the Receive DS3/E3 Framer block detects a string 32 bits that does not contain a string of four consecutive "0's").

The local µP can determine the current state of the LOS condition by reading bit 4 of the Rx E3 Configuration and Status Register (Address = 0x11).

NOTE: *For more information in the LOS of Signal (LOS) Alarm, refer to* Section 6.3.2.6.

Bit 0 - AIS Interrupt Status

This Reset Upon Read bit field will be set to "1", if the Receive DS3/E3 Framer block has detected a Change in the AIS condition, since the last time this register was read. This bit-field will be asserted under either of the following two conditions:

1. When the Receive DS3/E3 Framer block first detects an AIS Condition in the incoming E3 data stream.
2. When the Receive DS3/E3 Framer block has detected the end of an AIS Condition in the incoming E3 data stream.

The local µP can determine the current state of the AIS condition by reading bit 3 of the Rx E3 Configuration and Status Register (Address = 0x11).

NOTE: *For more information on the AIS Condition, refer to* Section 6.3.2.6.2.

2.3.3.6 *Receive E3 Interrupt Status Register 2 (E3, ITU-T G.832)*

RxE3 Interrupt Status Register 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 6 - TTB Change Interrupt Status (Receipt of New Trail Trace Buffer Message interrupt)

This Reset-upon-Read bit-field will be set to "1" if a Receipt of New Trail Trace Buffer Message interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate the Receipt of New Trail Trace Buffer Message interrupt, if it receives an E3 frame in which the value of the TR byte-field is of the form "1xxxxxxxb". A TR byte-field value of this form is identified as the frame start marker.

NOTE: *Please see Section 6.3.6.2.6 for a more detailed discussion of this interrupt.*

Bit 4 - FEBE (Far-End Block Error) Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the FEBE (Far-End-Block Error) interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate the FEBE interrupt anytime it detects a "1" in the FEBE bit-field within an incoming E3 frame.

NOTE: *Please see Section 6.3.6.2.8 for a more detailed discussion of this interrupt.*

Bit 3 - FERF Interrupt Status

This Reset Upon Read bit will be set to '1' if the Receive E3 Framer has detected a Change in the Rx FERF Condition, since the last time this register was read.

This bit-field will be asserted under either of the following two conditions.

1. When the Receive DS3/E3 Framer block first detects the occurrence of an RxFERF Condition (e.g., when the FERF bit, within the last 3 or 5 consecutive E3 frames are set to "1").
2. When the Receive DS3/E3 Framer block detects the end of the RxFERF Condition (e.g., when the FERF bit, within the last 3 or 5 consecutive E3 frames are set to "0").

NOTE: *For more information on the RxFERF (Yellow Alarm) condition, refer to Section 6.3.2.6.3.*

Bit 2 - BIP-8 (EM Byte) Error Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the BIP-8 Error interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate the BIP-8 Error interrupt if it has concluded that it has received an errored E3 frame, from the Remote Terminal.

NOTE: *Please see Section 6.3.6.2.9 for a more detailed discussion of this interrupt.*

Bit 1 - Framing Byte Error Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the Framing Byte Error interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate the Framing Byte Error interrupt if it has detected an error in the FA1 or FA2 bytes, on an incoming E3 frame.

NOTE: *Please see Section 6.3.6.2.10 for a more detailed discussion of this interrupt.*

Bit 0 - Rx Pld Mis Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the Payload Type Mismatch interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate the Payload Type Mismatch interrupt when it detects that the values, within the Payload Type bit-fields of the incoming E3 frame, has changed from that of the previous E3 frame.

NOTE: *Please see Section 6.3.6.2.11 for a more detailed discussion on this interrupt.*

2.3.3.7 *Receive E3 LAPD Control Register (E3, ITU-T G.832)*

RxE3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				DL from NR	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	R/W	R/W	R/W	RUR
0	0	0	0	0	0	0	0

Bit 3 - DL from NR

This Read/Write bit-field allows the user to specify whether the LAPD Receiver should retrieve the bytes, comprising the incoming LAPD Message frame, from the NR byte-field, or from the GC byte-field, within each incoming E3 frame.

Writing a "1" configures the LAPD Receiver to retrieve the incoming LAPD Message frame octets from the NR byte-field, within each incoming E3 frame. Writing a "0" configures the LAPD Receiver to retrieve the incoming LAPD Message frame octets from the GC byte.

Bit 2 - RxLAPD Enable

This Read/Write bit-field allows the user to enable or disable the LAPD Receiver, for reception of incoming LAPD Message frames from the Remote LAPD Transmitter.

Writing a "1" to this bit-field enables the LAPD Receiver. Writing a "0" to this bit-field disables the LAPD Receiver.

Bit 1 - RxLAPD (Received LAPD Message) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Received LAPD Message frame interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on this interrupt, refer to* Section 6.3.3.

Bit 0 - RxLAPD (Received LAPD Message) Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the Receipt of New LAPD Message frame interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate this Receipt of New LAPD Message frame interrupt when the LAPD Receiver has received a complete LAPD Message frame from the Remote LAPD Transmitter.

NOTE: *Please see* Section 6.3.6.2.12 *for a more detailed discussion of this interrupt.*

2.3.3.8 *Receive E3 LAPD Status Register (E3, ITU-T G.832*

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Rx ABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 6 - RxAbort (Receive Abort Sequence)

This Read-Only bit-field indicates whether or not the LAPD Receiver has detected the occurrence of an Abort Sequence (e.g., a string of seven or more consecutive "1's") from the remote LAPD Transmitter. A "0" in this bit-field indicates that no Abort-Sequence has been detected. A "1" in this bit-field indicates that the Abort-Sequence has been detected.

NOTE: *For more information on the LAPD Receiver, refer to* Section 4.3.3.2.

Bits, 5 and 4 - RxLAPDType[1:0]

These two Read Only bit-fields combine to indicate the type of LAPD Message frame that has been received by the LAPD Receiver. The relationship between these two bit-fields and the LAPD Message Type follows:

RXLAPDTYPE[1:0]		MESSAGE TYPE	MESSAGE LENGTH
0	0	CL Path Identification	76 Bytes
0	1	Idle Signal Identification	76 Bytes
1	0	Test Signal Identification	76 Bytes
1	1	ITU-T Path Identification	82 Bytes

Bit 3 - RxCR (Command/Response) Type

This Read Only bit field indicates the value of the C/R (Command/Response) bit-field of the latest received LAPD Message.

Bit 2 - Rx FCS (Frame Check Sequence) Error

This Read-Only bit-field indicates whether or not the LAPD Receiver has detected a Frame Check Sequence (FCS) error in the most recently received LAPD Message Frame. A "0" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is correct. A "1" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is incorrect.

NOTE: *For more information on the LAPD Receiver, refer to* Section 4.3.3.2.

Bit 1 - End Of Message

This Read-Only bit-field indicates whether or not the LAPD Receiver has completed its reception of the latest incoming LAPD Message frame. The local µP can poll the progress of the LAPD Receiver by periodically reading this bit-field.

The LAPD Receiver will assert this read-only bit-field, when it has received a complete LAPD Message frame. This bit-field, along with the Receipt of New LAPD Message frame interrupt, serves to inform the local µP that the Receive LAPD Message buffer contains a new PMDL message that needs to be read and processed.

This bit-field is cleared (to "0") when the LAPD receiver starts receiving a new LAPD frame. (The EOM bit goes “Low” once a valid header is received.).

A "0" in this bit-field indicates that the LAPD Receiver is still receiving the latest message from the remote LAPD Transmitter. A "1" in this bit-field indicates that the LAPD Receiver has finished receiving the complete LAPD Message Frame.

Bit 0 - Flag Present

The LAPD Receiver will assert this read-only bit-field when it is currently detecting the Flag Sequence octet (7Eh) in the incoming LAPD channel (e.g., either the GC or the NR byte-field, within each E3 frame). The LAPD Receiver will negate this bit-field when it is no longer receiving the Flag Sequence octet in the incoming LAPD channel.

2.3.3.9 *Receive E3 NR Byte Register (E3, ITU-T G.832)*

RxE3 NR Byte Register (Address = 0x1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxNR[7:0]							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the value of the NR byte, within the most recently received E3 frame.

NOTE: *Refer to Section 6.3.3 for a more detailed discussion on this register.*

2.3.3.10 *Receive E3 GC Byte Register (E3, ITU-T G.832)*

RxE3 GC Byte Register (Address = 0x1B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxGC[7:0]							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the value of the GC byte, residing in the most recently received E3 frame.

NOTE: *Refer to Section 6.3.3 for a more detailed discussion on this register.*

2.3.3.11 *Receive E3 TTB-0 Register (E3, ITU-T G.832)*

RxE3 TTB-0 Register (Address = 0x1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-0							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the frame start marker byte of the 16 byte Trail Trace Buffer Message that has been received from the Remote Terminal, via the TR byte-field within the incoming E3 frames. The remaining bytes, of this Trail Trace Buffer Message can be found in the RxTTB-1 through RxTTB-15 registers.

The data in this register is typically of the form [1, C6, C5, C4, C3, C2, C1, C0]. The "1" in the MSB position identifies this byte as being the frame start marker (e.g., the first byte within the 16 byte Trail Trace Buffer Message). The remaining bits: C0 - C6 contain the CRC-7 value that was calculated over the previous 16 byte Trail Trace Buffer Message.

NOTES:

1. *The XRT72L50 Framer will not compute or verify this CRC-7 value. It is up to the user's hardware and/or software to compute and verify this value.*
2. *For more information on the use of this register, refer to Section 6.3.2.9.*

2.3.3.12 *Receive E3 TTB-1 Register (E3, ITU-T G.832)*

RxE3 TTB-1 Register (Address = 0x1D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-1							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the second (2nd) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to Section 6.3.2.9.*

2.3.3.13 Receive E3 TTB-2 Register (E3, ITU-T G.832)

RxE3 TTB-2 Register (Address = 0x1E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-2							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the third (3rd) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.14 Receive E3 TTB-3 Register (E3, ITU-T G.832)

RxE3 TTB-3 Register (Address = 0x1F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-3							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the fourth (4th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.15 Receive E3 TTB-4 Register (E3, ITU-T G.832)

RxE3 TTB-4 Register (Address = 0x20)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-4							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the fifth (5th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.16 *Receive E3 TTB-5 Register (E3, ITU-T G.832)*

RxE3 TTB-5 Register (Address = 0x21)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-5							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the sixth (6th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.17 *Receive E3 TTB-6 Register (E3, ITU-T G.832)*

RxE3 TTB-6 Register (Address = 0x22)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-6							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the seventh (7th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.18 *Receive E3 TTB-7 Register (E3, ITU-T G.832)*

RxE3 TTB-7 Register (Address = 0x23)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-7							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the eighth (8th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.19 *Receive E3 TTB-8 Register (E3, ITU-T G.832)*

RxE3 TTB-8 Register (Address = 0x24)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-8							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the ninth (9th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.20 *Receive E3 TTB-9 Register (E3, ITU-T G.832)*

RxE3 TTB-9 Register (Address = 0x25)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-9							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the tenth (10th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.21 *Receive E3 TTB-10 Register (E3, ITU-T G.832)*

RxE3 TTB-10 Register (Address = 0x26)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-10							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the eleventh (11th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.22 *Receive E3 TTB-11 Register (E3, ITU-T G.832)*

RxE3 TTB-11 Register (Address = 0x27)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-11							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the twelfth (12th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.23 *Receive E3 TTB-12 Register (E3, ITU-T G.832)*

RxE3 TTB-12 Register (Address = 0x28)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-12							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the thirteenth (13th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.24 *Receive E3 TTB-13 Register (E3, ITU-T G.832)*

RxE3 TTB-13 Register (Address = 0x29)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-13							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the fourteenth (14th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.25 Receive E3 TTB-14 Register (E3, ITU-T G.832)

RxE3 TTB-14 Register (Address = 0x2A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-14							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the fifteenth (15th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.26 Receive E3 TTB-15 Register (E3, ITU-T G.832)

RxE3 TTB-15 Register (Address = 0x2B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB-15							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register contains the sixteenth (16th) byte within the 16 byte Trail Trace Buffer Message, that has been received from the Remote Terminal. This register typical contains an ASCII character that is required for the E.164 numbering format.

NOTE: *For more information on the use of this register, refer to* Section 6.3.2.9.

2.3.3.27 Receive E3 Framer SSM Register (E3, ITU-T G.832)

RxE3 ssm Register (Address = 0x2C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxSSM Enable	MFI[1:0]		Reserved	RxSSM[3:0]			
R/W	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 7 - RxSSM Enable

This Read/Write bit-field permits the user to configure the Receive Section of a given channel to support processing of the MA byte via either the old or the new ITU-T G.832 Framing format.

Setting this bit-field to “1” configures the Receive Section to support the new E3, ITU-T G.832 framing standard (October 1998 Revision). Setting this bit-field to “0” configures the Receive Section to support the old E3, ITU-T G.832 framing standard (November 1995).

Bits 6, 5 - MF[1:0] - SSM Multiframe Indicator Bits

These two bits reflect the states of the SSM Multi-frame phase indicators, within the most recently received E3 frame. Stated another ways, these two bit-fields reflect Bits 2 and 1 within the MA byte, in the most recently received E3 frame.

NOTE: *These two bit-fields are only valid if the Receive Section of the Channel has been configured to support the October 1998 Revision of the ITU-T G.832 Framing format for E3.*

Bits 3-0 - RxSSM[3:0] - Received Synchronization Status Message

These four Read-Only bits reflect the content of the SSM, which is currently being received via the inbound E3 data stream.

NOTE: *These four bit-fields are only valid if the Receive Section of the Channel has been configured to support the October 1998 Revision of the ITU-T G.832 Framing format for E3.*

2.3.4 Receive E3 Framer Configuration Registers (ITU-T G.751)

NOTE: *Device powers-up in E3 G.751 mode by default.*

2.3.4.1 *Receive E3 Configuration & Status Register 1 (E3, ITU-T G.751)*

RxE3 Configuration & Status Register 1 (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			RxFERF Algo	Reserved			RxBIP4
RO	RO	RO	R/W	RO	RO	RO	R/W
0	0	0	0	0	0	1	0

Bit 4 - RxFERF Algo(rithm) Select

This Read/Write bit-field permits the user to select the Received FERF Declaration Algorithm.

Setting this bit-field to "0", configures the Receive Section of the Channel to declare a FERF (Far-End-Receive Failure), after three (3) consecutive E3 frames, with the A-Bit set to "1", have been received. Further, the Receive Section of the Channel will clear FERF, after three (3) consecutive E3 frames, with the A-Bit set to "0", have been received.

Setting this bit-field to "1", configures the Receive Section of the Channel to declare a FERF, after five (5) consecutive E3 frames, with the A-Bit set to "1", have been received. Further, the Receive Section of the Channel will clear FERF after five (5) consecutive E3 frames, with the A-Bit set to "0", have been received.

Bit 0 - RxBIP4 Enable

This Read/Write bit-field permits the user to configure the Receive Section of the Channel to verify (or not verify) the BIP-4 value within each incoming E3 frame.

Setting this bit-field to "0", configures the Receive Section of the Channel to NOT verify the BIP-4 value within each incoming E3 frame.

Setting this bit-field to "1", configures the Receive Section of the Channel to verify the BIP-4 value within each incoming E3 frame.

2.3.4.2 *Receive E3 Configuration & Status Register 2 (E3, ITU-T G.751)*

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	1	0	0	1	0

Bit 7 - RxLOF (Receive Loss of Frame) Algo(rithm) Select

This Read/Write bit-field permits the user to select the Receive Loss of Frame Declaration Algorithm, for the Receive Section of the Channel.

Setting this bit-field to "0" configures the Receive Section to declare a Loss of Frame condition, if it resides in the OOF (Out of Frame) Condition for 24 E3 Frame periods. Likewise, the Receive Section will clear the Loss of Frame condition, if it resides in the In-Frame condition for 24 E3 Frame periods.

Setting this bit-field to "1" configures the Receive Section to declare a Loss of Frame condition, if it resides in the OOF (Out of Frame) condition for 8 E3 Frame periods. Likewise, the Receive Section will clear the Loss of Frame condition, if it resides in the In-Frame condition for 8 E3 Frame periods.

NOTE: *For more information on the LOF and OOF condition, refer to* Section 5.3.2.2.

Bit 6 - RxLOF (Receive Loss of Frame) Status

This Read-Only bit-field indicates whether or not the Receive Section of the Framer IC is operating in the Loss of Frame state.

If this bit-field is set to "0", then the Receive Section is NOT operating in the Loss of Frame state. Conversely, if this bit-field is set to "1", then the Receive Section is operating in the Loss of Frame state.

NOTE: *For more information on the "Loss of Frame" State, refer to* Section 5.3.2.2.

Bit 5 - RxOOF (Receive Out of Frame) Status

This Read-Only bit-field indicates whether or not the Receive Section of the Channel is operating in the Out of Frame state.

If this bit-field is set to "0", then the Receive Section is NOT operating in the Out of Frame state. Conversely, if this bit-field is set to "1", then the Receive Section is operating in the Out of Frame state.

NOTE: *For more information on the Out of Frame State, refer to* Section 5.3.2.2.

Bit 4 - RxLOS (Receive Loss of Signal) Status

This Read-Only bit-field indicates whether or not the Receive Section of the Channel is currently declaring an LOS (Loss of Signal) Condition.

If this bit-field is set to "0", then the Receive Section is NOT declaring a Loss of Signal condition. Conversely, if this bit-field is set to "1", then the Receive Section is declaring the Loss of Signal condition.

NOTE: *For more information on the Loss of Signal Condition, refer to* Section 5.3.2.7.

Bit 3 - RxAIS (Receive Alarm Indication Signal) Status

This Read-Only bit-field indicates whether or not the Receive Section of the Channel is currently declaring an AIS (Alarm Indication Signal) Condition.

If this bit-field is set to "0", then the Receive Section is NOT declaring a AIS condition. Conversely, if this bit-field is set to "1", then the Receive Section is declaring an AIS condition.

NOTE: *For more information on the AIS Condition, refer to* Section 5.3.2.8.

Bit 0 - RxFERF (Received Far-End-Receive-Failure) Status

This Read-Only bit-field indicates whether or not the Receive Section of the Channel is currently declaring a FERF (Far-End Receive Failure) Condition.

If this bit-field is set to "0", then the Receive Section is NOT declaring a FERF condition. Conversely, if this bit-field is set to "1", then the Receive Section is declaring an FERF condition.

NOTE: *For more information on the FERF Condition, refer to* Section 5.3.2.9.

2.3.4.3 *Receive E3 Framer Interrupt Enable Register 1 (E3, ITU-T G.751)*

RxE3 Interrupt Enable Register 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 4 - COFA (Change of Frame Alignment) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change of Frame Alignment interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

Bit 3 - OOF (Change in OOF Condition) Interrupt Enable

This Read/Write bit field allows the user to enable or disable the Change in Out-of-Frame (OOF) status interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the OOF Condition, refer to* Section 5.3.2.2.

Bit 2 - LOF (Change in LOF Condition) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change in Loss-of-Frame (LOF) status interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the LOF Condition, refer to* Section 5.3.2.2.

Bit 1 - LOS (Change in LOS Condition) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change in LOS condition interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the LOS Condition, refer to* Section 5.3.2.7.

Bit 0 - AIS (Change in AIS Condition) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change in AIS condition interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the AIS Condition, refer to* Section 5.3.2.8

2.3.4.4 *Receive E3 Interrupt Enable Register 2 (E3, ITU-T G.751)*

RxE3 Interrupt Enable Register 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Enable	BIP-4 Error Interrupt Enable	Framing Error Interrupt Enable	Not Used
RO	RO	RO	RO	R/W	R/W	R/W	RO
0	0	0	0	0	0	0	0

Bit 3 - FERF (Far-End Receive Failure) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Change in FERF Condition interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on the Change in FERF Condition interrupt, refer to* Section 5.3.2.9 *and* Section 5.3.6.2.6.

Bit 2 - BIP-4 Error Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the BIP-4 Error interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on this interrupt, refer to* Section 5.3.2.10*. and* Section 5.3.6.2.8*.*

Bit 1 - Framing Error Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Framing Error interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: *For more information on this interrupt, refer to* Section 5.3.6.2.8*.*

2.3.4.5 *Receive E3 Interrupt Status Register 1 (E3, ITU-T G.751)*

RxE3 Interrupt Status Register 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	1	0

Bit 4 - COFA (Change of Framing Alignment) Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the Change of Frame Alignment interrupt has occurred since the last read of this register.

The Receive E3 Framer will generate the Change of Frame Alignment interrupt if it has detected a change in frame alignment in the incoming E3 frames.

Bit 3 - OOF (Change in OOF Condition) Interrupt Status

This Reset Upon Read bit-field is set to "1" if the Receive DS3/E3 Framer block has detected a Change in the Out-of-Frame (OOF) Condition, since the last time this register was read. Therefore, this bit-field will be asserted under either of the following two conditions:

1. When the Receive DS3/E3 Framer block has detected the appropriate conditions to declare an OOF Condition.
2. When the Receive DS3/E3 Framer block has transitioned from the OOF Condition (Frame Acquisition Mode) into the In-Frame Condition (Frame Maintenance mode).

NOTE: *For more information of the OOF Condition, refer to* Section 5.3.2.2*.*

Bit 2 - LOF (Change in LOF Condition) Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if a Change in LOF Condition interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate the Change in LOF Condition interrupt is response to either of the following two occurrences.

1. Whenever the Receive DS3/E3 Framer block transitions from the OOF Condition state into the LOF Condition state, within the E3 Framing Acquisition/Maintenance algorithm (per Figure 124).
2. Whenever the Receive DS3/E3 Framer block transitions from the FAS Pattern Verification state to the In-frame state, within the E3 Framing Acquisition/Maintenance algorithm (per Figure 124).

Bit 1 - LOS (Change in LOS Condition) Interrupt Status

This Reset Upon Read bit will be set to "1", if the Receive DS3/E3 Framer block has detected a Change in the LOS Status condition, since the last time this register was read. This bit-field will be asserted under either of the following two conditions:

1. When the Receive DS3/E3 Framer block detects the occurrence of an LOS Condition (e.g., the occurrence of 32 consecutive spaces in the incoming E3 data stream), and

2. When the Receive DS3/E3 Framer block detects the end of an LOS Condition (e.g., when the Receive DS3/E3 Framer block detects a string 32 bits that does not contain a string of four consecutive "0's").

The local µP can determine the current state of the LOS condition by reading bit 4 of the Rx E3 Configuration and Status Register (Address = 0x11).

NOTE: *For more information in the LOS of Signal (LOS) Alarm, refer to* Section 5.3.2.7*.*

Bit 0 - AIS (Change in AIS Condition) Interrupt Status

This Reset Upon Read bit field will be set to "1", if the Receive DS3/E3 Framer block has detected a Change in the AIS condition, since the last time this register was read. This bit-field will be asserted under either of the following two conditions:

1. When the Receive DS3/E3 Framer block first detects an AIS Condition in the incoming E3 data stream.
2. When the Receive DS3/E3 Framer block has detected the end of an AIS Condition in the incoming E3 data stream.

The local µP can determine the current state of the AIS condition by reading bit 3 of the Rx E3 Configuration and Status Register (Address = 0x11).

NOTE: *For more information on the AIS Condition, refer to* Section 5.3.2.8*.*

2.3.4.6 *Receive E3 Interrupt Status Register 2 (E3, ITU-T G.751)*

RxE3 Interrupt Status Register 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Status	BIP-4 Error Interrupt Status	Framing Error Interrupt Status	Not Used
RO	RO	RO	RO	RUR	RUR	RUR	RO
0	0	0	0	1	0	1	0

Bit 3 - FERF (Change in FERF Condition) Interrupt Status

This Reset Upon Read bit will be set to '1' if the Receive DS3/E3 Framer block has detected a Change in the Rx FERF Condition, since the last time this register was read.

This bit-field will be asserted under either of the following two conditions.

1. When the Receive DS3/E3 Framer block first detects the occurrence of an Rx FERF Condition (e.g., when the FERF bit, within the last 3 or 5 consecutive E3 frames are set to "1").
2. When the Receive DS3/E3 Framer block detects the end of the Rx FERF Condition (e.g., when the FERF bit, within the last 3 or 5 consecutive E3 frames are set to "0").

NOTE: *For more information on the Rx FERF (Yellow Alarm) condition, refer to* Section 5.3.2.9*.*

Bit 2 - BIP-4 (Detection of BIP-4) Error Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the BIP-4 Error interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate the BIP-4 Error interrupt if it has concluded that it has received an errored E3 frame, from the Remote Terminal.

NOTE: *Please see* Section 5.3.6.2.7 *for a more detailed discussion of this interrupt.*

Bit 1 - Framing Error Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the Framing Byte Error interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer blockwill generate the Framing Error interrupt if it has detected an error in the FAS (or Framing Alignment), in an incoming E3 frame.

NOTE: Please see Section 5.3.6.2.8 for a more detailed discussion of this interrupt.

2.3.4.7 Receive E3 LAPD Control Register (E3, ITU-T G.751)

RxE3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	0	0

Bit 2 - RxLAPD Enable

This Read/Write bit-field allows the user to enable or disable the LAPD Receiver, for reception of incoming LAPD Message frames from the Remote LAPD Transmitter.

Writing a "1" to this bit-field enables the LAPD Receiver. Writing a "0" to this bit-field disables the LAPD Receiver.

Bit 1 - RxLAPD (Received LAPD Message) Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the Received LAPD Message frame interrupt. Setting this bit-field to "1" enables this interrupt. Setting this bit-field to "0" disables this interrupt.

NOTE: For more information on this interrupt, refer to Section 5.3.6.2.9.

Bit 0 - RxLAPD (Received LAPD Message) Interrupt Status

This Reset-upon-Read bit-field will be set to "1" if the Receipt of New LAPD Message frame interrupt has occurred since the last read of this register.

The Receive DS3/E3 Framer block will generate this Receipt of New LAPD Message frame interrupt when the LAPD Receiver has received a complete LAPD Message frame from the Remote LAPD Transmitter.

NOTE: Please see Section 5.3.6.2.9 for a more detailed discussion of this interrupt.

2.3.4.8 Receive E3 LAPD Status Register (E3, ITU-T G.751)

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxAbort	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 6 - RxAbort (Receive Abort Sequence)

This Read-Only bit-field indicates whether or not the LAPD Receiver has detected the occurrence of an Abort Sequence (e.g., a string of seven or more consecutive "1's") from the remote LAPD Transmitter. A "0" in this bit-field indicates that no Abort-Sequence has been detected. A "1" in this bit-field indicates that the Abort-Sequence has been detected.

NOTE: For more information on the LAPD Receiver, refer to Section 4.3.3.2.

Bits, 5 and 4 - RxLAPDType[1:0]

These two Read Only bit-fields combine to indicate the type of LAPD Message frame that has been received by the LAPD Receiver. The relationship between these two bit-fields and the LAPD Message Type follows:

RxLAPDType[1:0]		Message Type	Message length
Bit 5	Bit 4		
0	0	CL Path Identification	76 Bytes
0	1	Idle Signal Identification	76 Bytes
1	0	Test Signal Identification	76 Bytes
1	1	ITU-T Path Identification	82 Bytes

Bit 3 - RxCR (Command/Response) Type

This Read Only bit field indicates the value of the C/R (Command/Response) bit-field of the latest received LAPD Message.

Bit 2 - Rx FCS (Frame Check Sequence) Error

This Read-Only bit-field indicates whether or not the LAPD Receiver has detected a Frame Check Sequence (FCS) error in the most recently received LAPD Message Frame. A "0" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is correct. A "1" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is incorrect.

Note: *For more information on the LAPD Receiver, refer to* Section 4.3.3.2*.*

Bit 1 - End Of Message

This Read-Only bit-field indicates whether or not the LAPD Receiver has completed its reception of the latest incoming LAPD Message frame. The local µP can poll the progress of the LAPD Receiver by periodically reading this bit-field.

The LAPD Receiver will assert this read-only bit-field, when it has received a complete LAPD Message frame. This bit-field, along with the Receipt of New LAPD Message frame interrupt, serves to inform the local µP that the Receive LAPD Message buffer contains a new PMDL message that needs to be read and processed.

This bit-field is cleared (to "0") when the LAPD receiver starts receiving a new LAPD frame. (The EOM bit goes “Low” once a valid header is received.).

A "0" in this bit-field indicates that the LAPD Receiver is still receiving the latest message from the remote LAPD Transmitter. A "1" in this bit-field indicates that the LAPD Receiver has finished receiving the complete LAPD Message Frame.

Bit 0 - Flag Present

The LAPD Receiver will assert this read-only bit-field when it is currently detecting the Flag Sequence octet (0x7E) in the incoming LAPD channel (“N” bits of the E3 frame). The LAPD Receiver will negate this bit-field when it is no longer receiving the Flag Sequence octet in the incoming LAPD channel.

2.3.4.9 *Receive E3 Service Bits Register (E3, ITU-T G.751)*

RxE3 Service Bit Register (Address = 0x1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used						RxA	RxN
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 1 - RxA (A-Bit)

This Read-Only bit-field reflects the state of the A-Bit-field, within the most recently received E3 frame.

Bit 0 - RxN (N-Bit)

This Read-Only bit-field reflects the state of the N-Bit-field, within the most recently received E3 frame.

2.3.5 Transmit DS3 Configuration Registers

2.3.5.1 *Transmit DS3 Configuration Register*

Transmit DS3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx Yellow Alarm	Tx X Bits	Tx Idle	Tx AIS	Tx LOS	FERF on LOS	FERF on OOF	FERF on AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Tx Yellow Alarm

This Read/Write bit-field permits the user to command the Transmit DS3/E3 Framer block to transmit a Yellow Alarm (e.g., X bits are all "0") in the outbound DS3 data stream.

Writing a "0" to this bit-field disables this feature (the default condition). In this condition, the X-bits in the outbound DS3 frame, are internally generated (based upon receiver conditions).

Writing a "1" to this bit-field invokes this command. In this condition, the Transmit DS3/E3 Framer block will override the internally-generated X-bits and force all of the X-bits of each outbound DS3 frame to "0".

NOTES:

1. *For more information in this feature, refer to* Section 4.2.4.2.1.1.
2. *This bit-setting is ignored if Bits 3, 4 or 5 (within this register) are set to "1".*

Bit 6 - Tx X-Bit (Force X bits to "1")

This "Read/Write" bit-field permits the user to command the Transmit DS3/E3 Framer block to force all of the X-bits, in the outbound DS3 Frames, to "1".

Writing a "0" to this bit-field disables this feature (the default condition). In this case, the Transmit DS3/E3 Framer block will generate X-bits based upon the receive conditions.

Writing a "1" to this bit-field invokes this command. In this case, the Transmit DS3/E3 Framer block will overwrite the internally-generated X-bits and set them all to "1".

NOTES:

1. *For more information on this feature, refer to* Section 4.2.4.2.1.2.
2. *This bit-setting is ignored if Bits 3, 4, 5, or 7 (within this register) are set to "1".*

Bit 5 - Tx Idle (Pattern)

This Read/Write bit-field permits the user to command the Transmit DS3/E3 Framer block to transmit the Idle Condition pattern. If the user invokes this command, then the Transmit DS3/E3 Framer block will force the outbound DS3 Frames to have the following patterns.

- Valid M-bits, F-bits and P-bits
- The three CP-Bits (F-frame #3) are "0"
- The X-bits are set to "1"
- A repeating "1100..." pattern in written into the payload portion of the DS3 Frames.

Writing a "1" to this bit-field invokes this command. Writing a "0" allows the Transmit DS3/E3 Framer block to function normally (e.g., the Transmit DS3/E3 Framer block will transmit its payload and internally generated overhead bits).

NOTE: *For more information on this feature, refer to* Section 4.2.4.2.1.3.

NOTE: *This bit-setting is ignored if Bits 3 or 4 (within this register) are set to "1".*

Bit 4 - Tx AIS (Pattern)

This Read/Write bit-field permits the user to command the Transmit DS3/E3 Framer block to transmit an AIS pattern. If the user invokes this command, then the Transmit DS3/E3 Framer block will force the outbound DS3 frames to have the following patterns.

- Valid M-bits, F-bits, and P-bits
- All C-bits are set to '0'
- All X-bits are set to '1'
- A repeating '1010...' pattern is written into the payload of the DS3 Frames.

Writing a "1' to this bit-field invokes this command. Writing a "0" allows the Transmit DS3/E3 Framer block to function normally (e.g., the Transmit DS3/E3 Framer block will transmit its payload and internally generated overhead bits).

NOTE: *For more information on this feature, refer to* Section 4.2.4.2.1.4.

Bit 3 - Tx LOS (Loss of Signal)

This Read/Write bit-field permits the user to command the Transmit DS3/E3 Framer block to simulate an LOS Condition. If the user invokes this command, then the Transmit DS3/E3 Framer block will stop sending mark pulses out on the line and will transmit an all-zero pattern.

Writing a '0' to this bit-field disables (or shuts off) this feature, thereby allowing internally generated DS3 Frames to be generated and transmitted over the line.

Writing a '1' to this bit-field invokes this command, causing the Transmit DS3/E3 Framer block to generate an all '0' pattern.

NOTE: *For more information on this feature, refer to* Section 4.2.4.2.1.5.

Bit 2 - FERF on LOS

This Read/Write bit-field allows the user to configure the Transmit DS3/E3 Framer block to generate a Yellow Alarm if the Near-End Receive DS3/E3 Framer block (within the same channel) detects a LOS (Loss of Signal) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

NOTE: *For more information on this feature, refer to* Section 4.2.4.2.1.6.

Bit 1 - FERF on OOF

This Read/Write bit-field allows the user to configure the Transmit DS3/E3 Framer block to generate a Yellow Alarm if the Near-End Receive DS3/E3 Framer block (within the same channel) detects an OOF (Out-of-Frame) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

NOTE: *For more information on this feature, refer to* Section 4.2.4.2.1.7.

Bit 0 - FERF on AIS

This Read/Write bit-field allows the user to configure the Transmit DS3/E3 Framer block to generate a Yellow Alarm if the Near-End Receive DS3/E3 Framer block (within the same channel) detects an AIS (Alarm Indication Signal) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

NOTE: *For more information on this feature, refer to* Section 4.2.4.2.1.8.

2.3.5.2 *Transmit DS3 FEAC Configuration & Status Register*

Transmit DS3 FEAC Configuration & Status Register (Address = 0x31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			Tx FEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC GO	TxFEAC Busy
RO	RO	RO	R/W	RUR	R/W	R/W	RO
0	0	0	0	0	0	0	0

Bit 4 - Tx FEAC Interrupt Enable

This Read-Write bit-field permits the user to enable or disable the Transmit FEAC Interrupt.

Setting this bit-field to “0” disables this interrupt.

Conversely, setting this bit-field to “1” enables this interrupt.

Bit 3 - TxFEAC Interrupt Status

This Reset-upon-Read bit-field indicates whether or not the FEAC Message Transmission Complete interrupt has occurred since the last read of this register. This interrupt will occur once the Transmit FEAC Processor has finished its 10th transmission of the 16 bit FEAC Message (6 bit FEAC Code word + 10 framing bits). The purpose of this interrupt is to let the local µP know that the Transmit FEAC Processor has completed its transmission of its latest FEAC Message and is now ready to transmit another FEAC Message.

If this bit-field is "0", then the FEAC Message Transmission Complete interrupt has NOT occurred since the last read of this register.

If this bit-field is “1”, then the FEAC Message Transmission Complete interrupt has occurred since the last read of this register.

NOTE: *For more information on the Transmit FEAC Processor, refer to* Section 4.2.3.1.

Bit 2 - TxFEAC Enable

This Read/Write bit-field allows the user to enable or disable the Transmit FEAC Processor. The Transmit FEAC Processor will NOT function until it has been enabled.

Writing a "0" to this bit-field disables the Transmit FEAC Processor. Writing a "1" to this bit-field enables the Transmit FEAC Processor.

Bit 1 - TxFEAC Go

This bit-field allows the user to invoke the Transmit FEAC Message command. Once this command has been invoked, the Transmit FEAC Processor will do the following:

- Encapsulate the 6 bit FEAC code word, from the Tx DS3 FEAC Register (Address = 0x32) into a 16 bit FEAC Message
- Serially transmit this 16-bit FEAC Message to the far-end receiver via the outbound DS3 data-stream, recursively. After the 10^{th} transmission, generate the TxFEAC complete interrupt and continue transmitting.

NOTE: *For more information on the Transmit FEAC Processor, refer to* Section 4.2.3.1.

Bit 0 - TxFEAC Busy

This Read-Only bit-field allows the local µP to poll and determine if the Transmit FEAC Processor has completed its 10th transmission of the 16-bit FEAC Message. This bit-field will contain a "1", if the Transmit FEAC Processor is still transmitting the FEAC Message. This bit-field will toggle to "0", once the Transmit FEAC Processor has completed its 10th transmission of the FEAC Message.

NOTE: *For more information on the Transmit FEAC Processor, refer to* Section 4.2.3.1.

2.3.5.3 *Transmit DS3 FEAC Register*

TxDS3 FEAC RegisTer (Address = 0x32)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TxFEAC[5:0]						Not Used
RO	R/W	R/W	R/W	R/W	R/W	R/W	RO
0	1	1	1	1	1	1	0

This register contains a six (6) bit read/write field that allows the user to write in the six-bit FEAC code word, that is desired to be transmitted to the Far End Receive FEAC Processor, via the outgoing DS3 data stream. The Transmit FEAC Processor will encapsulate this six-bit code into a 16-bit FEAC message, and will proceed to transmit this message to the Remote Receiver via the FEAC bit-field within each out-going DS3 frame.

NOTE: *For more information on the operation of the Transmit FEAC Processor, refer to* Section 4.2.3.1.

2.3.5.4 *Transmit DS3 LAPD Configuration Register*

TxDS3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

Bit 3 - Auto Retransmit

This Read/Write bit-field allows the user to configure the LAPD Transmitter to either transmit the LAPD Message frame only once or, repeatedly at one-second intervals.

Writing a "0" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame once. Afterwards, the LAPD Transmitter will halt transmission, until it is commanded to transmit another LAPD Message frame.

Writing a "1" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame repeatedly at One-Second intervals. In this configuration, the LAPD Transmitter will repeat its transmission of the LAPD Message frame until it has been disabled.

Bit 1 - TxLAPD Message Length Select

This Read/Write bit-field permits the user to select the length of the outbound LAPD Message frame.

Setting this bit-field to "0" configures the outbound LAPD Message frame to be 76 bytes in length. Setting this bit-field to “1” configures the outbound LAPD Message frame to be 82 bytes in length.

NOTE: *This should match with the message type of the LAPD message to be sent. (See* Table 21 *.)*

Bit 0 - TxLAPD Enable

This Read/Write bit-field allows the user to enable or disable the LAPD Transmitter. The LAPD Transmitter must be enabled before it can be commanded to transmit a LAPD Message frame (containing a PMDL message) via the outbound DS3 frames, to the Far-End Terminal.

Writing a “0" disables the LAPD Transmitter (default condition). Writing a "1" enables the LAPD Transmitter.

NOTE: *For information on the LAPD Transmitter, refer to* Section 4.2.3.2.

2.3.5.5 *Transmit DS3 LAPD Status and Interrupt Register*

TxDS3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	0

Bit 3 - TxDL Start

This Read/Write bit-field allows the user to invoke the Transmit LAPD Message command. Once the user invokes this command, the LAPD Transmitter will do the following:

- Read in the PMDL Header and Message from the Transmit LAPD Message Buffer. (80 or 86 bytes)
- Compute the frame check sequence word (16 bit value)
- Insert the Frame Check Sequence value into the 2 octet slot after the payload section of the Message.
- Perform zero stuffing between 0x7E flag bytes. (81 or 87 bytes)
- Proceed to transmit the LAPD Message Frame to the far end terminal via the outgoing DS3 frames.

Writing a "1" to this bit-field start the transmission of the LAPD Message Frame, via the LAPD Transmitter.

NOTE: *For more information on the LAPD Transmitter, refer to* Section 4.2.3.2.

Bit 2 - TxDL Busy

This Read-Only bit-field allows the local µP to poll and determine if the LAPD Transmitter has completed its transmission of the LAPD Message frame. This bit-field will contain a "1", if the LAPD Transmitter is still transmitting the LAPD Message frame to the far-end terminal. This bit-field will toggle to "0", once the LAPD Transmitter has completed its transmission of the LAPD Message frame.

NOTE: *For more information on the LAPD Transmitter, refer to* Section 4.2.3.2.

Bit 1 - TxLAPD Interrupt Enable

This Read/Write bit-field allows the user to enable or disable the LAPD Message Frame Transmission Complete interrupt.

Writing a "0" to this bit-field disables this interrupt. Writing a "1" to this bit-field enables this interrupt.

Bit 0 - TxLAPD Interrupt Status

This Reset-upon-Read bit-field indicates whether or not the LAPD Message frame Transmission Complete interrupt has occurred since the last read of this register. The purpose of this interrupt is to let the local µP know that the LAPD Transmitter has completed its transmission of the LAPD Message frame (containing the latest PMDL message) and is now ready to transmit another LAPD Message frame.

A "0" in this bit-field indicates that the LAPD Message frame Transmission Complete interrupt has not occurred since the read of this register. A "1" in this bit-field indicates that this interrupt has occurred since the last read of this register.

NOTE: *For more information on the TxLAPD Interrupt, refer to* Section 4.2.3.2.

2.3.5.6 *Transmit DS3 M-Bit Mask Register*

TxDS3 M-Bit Mask Register (Address = 0x35)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFEBEDat[2:0]			FEBE Reg Enable	Tx Error P-Bit	MBit Mask[2]	MBit Mask[1]	MBit Mask[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - 5: TxFEBEDat[2:0]

These three (3) read/write bit-fields, along with Bit 4 of this register, allows the user to configure and transmit his/her choice for the three (3) FEBE (Far-End Block Error) bits in each outgoing DS3 Frame. The user will write his/her value for the FEBE bits into these bit-fields. The Transmit DS3 Framer block will insert these values into the FEBE bit-fields of each outgoing DS3 Frame, once the user has written a "1" to Bit 4 (FEBE Register Enable).

NOTE: *For more information on this feature, refer to* Section 4.2.4.2.1.9*.*

Bit 4 - FEBE Register Enable

This Read/Write bit-field permits the user to configure the Transmit DS3 Framer to insert the contents of TxFEBEDat[2:0] into the FEBE bit-fields each outbound DS3 Frame.

Writing a "0" to this bit-field disables this feature (e.g., the Transmit DS3 Framer block will transmit the internally generated FEBE bits). Writing a "1" to this bit-field enables this features (e.g., the internally generated FEBE bits are overwritten by the contents of the TxFEBEDat[2:0] bit-field).

NOTE: *For more information on this feature, refer to* Section 4.2.4.2.1.9*.*

Bit 3 - Transmit Erred P-Bit

This Read/Write bit-field permits the user to insert errors into the P-bits within the outbound DS3 frames (via the Transmit DS3/E3 Framer block). If the user enables this feature, then the Transmit DS3/E3 Framer block will proceed to invert each and every P-bit, from its computed value, prior to transmission to the Remote Terminal.

Writing a "0" to this bit-field (the default condition) disables this feature (e.g., the correct P-bits are sent). Writing a "1" to this bit-field enables this feature (e.g., the incorrect P-bits are sent).

NOTE: *For more information on this feature, refer to* Section 4.2.4.2.2*.*

Bit 2 - 0 M-Bit Mask[2:0]

These Read/Write bit-fields permit the user to insert errors in the M-bits for Test and Diagnostic purposes. The Transmit DS3/E3 Framer block automatically performs an XOR operation on the actual contents of the M-bit fields to these register bit-fields. Therefore, for every '1' that exists in these bit-fields, will result in a change of state of the corresponding M-bit, prior to being transmitted to the Remote Terminal Equipment.

If the Transmit DS3/E3 Framer block is to be operated in the normal mode (e.g., when no errors are being injected into the M-bit fields of the outbound DS3 Frame), then these bit-fields must be all “0’s”.

2.3.5.7 *Transmit DS3 F-Bit Mask Register 1*

TxDS3 F-Bit Mask Register 1 (Address = 0x36)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FBit Mask[27]	FBit Mask[26]	FBit Mask[25]	FBit Mask[24]
RO	RO	RO	RO	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 3 - 0 F-Bit Mask[27:24]

These Read/Write bit-fields permit the user to insert errors into the first four F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3/E3 Framer block automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Remote Receive DS3/E3 Framer.

If the Transmit DS3/E3 Framer block is to be operated in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then all of these bit-fields must be "0's".

2.3.5.8 *Transmit DS3 F-Bit Mask Register 2*

TxDS3 F-Bit Mask Register 2 (Address = 0x37)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FBit Mask[23]	FBit Mask[22]	FBit Mask[21]	FBit Mask[20]	FBit Mask[19]	FBit Mask[18]	FBit Mask[17]	FBit Mask[16]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 F-Bit Mask[23:16]

These Read/Write bit-fields permit the user to insert errors into the fifth through twelfth F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3/E3 Framer block automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Remote Terminal Equipment.

If the Transmit DS3/E3 Framer block is to be operated in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then all of these bit-fields must be "0's".

2.3.5.9 *Transmit F-Bit Mask Register 3*

TxDS3 F-Bit Mask Register 3 (Address = 0x38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FBit Mask[15]	FBit Mask[14]	FBit Mask[13]	FBit Mask[12]	FBit Mask[11]	FBit Mask[10]	FBit Mask[9]	FBit Mask[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 F-Bit Mask[15:8]

These Read/Write bit-fields permit the user to insert errors into the thirteenth through twentieth F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3/E3 Framer block automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that

exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Remote Terminal Equipment.

If the Transmit DS3/E3 Framer block is to be operated in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then all of these bit-fields must be "0's".

2.3.5.10 *Transmit F-Bit Mask Register 4*

TxDS3 F-Bit Mask Register 4 (Address = 0x39)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FBit Mask[7]	FBit Mask[6]	FBit Mask[5]	FBit Mask[4]	FBit Mask[3]	FBit Mask[2]	FBit Mask[1]	FBit Mask[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 F-Bit Mask[7:0]

These Read/Write bit-fields allow the user to insert errors into the last eight F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3/E3 Framer block automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Remote Terminal Equipment.

If the Transmit DS3/E3 Framer block is to be operated in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then all of these bit-fields must be "0's".

2.3.6 Transmit E3 (ITU-T G.832) Configuration Registers

2.3.6.1 *Transmit E3 Configuration Register (E3, ITU-T G.832)*

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			TxDL in NR	Not Used	TxAIS Enable	TxLOS Enable	TxMARx
RO	RO	RO	R/W	RO	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 4 - DLinNR

This Read/Write bit-field permits the user to specify whether the LAPD Transmitter should insert the outbound LAPD Message frame octets into the NR byte-field, or in the GC-byte-field, within each outbound E3 frame.

Writing a "1" configures the LAPD Transmitter to insert the octets of the outbound LAPD Message frame into the NR byte-field, within each outbound E3 frame. Writing in "0" configures the LAPD Transmitter to insert the octets of the outbound LAPD Message frame into the GC byte-field, within each outbound E3 frame.

Bit 2 - TxAIS Enable

This Read/Write bit-field allows the user to command the Transmit E3 Framer to transmit an AIS pattern, upon demand.

Writing a "0" to this bit-field allows the Transmit DS3/E3 Framer block to transmit internally generated data (e.g., the ITU-T G.832 compatible E3 frames with the E3 payload data) to the Remote Terminal. Writing a "1" to this bit-field causes the Transmit DS3/E3 Framer block to transmit an all "1's" pattern to the Remote Terminal.

NOTE: *If the Transmit DS3/E3 Framer block is transmitting an AIS pattern to the Remote Terminal, then it is not transmitting any E3 frames. Consequently, if this command is invoked, the Remote Terminal will experience an OOF (Out of Frame) condition.*

Bit 1 - TxLOS Enable

This Read/Write bit-field allows the user to command the Transmit E3 Framer to transmit an LOS pattern, upon demand.

Writing a "0" to this bit-field allows the Transmit E3 Framer to transmit internally generated data (e.g., the ITU-T G.832 compatible E3 frames with ATM cell data) to the Remote Terminal. Writing a "1" to this bit-field causes the Transmit DS3/E3 Framer block to transmit an "All 0's" pattern to the Remote Terminal.

NOTE: *If the Transmit DS3/E3 Framer block is transmitting an LOS pattern to the RemoteTerminal, then it is not transmitting any E3 frames. Consequently, the Remote Terminal will experience an LOS (Loss of Signal) and OOF (Out of Frame) condition.*

Bit 0 - MARx (FERF and FEBE bit-field Loop-back)

This Read/Write bit-field allows the user to specify whether the value of the FERF and FEBE bit-fields, in the outbound E3 frames, should be based upon Receive DS3/E3 Framer conditions or upon the content of the Tx MA Byte register (Address = 0x36).

FERF and FEBE values are based upon Receive E3 Framer Conditions

If the user selects Receive DS3/E3 Framer conditions, then the Transmit DS3/E3 Framer block will set and clear the FERF and FEBE bit-fields in response to the following conditions.

a. FERF Bit-field

If the Receive DS3/E3 Framer block (in the same channel) is currently experiencing an LOS, AIS, or LOF condition, then the Transmit DS3/E3 Framer block will set the FERF bit-field (in the outbound E3 frame) to "1". Conversely, if the Receive DS3/E3 Framer block is not experiencing any of these conditions, then the Transmit E3 Framer will set the FERF bit-field (in the outbound E3 frame) to "0".

b. FEBE bit-field

If the Receive DS3/E3 Framer block detects a BIP-8 error in the incoming E3 frame, then the Transmit DS3/E3 Framer block will set the FEBE bit-field (in the outbound E3 frame) to "1". Conversely, if the Receive DS3/E3 Framer block does not detect a BIP-8 error in the incoming E3 frame, then the Transmit DS3/E3 Framer block will set the FEBE bit-field (in the E3 outbound E3 frame) to "0".

FEBE and FERF values are based upon the contents of the Tx MA Byte register

If the user selects the contents of the Tx MA Byte register, then whatever value has been written into bit 7 (FERF), within the Tx MA Byte register (Address = 2Ah), will be the value of the FERF bit-field, in the outbound E3 frame. Likewise, whatever value has been written into Bit 6 (FEBE) within the Tx MA Byte register, will be the value of the FEBE bit-field, in the outbound E3 frame.

Writing a "1" into Bit 0 (MAx) within the Tx E3 Configuration register configures the Transmit DS3/E3 Framer block to set the FERF and FEBE bit-fields (in the outbound E3 frames) to values based upon Receive E3 Framer conditions. Writing a "0" into this bit-field configures the Transmit DS3/E3 Framer block to set the FEBE and FEBE bit-fields (in the outbound E3 frames) to the values written into bit-fields 6 and 7 within the Tx MA Byte register.

2.3.6.2 *Transmit E3 LAPD Configuration Register (E3, ITU-T G.832)*

TxE3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	1	0	0	0

Bit 3 - Auto Retransmit

This Read/Write bit-field permits the user to configure the LAPD Transmitter to either transmit the LAPD Message frame only once, or repeatedly at one-second intervals.

Writing a "0" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame once. Afterwards, the LAPD Transmitter will halt transmission, until it has commanded to transmit another LAPD Message frame.

Writing a "1" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame repeatedly at One-Second intervals. In this configuration, the LAPD Transmitter will repeat its transmission of the LAPD Message frame until it has been disabled.

Bit 1 - TxLAPD Message Length Select

This Read/Write bit-field permits the user to select the length of the outbound LAPD Message frame.

Setting this bit-field to "0" configures the outbound LAPD Message frame to be 76 bytes in length. Setting this bit-field to "1" configures the outbound LAPD Message frame to be 82 bytes in length.

NOTE: *This should match with the message type of the LAPD message to be sent. (See* Table 21 *.)*

Bit 0 - TxLAPD Enable

This Read/Write bit-field permits the user to enable or disable the LAPD Transmitter. The LAPD Transmitter must be enabled before it can be commanded to transmit a LAPD Message frame (containing a PMDL message) via the outbound E3 frames, to the Remote Terminal.

Writing a "0" disables the LAPD Transmitter (default condition). Writing a "1" enables the LAPD Transmitter.

NOTE: *For information on the LAPD Transmitter, refer to* Section 6.2.3.1.

2.3.6.3 *Transmit E3 LAPD Status and Interrupt Register (E3, ITU-T G.832)*

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	0

Bit 3 - TxDL Start

This Read/Write bit-field permits the user to command the LAPD Transmitter to do the following.

- Read in the PMDL Header and Message from the Transmit LAPD Message Buffer. (80 or 86 bytes)
- Compute the frame check sequence word (16 bit value)
- Insert the Frame Check Sequence value into the 2 octet slot after the payload section of the Message.
- Perform zero stuffing between 0x7E flag bytes. (81 or 87 bytes)

NOTE: *Zero Stuffing: search for a string of five (5) consecutive "1's" insert (or stuff) a "0" immediately following any string of 5 consecutive "1's".*

- Proceed to transmit the LAPD Message Frame to the far end terminal via the outgoing DS3 frames.
- Fragment the resulting LAPD Message frame into octets.
- Insert these octets into either the GC byte-field or the NR byte-field (depending upon the user's selection) into each outbound E3 frame.

A "0" to "1" transition, in this bit-field commands the LAPD Transmitter to initiate the above-mentioned procedure.

NOTE: *Once the user has commanded the LAPD Transmitter to start transmission, the LAPD Transmitter will repeat the above-mentioned process once each second and will insert flag sequence octets into the outbound LAPD channel, during the idle periods between transmissions.*

Bit 2 - TxDL Busy

This Read-Only bit-field permits the user to poll or monitor the status of the LAPD Transmitter to see if it has completed its transmission of the LAPD Message frame. The LAPD Transmitter will set this bit-field to "1", while it is in the process of transmitting the LAPD Message frame. However, the LAPD Transmitter will clear this bit-field to "0" once it has completed its transmission of the LAPD Message frame.

Bit 1 - TxLAPD Interrupt Enable

This Read/Write bit-field permits the user to enable or disable the LAPD Message frame Transmission Complete interrupt.

Writing a "0" to this bit-field disables this interrupt. Writing a "1" to this bit-field enables this interrupt.

Bit 0 - TxLAPD Interrupt Status

This Reset-upon-Read bit-field permits the user to determine if the LAPD Message Frame Transmission Complete interrupt has occurred since the last read of this register. If this bit-field contains a "1" then the LAPD Message Frame Transmission Complete interrupt has occurred since the last read of this register. Conversely, if this bit-field contains a "0" then it has not.

2.3.6.4 *Transmit E3 GC Byte Register (E3, ITU-T G.832)*

TxE3 GC Byte Register (Address = 0x35)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxGC[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field permits the user to specify the contents of the GC byte-field in each outbound E3 frame.

NOTE: *The contents of this register is ignored, if the LAPD Transmitter is enabled and has been configured to insert the comprising octets of an outbound LAPD Message frame into the GC byte-field of each outbound E3 frame (e.g., if DLinNR = "0").*

2.3.6.5 *Transmit E3 MA Byte Register (E3, ITU-T G.832)*

The bit-format of the TxE3 MA Byte register depends upon whether the channel has been configured to support the November 1995 or the October 1998 revision of the ITU-T G.832 framing format for E3.

The bit-format of the TxE3 MA Byte register, for each of these cases is discussed below.

2.3.6.5.1 The November 1995 Revision

If the channel has been configured to support the November 1995 revision of the ITU-T G.832 Framing Format for E3, then the bit-format of the TxE3 MA Byte register is as presented below.

TxE3 MA Byte Register (Address = 0x36)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit MA Byte							
FERF	FEBE	Payload Type			Payload Dependent		Timing Marker
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	0	0	0

This Read/Write byte-fields permits the user to specify the contents of the MA byte-field in each outbound E3 frame.

NOTE: *The values written into bit-fields 6 (FEBE) and 7 (FERF) are inserted into outbound E3 frames, only if bit-field 0 (TxMARx) within the Tx E3 Configuration Register (Address = 0x30) is set to "0". Otherwise, the Transmit DS3/E3 Framer block will set the FERF and FEBE values, within each outbound E3 frame, to values based upon Receive DS3/E3 Framer block conditions.*

2.3.6.5.2 The October 1998 Revision

If the channel has been configured to support the October 1998 revision of the ITU-T G.832 framing format for E3; then the bit-format of the TxE3 MA Byte register is as presented below.

TxE3 MA Byte Register (Address = 0x36)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit MA Byte							
FERF	FEBE	Payload Type			MFI[1:0]		SSM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	0	0	0

This Read/Write byte-fields permits the user to specify the contents of the MA byte-field in each outbound E3 frame.

NOTE: *The values written into bit-fields 6 (FEBE) and 7 (FERF) are inserted into outbound E3 frames, only if bit-field 0 (TxMARx) within the Tx E3 Configuration Register (Address = 0x30) is set to "0". Otherwise, the Transmit DS3/E3 Framer block will set the FERF and FEBE values, within each outbound E3 frame, to values based upon Receive DS3/E3 Framer block conditions.*

2.3.6.6 *Transmit E3 NR Byte Register (E3, ITU-T G.832)*

TxE3 NR Byte Register (Address = 0x37)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxNR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field permits the user to specify the contents of the NR byte-field in each outbound E3 frame.

NOTE: *The contents of this register is ignored, if the LAPD Transmitter is enabled and has been configured to insert the comprising octets of an outbound LAPD Message frame into the NR byte-field of each outbound E3 frame (e.g., if DLinNR = "1").*

2.3.6.7 *Transmit E3 TTB-0 Register (E3, ITU-T G.832)*

TxE3 TTB-0 Register (Address = 0x38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-0[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-1 through Tx TTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the first of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block

will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

This particular byte-field should contain the pattern "[1, C6, C5, C4, C3, C2, C1, C0]" where the bits C6 through C0 are the results of a CRC-7 calculation over the previous 16-byte frame.

NOTE: *The XRT72L50 Framer IC will not compute this CRC-7 value. It is up to the user's hardware and/or software to compute this value, prior to writing it into this register.*

2.3.6.8 *Transmit E3 TTB-1 Register (E3, ITU-T G.832)*

TxE3 TTB-1 Register (Address = 0x39)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-1[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the TxTTB-0 and TxTTB-2 through TxTTB-15 register permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the second of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-2 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.9 *Transmit E3 TTB-2 Register (E3, ITU-T G.832)*

TxE3 TTB-2 Register (Address = 0x3A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-2[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the TxTTB-0, TxTTB-1 and TxTTB-3 through TxTTB-15 register permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the third of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1, and Tx TTB-3 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.10 *Transmit E3 TTB-3 Register (E3, ITU-T G.832)*

TxE3 TTB-3 Register (Address = 0x3B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-3[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the TxTTB-0 through TxTTB-2 and TxTTB-4 through TxTTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the fourth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1, Tx TTB-2 and Tx TTB-4 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.11 *Transmit E3 TTB-4 Register (E3, ITU-T G.832)*

TxE3 TTB-4 Register (Address = 0x3C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-4[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the TxTTB-0 through TxTTB-3 and TxTTB-5 through TxTTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the fifth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-3 and Tx TTB-5 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.12 *Transmit E3 TTB-5 Register (E3, ITU-T G.832)*

TxE3 TTB-5 Register (Address = 0x3D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-5[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-4 and Tx TTB-6 through Tx TTB-15 registers allows a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16

registers, and insert them into the TR byte of the outbound E3 frame. In the sixth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-4 and Tx TTB-6 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.13 *Transmit E3 TTB-6 Register (E3, ITU-T G.832)*

TxE3 TTB-6 Register (Address = 0x3E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-6[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-5 and Tx TTB-7 through Tx TTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the seventh of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-5 and Tx TTB-7 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.14 *Transmit E3 TTB-7 Register (E3, ITU-T G.832)*

TxE3 TTB-7 Register (Address = 0x3F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-7[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-6 and Tx TTB-8 through Tx TTB-15 registers allows a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the eighth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-6 and Tx TTB-8 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.15 *Transmit E3 TTB-8 Register (E3, ITU-T G.832)*

TxE3 TTB-8 Register (Address = 0x40)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-8[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-7 and Tx TTB-9 through Tx TTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the ninth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-7 and Tx TTB-9 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.16 *Transmit E3 TTB-9 Register (E3, ITU-T G.832)*

TxE3 TTB-9 Register (Address = 0x41)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-9[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-8 and Tx TTB-10 through Tx TTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the tenth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-8 and Tx TTB-10 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.17 *Transmit E3 TTB-10 Register (E3, ITU-T G.832)*

TxE3 TTB-10 Register (Address = 0x42)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-10[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-9 and Tx TTB-11 through Tx TTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16

registers, and insert them into the TR byte of the outbound E3 frame. In the eleventh of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-9 and Tx TTB-11 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.18 *Transmit E3 TTB-11 Register (E3, ITU-T G.832)*

TxE3 TTB-11 Register (Address = 0x43)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-11[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-10 and Tx TTB-12 through Tx TTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the twelfth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-10 and Tx TTB-12 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.19 *Transmit E3 TTB-12 Register (E3, ITU-T G.832)*

TxE3 TTB-12 Register (Address = 0x44)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-12[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-11 and Tx TTB-13 through Tx TTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the thirteenth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-11 and Tx TTB-13 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.20 *Transmit E3 TTB-13 Register (E3, ITU-T G.832)*

TxE3 TTB-13 Register (Address = 0x45)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-13[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-12, Tx-TTB-14, and Tx TTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the fourteenth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-12, Tx TTB-14 and Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.21 *Transmit E3 TTB-14 Register (E3, ITU-T G.832)*

TxE3 TTB-14 Register (Address = 0x46)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-14[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-13 and Tx TTB-15 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into the TR byte of the outbound E3 frame. In the fifteenth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-13 and Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.22 *Transmit E3 TTB-15 Register (E3, ITU-T G.832)*

TxE3 TTB-15 Register (Address = 0x47)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB-15[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write byte-field, along with the Tx TTB-0 through Tx TTB-14 registers permit a user to define a Trail Access Point Identifier sequence of bytes, that will be transmitted to the Remote Terminal. The Remote Receiving Terminal will use this sequence of bytes to verify that it is connected to the proper Transmitting Terminal. The Transmit DS3/E3 Framer block will take the contents of these 16 registers, and insert them into

the TR byte of the outbound E3 frame. In the sixteenth of a set of 16 E3 Frames, the Transmit DS3/E3 Framer block will read in the contents of this register, and insert it into the TR byte-field, within the very next outbound E3 frame.

The contents of this register, along with Tx TTB-1 through Tx TTB-15 are used to transmit 15 ASCII characters required for the E.164 numbering format.

2.3.6.23 *Transmit E3 FA1 Byte Error Mask Register (E3, ITU-T G.832)*

TxE3 FA1 Error Mask Register (Address = 0x48)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFA1_Error_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write bit-field permits the user to insert errors into the Framing Alignment octet, FA1 of each outbound E3 frame. The user may wish to do this for equipment testing purposes. Prior to transmission, the Transmit DS3/E3 Framer block reads in the FA1 byte, and performs an XOR operation with it and the contents of this register. The results of this operation are written back into the FA1 octet position, in each outbound E3 frame. Consequently, to insure errors are not injected into the FA1 octet of the outbound E3 frames, the contents of this register must be set to all “0’s” (the default value).

2.3.6.24 *Transmit E3 FA2 Byte Error Mask Register (E3, ITU-T G.832)*

TxE3 FA2 Error Mask Register (Address = 0x49)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFA2_Error_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write bit-field permits the user to insert errors into the Framing Alignment octet, FA2 of each outbound E3 frame. The user may wish to do this for equipment testing purposes. Prior to transmission, the Transmit DS3/E3 Framer block reads in the FA2 byte, and performs an XOR operation with it and the contents of this register. The results of this operation are written back into the FA2 octet position, in each outbound E3 frame. Consequently, to insure errors are not injected into the FA2 octet of the outbound E3 frames, the contents of this register must be set to all "0’s" (the default value).

2.3.6.25 *Transmit E3 BIP-8 Error Mask Register (E3, ITU-T G.832)*

TxE3 BIP-8 Error Mask Register (Address = 0x4A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxBIP-8_Error_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This Read/Write bit-field permits the user to insert errors into EM (Error Monitor) octet of each outbound E3 frame. The user may wish to do this for equipment testing purposes. Prior to transmission, the Transmit DS3/E3 Framer block reads in the EM byte, and performs an XOR operation with it and the contents of this register. The results of this operation are written back into the EM octet position, in each outbound E3 frame.

Consequently, to insure errors are not injected into the EM octet of the outbound E3 frames, the contents of this register must be set to all "0's" (the default value).

2.3.6.26 *TXE3 SSM REGISTER - G.832*

TxE3 SSM Register - G.832 (Direct Address = 0x4B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxSSM Enable	Unused			TxSSM[3:0]			
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Transmit SSM Enable

This Read/Write bit-field is used to configure the Frame Transmitter block to operate in either the Old ITU-T G.832 Framing format or in the New ITU-T G.832 Framing format.

"0" - Configures the Frame Transmitter block to support the Pre October 1998 version of the E3, ITU-T G.832 framing format.

"1" - Configures the Frame Transmitter block to support the October 1998 version of the E3, ITU-T G.832 framing format.

Bits [3:0] - Transmit Synchronization Status Message[3:0]

These Read/Write bit-fields are used to exercise software control over the contents of the SSM bits within the MA byte of the outbound E3 data-stream.

NOTE: *These bit-fields are only active if Bit 7 (TxSSM Enable) of this register is set to "1".*

2.3.7 Transmit E3 Framer Configuration Registers (ITU-T G.751)

2.3.7.1 *Transmit E3 Configuration Register (ITU-T G.751)*

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx BIP-4 Enable	TxASourceSel[1:0]		TxNSourceSel[1:0]		Tx AIS Enable	Tx LOS Enable	Tx FAS Source Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - TxBIP-4 Enable

This Read/Write bit-field permits the user to configure the Transmit Section of the Channel, to compute an insert the BIP-4 value into each outbound E3 frame.

Setting this bit-field to "0", configures the Transmit Section of the Channel to NOT compute and insert the BIP-4 value into each outbound E3 frame. Instead these four bits will contain data that has been input via the Input Interface.

Setting this bit-field to "1", configures the Transmit Section of the Channel to compute and insert the BIP-4 value into each outbound E3 frame.

NOTE: *For more information on these BIP-4 Calculations, refer to* Section 5.2.4.2.2.

Bit 6, 5, TxASourceSel[1:0]

These two Read/Write bit-fields combine to specify the source of the A-Bit, within each outbound E3 frame. The relationship between these two bit-fields and the resulting source of the A-Bit is tabulated below.

TXASOURCESEL[1:0]	SOURCE OF A-BIT
00	TxE3 Service Bits Register (Address = 0x35)
01	Transmit Overhead Data Input Interface
10	Transmit Payload Data Input Interface
11	Functions as a FEBE (Far-End-Block Error) bit-field. This bit-field is set to "0", if the Near-End Receive Section (within this chip) detects no BIP-4 Errors within the incoming E3 frames. This bit-field is set to "1", if the Near-End Receive Section (within this chip) detects a BIP-4 Error within the incoming E3 frame.

NOTE: *For more information on the A-Bit, within the ITU-T G.751 frame, refer to* Section 5.1.1.1.

Bits 4, 3, TxNSourceSel[1:0]

These two Read/Write bit-fields combine to specify the source of the N-Bit, within each outbound E3 frame. The relationship between these two bit-fields and the resulting source of the N-Bit is tabulated below.

TXNSOURCESEL[1:0]	SOURCE OF N-BIT
00	TxE3 Service Bits Register (Address = 0x35)
01	Transmit Overhead Data Input Interface
10	Transmit LAPD Controller
11	Transmit Payload Data Input Interface.

NOTE: *For more information on the N-Bit, within the ITU-T G.751 frame, refer to* Section 5.1.1.2.

Bit 2 - TxAIS Enable

This Read/Write bit-field permits the user to configure the Transmit Section of the Framer IC to transmit an AIS pattern to the remote terminal

Setting this bit-field to "0" configures the Transmit Section (of the chip) to transmit data in a normal manner (e.g., as received via the Input Interface).

Setting this bit-field to "1" configures the Transmit Section (of the chip) to transmit an "All Ones" pattern (e.g., an AIS pattern) to the remote terminal.

NOTE: *For more information on the AIS pattern, refer to* Section 5.2.4.2.1.1.

Bit 1 - TxLOS Enable

This Read/Write bit-field permits the user to configure the Transmit Section of the Framer IC to transmit an LOS (e.g., All Zeros) pattern to the remote terminal

Setting this bit-field to "0" configures the Transmit Section (of the chip) to transmit data in a normal manner (e.g., as received via the Input Interface).

Setting this bit-field to "1" configures the Transmit Section (of the chip) to transmit an "All Zeros" pattern (e.g., an LOS pattern) to the remote terminal.

NOTE: *For more information on the LOS pattern, refer to* Section 5.2.4.2.1.2.

Bit 0 - TxFAS Source Select

This Read/Write bit-field permits the user to configure the Transmit Section of the Channel to either:

a. Internally generate the FAS (Framing Alignment Signal) pattern, within the outbound E3 frames, or to

b. use the Input Interface as the source for the FAS pattern.

Setting this bit-field to "0" configures the Transmit Section of the Channel to internally generate the FAS pattern, for each outbound E3 frame.

Setting this bit-field to "1" configures the Transmit Section of the Channel to use the Input Interface as the source for the FAS pattern.

NOTE: *For more information on the FAS pattern, refer to* Section 5.1.

2.3.7.2 *Transmit E3 LAPD Configuration Register (ITU-T G.751)*

TxE3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				Auto Retrans-mit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	1	0	0	0

Bit 3 - Auto Retransmit

This Read/Write bit-field permits the user to configure the LAPD Transmitter to either transmit the LAPD Message frame only once, or repeatedly at one-second intervals.

Writing a "0" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame once. Afterwards, the LAPD Transmitter will halt transmission, until it has commanded to transmit another LAPD Message frame.

Writing a "1" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame repeatedly at One-Second intervals. In this configuration, the LAPD Transmitter will repeat its transmission of the LAPD Message frame until it has been disabled.

Bit 1 - TxLAPD Message Length Select

This Read/Write bit-field permits the user to select the length of the outbound LAPD Message frame.

Setting this bit-field to "0" configures the outbound LAPD Message frame to be 76 bytes in length. Setting this bit-field to "1" configures the outbound LAPD Message frame to be 82 bytes in length.

NOTE: *This should match with the message type of the LAPD message to be sent. (See* Table 21 *.)*

Bit 0 - TxLAPD Enable

This Read/Write bit-field permits the user to enable or disable the LAPD Transmitter. The LAPD Transmitter must be enabled before it can be commanded to transmit a LAPD Message frame (containing a PMDL message) via the outbound E3 frames, to the Remote Terminal.

Writing a "0" disables the LAPD Transmitter (default condition). Writing a "1" enables the LAPD Transmitter.

NOTE: *For information on the LAPD Transmitter, refer to* Section 5.2.3.

2.3.7.3 *Transmit E3 LAPD Status and Interrupt Register (ITU-T G.751)*

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TXDL Start	TXDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	0

Bit 3 - TxDL Start

This Read/Write bit-field permits the user to command the LAPD Transmitter to do the following.

- Read in the PMDL Header and Message from the Transmit LAPD Message Buffer. (80 or 86 bytes)

- Compute the frame check sequence word (16 bit value)
- Insert the Frame Check Sequence value into the 2 octet slot after the payload section of the Message.
- Perform zero stuffing between 0x7E flag bytes. (81 or 87 bytes)
- Send LAPD Message single bit at a time in the “N” bit position.
- Source of “N” bits should be set as transmit LAPD controller, (bits 4 and 3 set to “10” in 0x30).

A "0" to "1" transition, in this bit-field commands the LAPD Transmitter to initiate the above-mentioned procedure.

NOTE: *Once the LAPD Transmitter has been commanded to start transmission, the LAPD Transmitter will repeat the above-mentioned process once each second and will insert flag sequence octets into the outbound LAPD channel, during the idle periods between transmissions.*

Bit 2 - TxDL Busy

This Read-Only bit-field permits the user to poll or monitor the status of the LAPD Transmitter to see if it has completed its transmission of the LAPD Message frame. The LAPD Transmitter will set this bit-field to "1", while it is in the process of transmitting the LAPD Message frame. However, the LAPD Transmitter will clear this bit-field to "0" once it has completed its transmission of the LAPD Message frame.

Bit 1 - TxLAPD Interrupt Enable

This Read/Write bit-field permits the user to enable or disable the LAPD Message frame Transmission Complete interrupt.

Writing a "0" to this bit-field disables this interrupt. Writing a "1" to this bit-field enables this interrupt.

Bit 0 - TxLAPD Interrupt Status

This Reset-upon-Read bit-field permits the user to determine if the LAPD Message Frame Transmission Complete interrupt has occurred since the last read of this register. If this bit-field contains a "1" then the LAPD Message Frame Transmission Complete interrupt has occurred since the last read of this register. Conversely, if this bit-field contains a "0" then it has not.

2.3.7.4 *Transmit E3 Service Bits Register (ITU-T G.751)*

TxE3 Service Bits Register (Address = 0x35)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used						A-Bit	N-Bit
RO	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	0	0

Bit 1 - A-Bit

This Read/Write bit-field permits the user to define the value of the A-Bit within a given outbound E3 frame. If the user has configured the source of the A-Bit to be the TxE3 Service Bits Register (by setting TxASource[1:0] = 00, within the TxE3 Configuration Register, Address = 0x30), then the value written in this bit-field will specify the value of the A-Bit within the outbound E3 Frame.

Bit 0 - N-Bit

This Read/Write bit-field permits the user to define the value of the N-Bit within a given outbound E3 frame. If the user has configured the source of the N-Bit to be the TxE3 Service Bits Register (by setting TxNSource[1:0] = 00, within the TxE3 Configuration Register, Address = 0x30), then the value written in this bit-field will specify the value of the N-Bit within the outbound E3 Frame.

2.3.7.5 *Transmit E3 FAS Mask Register - 0 (ITU-T G.751)*

TxE3 FAS Error Mask Register - 0 (Address = 0x48)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			TxFAS_Error_Mask_Upper[4:0]				
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 4 - 0, TxFAS_Error_Mask_Upper[4:0]

This Read/Write bit-field permits the user to insert errors into the upper five bits of the Framing Alignment Signal, FAS of each outbound E3 frame. The user may wish to do this for equipment testing purposes. Prior to transmission, the Transmit E3 Framer block reads in the upper five (5) bits of the FAS value, and performs an XOR operation with it and the contents of this register. The results of this operation are written back into the upper five (5) bits of the FAS value, in each outbound E3 frame. Consequently, to insure errors are not injected into the FAS of the outbound E3 frames, the contents of this register must be set to all "0's" (the default value).

2.3.7.6 *Transmit E3 FAS Error Mask Register - 1 (ITU-T G.751)*

TxE3 FAS Error Mask Register - 1 (Address = 0x49)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			TxFAS_Error_Mask_Lower[4:0]				
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 4 - 0, TxFAS_Error_Mask_Lower[4:0]

This Read/Write bit-field permits the user to insert errors into the lower five bits of the Framing Alignment Signal, FAS of each outbound E3 frame. The user may wish to do this for equipment testing purposes. Prior to transmission, the Transmit E3 Framer block reads in the lower five (5) bits of the FAS value, and performs an XOR operation with it and the contents of this register. The results of this operation are written back into the lower five (5) bits of the FAS value, in each outbound E3 frame. Consequently, to insure errors are not injected into the FAS of the outbound E3 frames, the contents of this register must be set to all "0's" (the default value).

2.3.7.7 *Transmit E3 BIP-4 Error Mask Register (ITU-T G.751)*

TxE3 BIP-4 Error Mask Register (Address = 0x4A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxBIP-4 Mask[3:0]			
RO	RO	RO	RO	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 3 - 0: TxBIP-4 Mask[3:0]

This Read/Write bit-field permits the user to insert errors into the BIP-4 value within each outbound E3 frame. The user may wish to do this for equipment testing purposes. Prior to transmission, the Transmit DS3/E3 Framer block reads in the BIP-4 value, and performs an XOR operation with it and the contents of this register. The results of this operation are written back into the BIP-4 nibble position, in each outbound E3 frame. Consequently, to insure errors are not injected into the BIP-4 value of the outbound E3 frames, the contents of this register must be set to all "0's" (the default value).

NOTE: *This register is ignored if Bit 7 (Tx BIP-4 Enable) within the TxE3 Configuration register (Address = 0x30) is set to "0".*

2.3.8 Performance Monitor Registers

2.3.8.1 *PMON Line Code Violation Count Register - MSB*

PMON LCV Event Count Register - MSB (Address = 0x50)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON LCV Event Count Register - LSB (Address = 0x51) contains a 16-bit representation of the number of Line Code Violations that have been detected by the Receive DS3/E3 Framer block, since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.8.2 *PMON Line Code Violation Count Register - LSB*

PMON LCV Event Count Register - LSB (Address = 0x51)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON LCV Event Count Register - LSB (Address = 0x50) contains a 16-bit representation of the number of Line Code Violations that have been detected by the Receive DS3/E3 Framer block, since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.8.3 *PMON Framing Bit/Byte Error Count Register - MSB*

PMON Framing Bit/Byte Error Count Register - MSB (Address = 0x52)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit/Byte Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON Framing Bit/Byte Error Count Register - LSB (Address = 0x53) contains a 16-bit representation of the number of Framing Bit or Byte Errors that have been detected by the Receive DS3/E3 Framer block, since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.8.4 *PMON Framing Bit/Byte Error Count Register - LSB*

PMON Framing Bit/Byte Error Count Register - LSB (Address = 0x53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit/Byte Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON Framing Bit/Byte Error Count Register - MSB (Address = 0x52) contains a 16-bit representation of the number of Framing Bit or Byte Errors that have been detected by the Receive DS3/E3 Framer block, since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.8.5 *PMON Parity Error Count Register - MSB*

PMON Parity Error Count Register - MSB (Address = 0x54)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Parity Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON Parity Error Count Register - LSB (Address = 0x55) contains a 16-bit representation of the number of P-bit Errors (for DS3 applications), BIP-4 Errors (for E3/ITU-T G.751 applications) or BIP-8 Errors (for E3/ITU-T G.832 applications) that have been detected by the Receive DS3/E3 Framer block, since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.8.6 *PMON Parity Error Count Register - LSB*

PMON Parity Error Count Register - LSB (Address = 0x55)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Parity Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON Parity Error Count Register - MSB (Address = 0x54) contains a 16-bit representation of the number of P-bit Errors (for DS3 applications), BIP-4 Errors (for E3/ITU-T G.751 applications) or BIP-8 Errors (for E3/ITU-T G.832 applications) that have been detected by the Receive DS3/E3 Framer block, since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.8.7 *PMON FEBE Event Count Register - MSB*

PMON FEBE Event Count Register - MSB (Address = 0x56)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FEBE Event Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON FEBE Event Count Register - LSB (Address = 0x57) contains a 16-bit representation of the number of FEBE Events that have been detected by the Receive DS3/ E3 Framer block, since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.8.8 *PMON FEBE Event Count Register - LSB*

PMON FEBE Event Count Register - LSB (Address = 0x57)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FEBE Event Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON FEBE Event Count Register - MSB (Address = 0x56) contains a 16-bit representation of the number of FEBE Events that have been detected by the Receive DS3/ E3 Framer block, since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.8.9 *PMON CP-Bit Error Event Count Register - MSB*

PMON CP-Bit Error Count Register - MSB (Address = 0x58)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON CP-Bit Error Count Register - LSB (Address = 0x59) contains a 16-bit representation of the number of CP-bit Errors that have been detected by the Receive DS3/ E3 Framer block (within the channel), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

NOTE: *This register is only active if the Channel has been configured to operate in the DS3, C-bit Parity Framing format.*

2.3.8.10 *PMON CP-Bit Error Event Count Register - LSB*

PMON CP-Bit Error Count Register - LSB (Address = 0x59)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This Reset-upon-Read register, along with the PMON CP-Bit Error Count Register - MSB (Address = 0x58) contains a 16-bit representation of the number of CP-bit Errors that have been detected by the Receive DS3/E3 Framer block (within the channel), since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

NOTE: *This register is only active if the Channel has been configured to operate in the DS3, C-bit Parity Framing format.*

2.3.8.11 *PRBS Error Count Register - MSB*

PRBS Error Count Register - MSB (Direct Address = 0x68)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

These Reset-upon-Read bits along with that within the PRBS Error Count Register - LSB combine to reflect the cumulative number of PRBS bit errors that have been detected by the Framer Rx block since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

NOTE: *These register bits are not active if the PRBS Receiver has not been enabled.*

2.3.8.12 *PRBS Error Count Register - LSB*

PRBS Error Count Register - LSB (Direct Address = 0x69)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

These Reset-upon-Read bits along with that within the PRBS Error Count Register - MSB combine to reflect the cumulative number of PRBS bit errors that have been detected by the Framer Rx block since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

NOTE: *These register bits are not active if the PRBS Receiver has not been enabled.*

2.3.8.13 *PMON Holding Register*

PMON Holding Register (Address = 0x6C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON Holding Value							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Each of the above-defined PMON registers are 16 bit Reset-upon-Read registers. However, the bi-drectional data bus (of the Framer IC) is only 8-bits wide. As a consequence, whenever the Microprocessor intends to read a PMON register, there are two things to bear in mind.

1. This Microprocessor is going to require two read accesses in order read out the full 16-bit expression of these PMON registers.
2. The entire 16-bit expression (of a given PMON register) is going to be reset to 0x0000, immediately after the Microprocessor has completed its first read access to the PMON register.

Hence, the contents of the other byte (of the partially read PMON register) will reside within the PMON Holding register.

2.3.8.14 *One-Second Error Status Register*

One-Second Error Status Register (Address = 0x6D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Errored Second	Severely Errored Second
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 1 - Errored Second

This bit field indicates whether or not an error has occurred within the last One-Second accumulation interval. This bit-field will be set to “1” if at least one error has occurred during the last One-Second accumulation interval. Conversely, this bit-field will be set to "0" if no errors has occurred during the last one-second accumulation interval.

Bit 0 - Severely Errored Second

This bit-field indicates whether or not the error rate in the last one-second interval was greater than 1 in 1000. A "0" indicates that the error rate did not exceed 1 in 1000 in the last One-Second interval.

2.3.8.15 *One-Second Line Code Violation Accumulator Register - MSB*

LCV - One-Second Accumulator Register - MSB (Address = 0x6E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV - One-Second Count - High Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register, along with the LCV - One-Second Accumulator Register - LSB (Address = 0x6F) contains a 16-bit representation of the number of LCV (Line Code Violation) Events that have been detected by

the Receive DS3/E3 Framer block, within the last one-second sampling period. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.8.16 *One-Second Line Code Violation Accumulator Register - LSB*

LCV - One-Second Accumulator Register - LSB (Address = 0x6F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV - One-Second Count - Low Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register, along with the LCV - One-Second Accumulator Register - MSB (Address = 0x6E) contains a 16-bit representation of the number of LCV (Line Code Violation) Events that have been detected by the Receive DS3/E3 Framer block, within the last One-Second sampling period. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.8.17 *One-Second Frame Parity Error Accumulator Register - MSB*

Frame Parity Errors - One-Second Accumulator Register - MSB (Address = 0x70)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Frame Parity Error Count - High Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register, along with the Frame Parity Errors - One-Second Accumulator Register - LSB (Address = 0x71) contains a 16-bit representation of the number of Frame Parity Errors that have been detected by the Receive DS3/E3 Framer block, within the last One-Second sampling period. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

NOTES:

1. *For DS3 applications, the Frame-Parity Errors - One Second Accumulator" register contains the number of P-bit errors that have been detected in the last one-second sampling period.*
2. *For E3, ITU-T G.751 applications, the Frame-Parity Error - One Second Accumulator" register contains the number of BIP-4 errors that have been detected in the last one-second sampling period.*
3. *For E3, ITU-T G.832 applications, the Frame-Parity Error - One Second Accumulator register contains the number of BIP-8 errors that have been detected in the last one-second sampling period.*

2.3.8.18 *One-Second Frame Parity Error Accumulator Register - LSB*

Frame Parity Errors - One-Second Accumulator Register - LSB (Address = 0x71)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Frame Parity Error Count - Low Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register, along with the Frame Parity Errors - One-Second Accumulator Register - MSB (Address = 0x70) contains a 16-bit representation of the number of Frame Parity Errors that have been detected by the Receive DS3/E3 Framer block, within the last one-second sampling period. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

NOTES:

1. *For DS3 applications, the Frame-Parity Errors - One Second Accumulator" register contains the number of P-bit errors that have been detected in the last one-second sampling period.*
2. *For E3, ITU-T G.751 applications, the Frame-Parity Error - One Second Accumulator" register contains the number of BIP-4 errors that have been detected in the last one-second sampling period.*
3. *For E3, ITU-T G.832 applications, the Frame-Parity Error - One Second Accumulator register contains the number of BIP-8 errors that have been detected in the last one-second sampling period.*

2.3.8.19 *One-Second Frame CP-Bit Error Accumulator Register - MSB*

Frame CP-Bit Errors - One-Second Accumulator Register - MSB (Address = 0x72)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Count - High Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register, along with the Frame CP-Bit Error - One-Second Accumulator Register - LSB (Address = 0x73) contains a 16-bit representation of the number of CP Bit Errors tjhat have been detected by the Receive DS3/E3 Framer block, within the last one-second sampling period. This register contains the MSB (or Upper Byte) value of this 16-bit expression.

NOTE: *This register is only active if the Channel has been configured to operate in the DS3, C-bit Parity framing format.*

2.3.8.20 *One-Second Frame CP-Bit Error Accumulator Register - LSB*

Frame CP-Bit Errors - One-Second Accumulator Register - LSB (Address = 0x73)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Count - Low Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This Read-Only register, along with the Frame CP-Bit Error - One-Second Accumulator Register - MSB (Address = 0x72) contains a 16-bit representation of the number of CP Bit Errors tjhat have been detected by the Receive DS3/E3 Framer block, within the last one-second sampling period. This register contains the LSB (or Lower Byte) value of this 16-bit expression.

NOTE: *This register is only active if the Channel has been configured to operate in the DS3, C-bit Parity framing format.*

2.3.8.21 *Line Interface Drive Register*

NOTE: *This data sheet makes reference to the XRT730x and XRT73L0xA families of DS3/E3/STS-1 LIU ICs. For more information on the operation of these Exar DS3/E3/STS-1 LIU ICs, please consult any of the following data sheets.*

- *XRT7300 1-Channel DS3/E3/STS-1 LIU IC (5V)*
- *XRT73L00A 1-Channel DS3/E3/STS-1 LIU IC (3.3V)*
- *XRT7302 2-Channel DS3/E3/STS-1 LIU IC (5V)*
- *XRT73L02A 2-Channel DS3/E3/STS-1 LIU IC (3.3V)*
- *XRT73L03A 3-Channel DS3/E3/STS-1 LIU IC (3.3V)*
- *XRT73L04A 4-Channel DS3/E3/STS-1 LIU IC (3.3V)*
- *XRT73L06 6-Channel DS3/E3/STS-1 LIU IC (3.3V)*
- *XRT73L12 12-Channel DS3/E3/STS-1 LIU IC (3.3V)*

Line Interface Drive Register (Address = 0x80)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ILOOP	Not Used	REQB	TAOS	ENCODIS	TxLEV	RLOOP	LLOOP
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - ILOOP (Internal Remote Loop-back)

This Read/Write bit-field permits the user to configure the corresponding channel (within the XRT72L50) to operate in the Internal Remote Loop-back Mode. Once the user configures the channel to operate in this remote loop-back mode, then the RxPOSn, RxNEGn and RxLineClk signals will be routed directly to the TxPOSn, TxNEGn and TxLineClk signals.

Setting this bit-field to “1” configures the channel to operate in the Remote Loop-Back Mode.

Bit 5 - REQB - (Receive Equalization Enable/Disable Select)

This Read/Write bit-field allows the user to control the state of the REQB output pin of the Framer. This output pin is intended to be connected to the REQB input pin of the XRT73L0x DS3/E3/STS-1 LIU IC. If the user forces this signal to toggle "High”, then the internal Receive Equalizer (within the XRT73L0x) will be disabled for using short cable length. Conversely, if the user forces this signal to toggle "Low”, then the Receive Equalizer (within the XRT73L0x) will be enabled for short cable length.

The purpose of the internal Receive Equalizer (within the XRT73L0x) is to compensate for the Frequency-Dependent attenuation (e.g., cable loss), that a line signal will experience as it travels through coaxial cable, from the transmitting to the receiving terminal.

Writing a “1” to this bit-field causes the Framer to toggle the REQB output pin "High”. Writing a “0” to this bit-field causes the Framer to toggle the REQB output pin "Low”.

For information on the criteria that should be used when deciding whether to enable or disable the Receive Equalizer, please consult the XRT73L0x DS3/E3/STS-1 LIU IC Data Sheet.

NOTE: *If the customer is not using the XRT73L0x DS3/E3/STS-1 IC, then this bit-field and the REQB output pin can be used for other purposes.*

Bit 4 - TAOS - (Transmit All Ones Signal)

This Read/Write bit-field permits the user to control the state of the TAOS output pin of the Framer. This output pin is intended to be connected to the TAOS input pin of the DS3/E3 LIU IC. If the user forces this signal to toggle "High", then the LIU will transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "Low" then the LIU IC will proceed to transmit data based upon the pattern that it receives via the TxPOS[n] and TxNEG[n] output pins (of the Framer IC).

Writing a "1" to this bit-field will cause the TAOS[n] output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low".

NOTE: *If the customer is not using an Exar XRT73L0X DS3/E3/STS-1 LIU IC, then this bit-field, and the TAOS output pin can be used for other purposes.*

Bit 3 - Encodis - (B3ZS Encoder Disable)

This Read/Write bit-field allows the user to control the state of the Encodis output pin of the Framer. This output pin is intended to be connected to the ENDECDIS input pin of the DS3/E3 LIU IC. If the user forces this signal to toggle "High", then the internal B3ZS/HDB3 encoder (within the LIU) will be disabled. Conversely, if the user command this output signal to toggle "Low", then the internal B3ZS/HDB3 encoder (within the LIU) will be enabled.

Writing a "1" to this bit-field causes the Framer to toggle the Encodis output pin "High". Writing a "0" to this bit-field will cause the Channel to toggle this output pin "Low".

NOTES:

1. *The B3ZS/HDB3 encoder, within the DS3/E3 LIU, is not to be confused with the B3ZS/HDB3 encoding capability that exists within the Transmit Section of the Framer IC.*

2. *The user is advised to disable the B3ZS/HDB3 encoder (within the LIU IC) if the channel is configured to operate in the B3ZS/HDB3 line code.*
3. *If the customer is not using an Exar XRT73L0X DS3/E3/STS-1 LIU IC, then this bit-field and the Encodis output pin can be used for other purposes.*

Bit 2 - TxLev - (Transmit Output Line Build-Out Select Output)

This Read/Write bit-field permits the user to control the state of the TxLev[n] output pin of the Framer. This output pin is intended to be connected to the TxLev input pin of the DS3/E3 LIU IC. If the user commands this signal to toggle "High", then the DS3/E3 LIU IC will disable the Transmit Line Build-Out circuitry, and will transmit unshaped (square-wave) pulses onto the line. If the user commands this signal to toggle "Low", then the DS3/E3 LIU IC will enable the Transmit Line Build-Out circuitry, and will transmit shaped pulses onto the line.

In order to insure that the transmit output pulses of the LIU meet the DSX-3 Isolated Pulse Template Requirements (per Bellcore GR-499-CORE), the user is advised to set this bit-field to "0", if the length of cable (between the LIU transmit output and the DSX-3 Cross Connect System) is greater than 225 feet.

Conversely, the user is advised to set this bit-field to "1", if the length of cable (between the LIU transmit output and the DSX-3 Cross Connect system) is less than 225 feet.

Writing a "1" to this bit-field commands the Framer to toggle the TxLev output "High". Writing a "0" to this bit-field commands the Framer to toggle this output signal "Low".

NOTES:

1. *The TxLEV function is only applicable to DS3 applications. E3 LIUs do not support this kind of Line Build out feature.*
2. *If the customer is not using an Exar XRT73L0X DS3/E3 LIU IC, then this bit-field and the TxLev output pin can be used for other purposes.*

Bit 1 - RLOOP - (Remote Loop-back)

This Read/Write bit-field permits the user to control the state of the RLOOP[n] output pin of the Framer. This output pin is intended to be connected to the RLOOP input pin of the DS3/E3 LIU IC.

When using Exar's family of XRT73L0X DS3/E3 LIUs, the state of the RLOOP and the LLOOP pins are used to dictate which loop-back mode the LIU will operate in. The following table presents the relationship between the state of these two input pins (or bit-fields) and the resulting loop-back modes.

RLOOP	LLOOP	RESULTING LOOP-BACK MODE OF THE DS3/E3 LIU
0	0	Normal Operation (No Loop-back Mode)
0	1	Analog Local Loop-back Mode
1	0	Remote Loop-back Mode
1	1	Digital Local Loop-back Mode

Writing a "1" into this bit-field commands the Framer IC to toggle the RLOOP[n] output signal "High". Writing a "0" into this bit-field commands the Framer IC to toggle this output signal "Low".

For a detailed description on the operation of a particular Exar XRT73L0X DS3/E3 LIU, while configured into each of these above-mentioned loop-back modes, please consult the appropriate LIU Data Sheet.

NOTE: *If the customer is not using an Exar XRT73L0X DS3/E3/STS-1 LIU IC, then this bit-field and the RLOOP[n] output pin can be used for other purposes.*

Bit 0 - LLOOP - (Local Loop-back)

This Read/Write bit-field permits the user to control the state of the LLOOP[n] output pin of the Framer. This output pin is intended to be connected to the LLOOP input pin of the DS3/E3 LIU IC.

When using Exar's family of XRT73L0X DS3/E3 LIUs, the state of the RLOOP and the LLOOP pins are used to dictate which loop-back mode the LIU will operate in. The previous table presents the relationship between the state of these two input pins (or bit-fields) and the resulting loop-back modes.

Writing a "1" into this bit-field commands the Framer to toggle the LLOOP[n] output signal "High". Writing a "0" into this bit-field commands the Framer to toggle this output signal "Low".

For a detailed description of the operation of a particular Exar XRT73L0X DS3/E3 LIU, while configured into each of these above-mentioned loop-back modes, please consult the appropriate LIU IC Data Sheet.

NOTE: *If the customer is not using an Exar XRT73L0X DS3/E3/STS-1 LIU IC, then this bit-field and the LLOOP[n] output pin can be used for other purposes.*

2.3.8.22 *Line Interface Scan Register*

Line Interface Scan Register (Address = 0x81)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					DMO	RLOL	RLOS
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	1	1

Bit 2 - DMO - (Drive Monitor Output)

This Read-Only bit-field indicates the logic state of the DMO[n] input pin of the Framer. This input pin is intended to be connected to the DMO output pin of an Exar XRT73L0X-type of DS3/E3 LIU IC. If this bit-field contains a logic "1", then the DMO input pin is "High". An Exar XRT73L0X-type of DS3/E3 LIU IC will set this pin "High" if the drive monitor circuitry (within the LIU) has not detected any bipolar signals at the MTIP and MRING inputs (of the LIU) within the last 128 $\pm$ 32 bit periods.

Conversely, if this bit-field contains a logic "0", then the DMO input pin is "High". The DS3/E3 LIU IC will set this pin "Low" if bipolar signals are being detected at the MTIP and MRING input pins.

As a consequence, the DMO output pin can be thought of as a Transmit Driver Failure indicator.

NOTE: *If this customer is not using an Exar XRT73L0X-type of DS3/E3 LIU IC, then this input pin and bit-field can be used for a variety of other purposes.*

Bit 1 - RLOL - (Receive Loss of Lock)

This Read-Only bit-field indicates the logic state of the RLOL[n] input pin of the Framer. This input pin is intended to be connected to the RLOL output pin of an Exar XRT73L0X-type of DS3/E3 LIU IC. If this bit-field contains a logic "1", then the RLOL[n] input pin is "High". An Exar XRT73L0X-type of DS3/E3 LIU IC will set this pin "High" if the clock recovery phase-locked-loop circuitry (within the LIU) has lost lock with the incoming DS3/E3 data-stream and is not properly recovering clock and data.

Conversely, if this bit-field contains a logic "0", then the RLOL input pin is "Low". The DS3/E3 LIU IC will hold this pin "Low" as long as this clock recovery phase-locked-loop circuitry (within the LIU) is properly locked onto the incoming DS3 or E3 data-stream, and is properly recovering clock and data from this data-stream.

NOTE: *If the customer is not using an Exar XRT73L0X-type of DS3/E3/STS-1 IC, then this bit-field, and the RLOL[n] input pin can be used for other purposes.*

Bit 0 - RLOS - (Receive Loss of Signal)

This Read-Only bit-field indicates the logic state of the RLOS[n] input pin of the Framer. This input pin is intended to be connected to the RLOS output pin of the DS3/E3 LIU IC. If this bit-field contains a logic "1", then the RLOS[n] input pin is "High". The LIU will toggle this signal "High" if it (the LIU IC) is currently declaring an LOS (Loss of Signal) condition.

Conversely, if this bit-field contains a logic "0", then the RLOS input pin is "Low". The LIU will hold this signal "Low" if it is NOT currently declaring an LOS (Loss of Signal) condition.

NOTE: *Asserting the RLOS input pin will cause the XRT72L50 Framer to generate the Change in LOS Condition interrupt and declare an LOS (Loss of Signal) condition. Therefore, this input pin should not be used as a general purpose input.*

2.3.8.23 *HDLC Control Register*

HDLC Control Register (Address = 0x82)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framer By-Pass	HDLC ON	CRC-32 Select	Reserved	HDLC Loop-Back	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	0

Bit 7 - Framer By-Pass

This Read/Write bit-field permits the user to enable or disable (by-pass) the DS3/E3 Framer circuitry, within a given channel in the XRT72L50.

This feature permits the user to operate a given Channel in the Un-framed Mode. Further, this feature also permits the user to transmit and receive HDLC frames at the DS3 or E3 line rate of 44.736Mbps or 34.368Mbps, without sacrificing any bandwidth to support the overhead bits/bytes/

Setting this bit-field to "1" disables the Transmit and Receive DS3/E3 Framer blocks within the channel. Setting this bit-field to "0" enables the Transmit and Receive DS3/E3 Framer blocks.

Bit 6 - HDLC ON

This Read/Write bit-field permits the user to configure a given channel to operate in the High-Speed HDLC Controller Mode. If the user invokes this feature, then a Transmit and Receive byte-wide interface will be enabled, and the channel will be configured to transmit and receive HDLC Frames via the DS3 or E3 payload bits.

Setting this bit-field to "1" configures the channel to operate in the High-Speed HDLC Controller Mode.

Bit 5 - CRC-32

This Read/Write bit-field permits the user to configure a given channel to do the following.

1. To configure the Transmit HDLC Controller block to compute and append either a CRC-16 or a CRC-32 value as a trailer to the outbound HDLC frame.
2. To configure the Receive HDLC Controller block to compute and verify either CRC-16 or the CRC-32 value within each inbound HDLC frame.

Setting this bit-field to "0" configures the Transmit HDLC Controller block to compute and append the CRC-16 value to the end of the outbound HDLC frame. Further, this setting also configures the Receive HDLC Controller block compute and verify the CRC-32 value, which has been appended to the end of the inbound HDLC frame.

Setting this bit-field to "1" configures the Transmit HDLC Controller block to compute and append the CRC-32 value to the end of the outbound HDLC frame. Further, this same setting also configures the Receive HDLC Controller block to compute and verify the CRC-32 value, which has been appended to the end of the inbound HDLC frame.

NOTE: *This bit-field is only active if the channel has been configured to operate in the High-Speed HDLC Controller Mode.*

Bit 3 - HDLC Loop-Back

This R/W bit allows the user to loopback data presented to the HDLC block prior to D3/E3framing. When this bit is set to "1" loopback is enabled, when "0" this loopback path is disabled.

2.4 *The Loss of Clock Enable Feature*

The timing for the Microprocessor Interface section, originates from a line rate (e.g., either a 34.368MHz or 44.736 MHz) signal that is provided by either the TxInClk[n] or the RxLineClk[n] signals. However, if the Framer experiences a Loss of Clock signal event such that neither the TxInClk[n] nor the RxLineClk[n] signal are present, then the Framer Microprocessor Interface section cannot function.

The Framer offers a Loss of Clock (LOC) protection feature that allows the Microprocessor Interface section to at least complete or terminate an in-process Read or Write cycle (with the local µP) should this Loss of Clock event occur. The LOC circuitry consists of a ring oscillator that continuously checks for signal transitions at the TxInClk[n] and RxLineClk[n] input pins. If a Loss of Clock Signal event occur such that no transitions are occurring on these pins, then the LOC circuitry will automatically assert the $\overline{\text{RDY}}_\overline{\text{DTCK}}$ signal in order to complete (or terminate) the current Read or Write cycle with the Framer Microprocessor Interface section.

The user may enable or disable this LOC Protection feature by writing to Framer I/O Control Register, Bit 7 (Disable TxLOC), as depicted below.

Framer I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxLOC Disable	LOC	Disable RxLOc	AMI/Zero Sup	Unipolar/ $\overline{\text{Bipolar}}$	TxLine Clk Invert	RxLine Clk Invert	Reframe
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Writing a "1" to this bit-field disables the TxLOC Protection feature. Writing a "0" to this bit-field disables this feature.

NOTE: *The Ring Oscillator can be a source of noise, within the Framer chip. Hence, there may be situations where the user will wish to disable the LOC Protection feature.*

2.5 *Using the PMON Holding Register*

The Microprocessor Interface section consists of an 8-bit bi-directional data bus. As a consequence, the local µP will be able to read from and write to the Framer on-chip registers, 8 bit per (read or write) cycle. Since most of the Framer on-chip registers contain 8-bits, communicating with the local µP over an 8-bit data bus is not much of an inconvenience. However, all of the PMON registers contain 16 bits. Consequently, any reads of the PMON registers, will require two read cycles. To make matters potentially more complicated, these PMON registers are Reset-upon-Read registers. Therefore, the contents of both the MSB and LSB registers (of the READ PMON register) are reset to zero upon the first of these two read cycles.

Fortunately, the XRT72L50 Framer IC includes a feature that will make reading a PMON register a slightly less complicated task. The Framer chip address space contains a Read-Only register known as the PMON Holding register, which is located at 0x6C. Whenever the local µP reads in an 8-bit value of a given PMON registers (e.g., either the upper-byte or the lower byte value of the PMON register), the other 8-bit value of that PMON register will automatically be loaded into the PMON Holding register. As a consequence, the other 8-bit value of the PMON register is accessible by reading the PMON Holding register.

Hence, anytime the local µP is trying to read in the contents of a PMON register, the first read access must be made directly to one of the 8-bit values of the PMON registers (e.g., for example: the PMON LCV Event Count Register - MSB, Address = 0x50). However, the second read must always be made to a constant location in system memory, the PMON Holding Register.

2.6 *The Interrupt Structure within the Framer Microprocessor Interface Section*

The XRT72L50 Framer is equipped with a sophisticated Interrupt Servicing Structure. This Interrupt Structure includes an Interrupt Request output, $\overline{\text{Int}}$, numerous Interrupt Enable Registers and numerous Interrupt Status Registers. The Interrupt Servicing Structure, within each of the three channels contains two levels of hierarchy. The top level is at the functional block level (e.g., the Receive Section, the Transmit Section, etc.). The lower hierarchical level is at the individual interrupt or source level. Each hierarchical level consists of a complete set of Interrupt Status Registers/bits and Interrupt Enable Registers/bits, as will be discussed below.

Both of the functional sections, within each channel, are capable of generating Interrupt Requests to the local µP/µC. The Framer Interrupt Structure has been carefully designed to allow the user to quickly determine the exact source of the interrupt (with minimal latency) which will aid the local µP/µC in determining which interrupt service routine to call up in order to respond to or eliminate the condition(s) causing the interrupt.

Table 5 lists all of the possible conditions that can generate interrupts, with each functional section of a given channel.

TABLE 5: LIST OF ALL OF THE POSSIBLE CONDITIONS THAT CAN GENERATE INTERRUPTS WITHIN EACH CHANNEL OF THE XRT72L50 FRAMER

FUNCTION SECTION	INTERRUPTING CONDITION
Transmit Section	FEAC Message Transfer Complete (DS3, C-Bit Parity Only) LAPD Message frame Transfer Complete (DS3, C-Bit Parity, All E3)
Receive Section	Change of Status on Receive LOS, OOF, AIS Idle Detection Validation and removal of received FEAC Code (DS3, C-Bit Parity Only) New PMDL Message in Receive LAPD Message Buffer. Detection of Parity Errors (e.g., P-Bit, CP-Bit, BIP-4 and BIP-8 Errors) Detection of Framing Bit/Byte Errors.
Framer Chip Level	One-Second Interrupt

Each of the three channels, within the XRT72L50 Framer contains an Interrupt Block that comes equipped with the following registers to support the servicing of these potential interrupt request sources. Table 6, 7, and 8lists these registers, and their addresses for DS3, E3 (ITU-T G.832) and E3 (ITU-T G.751) framing formats.

TABLE 6: A LISTING OF THE XRT72L50 FRAMER INTERRUPT BLOCK REGISTERS (FOR DS3 APPLICATIONS)

ADDRESS LOCATION	REGISTER NAME
0 x 04	Block Interrupt Enable Register
0 x 05	Block Interrupt Status Register
0 x 12	RxDS3 Interrupt Enable Register
0 x 13	RxDS3 Interrupt Status Register
0 x 17	RxDS3 FEAC Interrupt Enable/Status Register
0 x 18	RxDS3 LAPD Control Register
0 x 31	TxDS3 FEAC Configuration and Status Register
0 x 34	TxDS3 LAPD Status/Interrupt Register

TABLE 7: A LISTING OF THE XRT72L50 FRAMER INTERRUPT BLOCK REGISTERS (FOR E3, ITU-T G.832 APPLICATIONS)

ADDRESS LOCATION	REGISTER NAME
0 x 04	Block Interrupt Enable Register
0 x 05	Block Interrupt Status Register
0 x 12	RxE3 Interrupt Enable Register -1
0 x 13	RxE3 Interrupt Enable Register -2
0 x 14	RxE3 Interrupt Status Register - 1
0 x 15	RxE3 Interrupt Status Register - 2
0 x 18	RxE3 LAPD Control Register
0 x 34	TxE3 LAPD Status/Interrupt Status

TABLE 8: A LISTING OF THE XRT72L50 FRAMER INTERRUPT BLOCK REGISTER (FOR E3, ITU-T G.751 APPLICATIONS)

ADDRESS LOCATION	REGISTER NAME
0 x 04	Block Interrupt Enable Register
0 x 05	Block Interrupt Status Register
0 x 12	RxE3 Interrupt Enable Register -1
0 x 13	RxE3 Interrupt Enable Register -2
0 x 14	RxE3 Interrupt Status Register - 1
0 x 15	RxE3 Interrupt Status Register - 2
0 x 18	RxE3 LAPD Control Register
0 x 34	TxE3 LAPD Status/Interrupt Status

General Flow of Framer Chip Interrupt Servicing

When any of the conditions, presented in Table 5 occurs, (if their Interrupts is enabled), then the Framer will generate an interrupt request to the local µP/µC by asserting the active-low interrupt request output pin, $\overline{\text{Int}}$. Shortly after the local µP/µC has detected the activated $\overline{\text{Int}}$ signal, it will enter into the appropriate user-supplied interrupt service routine. The first task for the local µP/µC, while running this interrupt service routine, may be to isolate the source of the interrupt request down to the device level (e.g., the XRT72L50 Framer), if multiple peripheral devices exist in the user's system. However, once the interrupting peripheral device has been identified, the next task for the local µP/µC is to determine exactly what feature or functional section within the device requested the interrupt.

Determine the Channel and Functional Block(s) Requesting the Interrupt

If the interrupt device turns out to be the XRT72L50 DS3/E3 Framer IC, then the local µC/µP must determine which channel functional block requested the interrupt. Hence, upon reaching this state, one of the very first things that the local µC/µP must do within the user supplied Framer Interrupt Service routine, is to perform a read of the Block Interrupt Status Register (Address = 0x05) for every channel within the XRT72L50 Framer. The bit format of the Block Interrupt Status register is presented below.

Block Interrupt Status Register (Address = 0x05)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Status	Not Used					TxDS3/E3 Interrupt Status	One-Second Interrupt Status
RO	RO	RO	RO	RO	RO	RO	RUR
0	0	0	0	0	0	0	1

The Block Interrupt Status Register presents the interrupt request status of each functional block, within the chip. The purpose of the Block Interrupt Status Register is to help the local µP/µC identify which functional block(s) within a given channel has requested the interrupt. Whichever bit(s) are asserted in this register, identifies which block(s) have experienced an interrupt-generating condition as presented in Table 5. Once the local µP/µC has read this register, it can determine which branch within the interrupt service routine that it must follow, in order to properly service this interrupt.

The Framer further supports the Functional Block hierarchy by providing the Block Interrupt Enable Register (Address = 0x04). The bit format of this register is identical to that for the Block Interrupt Status register, and is presented below for the sake of completeness.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One-Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	0	0

The Block Interrupt Enable register allows the user to individually enable or disable the interrupt requesting capability of the functional blocks. If a particular bit-field, within this register contains the value "0", then the corresponding functional block has been disabled from generating any interrupt requests. Conversely, if that bit-field contains the value "1", then the corresponding functional block has been enabled for interrupt generation (e.g., those potential interrupts, within the enabled functional block that are enabled at the source level, are now enabled). The user should be aware of the fact that each functional block contains anywhere from 1 to 12 potential interrupt sources. Each of these lower level interrupt sources contain their own set of interrupt enable bits and interrupt status bits, existing in various on-chip registers.

Interrupt Service Routing Branching: after reading the Block Interrupt Status Register.

The contents of the Block Interrupt Status Register identify which of 3 functional blocks has requested interrupt service. The local µP should use this information in order to determine where, within the Interrupt Service Routing, program control should branch to. Table 9 can be viewed as an interrupt service routine guide. It lists each of the Functional Blocks, that contain a bit-field in the Block Interrupt Status Register. Additionally, this table also presents a list and addresses of corresponding on-chip Registers that the Interrupt Service Routine should branch to and read, based upon the Interrupting Functional Block.

Table 9, Table 10, and Table 11 presents the Interrupt Service Routine guide for DS3, E3/ITU-T G.832 and E3/ITU-T G.751 applications, respectively.

TABLE 9: INTERRUPT SERVICE ROUTINE GUIDE (FOR DS3 APPLICATIONS)

INTERRUPTING FUNCTIONAL BLOCK	THE NEXT REGISTERS TO BE READ DURING THE INTERRUPT SERVICE ROUTINE	REGISTER ADDRESS
Receive Section	RxDS3 Interrupt Status Register	0 x 13
	RxDS3 FEAC Interrupt Enable/Status Register	0 x 17
	RxDS3 LAPD Control Register	0 x 18
Transmit Section	TxDS3 FEAC Configuration and Status Register	0 x 31
	TxDS3 LAPD Status/Interrupt Register	0 x 34

TABLE 10: INTERRUPT SERVICE ROUTINE GUIDE (FOR E3, ITU-T G.832 APPLICATIONS)

INTERRUPTING FUNCTIONAL BLOCK	THE NEXT REGISTERS TO BE READ DURING THE INTERRUPT SERVICE ROUTINE	REGISTER ADDRESS
Receive Section	RxE3 Interrupt Status Register - 1	0 x 14
	RxE3 Interrupt Status Register - 2	0 x 15
	RxE3 LAPD Control Register	0 x 18
Transmit Section	TxE3 LAPD Status and Interrupt Register	0 x 34

TABLE 11: INTERRUPT SERVICE ROUTINE GUIDE (FOR E3, ITU-T G.751 APPLICATIONS)

INTERRUPTING FUNCTIONAL BLOCK	THE NEXT REGISTERS TO BE READ DURING THE INTERRUPT SERVICE ROUTINE	REGISTER ADDRESS
Receive Section	RxE3 Interrupt Status Register - 1	0 x 014
	RxE3 Interrupt Status Register - 2	0 x 15
	RxE3 LAPD Control Register	0 x 18
Transmit Section	TxE3 LAPD Status and Interrupt Register	0 x 34

Once the Microprocessor/Microcontroller has read the register that corresponds to the interrupting source, the following happens:

1. The Asserted Interrupt Status bit-fields within this register will be reset upon read.
2. The Asserted bit-field, within the Block Interrupt Status register will be reset.
3. The Framer will negate the $\overline{Int}$ (Interrupt Request) output pin, by drving this output pin "High".

2.6.1 Automatic Reset of Interrupt Enable Bits

Occassionally, the user's system (which includes the Framer) may experience a fault condition, such that a Framer Interrupt Condition will continuously exist. If this particular interrupt condition has been enabled, then the Framer will generate an interrupt request to the MIcroprocessor/Microcontroller. Afterwards, the Microprocessor/Microcontroller will attempt to service this interrupt by reading the Block Interrupt Status register and the subsequent source level interrupt status registers. Additionally, the Microprocessor/ Microcontroller will attempl to perform some system-related tasks in order to try to resolve those conditions causing the interrupt. After the Microprocessor/Microcontroller has attempted all of these things, the Framer IC will negate the $\overline{Int}$ output pin. However, because the system fault still remains, the conditions causing the Framer to issue this interrupt request, also still exists. Consequently, the Framer will generate another interrupt request, which forces the Microprocessor/Microcontroller to once again attempt to service this interrupt. This phenomenon quickly results in the local Microprocessor/Microcontroller being tied up in a continuous cycle of

executing this one interrupt service routine. Consequently, the local Microprocessor/Microcontroller (along with portions of the overall system) now becomes non-functional.

In order to prevent this phenomenon from ever occuring, the Framer IC allows the user to automatically reset the interrupt enable bits, following their activation. The user can implement this feature by writing the appropriate value into Bit 3 (Interrupt Enable Reset) within the Framer Operating Mode register, as illustrated below.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Local Loop-Back	$\overline{DS3}$/E3	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	1

Writing a “1” to this bit-field configures the Framer to automatically disable a given interrupt, following its activation. Writing a “0” to this bit-field configures the Framer to leave the Interrupt Enable bit as is, following interrupt activation.

If a user opts to implement the Automatic Reset of Interrupt Enable Bits feature, then he/she might wish to configure the Microprocessor/Microcontroller to go back and re-enable these interrupts at a later time.

2.6.2 One-Second Interrupts

The Block Interrupt Status register, and Block Interrupt Enable register each contain a bit-field for the One-Second Interrupt. If this interrupt is enabled (within the Block Interrupt Enable register), then the Framer will automatically generate an interrupt request to the Microprocessor/Microcontroller repeatedly at one-second intervals. At a minimum, the user’s interrupt service routine must service this interrupt by reading the Block Interrupt Status register (Address = 0x05). Once the Microprocessor/Microcontroller has read this register, then the following things will happen.

1. The One-Second Interrupt bit-field, within the Block Interrupt Status register, will be reset to “0”.
2. The Framer will negate the $\overline{Int}$ (Interrupt Request) output pin.

The purpose of providing this One-Second interrupt is to allow the Microprocessor/Microcontroller the opportunity to perform certain tasks at One-Second intervals. The user can accomplish this by including the necessary code (for these various tasks) as a part of the interrupt service routine, for the One-Second type interrupt. Some of these tasks could include:

- Reading in the contents of the One-Second Performance Monitor registers.
- Reading various other Performance Monitor registers.
- Writing a new PMDL Message into the Transmit LAPD Message buffer. After the LAPD Transmitter has been enabled and commanded to initiate transmission of the LAPD Message frame (containing the PMDL Message, residing within the Transmit LAPD Message buffer), the LAPD Transmitter will continue to re-transmit this same LAPD Message frame, repeatedly at One-Second intervals, until it has been disabled. If a new PMDL message is written into the Transmit LAPD Message buffer immediately following the occurrence of a One-Second Interrupt, then this will ensure that this Write activity will not interfere with this periodic transmission of the LAPD Message frames.

Notes regarding the Block Interrupt Enable and Block Interrupt Status Registers:

1. The Block Interrupt Enable Register allows the user to globally disable all potential interrupts within either the Transmit or Receive sections, by writing a “0” into the appropriate bit-field of this register. However, the Block Interrupt Enable register does not allow the user to globally enable all potential interrupts within a given functional block. In other words, enabling a given functional block does not automatically enable all of its potential interrupt sources. Those potential interrupt sources that have been disabled at the source level will remain disabled, independent of the status of their associated functional blocks.
2. The Block Interrupt Enable register is set to 0x00 upon power or reset. Therefore, the user will have to write some “1’s” into this register, in order to enable some of the interrupts.

The remaining registers, listed in Table 9, Table 10 and Table 11 will be presented in the discussion of the functional blocks, within the XRT72L50 Framer IC. These discussions will present more details about the interrupt causes and how to properly service. them.

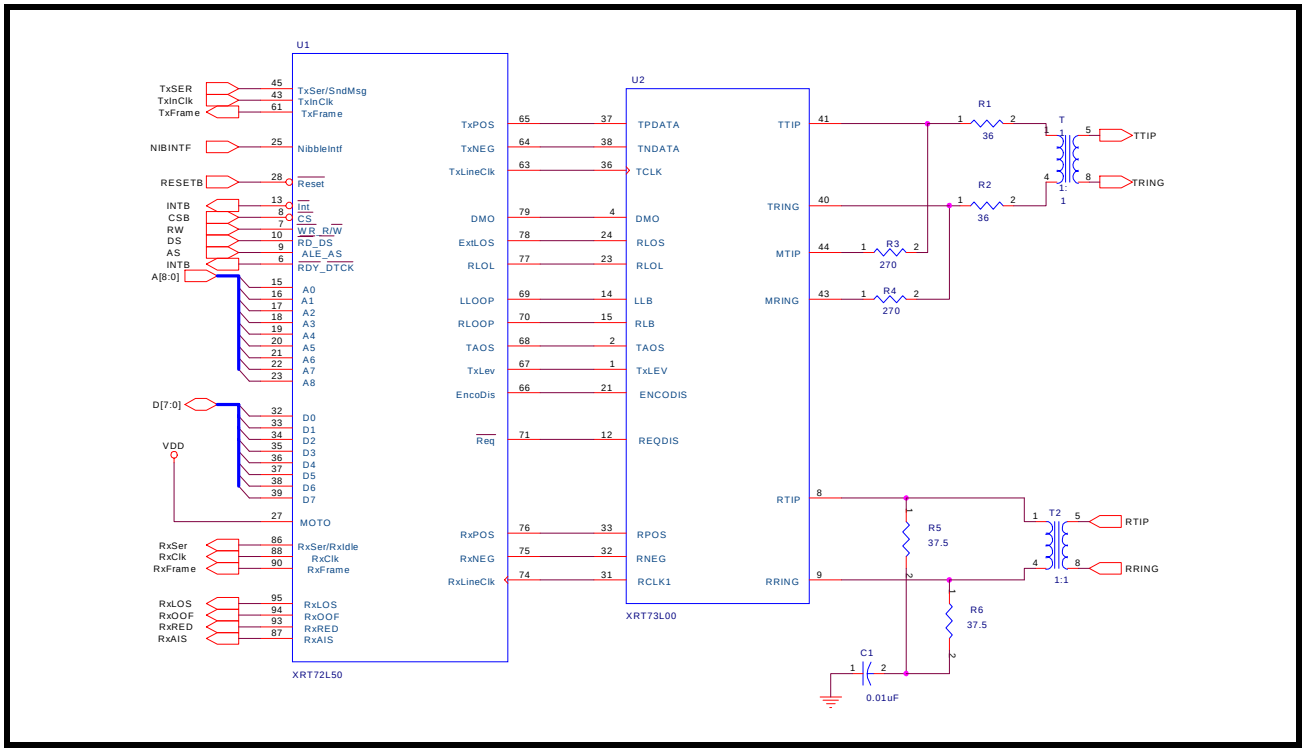
3.0 THE LINE INTERFACE AND SCAN SECTION

The Line Interface and Scan Section of the XRT72L50 DS3/E3 Framer IC consists of 5 output pins, 3 input pins, a Read/Write register, and a Read-Only register.

The purpose of the Line Interface Drive and Scan section is to permit the user to monitor and exercise control over many aspects of the XRT73L0x DS3/E3/STS-1 LIU IC without having to develop the necessary off-chip glue-logic.

Figure 27 presents a simple circuit schematic that depicts how the XRT72L50 DS3/E3 Framer IC could be interfaced to the XRT73L0x DS3/E3/STS-1 LIU IC.

FIGURE 27. XRT72L50 DS3/E3 FRAMER INTERFACED TO THE XRT73L0X DS3/E3/STS-1 LIU



3.1 *Bit-Fields within the Line Interface Drive Register*

As mentioned above, the Line Interface Drive and Scan section consists of five output pins and three input pins. The logic state of the output pins are controlled by the contents within the Line Interface Drive register, as depicted below.

LINE INTERFACE DRIVE Register (Address = 0x80)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ILOOP	Not Used	REQB	TAOS	ENCODIS	TxLEV	RLOOP	LLOOP
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

Bit 7 - ILOOP (Internal Remote Loop-back)

This Read/Write bit-field permits the user to configure the corresponding channel (within the XRT72L50) to operate in the Internal Remote Loop-back Mode. Once the user configures the channel to operate in this remote loop-back mode, then the RxPOSn, RxNEGn and RxLineClk signals will be routed directly to the TxPOSn, TxNEGn and TxLineClk signals.

Setting this bit-field to “1” configures the channel to operate in the Remote Loop-Back Mode.

Bit 5 - REQB - (Receive Equalization Enable/Disable Select)

This Read/Write bit-field allows the user to control the state of the REQB output pin of the Framer. This output pin is intended to be connected to the REQB input pin of the XRT73L0x DS3/E3/STS-1 LIU IC. If the user forces this signal to toggle "High”, then the internal Receive Equalizer (within the XRT73L0x) will be disabled for using short cable length. Conversely, if the user forces this signal to toggle "Low”, then the Receive Equalizer (within the XRT73L0x) will be enabled for short cable length.

The purpose of the internal Receive Equalizer (within the XRT73L0x) is to compensate for the Frequency-Dependent attenuation (e.g., cable loss), that a line signal will experience as it travels through coaxial cable, from the transmitting to the receiving terminal.

Writing a “1” to this bit-field causes the Framer to toggle the REQB output pin "High”. Writing a “0” to this bit-field causes the Framer to toggle the REQB output pin "Low”.

For information on the criteria that should be used when deciding whether to enable or disable the Receive Equalizer, please consult the XRT73L0x DS3/E3/STS-1 LIU IC Data Sheet.

NOTE: *If the customer is not using the XRT73L0x DS3/E3/STS-1 IC, then this bit-field and the REQB output pin can be used for other purposes.*

Bit 4 - TAOS - (Transmit All Ones Signal)

This Read/Write bit-field allows the user to control the state of the TAOS output pin of the Framer. This output pin is intended to be connected to the TAOS input pin of the XRT73L0x DS3/E3/STS-1 LIU IC. if the user forces this signal to toggle "High”, then the XRT73L0x will transmit an all 1’s pattern onto the line. Conversely, if the user commands this output signal to toggle "Low” then the XRT73L0x DS3/E3/STS-1 LIU IC will proceed to transmit data based upon the data that it receives via the TxPOS and TxNEG output pins (of the Framer IC).

Writing a “1” to this bit-field causes the TAOS output pin to toggle "High”. Writing a “0” to this bit-field will cause this output pin to toggle "Low”.

NOTE: *If the customer is not using the XRT73L0x DS3/E3/STS-1 LIU IC, then this bit-field, and the TAOS output pin can be used for other purposes.*

Bit 3 - ENCODIS - (B3ZS/HDB3 Encoder Disable)

This Read/Write bit-field allows the user to control the state of the ENCODIS output pin of the Framer. This output pin is intended to be connected to the ENDECDIS input pin of the XRT73L0x DS3/E3/STS-1 LIU IC. If the user forces this signal to toggle "High”, then the internal B3ZS/HDB3 encoder (within the XRT73L0x) will be disabled. Conversely, if the user commands this output signal to toggle "Low”, then the internal B3ZS/HDB3 encoder (within the XRT73L0x) will be enabled.

Writing a “1” to this bit-field causes the Framer IC to toggle the Encodis output pin "High”. Writing a “0” to this bit-field will cause the Framer IC to toggle this output pin "Low”.

NOTES:

1. *The B3ZS/HDB3 encoder, within the XRT73L0x is not to be confused with the B3ZS/HDB3 encoding capabilities that exists within the Transmit DS3/E3 Framer block of the Framer IC.*
2. *The user is advised to disable the B3ZS/HDB3 encoder (within the XRT73L0x IC) if the Transmit and Receive DS3/E3 Framer (within the XRT72L50) are configured to operate in the B3ZS/HDB3 line code.*
3. *If the customer is not using the XRT73L0x DS3/E3/STS-1 LIU IC, then this bit-field and the Encodis output pin can be used for other purposes.*

Bit 2 - TxLEV (Transmit Line Build-Out Enable/Disable Select)

This Read/Write bit-field allows the user to control the state of the TxLEV output pin of the Framer. This output pin is intended to be connected to the TxLEV input pin of the XRT73L0x DS3/E3/STS-1 LIU IC.

Writing a “1” to this bit-field commands the Framer to drive the TxLEV output pin "High”.

Writing a “0” to this bit-field commands the Framer to drive this output signal "Low”.

If the user commands this signal to toggle "High", then the Transmit Line Build-Out circuitry, within the XRT73L0x will be disabled. In this mode, the XRT73L0x LIU IC will generate unshaped (e.g., square) pulses out onto the line, via the TTIP and TRING output pins.

Conversely, if the user commands this signal to toggle "Low", then the Transmit Line Build-Out circuitry, within the XRT73L0x will be enabled. In this mode, the XRT73L0x will generate shaped pulses onto the line, via the TTIP and TRING output pins.

In order to comply with the Isolated DSX-3 Pulse Template requirements (per Bellcore GR-499-CORE), the user is advised to set this bit-field to "0" if the cable length (between the transmit output of the XRT73L0x and the DSX-3 Cross Connect System) is less than 225 feet. Conversely, the user is advised to set this bit-field to "1" if the cable length (between the transmit output of the XRT73L0x and the DSX-3 Cross Connect System) is greater than 225 feet.

NOTE: *If the customer is not using the XRT73L0x DS3/E3/STS-1 IC, then this bit-field and the TxLEV output pin can be used for other purposes.*

Bit 1 - RLOOP (Remote Loop-Back Select)

This Read/Write bit-field permits the user to control the state of the RLOOP output pin of the Framer. This output pin is intended to be connected to the RLOOP input pin of the XRT73L0x LIU IC.

The state of this bit-field (or pin) along with LLOOP are used to configure the XRT73L0x into one of four (4) loop-back modes. The relationship of the values of RLOOP, LLOOP and the resulting loop-back mode (within the XRT73L0x) is tabulated below.

TABLE 12: THE RELATIONSHIP BETWEEN THE STATES OF RLOOP, LLOOP AND THE RESULTING LOOP-BACK MODE WITH THE XRT73L0X

RLOOP	LLOOP	RESULTING LOOP-BACK MODE (WITHIN THE XRT73L0X DS3/E3/STS-1 LIU IC)
0	0	Normal Mode (No Loop-back)
0	1	Analog Local Loop-back Mode
1	0	Remote Loop-back Mode
1	1	Digital Local Loop-back Mode

Writing a "1" into this bit-field commands the Framer to drive the RLOOP output signal "High". Writing a "0" into this bit-field commands the Framer to drive this output signal "Low".

For a detailed description of the XRT73L0x LIU's operation during each of these loop-back modes, refer to the XRT73L0x DS3/E3/STS-1 LIU IC data sheet.

NOTE: *If the customer is not using the XRT73L0x DS3/E3/STS-1 LIU IC, then this bit-field and the RLOOP output pin can be used for other purposes.*

Bit 0 - LLOOP (Local Loop-back Select)

This Read/Write bit-field allows the user to control the state of the LLOOP output pin of the Framer. This output pin is intended to be connected to the LLOOP input pin of the XRT73L0x DS3/E3/STS-1 LIU IC.

The state of this bit-field (or pin) along with RLOOP are used to configure the XRT73L0x into one of four (4) loop-back modes. The relationship of the values of RLOOP, LLOOP and the resulting loop-back modes (within the XRT73L0x) are presented in Table 12.

Writing a "1" into this bit-field commands the Framer to toggle the LLOOP output pin "High". Writing a "0" into this bit-field commands the Framer to toggle this output signal "Low".

For a detailed description of the XRT73L0x LIU's operation during each of these loop-back modes, refer to the XRT73L0x DS3/E3/STS-1 LIU IC Data Sheet.

NOTE: *If the customer is not using the XRT73L0x DS3/E3/STS-1 LIU IC, then this bit-field and the LLOOP output pin can be used for other purposes.*

3.2 *Bit-Fields within the Line Interface Scan Register*

The XRT73L0x contains three output pins which can be made accessible to the Microprocessor Interface, via the Line Interface Scan register. These three output pins are listed below.

- DMO - Drive Monitor Output
- RLOL - Receive Loss of Lock Indicator
- RLOS - Receive Loss of Signal Indicator.

The logic state of each of these input pins (or output pins from the LIU) can be monitored by reading the contents of the Line Interface Scan register, as depicted below.

Line Interface Scan Register (Address = 0x81)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					DMO	RLOL	RLOS
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	1	1

Bit 2 - DMO - Drive Monitor Output

This Read-Only bit-field indicates the logic state of the DMO output pin of the Framer. This input pin is intended to be connected to the DMO output pin of the XRT73L0x DS3/E3/STS-1 LIU IC. If this bit-field contains a logic “1”, then the DMO input pin is "High”. The XRT73L0x DS3/E3/STS-1 LIU IC will set this pin "High” if the Transmit Driver Monitor circuitry (within the XRT73L0x) has not detected any bipolar signals at the MTIP and MRING inputs (of the XRT73L0x) within the last 128 $\pm$ 32 bit periods.

Conversely, if this bit-field is set to “0”, then the DMO input pin is "Low”. The XRT73L0x DS3/E3/STS-1 LIU IC will set this pin "Low” if bipolar signals are being detected at the MTIP and MRING input pins.

For more information on the user/purpose of the Drive Monitor feature, within the XRT73L0x LIU IC, refer to the XRT73L0x DS3/E3/STS-1 LIU IC Data Sheet.

NOTE: *If this customer is not using the XRT73L0x DS3/E3/STS-1 LIU IC, then this register bit-field and input pin can be used for a variety of other purposes.*

Bit 1 - RLOL - Receive Loss of Lock

This Read-Only bit-field indicates the logic state of the RLOL input pin of the Framer. This input pin is intended to be connected to the RLOL output pin of the XRT73L0x DS3/E3/STS-1 LIU IC. If this bit-field contains a logic “1”, then the RLOL input pin is "High”. The XRT73L0x LIU IC will drive this pin "High” if the clock recovery phase locked loop circuitry (within the XRT73L0x) has lost lock with the incoming DS3 or E3 data-stream and is not properly recovering clock and data.

Conversely, if this bit-field contains a logic “0”, then the RLOL input pin is "Low”. The XRT73L0x DS3/E3/STS-1 LIU IC will hold this pin "Low” for as long as this clock recovery phase-locked-loop circuit (within the XRT73L0x) is properly locked onto the incoming DS3 or E3 data stream and is properly recovering clock and data from this data stream.

Bit 0 - RLOS- Receive Loss of Signal

This Read-Only bit-field indicates the logic state of the RLOS input pin of the Framer. This input pin is intended to be connected to the RLOS output pin of the XRT73L0x DS3/E3/STS-1 LIU IC. If this bit-field contains a logic “1”, then the RLOS input pin is "High”. The XRT73L0x LIU IC will drive this signal "High” if it is currently declaring an LOS (Loss of Signal) condition.

Conversely, if this bit-field contains a logic “0”, then the RLOS input pin is "Low”. The XRT73L0x LIU IC will drive this signal "Low”, if it is NOT currently declaring an LOS (Loss of Signal) condition.

For more information on the LOS Declaration/Clearance criteria, used by the XRT73L0x, refer to the XRT73L0x DS3/E3/STS-1 LIU IC Data Sheet.

NOTE: *Asserting the RLOS input pin will cause the Framer to generate a Change in LOS Condition interrupt and declare an LOS (Loss of Signal) condition to the Microprocessor/Microcontroller. Therefore, the user is not advised to use the RLOS input pin as a General Purpose Input pin.*

4.0 DS3 OPERATION OF THE XRT72L50

The XRT72L50 can be configured to operate in the DS3 Mode by writing a “1” into bit-field 6 within the Framer Operating Mode register, as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	1	x	0	x	x	x	x

4.1 *Description of the DS3 Frames and Associated Overhead Bits*

The DS3 Frame contains 4760 bits, of which 56 bits are overhead and the remaining 4704 bits are payload bits. The payload data is formatted into packets of 84 bits and the overhead (OH) bits are inserted between these payload packets. The XRT72L50 Framer supports the following two DS3 framing formats:

- C-bit Parity
- M13

Figures 28 and 29 present the DS3 Frame Format for C-bit Parity and M13, respectively.

FIGURE 28. DS3 FRAME FORMAT FOR C-BIT PARITY

X	I	F1	I	AIC	I	F0	I	NA	I	F0	I	FEAC	I	F1	I
								I							
X	I	F1	I	UDL	I	F0	I	NA	I	F0	I	UDL	I	F1	I
P	I	F1	I	CP	I	F0	I	CP	I	F0	I	CP	I	F1	I
P	I	F1	I	FEBE	I	F0	I	FEBE	I	F0	I	FEBE	I	F1	I
M0	I	F1	I	DL	I	F0	I	DL	I	F0	I	DL	I	F1	I
M1	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I
M0	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I

X = Signaling bit for network control

I = Payload Information (84 bit packets)

Fi = Frame synchronization bit with logic value i

P = Parity bit

Mi = Multiframe synchronization bit with logic value i

AIC = Application Identification Channel

NA = reserved for network application

FEAC = Far End Alarm and Control

DL = Data Link

CP = CP (Path)-bit parity

FEBE = Far End Block Error

UDL = User Data Link

FIGURE 29. DS3 FRAME FORMAT FOR M13

X	I	F1	I	C11	I	F0	I	C12	I	F0	I	C13	I	F1	I
							I								
X	I	F1	I	C21	I	F0	I	C22	I	F0	I	C23	I	F1	I
P	I	F1	I	C31	I	F0	I	C32	I	F0	I	C33	I	F1	I
P	I	F1	I	C41	I	F0	I	C42	I	F0	I	C43	I	F1	I
M0	I	F1	I	C51	I	F0	I	C52	I	F0	I	C53	I	F1	I
M1	I	F1	I	C61	I	F0	I	C62	I	F0	I	C63	I	F1	I
M0	I	F1	I	C71	I	F0	I	C72	I	F0	I	C73	I	F1	I

X = Signaling bit for network control

I = Payload Information (84 bit packets)

Fi = Frame synchronization bit with logic value i

Cij = jth stuff code bit of ith channel

P = Parity bit

Mi = multiframe synchronization bit with logic values i

To choose between these two frame formats, write the appropriate data to bit 2 of the Framer Operating Mode Register (Address = 0x00), as depicted below.

This bit setting configures the frame format for both the Transmit and Receive Section of the XRT72L50..

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	1	x	0	x	x	x	x

TABLE 13: BIT 2 SETTING WITHIN THE FRAMER OPERATING MODE REGISTER AND THE RESULTING DS3 FRAMING FORMAT

BIT 2	DS3 FRAME FORMAT
0	C-Bit Parity
1	M13

Each of the two DS3 Frame Formats, as presented in Figure 28 and Figure 29, constitute an M-frame or a full DS3 Frame. Each M-frame consists of 7 - 680 bit F-frames, sometimes referred to as subframes. Each F-frame is represented by the individual rows of payload and overhead bits and can be further divided into 8

blocks of 85 bits, with 84 of the 85 bits available for payload information and the remaining one bit used for frame overhead.

Differences Between the M13 and C-Bit Parity Frame Formats

The frame formats for M13 and C-bit Parity are very similar. However, the main difference between these two framing formats is in the use of the C-bits. In the M13 Format, the C-bits reflect the status of stuff-opportunities that either were or were not used while multiplexing the 7 DS2 signals into this DS3 signal. If two of the three stuff bits within a F-frame are "1", then the associated stuff bit, Si (not shown in Figure 29), is interpreted as being a stuff bit. In the C-bit Parity framing format, the C bits take on different roles, as presented in Table 14.

TABLE 14: C-BIT FUNCTIONS FOR THE C-BIT PARITY DS3 FRAME FORMAT

C - BIT	C-BIT FUNCTION IN THE C-BIT PARITY FRAMING FORMAT
C11	AIC (C-Bit Parity Mode)
C12	NA (Reserved for Network Application)
C13	FEAC (Far End Alarm & Control)
C21, C22, C23	(UDL) User Data Link (undefined for DS3 Frame)
C31, C32, C33	CP (Path) Parity Bits
C41, C42, C43	FEBE (Far End Block Error) Indicators
C51, C52, C53	(DL) Path Maintenance Data Link
C61, C62, C63, C71, C72, C73	(UDL) User Data Link (undefined for DS3 Frame)

Definition of the DS3 Frame Overhead Bits

In general, the DS3 Frame Overhead Bits serve the following three purposes:

1. Support Frame Synchronization between the Local and Remote DS3 Terminals
2. Provide parity bits to facilitate performance monitoring and error detection.
3. Support the transmission of Alarms, Status and Data Link information to the Remote DS3 Terminal.

4.1.1 Frame Synchronization Bits (Applies to both M13 and C-bit Parity Framing Formats)

Each DS3 Frame (M-frame) contains a total of 31 bits that support frame synchronization. Each DS3 M-frame contains three M-bits. According to Figure 28 and Figure 29, these M-bits are the first bits in F-frames 5, 6 and 7. These three bits appear in each M-frame with the repeating pattern of "010". This fact is also presented in Figure 28 and Figure 29, which contains bit-fields that are designated as: M0, M1, and M0 (where M0 = "0", and M1 = "1").

Each F-frame contains four F-bits, which also aid in synchronization between the Local and the remote DS3 terminals. Therefore, each DS3 M-frame consists of a total of 28 F-bits. These F-bits exhibit a repeating pattern of "1001" within each F-frame. This fact is also presented in Figure 28 and Figure 29, which contains bit-fields that are designated as: F1, F0, F0, and F1 (where F0 = "0", and F1 = "1").

Each of these bit-fields are used by the Receive DS3 Framer block within the remote terminal equipment to perform Frame Acquisition and Frame Maintenance functions.

NOTE: *For more information on how the Receive DS3 Framer uses these bit-fields, please see* Section 4.3.2

4.1.2 Performance Monitoring/Error Detection Bits (Parity)

The DS3 Frame uses numerous bit fields to support performance monitoring of the transmission link between the Local Transmitting Terminal and the Remote Receiving Terminal. The DS3 frame can contain two types of parity bits, depending upon the framing format chosen. P-bits are available in both the M13 and C-bit Parity Formats. However, the C-bit Parity format also includes additional CP-Parity bits.

P-Bits (Applies to both M13 and C-Bit Parity Frame Formats)

Each DS3 M-frame consists of two (2) P-bits. These two P-bits carry the parity information of the previous DS3 frame for performance monitoring. These two P-bits must be identical within a given DS3 frame. The Transmit Section computes the even parity over all 4704 payload bits within a given DS3 frame and inserts the resulting parity information in the P-bit fields of the very next DS3 frame. The two P-bits are set to "1" if the payload of the previous DS3 frame consists of an odd number of "ones" in the frame. The two P-bits are set to zero if an even number of "ones" is found in the payload of the previous DS3 frame.

NOTE: *For information on how the Receive DS3 Framer handles P-bits, please see* Section 4.3.2.6.1.

CP-(Path) Parity Bits (Applies to only the C-Bit Parity Framing Format)

Each DS3 M-Frame consists of two (2) CP-Bits. These two bits have a very similar role to those of P-Bits. Further, the XRT72L50 processes CP-Bits in an identical manner that it handles P-Bits.

Both P and CP Bits are computed over the Payload Bits only.

However for some DS3 applications there is a difference between P and CP-bits, that should be noted.

- P-Bits are used to support error detection of a DS3 data stream as it travels from one T.E. to the next. (e.g., a single DS3 link between two T.E.)
- CP-Bits are used to support error detection of DS3 data stream as it travels from the Source T.E., where the DS3 Data Stream originated, to the Sink T.E, where the DS3 Data Stream is terminated. This transmission path from Source T.E. to Sink T.E. may involve numerous T.E.
- P-Bits are verified and recomputed as it passes through a Mid-Network T.E., which is neither a Source nor Sink T.E.
- The values of the CP-Bits as generated by the Source T.E. must be preserved as a DS3 frame travels to the Sink T.E. through any number of Mid-Network T.E.

NOTE: *For more information on how CP-Bits are processed, please see* Section 4.3.2.6.2

4.1.3 Alarm and Signaling-Related Overhead Bits

The DS3 frame consists of numerous bit-fields which are used to support the handling of alarm and signaling information.

The Alarm Indication Signal (AIS) Pattern (Applies to both M13 and C-Bit Parity Frame Formats)

The AIS pattern is an alarm signal that is inserted into the outbound DS3 stream when a failure is detected by the Local Terminal. The Transmit DS3 Framer generates the AIS pattern as defined in ANSI.T1.107a-1990 which is described as follows.

- All C-bits are zeros
- All X-bits are set to "1"
- Valid M-bits, F-bits, and P-bits
- A repeating "1010..." pattern is written into the payload of the DS3 frames.

No user or payload data will be transmitted while the Transmit Section of the chip is transmitting the AIS pattern.

The IDLE Condition Signal (Applies to both M13 and C-Bit Parity Frame Formats)

The IDLE Condition signal is used to indicate that the DS3 channel is functionally sound, but has not yet been assigned any traffic. The Transmit Section will transmit the IDLE Condition signal as defined in ANSI T1.107a-1990, which is described as follows.

- Valid M-bits, F-bits, and P-bits
- The three CP-bits (F-frame #3) are zeros
- The X-bits are set to "1"
- A repeating "1100.." pattern is written into the payload of the DS3 frames.

FEAC - Far End Alarm & Control (Only available for the C-bit Parity Frame Format)

The third C-bit (C13 or FEAC) in the first F-frame is used as the FEAC channel between the Near-End DS3 terminal and the Remote DS3 terminal. The FEAC channel carries:

- Alarm and Status Information
- Loop-back commands to initiate and deactivate DS3 and DS1 loop-backs at the distant terminals.

The FEAC message consists of a six (6) bit code word of the form [d5, d4, d3, d2, d1 d0]. This message is encapsulated with 10 framing bits to form a 16 bit FEAC Message, as illustrated below. The FEAC signals are encoded into repeating 16 bit message of the form:

0	d5	d4	d3	d2	d1	d0	0	1	1	1	1	1	1	1	1

Since each DS3 frame carries only one FEAC bit, 16 DS3 frames are required to deliver 1 complete FEAC message. The six bits labeled "dx" can represent upto 64 distinct messages, of which 43 have been defined in the standards.

NOTE: *For more information on the transmission of FEAC Messages, please see* Section 4.2.3.1.

FEBE - Far End Block Error (Only available for the C-bit Parity Frame Format)

F-Frame # 4 consists of 3 bit fields for the FEBE channel. If the Local Receive Section detects P-bit parity errors, CP-bit errors or a framing error on the incoming (received) DS3 stream it informs the Transmit Section. The Transmit Section then sets the three FEBE bits within an outgoing DS3 Frame to any pattern other than "111" to indicate an error and then transmits this information out to the Remote Terminal (e.g., the source of the errored-data). The FEBE bits in the outbound DS3 frames are set to "111" only if both of the following conditions are true:

- The Receive DS3 Framer has detected no M-bit or F-bit framing errors, and
- No P-Bit parity errors have been detected.
- No CP-Bit errors have been detected.

NOTE: *For more information on the Transmit Section's handling of the FEBE bit-fields, see* Section 4.2.4.2.1.9.

The Yellow Alarm or FERF (Far-End Receive Failure) Indicator

The X-bits are used for sending Yellow Alarms or the FERF indication. When the Receive Section of the XRT72L50 within the Remote Receiving terminal equipment, cannot identify valid framing or detects an AIS pattern in the incoming DS3 data-stream, the Framer can be configured such that the Transmit Section will send a Yellow Alarm or a FERF indication to the Remote Terminal by setting both of the X-bits to zero in the outbound (returning) DS3 path. The X-bits are set to "1" during non-alarm conditions.

4.1.4 The Data Link Related Overhead Bits

UDL: User Data Link (C-bit Parity Frame Format Only)

These bit-fields are not used by the framer and are set to "1" by default. However, these bits may be used for the transmission of data via a proprietary data link. These bit-fields can be accessed via the Transmit Overhead Data Input Interface and the Receive Overhead Data Output Interface blocks.

DL: Path Maintenance Data Link (C-bit Parity Frame Format Only)

The LAPD transceiver block uses these bit-fields for the transmission and reception of path maintenance data link (PMDL) messages via ITU-T Q.921 (LAP-D) Message frames.

NOTE: *For more information on the LAPD Transmitter, see* Section 4.2.3.2 *and* Section 4.3.3.2 .

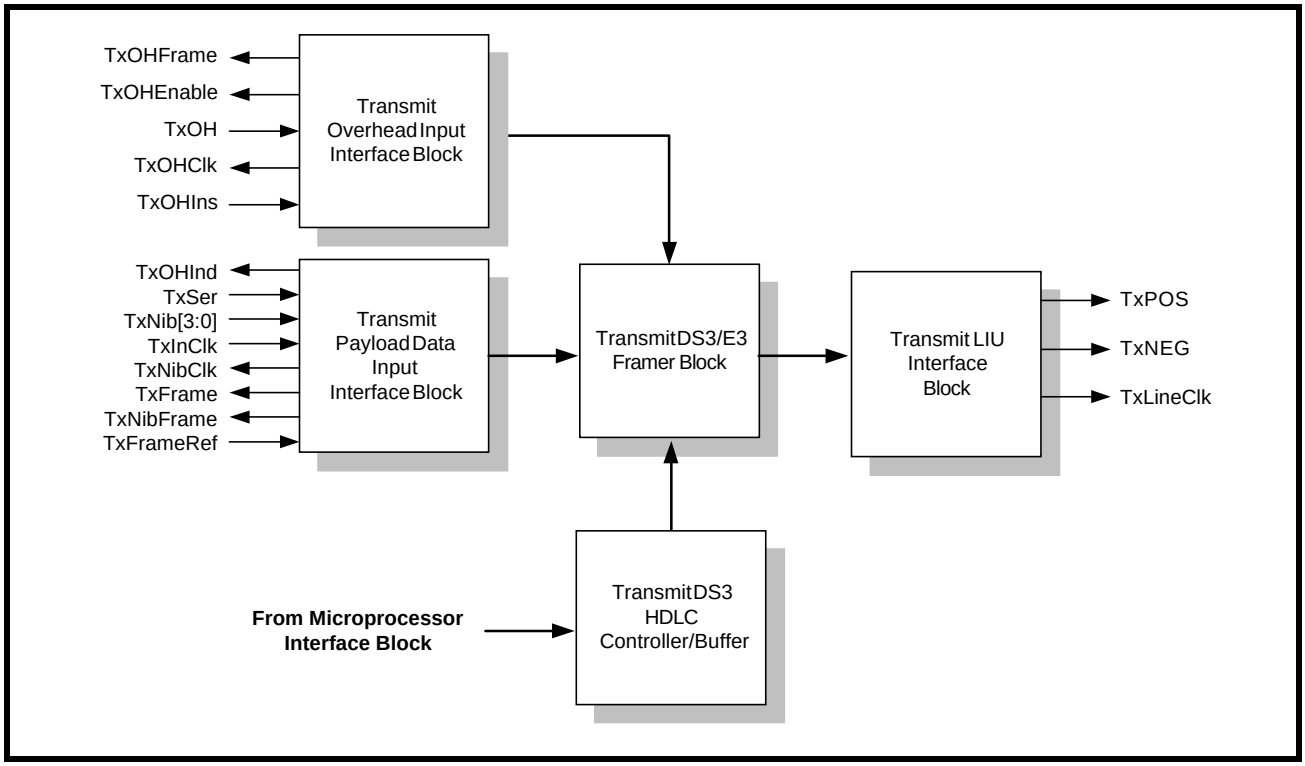
4.2 *The Transmit Section of the XRT72L50 (DS3 Mode Operation)*

When the XRT72L50 has been configured to operate in the DS3 Mode, the Transmit Section of the XRT72L50 consists of the following functional blocks (Figure 30).

- Transmit Payload Data Input Interface block
- Transmit Overhead Data Input Interface block
- Transmit DS3 Framer block
- Transmit DS3 HDLC Controller block

- Transmit LIU Interface block

FIGURE 30. THE XRT72L50 TRANSMIT SECTION CONFIGURED TO OPERATE IN THE DS3 MODE



4.2.1 The Transmit Payload Data Input Interface Block

FIGURE 31. THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK

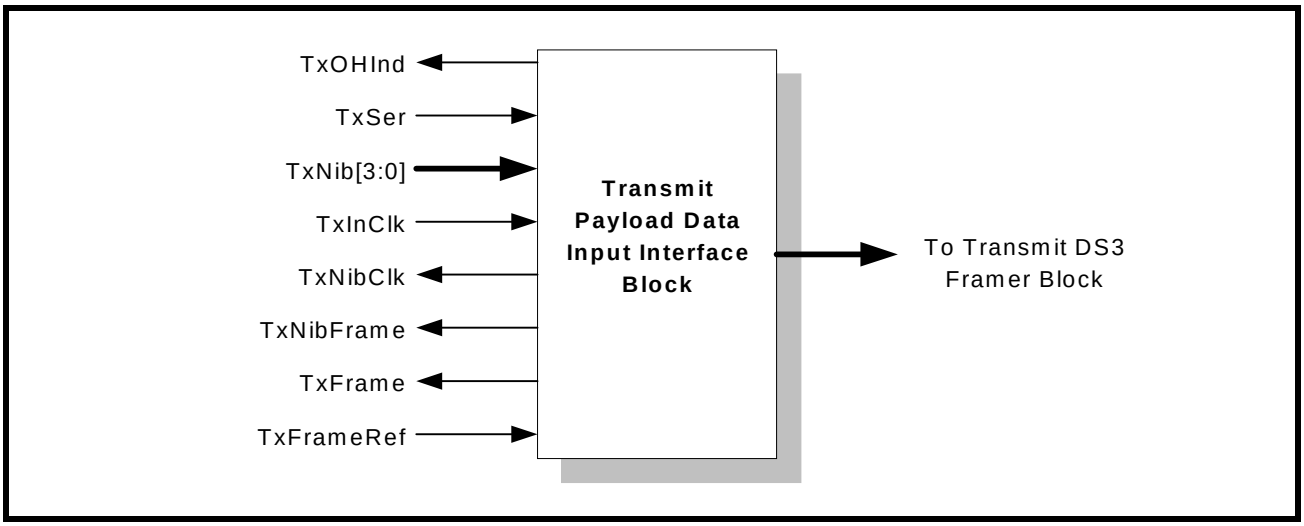


TABLE 15: DESCRIPTIONS FOR THE PINS ASSOCIATED WITH THE TRANSMIT PAYLOAD DATA INPUT INTERFACE

SIGNAL NAME	TYPE	DESCRIPTION
TxSer	I	**Transmit Serial Payload Data Input Pin:** To operate the XRT72L50 in the serial mode, the Terminal Equipment is expected to apply the payload data that is to be transported via the outbound DS3 data stream to this input pin. The XRT72L50 samples the data that is at this input pin upon the rising edge of either the RxOutClk or the TxInClk signal (whichever is appropriate). This signal is only active if the NibIntf input pin is pulled "Low".
TxNib[3:0]	I	**Transmit Nibble-Parallel Payload Data Input pins:** To operate the XRT72L50 in the Nibble-Parallel mode, the Terminal Equipment is expected to apply the payload data that is to be transported via the outbound DS3 data stream to these input pins. The XRT72L50 samples the data that is at these input pins upon the rising edge of the TxNibClk signal. These pins are only active if the NibIntf input pin is pulled "High".
TxNibFrame	O	**Transmit End of Frame Output Indicator - Nibble Mode** The Transmit Section of the XRT72L50 pulses this output pin "High" for one nibble-period when the Transmit Payload Data Input Interface is processing the last nibble of a given DS3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 frame to the XRT72L50.
TxInClk	I	**Transmit Section Timing Reference Clock Input pin:** The Transmit Section of the XRT72L50 can be configured to use this clock signal as the Timing Reference. If this configuration is selected, then the XRT72L50 uses this clock signal to sample the data on the TxSer input pin and a DS3 or E3 clock signal must be applied to this pin.
TxNibClk	O	**Transmit Nibble Mode Output** To operate the XRT72L50 in the Nibble-Parallel mode, then the XRT72L50 will derive this clock signal from the selected Timing Reference for the Transmit Section of the chip (e.g., either the TxInClk or the RxLineClk signals). It is advisable to configure the Terminal Equipment to output the outbound payload data (to the XRT72L50 Framer IC) onto the TxNib[3:0] input pins, upon the rising edge of this clock signal. For DS3 Applications, the XRT72L50 Framer IC will output 1176 clock edges (to the Terminal Equipment) for each outbound DS3 frame.

TABLE 15: DESCRIPTIONS FOR THE PINS ASSOCIATED WITH THE TRANSMIT PAYLOAD DATA INPUT INTERFACE

SIGNAL NAME	TYPE	DESCRIPTION
TxOHInd	O	**Transmit Overhead Bit Indicator Output:** This output pin pulses "High" one-bit period prior to the time that the Transmit Section of the XRT72L50 is processing an Overhead bit. The purpose of this output pin is to warn the Terminal Equipment that during the very next bit-period, the XRT72L50 is going to be processing an Overhead bit and ignoring any data that is applied to the TxSer input pin. For DS3 applications, this output pin is only active if the XRT72L50 is operating in the Serial Mode. This output pin is pulled "Low" if the device is operating in the Nibble-Parallel Mode.
TxFrame	O	**Transmit End of Frame Output Indicator:** The Transmit Section of the XRT72L50 pulses this output pin "High" for one bit-period when the Transmit Payload Data Input Interface is processing the last bit of a given DS3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 frame to the XRT72L50 (e.g., to permit the XRT72L50 to maintain Transmit DS3 framing alignment control over the Terminal Equipment).
TxFrameRef	I	**Transmit Frame Reference Input:** The XRT72L50 permits the configuration of the Transmit Section to use this input pin as a frame reference. If this configuration is selected, then the Transmit Section initiates its transmission of a new DS3 frame upon the rising edge of this signal. The purpose of this input pin is to permit the Terminal Equipment to maintain Transmit DS3 Framing alignment control over the XRT72L50.
RxOutClk	O	**Loop-Timed Timing Reference Clock Output pin:** The Transmit Section of the XRT72L50 can be configured to use the RxLineClk signal as the Timing Reference (e.g., loop-timing). If this configuration is selected, then the XRT72L50 outputs a 44.736 MHz clock signal via this pin to the Terminal Equipment and samples the data on the TxSer input pin upon the rising edge of this clock signal.

Operation of the Transmit Payload Data Input Interface

The Transmit Payload Data Input Interface permits the following configuration options.

- The Serial or the Nibble-Parallel Interface Mode
- The Loop-Timing or the TxInClk (Local Timing) Mode

If the XRT72L50 has been configured to operate in the TxInClk mode, then there are two additional options.

- The XRT72L50 functions as the Frame Master (e.g., it dictates when the Terminal Equipment initiates the transmission of data within a new DS3 frame).
- The XRT72L50 functions as the Frame Slave (e.g., the Terminal Equipment dictates when the XRT72L50 initiates the transmission of a new DS3 frame).

Given these three set of options, the Transmit Terminal Input Interface can be configured to operate in one of the six (6) following modes.

- Mode 1 - Serial/Loop-Timed Mode
- Mode 2 - Serial/Local-Timed/Frame Slave Mode
- Mode 3 - Serial/Local-Timed/Frame Master Mode
- Mode 4 - Nibble/Loop-Timed Mode
- Mode 5 - Nibble/Local-Timed/Frame Slave Mode
- Mode 6 - Nibble/Local-Timed/Frame Master Mode

4.2.1.1 *Mode 1 - Serial/Loop-Timing Mode Behavior of the XRT72L50*

The XRT72L50 configured to operate in this mode behaves as follows.

Loop-Timing

The Transmit Section of the XRT72L50 uses the RxLineClk input clock signal (e.g., the Recovered Clock signal, from the LIU) as its timing source and does the following:

- Ignores any signal at the TxInClk input pin.
- The XRT72L50 outputs a 44.736MHz clock signal via the RxOutClk output pin. This clock signal functions as the Transmit Payload Data Input Interface block clock signal.
- The XRT72L50 uses the rising edge of the RxOutClk signal to latch in the data residing on the TxSer input pin.

Serial Mode

The XRT72L50 accepts the DS3 payload data from the Terminal Equipment in a serial-manner via the TxSer input pin. The Transmit Payload Data Input Interface block samples this data on the rising edge of the RxOutClk signal.

Delineation of outbound DS3 frames

The XRT72L50 pulses the TxFrame output pin "High" for one bit-period coincident with the XRT72L50 processing the last bit of a given DS3 frame.

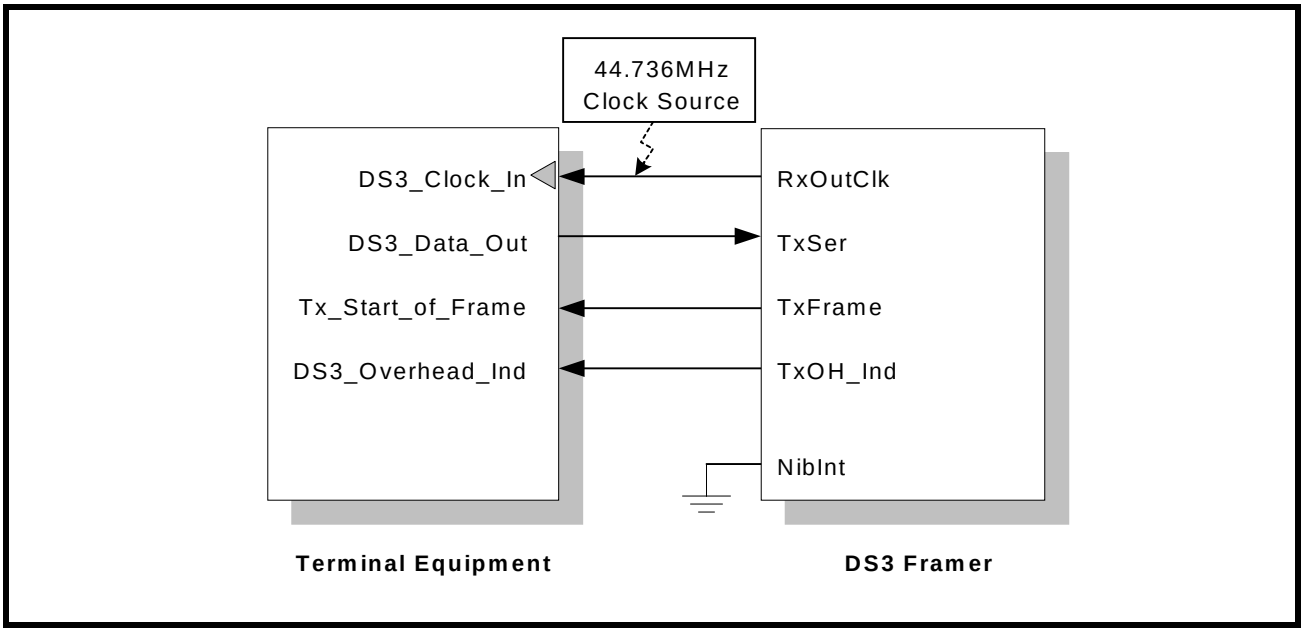
Sampling of Payload Data from the Terminal Equipment

The XRT72L50 samples the data at the TxSer input on the rising edge of RxOutClk.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 1 Operation

This is illustrated in Figure 32.

FIGURE 32. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 1(SERIAL/LOOP-TIMED) OPERATION



Mode 1, Operation of the Terminal Equipment

When the XRT72L50 is operating in this mode it functions as the source of the 44.736MHz clock signal via the RxOutClk signal. This clock signal is used as the Terminal Equipment Interface clock by both the XRT72L50 and the Terminal Equipment.

The Terminal Equipment serially outputs the payload data of the outbound DS3 data stream via its DS3_Data_Out pin. The Terminal Equipment updates the data on the DS3_Data_Out pin upon the rising edge of the 44.736 MHz clock signal at its DS3_Clock_In input pin as depicted in Figure 32 and Figure 33.

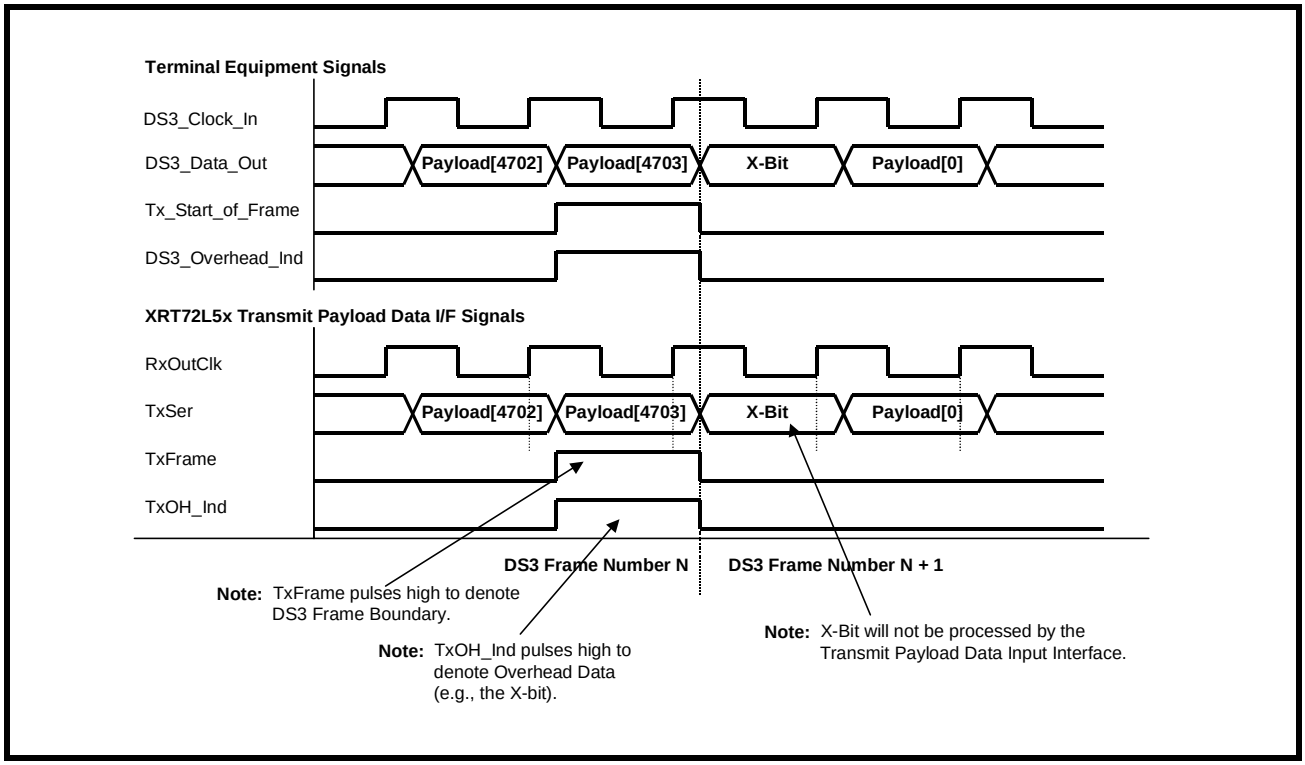
The XRT72L50 latches the outbound DS3 data stream from the Terminal Equipment on the rising edge of the RxOutClk signal.

The XRT72L50 indicates that it is processing the last bit within a given outbound DS3 frame by pulsing its TxFrame output pin "High" for one bit-period. When the Terminal Equipment detects this pulse at its Tx_Start_of_Frame input, it is expected to begin transmission of the very next outbound DS3 frame to the XRT72L50 via the DS3_Data_Out (or TxSer pin).

Finally, the XRT72L50 indicates that it is about to process an overhead bit by pulsing the TxOH_Ind output pin "High" one bit period prior to its processing. In Figure 32, the TxOH_Ind output pin is connected to the DS3_Overhead_Ind input pin of the Terminal Equipment. Whenever the DS3_Overhead_Ind pin is pulsed "High", the Terminal Equipment is expected to not transmit a DS3 payload bit upon the very next clock edge. Instead, the Terminal Equipment is expected to delay its transmission of the very next payload bit by one clock cycle.

The behavior of the signals between the XRT72L50 and the Terminal Equipment for DS3 Mode 1 operation is illustrated in Figure 33.

FIGURE 33. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK OF THE XRT72L50 AND THE TERMINAL EQUIPMENT (MODE 1 OPERATION)



How to configure the XRT72L50 into the Serial/Loop-Timed/Non-Overhead Interface Mode

1. Set the NibIntf input pin "Low".
2. Set the TimRefSel[1:0] bit fields within the Framer Operating Mode Register to "00", as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	0

3. Interface the XRT72L50 to the Terminal Equipmen as illustrated in Figure 32.

The XRT72L50 cannot support the Framer Local Loop-back Mode of operation when operating in the Loop-Timing Mode. The XRT72L50 must be configured into any of the following modes prior to configuring the Framer Local Loop-back Mode.

- Mode 2 - Serial/Local-Timed/Frame-Slave Mode.
- Mode 3 - Serial/Local-Timed/Frame-Master Mode.
- Mode 5 - Nibble-Parallel/Local-Timed/Frame-Slave Mode.
- Mode 6 - Nibble-Parallel/Local-Timed/Frame-Master Mode.

NOTE: *For more detailed information on Framer Local Loop-back Mode of operation, see* Section 7.0.

4.2.1.2 *Mode 2 - The Serial/Local-Timed/Frame-Slave Mode Behavior of the XRT72L50*

The XRT72L50 configured to operate in this mode functions as follows.

Local-Timing

The Transmit Section of the XRT72L50 uses the TxInClk signal as its timing reference.

Serial Mode

The XRT72L50 receives the DS3 payload data in a serial manner via the TxSer input pin. The Transmit Payload Data Input Interface within the XRT72L50 latches this data into its circuitry on the rising edge of the TxInClk input clock signal.

Delineation of outbound DS3 frames (Frame Slave Mode)

The Transmit Section of the XRT72L50 uses the TxInClk input as its timing reference and the TxFrameRef input signal as its framing reference. The Transmit Section of the XRT72L50 initiates frame generation upon the rising edge of the TxFrameRef input signal.

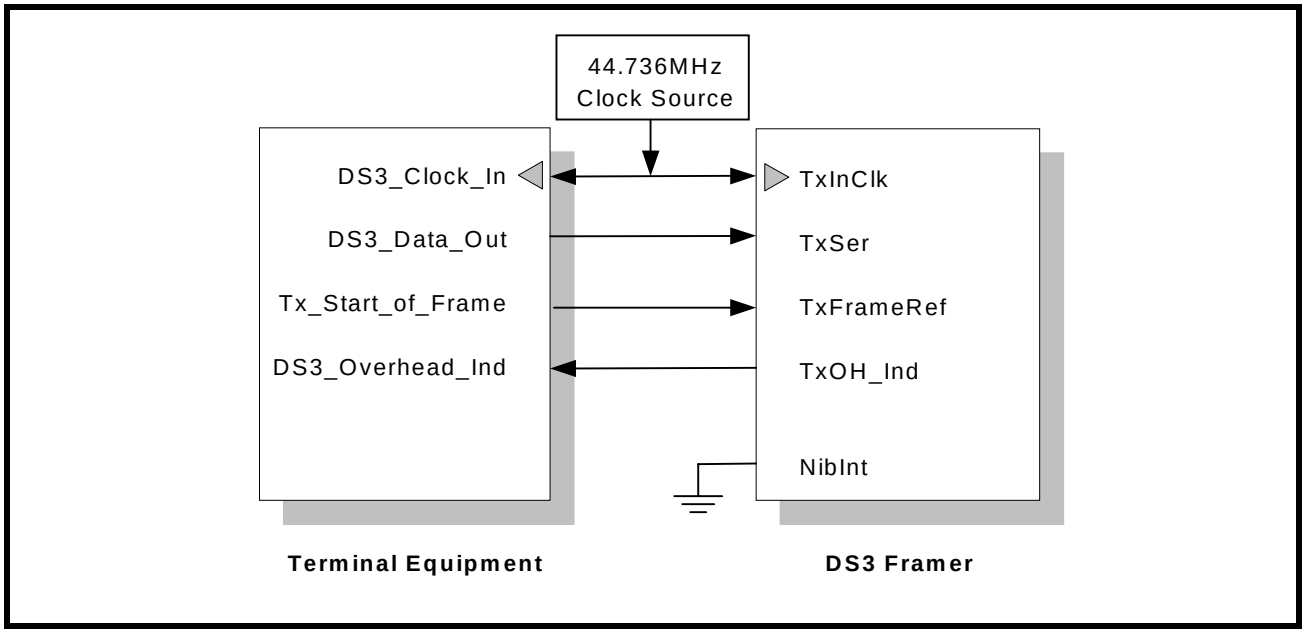
Sampling of payload data from the Terminal Equipment

In Mode 2, the XRT72L50 samples the data at the TxSer input pin on the rising edge of TxInClk.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 2 Operation

This is illustrated in Figure 34.

FIGURE 34. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 2 (SERIAL/LOCAL-TIMED/FRAME-SLAVE) OPERATION



Mode 2, Operation of the Terminal Equipment

As shown in Figure 34, both the Terminal Equipment and the XRT72L50 are driven by an external 44.736MHz clock signal. The Terminal Equipment receives the 44.736MHz clock signal via its DS3_Clock_In input pin and the XRT72L50 Framer receives the 44.736MHz clock signal via the TxInClk input pin.

The Terminal Equipment serially outputs the payload data of the outbound DS3 data stream via the DS3_Data_Out output pin upon the rising edge of the signal at the DS3_Clock_In input pin.The DS3_Data_Out output pin of the Terminal Equipment is electrically connected to the TxSer input pin.

The XRT72L50 Framer latches the data residing on the TxSer input line on the rising edge of the TxInClk signal.

The Terminal Equipment has the responsibility of providing the framing reference signal by pulsing its Tx_Start_of_Frame output signal and the TxFrameRef input pin of the XRT72L50 "High" for one-bit period, coincident with the first bit of a new DS3 frame. Once the XRT72L50 detects the rising edge of the input at its TxFrameRef input pin, it begins generation of a new DS3 frame.

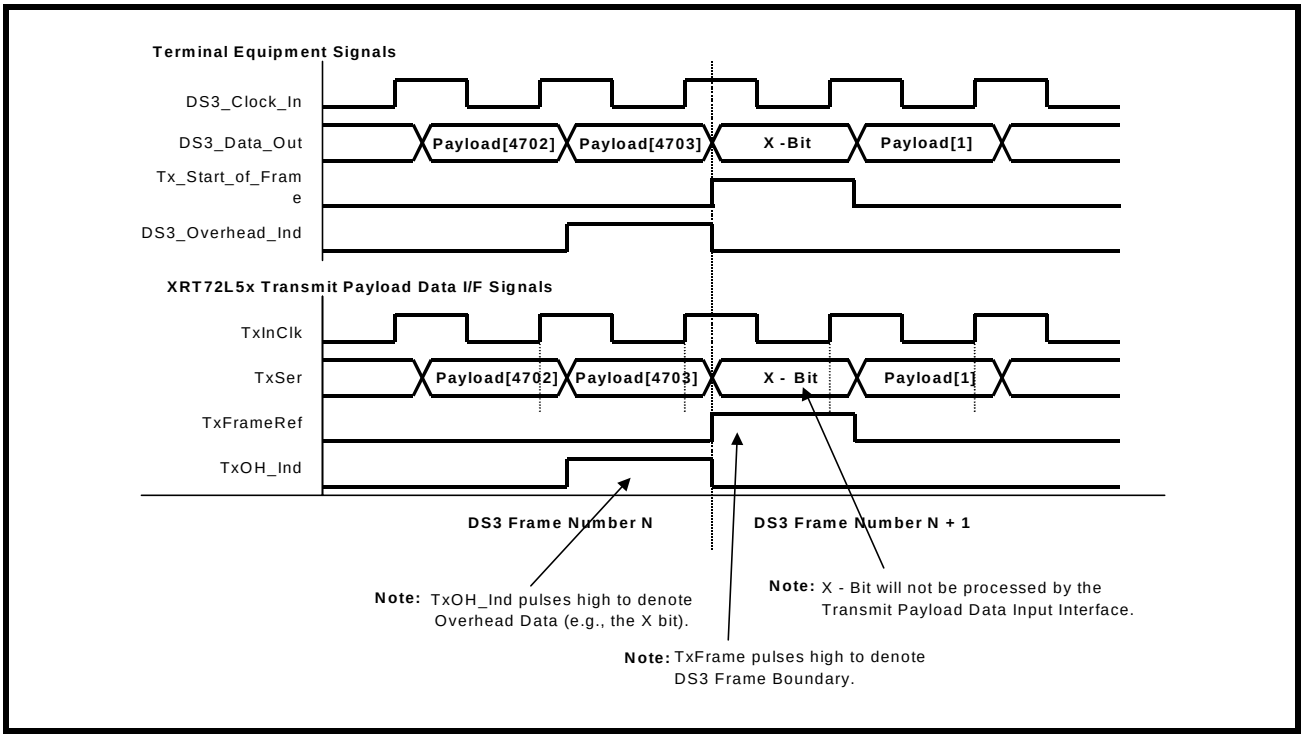
In this case, the Terminal Equipment is controlling the start of Frame Generation and is referred to as the Frame Master. Since the XRT72L50 does not control the generation of a new DS3 frame, but is rather driven by the Terminal Equipment it is referred to as the Frame Slave.

If the XRT72L50 is configured to operate in Mode 2, it is imperative that the Tx_Start_of_Frame or TxFrameRef signal is synchronized to the TxInClk input clock signal.

Finally, the XRT72L50 pulses its TxOH_Ind output pin one bit-period prior to it processing a given overhead bit within the outbound DS3 frame. Since the TxOH_Ind output pin of the XRT72L50 is electrically connected to the DS3_Overhead_Ind whenever the XRT72L50 pulses the TxOH_Ind output pin "High", it also drives the DS3_Overhead_Ind input pin of the Terminal Equipment "High". Whenever the Terminal Equipment detects this pin toggling "High" it should delay transmission of the very next DS3 frame payload bit by one clock cycle.

The behavior of the signals between the XRT72L50 and the Terminal Equipment for DS3 Mode 2 Operation is illustrated in Figure 35.

FIGURE 35. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (MODE 2 OPERATION)



How to configure the XRT72L50 to operate in this mode.

1. Set the NibIntf input pin "Low".
2. Set the TimRefSel[1:0] bit-fields within the Framer Operating Mode Register to "01" as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	1

3. Interface the XRT72L50 to the Terminal Equipment as illustrated in Figure 34.

4.2.1.3 *Mode 3 - The Serial/Local-Timed/Frame-Master Mode Behavior of the XRT72L50*

The XRT72L50 configured to operate in this mode functions as follows.

Local Timing

The Transmit Section of the XRT72L50 uses the TxInClk signal as its timing reference.

Serial Mode

The XRT72L50 receives the DS3 payload data in a serial manner via the TxSer input pin. The Transmit Payload Data Input Interface within the XRT72L50 latches this data into its circuitry on the rising edge of the TxInClk input clock signal.

Delineation of outbound DS3 frames (Frame Master Mode)

The Transmit Section of the XRT72L50 uses the TxInClk signal as its timing reference and initiates DS3 frame generation asynchronously with respect to any externally applied signal. The XRT72L50 pulses its TxFrame output pin "High" whenever it is processing the very last bit-field within a given DS3 frame.

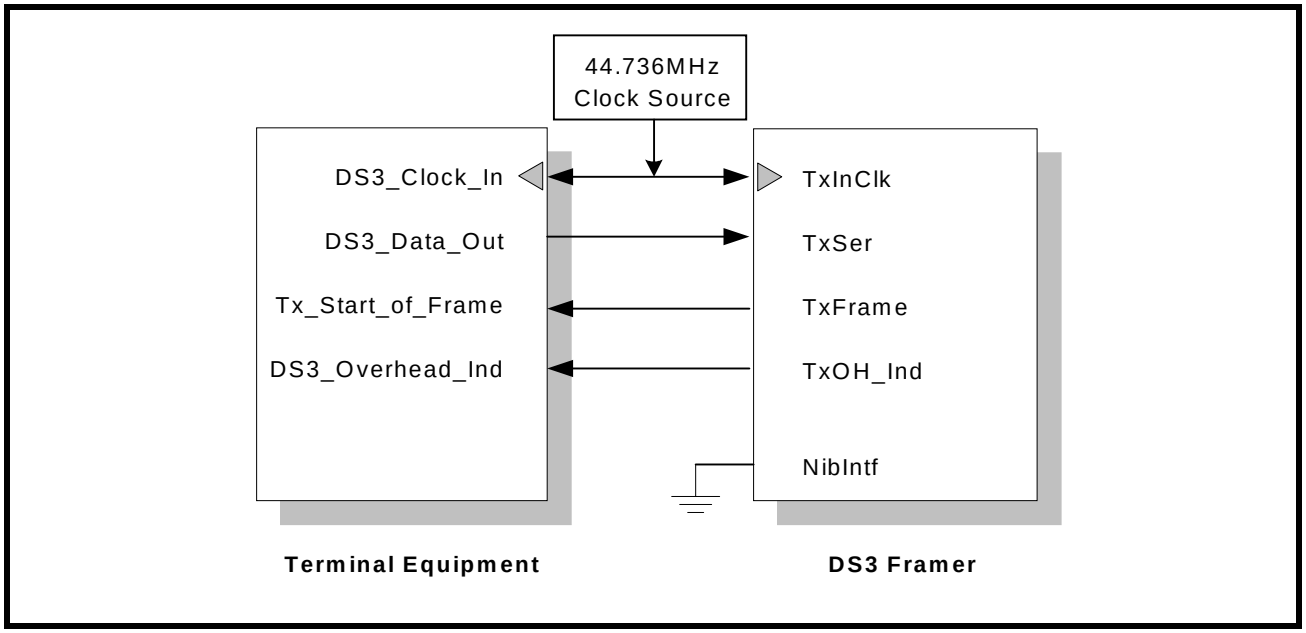
Sampling of payload data from the Terminal Equipment

In Mode 3, the XRT72L50 samples the data at the TxSer input pin on the rising edge of TxInClk.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 3 Operation

This is illustrated in Figure 36.

FIGURE 36. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 3 (SERIAL/LOCAL-TIMED/FRAME-MASTER) OPERATION



Mode 3 Operation of the Terminal Equipment

In Figure 36, both the Terminal Equipment and the XRT72L50 are driven by an external 44.736MHz clock signal. This clock signal is connected to the DS3_Clock_In input pin of the Terminal Equipment and the TxInClk input pin of the XRT72L50.

The Terminal Equipment serially outputs the payload data on its DS3_Data_Out output pin upon the rising edge of the signal at the DS3_Clock_In input pin. The XRT72L50 latches the data residing on the TxSer input pin on the rising edge of TxInClk.

The XRT72L50 pulses the TxFrame output pin "High" for one bit-period coincident while it is processing the last bit-field within a given outbound DS3 frame. The Terminal Equipment is expected to monitor the TxFrame signal from the XRT72L50 and to place the first bit within the very next outbound DS3 frame on the TxSer input pin.

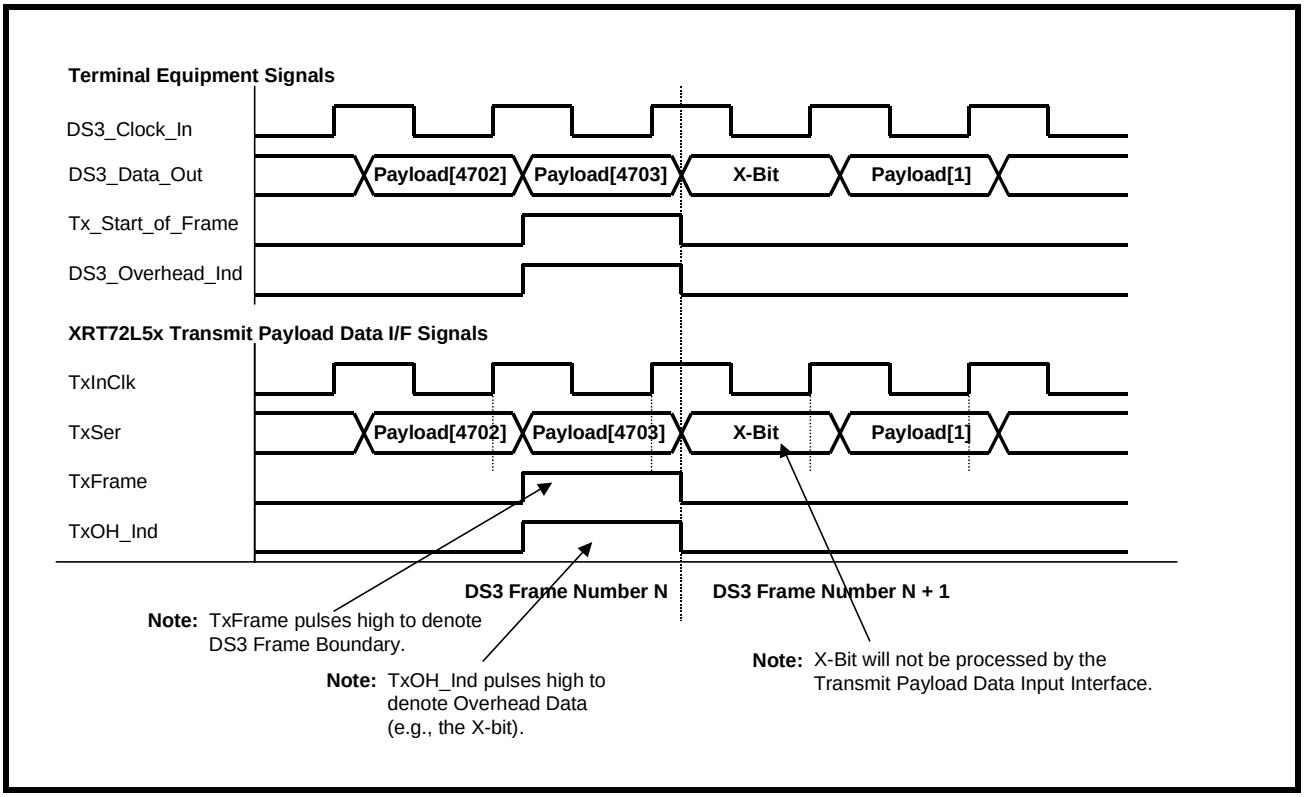
In this case, the XRT72L50 dictates exactly when the very next DS3 frame is generated.

The Terminal Equipment is expected to respond appropriately by providing the XRT72L50 with the first bit of the new DS3 frame upon demand. In this mode the XRT72L50 is referred to as the Frame Master and the Terminal Equipment is referred to as the Frame Slave.

Finally, the XRT72L50 pulses its TxOH_Ind output pin one bit-period prior to it processing a given overhead bit within the outbound DS3 frame. Since the TxOH_Ind output pin of the XRT72L50 is electrically connected to the DS3_Overhead_Ind whenever the XRT72L50 pulses the TxOH_Ind output pin "High", it also drives the DS3_Overhead_Ind input pin of the Terminal Equipment "High". Whenever the Terminal Equipment detects this pin toggling "High", it should delay transmission of the very next DS3 frame payload bit by one clock cycle.

The behavior of the signal between the XRT72L50 and the Terminal Equipment for DS3 Mode 3 Operation is illustrated in Figure 37.

FIGURE 37. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (DS3 MODE 3 OPERATION)



How to configure the XRT72L50 to operate in this mode.

1. Set the NibIntf input pin "Low".
2. Set the TimRefSel[1:0] bit-fields within the Framer Operating Mode Register to "10" or "11" as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	X

3. Interface the XRT72L50 to the Terminal Equipment as illustrated in Figure 36.

4.2.1.4 *Mode 4 - The Nibble-Parallel/Loop-Timed Mode Behavior of the XRT72L50*

The XRT72L50 configured to operate in this mode behaves as follows:

Looped Timing

The Transmit Section of the XRT72L50 uses the RxLineClk signal as its timing reference. When the XRT72L50 is operating in the Nibble-Mode, it internally divides the RxLineClk signal by a factor of four (4) and outputs this signal via the TxNibClk output pin.

Nibble-Parallel Mode

The XRT72L50 accepts the DS3 payload data from the Terminal Equipment in a nibble-parallel manner via the TxNib[3:0] input pins. The Transmit Terminal Equipment Input Interface block latches this data into its circuitry on the rising edge of the TxNibClk output signal.

Delineation of the outbound DS3 frames

The XRT72L50 pulses the TxNibFrame output pin "High" for one bit-period coincident with the XRT72L50 processing the last nibble of a given DS3 frame.

Sampling of payload data from the Terminal Equipment

In Mode 4, the XRT72L50 samples the data at the TxNib[3:0] input pins on the third rising edge of the RxOutClk clock signal following a pulse in the TxNibClk signal (see Figure 39).

The TxNibClk signal from the XRT72L50 operates nominally at 11.184 MHz (e.g., 44.736 MHz divided by 4). However, TxNibClk effectively operates at a Low clock frequency. The Transmit Payload Data Input Interface is only used to accept the payload data which is intended to be carried by outbound DS3 frames. The Transmit Payload Data Input Interface is not designed to accommodate the entire DS3 data stream.

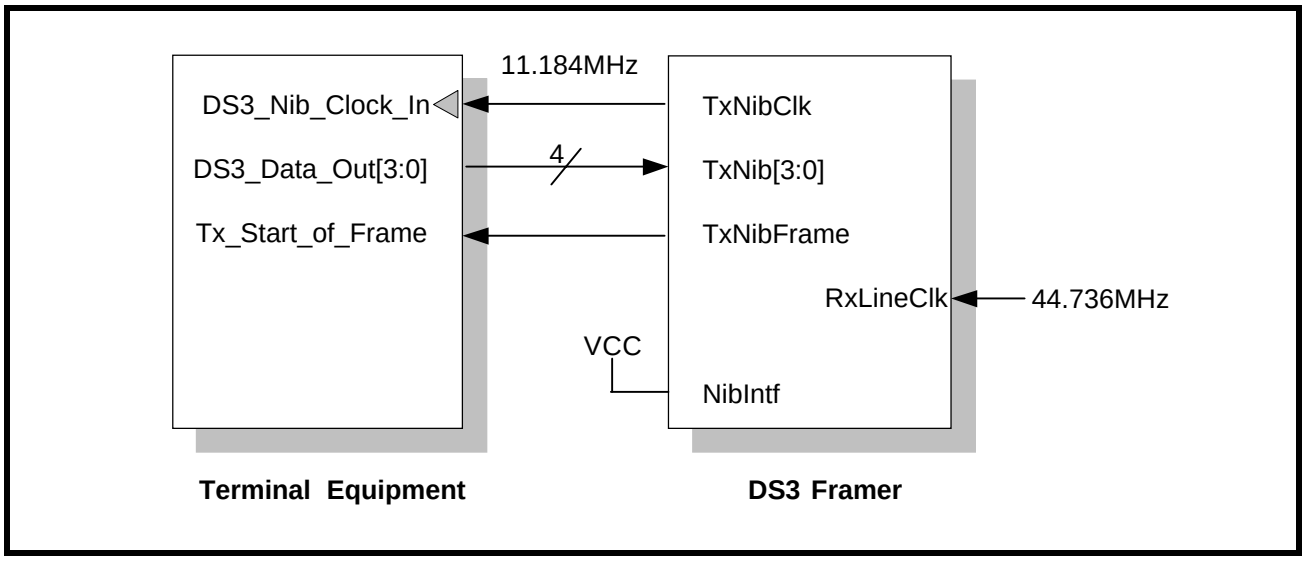
The DS3 Frame consists of 4704 payload bits or 1176 nibbles. Therefore, the XRT72L50 supplies 1176 TxNibClk pulses between the rising edges of two consecutive TxNibFrame pulses. The DS3 Frame repetition rate is 9.398kHz. Hence, 1176 TxNibClk pulses for each DS3 frame period amounts to TxNibClk running at approximately 11.052 MHz. The method by which the 1176 TxNibClk pulses are distributed throughout the DS3 frame period is presented below.

Nominally, the Transmit Section within the XRT72L50 will generate a TxNibClk pulse for every 4 RxOutClk or TxInClk periods. However, in 14 cases within a DS3 frame period, the Transmit Payload Data Input Interface allows 5 TxInClk periods to occur between two consecutive TxNibClk pulses.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 4 Operation

This is illustrated in Figure 38

FIGURE 38. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 4 (NIBBLE-PARALLEL/LOOP-TIMED) OPERATION



Mode 4 Operation of the Terminal Equipment

The XRT72L50 operating in this mode functions as the source of the 11.184MHz (e.g., the 44.736MHz clock signal divided by 4) clock signal that is used as the Terminal Equipment Interface clock by both the XRT72L50 and the Terminal Equipment.

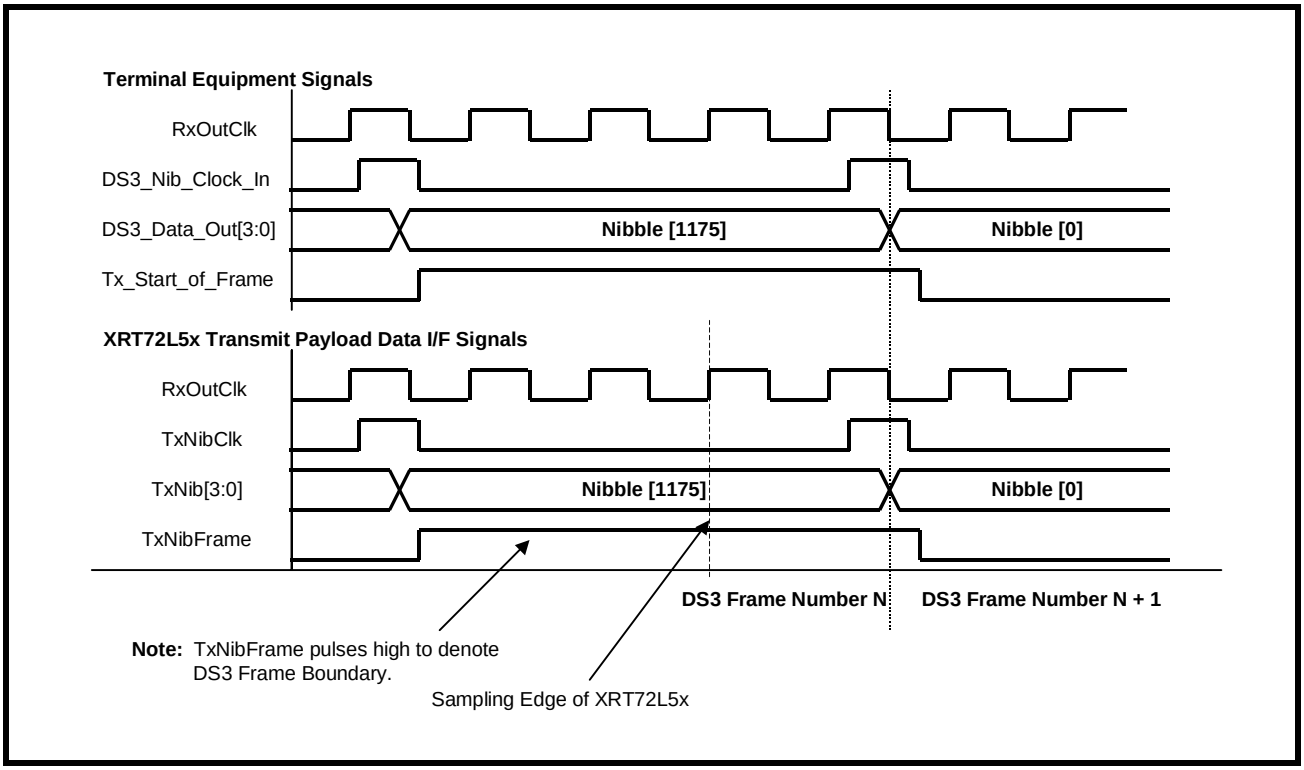
The Terminal Equipment outputs the payload data of the outbound DS3 data stream via its DS3_Data_Out[3:0] pins on the rising edge of the 11.184MHz clock signal at the DS3_Nib_Clock_In input pin.

The XRT72L50 latches the outbound DS3 data stream from the Terminal Equipment on the rising edge of the TxNibClk output clock signal. The XRT72L50 indicates that it is processing the last nibble within a given DS3 frame by pulsing its TxNibFrame output pin "High" for one TxNibClk clock period. When the Terminal Equipment detects a pulse at its Tx_Start_of_Frame input pin, it is expected to transmit the first nibble of the very next outbound DS3 frame to the XRT72L50 via the DS3_Data_Out[3:0] or TxNib[3:0] pins.

Finally, for the Nibble-Parallel Mode operation, the XRT72L50 continuously pulls the TxOHInd output pin "Low".

The behavior of the signals between the XRT72L50 and the Terminal Equipment for DS3 Mode 4 Operation is illustrated in Figure 39.

FIGURE 39. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (MODE 4 OPERATION)



How to configure the XRT72L50 into Mode 4

1. Set the NibIntf input pin "High".
2. Set the TimRefSel[1:0] bit-fields within the Framer Operating Mode Register to “00" as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	0

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 38.

The XRT72L50 cannot support the Framer Local Loop-back Mode of operation. The XRT72L50 Framer must be configured into any of the following modes prior to configuring the Framer Local-Loop-back Mode operation.

- Mode 2 - Serial/Local-Timed/Frame-Slave Mode.
- Mode 3 - Serial/Local-Timed/Frame-Master Mode.
- Mode 5 - Nibble-Parallel/Local-Timed/Frame-Slave Mode.
- Mode 6 - Nibble-Parallel/Local-Timed/Frame-Master Mode.

NOTE: *For more detailed information on the Framer Local Loop-back Mode Operation, please see* Section 7.0.

4.2.1.5 *Mode 5 - The Nibble-Parallel/Local-Timed/Frame-Slave Interface Mode Behavior of the XRT72L50*

The XRT72L50 configured to operate in this mode functions as follows:

Local-Timed

The Transmit Section of the XRT72L50 uses the TxInClk signal as its timing reference. The chip internally divides the TxInClk clock signal by a factor of 4 and outputs this divided clock signal via the TxNibClk output pin. The Transmit Terminal Equipment Input Interface block within the XRT72L50 uses the rising edge of the TxNibClk signal to latch the data residing on the TxNib[3:0] into its circuitry.

Nibble-Parallel Mode

The XRT72L50 accepts the DS3 payload data from the Terminal Equipment in a parallel manner via the TxNib[3:0] input pins. The Transmit Terminal Equipment Input Interface latches this data into its circuitry on the rising edge of the TxNibClk output signal.

Delineation of outbound DS3 Frames

The Transmit Section uses the TxInClk input signal as its timing reference and the TxFrameRef input signal as its Framing Reference (e.g., the Transmit Section of the XRT72L50 initiates frame generation upon the rising edge of the TxFrameRef signal).

In this case, the Terminal Equipment should pulse the TxFrameRef input signal of the XRT72L50 coincident with it applying the first payload nibble within a given outbound DS3 frame. The duration of this pulse should be one nibble-period of the DS3 signal (see Figure 41).

Sampling of payload data, from the Terminal Equipment

In Mode 5, the XRT72L50 samples the data at the TxNib[3:0] input pins on the third rising edge of the TxInClk clock signal following a pulse in the TxNibClk signal (see Figure 41).

The TxNibClk signal from the XRT72L50 operates nominally at 11.184 MHz (e.g., 44.736 MHz divided by 4). However, TxNibClk effectively operates at a Low clock frequency. The Transmit Payload Data Input Interface is only used to accept the payload data which is intended to be carried by outbound DS3 frames. The Transmit Payload Data Input Interface is not designed to accommodate the entire DS3 data stream.

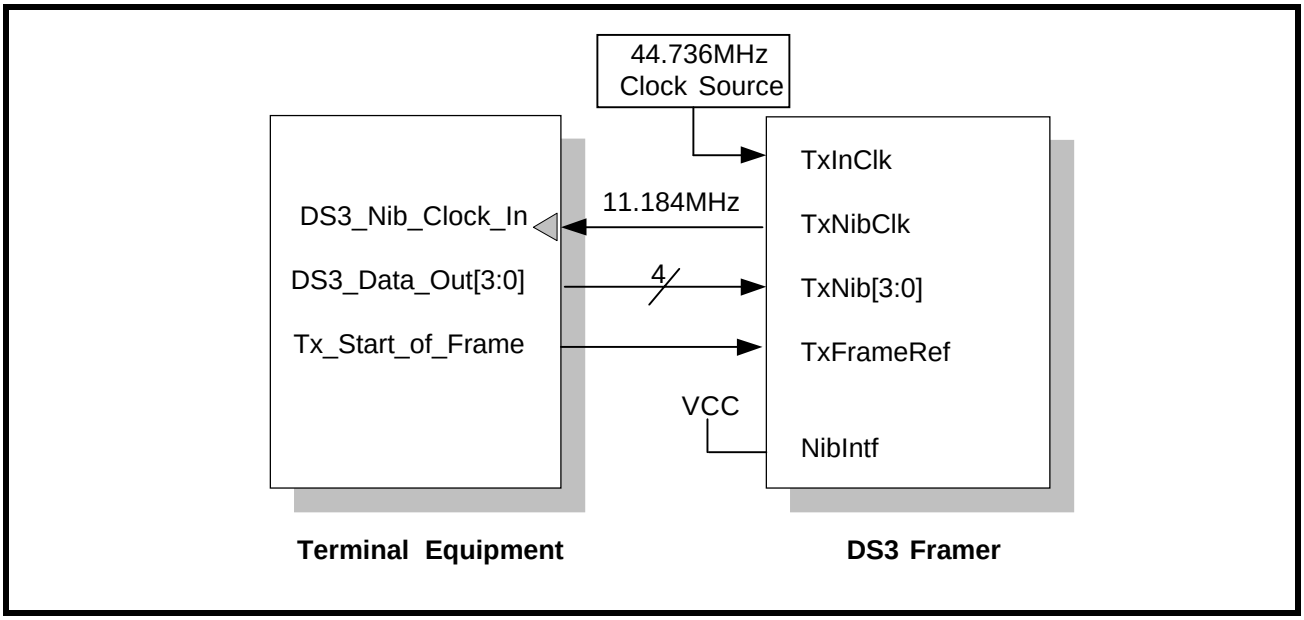
The DS3 Frame consists of 4704 payload bits or 1176 nibbles. The XRT72L50 supplies 1176 TxNibClk pulses between the rising edges of two consecutive TxNibFrame pulses. The DS3 Frame repetition rate is 9.398kHz. 1176 TxNibClk pulses for each DS3 frame period amounts to TxNibClk running at approximately 11.052 MHz.

Nominally, the Transmit Section within the XRT72L50 generates a TxNibClk pulse for every 4 RxOutClk or TxInClk periods. However, in 14 cases within a DS3 frame period, the Transmit Payload Data Input Interface allows 5 TxInClk periods to occur between two consecutive TxNibClk pulses.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 5 Operation

This is illustrated in Figure 40

FIGURE 40. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 5 (NIBBLE-PARALLEL/LOCAL-TIMED/FRAME-SLAVE) OPERATION



Mode 5 Operation of the Terminal Equipment

In Figure 40, both the Terminal Equipment and the XRT72L50 is driven by an external 11.184MHz clock signal. The Terminal Equipment receives the 11.184MHz clock signal via the DS3_Nib_Clock_In input pin. The XRT72L50 outputs the 11.184MHz clock signal via the TxNibClk output pin.

The Terminal Equipment serially outputs the data on the DS3_Data_Out[3:0] pins upon the rising edge of the signal at the DS3_Clock_In input pin. The DS3_Data_Out[3:0] output pins of the Terminal Equipment is electrically connected to the TxNib[3:0] input pins.

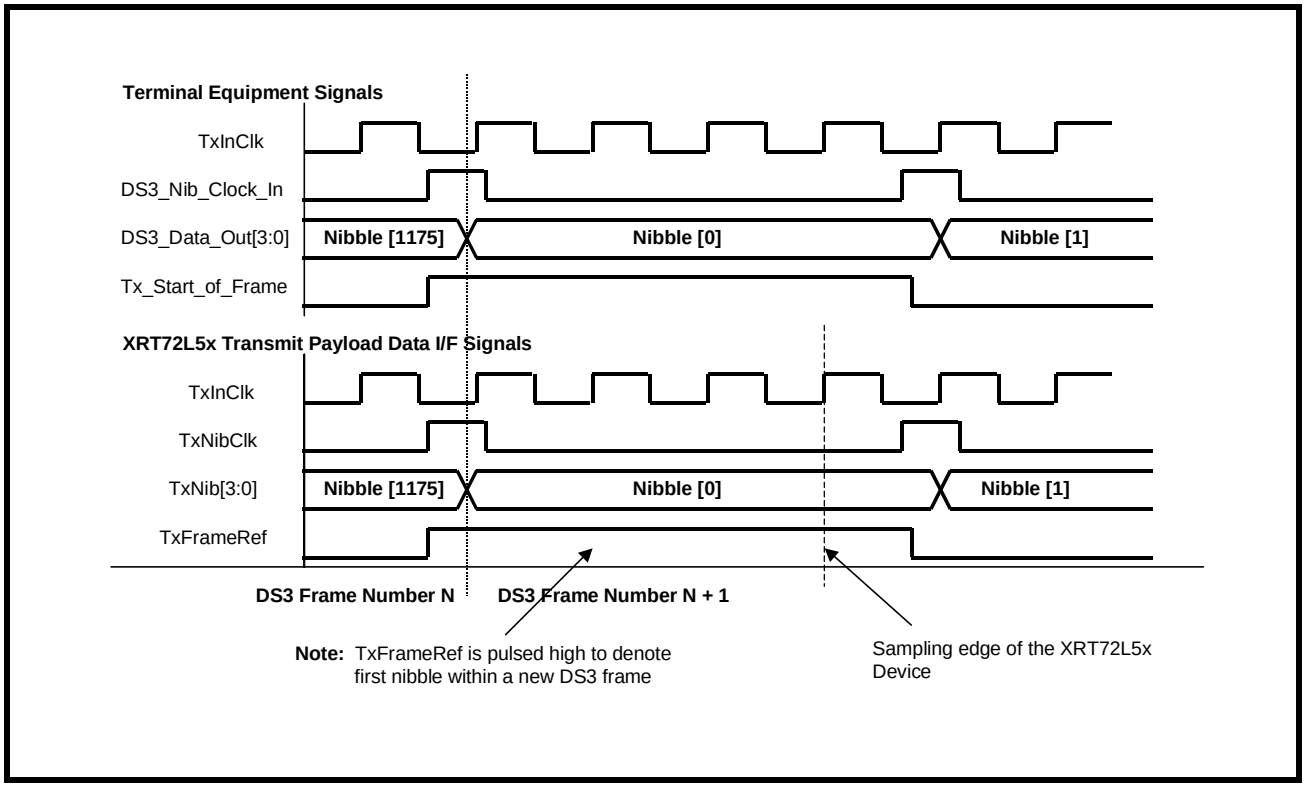
The XRT72L50 latches the data residing on the TxNib[3:0] input pins on the rising edge of the TxNibClk signal.

In this case, the Terminal Equipment has the responsibility of providing the framing reference signal by pulsing the Tx_Start_of_Frame output pin and in turn, the TxFrameRef input pin of the XRT72L50 "High" for one bit-period coincident with the first nibble of a new DS3 frame. Once the XRT72L50 detects the rising edge of the input at its TxFrameRef input pin, it begins generation of a new DS3 frame.

Finally, the XRT72L50 always internally generates the Overhead bits when it is operating in both the DS3 and Nibble-parallel modes. The XRT72L50 pulls the TxOHInd input pin "Low".

The behavior of the signals between the XRT72L50 and the Terminal Equipment for DS3 Mode 5 Operation is illustrated in Figure 41.

FIGURE 41. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (DS3 MODE 5 OPERATION)



How to configure the XRT72L50 into Mode 5

1. Set the NibIntf input pin "High".
2. Set the TimRefSel[1:0] bit-fields within the Framer Operating Mode Register to "01" as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	1

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 40.

4.2.1.6 *Mode 6 - The Nibble-Parallel/TxInClk/Frame-Master Interface Mode Behavior of the XRT72L50*

The XRT72L50 configured to operate in this mode, functions as follows:

Local-Timed

The Transmit Section of the XRT72L50 uses the TxInClk signal at its timing reference. The chip internally divides the TxInClk clock signal by a factor of 4 and outputs this divided clock signal via the TxNibClk output pin. The Transmit Terminal Equipment Input Interface block within the XRT72L50 uses the rising edge of the TxNibClk signal to latch the data residing on the TxNib[3:0] into its circuitry.

Nibble-Parallel Mode

The XRT72L50 accepts the DS3 payload data from the Terminal Equipment in a parallel manner via the TxNib[3:0] input pins. The Transmit Terminal Equipment Input Interface latches this data into its circuitry on the rising edge of the TxNibClk output signal.

Delineation of outbound DS3 Frames

The Transmit Section uses the TxInClk input signal as its timing reference and initiates the generation of DS3 frames asynchronous with respect to any external signal. The XRT72L50 pulses the TxFrame output pin "High" whenever it is processing the last nibble within a given outbound DS3 frame.

Sampling of payload data, from the Terminal Equipment

In Mode 6, the XRT72L50 samples the data at the TxNib[3:0] input pins on the third rising edge of the TxInClk clock signal following a pulse in the TxNibClk signal (see Figure 43).

The TxNibClk signal from the XRT72L50, operates nominally at 11.184 MHz (e.g., 44.736 MHz divided by 4). However, TxNibClk effectively operates at a Low clock frequency. The Transmit Payload Data Input Interface is only used to accept the payload data which is intended to be carried by outbound DS3 frames. The Transmit Payload Data Input Interface is not designed to accommodate the entire DS3 data stream.

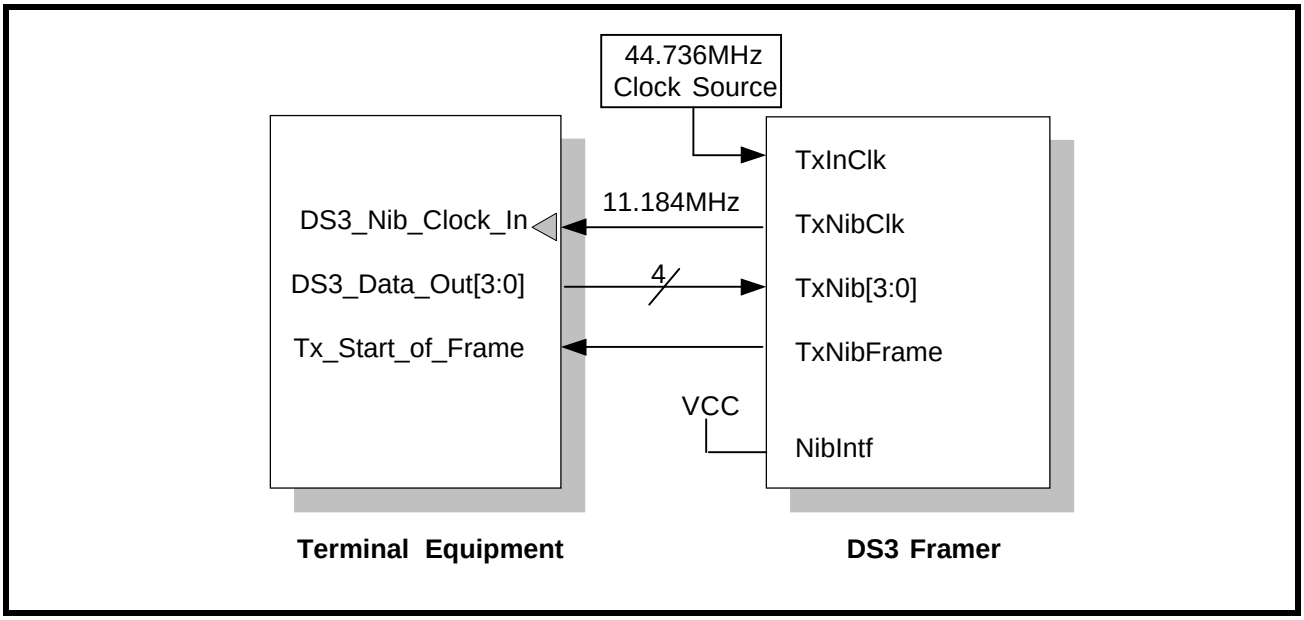
The DS3 Frame consists of 4704 payload bits or 1176 nibbles. The XRT72L50 supplies 1176 TxNibClk pulses between the rising edges of two consecutive TxNibFrame pulses. The DS3 Frame repetition rate is 9.398kHz. 1176 TxNibClk pulses for each DS3 frame period amounts to TxNibClk running at approximately 11.052 MHz.

Nominally, the Transmit Section within the XRT72L50 generates a TxNibClk pulse for every 4 RxOutClk or TxInClk periods. However, in 14 cases within a DS3 frame period, the Transmit Payload Data Input Interface allows 5 TxInClk periods to occur between two consecutive TxNibClk pulses.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 6 Operation

This is illustrated in Figure 42.

FIGURE 42. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 6 (NIBBLE-PARALLEL/LOCAL-TIMED/FRAME-MASTER) OPERATION



Mode 6 Operation of the Terminal Equipment

In Figure 42 both the Terminal Equipment and the XRT72L50 is driven by an external 11.184MHz clock signal. The Teriminal Equipment receives the 11.184MHz clock signal via the DS3_Nib_Clock_In input pin. The XRT72L50 outputs the 11.184MHz clock signal via the TxNibClk output pin.

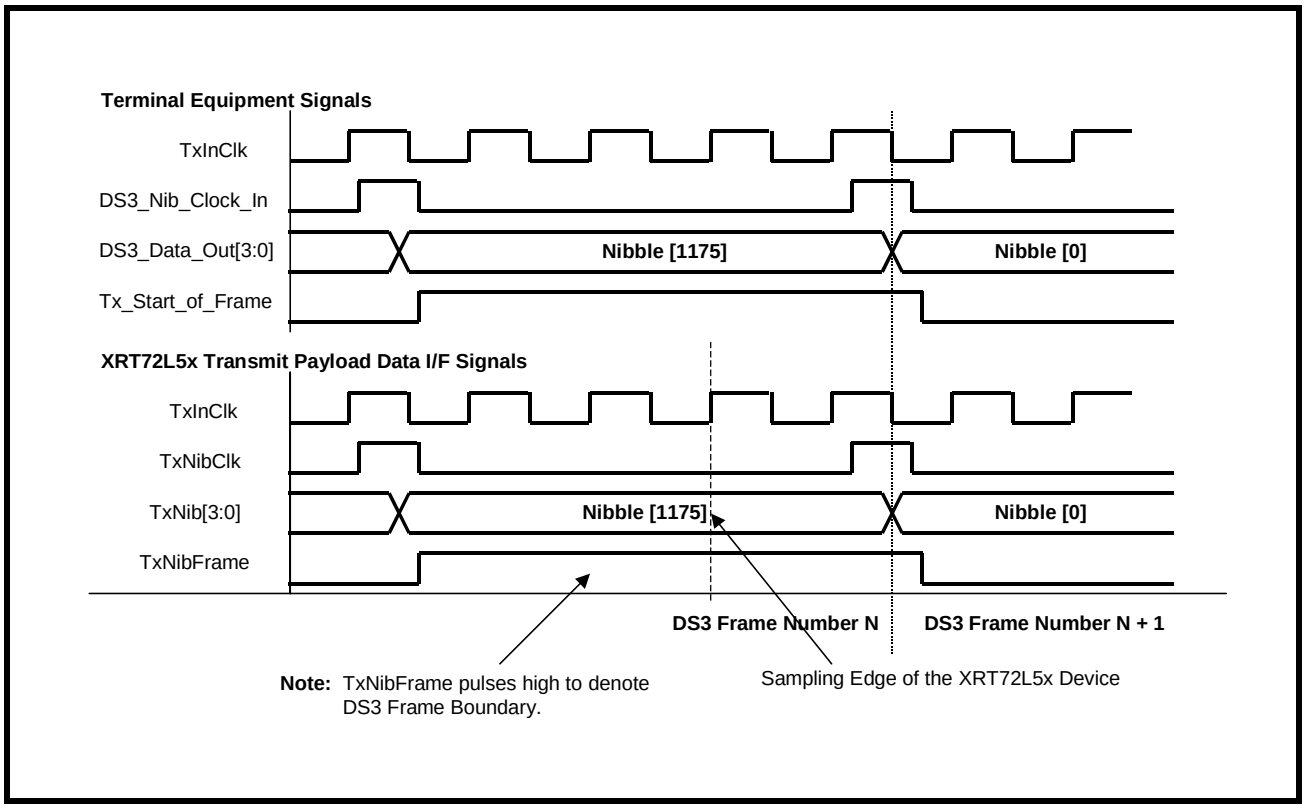
The Terminal Equipment serially outputs the data on the DS3_Data_Out[3:0] pins upon the rising edge of the signal at the DS3_Clock_In input pin. The XRT72L50 latches the data residing on the TxNib[3:0] input pins on the rising edge of the TxNibClk signal.

In this case, the XRT72L50 provides the framing reference signal by pulsing the TxFrame output pin and in turn, the Tx_Start_of_Frame input pin of the Terminal Equipment "High" for one nibble-period coincident with the last nibble within a given DS3 frame.

Finally, the XRT72L50 always internally generates the Overhead bits when it is operating in both the DS3 and Nibble-parallel modes. The XRT72L50 pulls the TxOHInd input pin "Low".

The behavior of the signals between the XRT72L50 and the Terminal Equipment for DS3 Mode 6 Operation is illustrated in Figure 43.

FIGURE 43. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (DS3 MODE 6 OPERATION)



How to configure the XRT72L50 into Mode 6

1. Set the NibIntf input pin "High".
2. Set the TimRefSel[1:0] bit-fields within the Framer Operating Mode Register to “1X” as illustrated below.

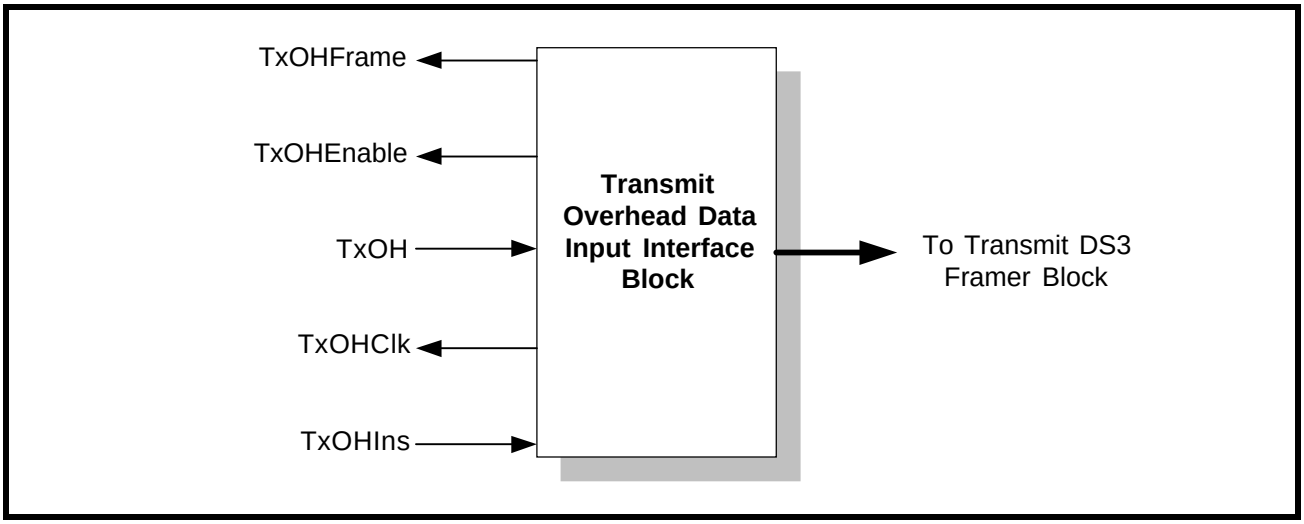
Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	x

3. Interface the XRT72L50 to the Terminal Equipment, as illustrated in Figure 42.

4.2.2 The Transmit Overhead Data Input Interface

FIGURE 44. THE TRANSMIT OVERHEAD DATA INPUT INTERFACE BLOCK



The DS3 Frame consists of 4760 bits. Of these bits, 4704 bits are payload bits and the remaining 56 bits are overhead bits. The XRT72L50 has been designed to handle and process both the payload type and overhead type bits for each DS3 frame. Within the XRT72L50 Transmit Section, the Transmit Payload Data Input Interface has been designed to handle the payload data. Likewise, the Transmit Overhead Data Input Interface has been designed to handle and process the overhead bits.

The Transmit Section of the XRT72L50 generates or processes the various overhead bits within the DS3 frame, in the following manner.

The Frame Synchronization Overhead Bits (e.g., the F and M bits)

The F and M bits are always internally generated by the Transmit Section of the XRT72L50. These overhead bits are used by the Remote Terminal Equipment for Frame Synchronization purposes. User values cannot be inserted for the F and M bits into the outbound DS3 data stream via the Transmit Overhead Data Input Interface. Any attempt to externally insert values for the F and M bits will be ignored by the Transmit Overhead Data Input Interface “High” block.

The Performance Monitoring Overhead Bits (P and CP Bits)

The P-bits are always internally generated by the Transmit Section of the XRT72L50. The P bits are used by the Remote Terminal Equipment to perform error-checking/detection of a DS3 data stream as it is transmitted from one Terminal Equipment to adjacent Terminal Equipment (e.g., point-to-point checking). User values cannot be inserted for the P-bits into the outbound DS3 data stream via the Transmit Overhead Data Input Interface.

In contrast to P bits, CP bits are used to perform error-checking/detection of a DS3 data stream from the Source Terminal Equipment to the Sink Terminal Equipment. In applications where a given DS3 data stream is received via one port and is output via another port, it is necessary that the CP bit-values remain constant. The only way to insure this is to (1) extract out the CP bit values via the Receiving Line Card and (2) insert these CP-bit values into the outbound DS3 data stream via the Transmit Overhead Data Input Interface block. Hence, the Transmit Overhead Data Input Interface block will permit the user to externally insert the CP bits into the outbound DS3 data stream.

The Alarm and signaling related Overhead bits

Bits that are used to transport the alarm conditions can be either internally generated by the Transmit Section within the XRT72L50 or externally generated and inserted into the outbound DS3 data stream via the Transmit Overhead Data Input Interface or TxSER (Payload Data Pin). The DS3 frame overhead bits that fall into this category are:

- The X bits
- The FEAC bits
- The FEBE bits.

The Data Link Related Overhead Bits

The DS3 frame structure also contains bits which can be used to transport User Data Link information and Path Maintenance Data Link information. The UDL (User Data Link) bits are only accessible via the Transmit Overhead Data Input Interface. The Path Maintenance Data Link (PMDL) bits can either be sourced from the Transmit LAPD Controller/Buffer or via the Transmit Overhead Data Input Interface.

Table 16 lists the Overhead Bits within the DS3 frame. This table also indicates whether or not these overhead bits can be sourced by the Transmit Overhead Data Input Interface.

TABLE 16: OVERHEAD BITS WITHIN THE DS3 FRAME AND THEIR POTENTIAL SOURCES WITHIN THE XRT72L50 IC

OVERHEAD BIT	INTERNALLY GENERATED	ACCESSIBLE VIA THE TRANSMIT OVERHEAD DATA INPUT INTERFACE	BUFFER/REGISTER ACCESSIBLE
P	Yes	No	Yes*
X	Yes	Yes	Yes*
F	Yes	No	Yes*
M	Yes	No	Yes*
FEAC	No	Yes	Yes
FEBE	Yes	Yes	Yes
DL	No	Yes	Yes+
UDL	No	Yes	No
CP	Yes	Yes	No

* The XRT72L50 contains mask register bits that permit the altering to fhe state of the internally generated value for these bits.

+ The Transmit LAPD Controller/Buffer can be configured to be the source of the DL bits within the outbound DS3 data stream.

In all, the Transmit Overhead Data Input Interface permits the insertion of overhead data into the outbound DS3 frames via the following methods:

- Method 1 - Using the TxOHClk clock signal
- Method 2 - Using the TxInClk and the TxOHEnable signals.

4.2.2.1 *Method 1 - Using the TxOHClk Clock Signal*

The Transmit Overhead Data Input Interface consists of five signals. Of these five signals, the following four signals are to be used when implementing Method 1.

- TxOH
- TxOHClk
- TxOHFrame
- TxOHIns

Each of these signals are listed and described in Table 17.

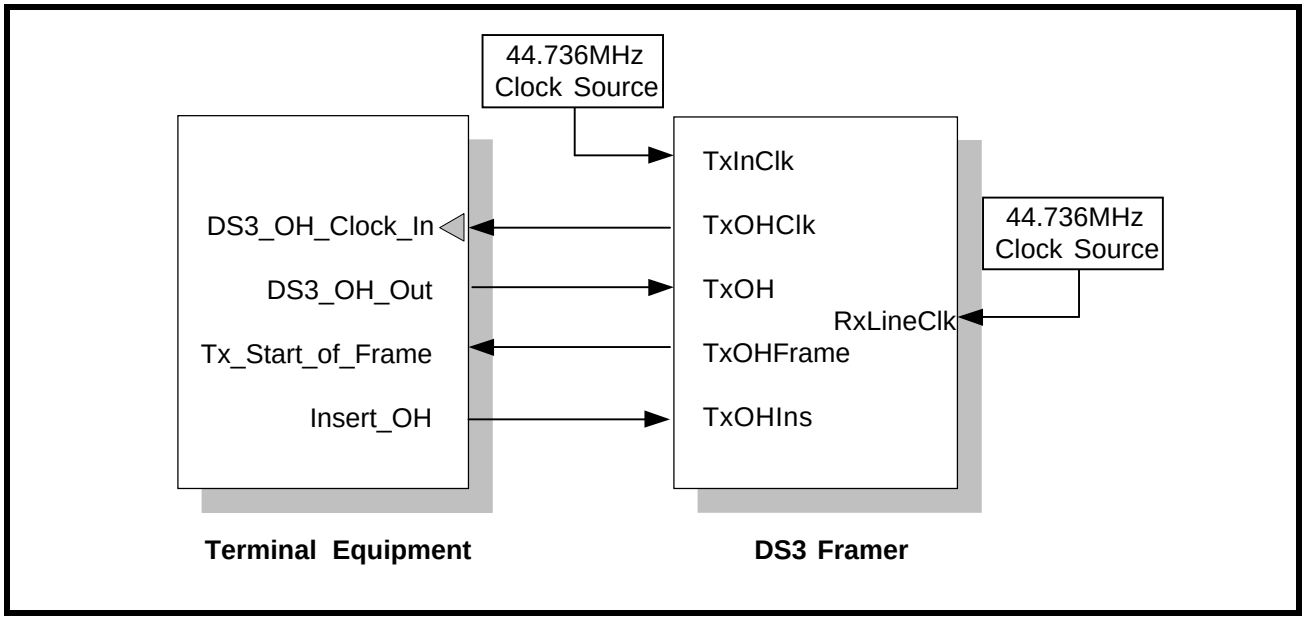
TABLE 17: DESCRIPTION OF METHOD 1 TRANSMIT OVERHEAD INPUT INTERFACE SIGNALS

NAME	TYPE	DESCRIPTION
TxOHIns	I	**Transmit Overhead Data Insert Enable input pin.** Asserting this input signal (e.g., setting it "High") enables the Transmit Overhead Data Input Interface to accept overhead data from the Terminal Equipment. In other words, while this input pin is "High", the Transmit Overhead Data Input Interface samples the data at the TxOH input pin on the falling edge of the TxOHClk output signal. Setting this pin "Low" configures the Transmit Overhead Data Input Interface to NOT sample (e.g., ignore) the data at the TxOH input pin on the falling edge of the TxOHClk output signal. If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the Transmit Overhead Data Input Interface (e.g., if the Terminal Equipment asserts the TxOHIns signal at a time when one of these non-insertable overhead bits are being processed), that particular insertion effort is ignored.
TxOH	I	**Transmit Overhead Data Input pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin and inserts into the overhead bit position within the very next outbound DS3 frame. If the TxOHIns pin is pulled "High", the Transmit Overhead Data Input Interface samples the data at this input pin on the falling edge of the TxOHClk output pin. If the TxOHIns pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin and this data is ignored.
TxOHClk	O	**Transmit Overhead Input Interface Clock Output signal:** This output signal serves two purposes: 1. The Transmit Overhead Data Input Interface provides a rising clock edge on this signal one bit-period prior to the instant that the Transmit Overhead Data Input Interface is processing an overhead bit. 2. The Transmit Overhead Data Input Interface sample the data at the TxOH input on the falling edge of this clock signal provided that the TxOHIns input pin is "High". The Transmit Overhead Data Input Interface supplies a clock edge for all overhead bits within the DS3 frame via the TxOHClk output signal. This includes those overhead bits that the Transmit Overhead Data Input Interface will not accept from the Terminal Equipment.
TxOHFrame	O	**Transmit Overhead Input Interface Frame Boundary Indicator Output:** This output signal pulses "High" when the XRT72L50 is processing the last bit within a given DS3 frame. The purpose of this output signal is to alert the Terminal Equipment that the Transmit Overhead Data Input Interface block is about to begin processing the overhead bits for a new DS3 frame.

Interfacing the Transmit Overhead Data Input Interface to the Terminal Equipment.

Figure 45 illustrates how one should interface the Transmit Overhead Data Input Interface to the Terminal Equipment, when using Method 1.

FIGURE 45. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 1)



Method 1 Operation of the Terminal Equipment

If the Terminal Equipment intends to insert any overhead data into the outbound DS3 data stream via the Transmit Overhead Data Input Interface, then it is expected to do the following.

1. To sample the state of the TxOHFrame signal (e.g., the Tx_Start_of_Frame input signal) on the rising edge of the TxOHClk (e.g., the DS3_OH_Clock_In signal).
2. To keep track of the number of rising clock edges that have occurred via the TxOHClk (e.g., the DS3_OH_Clock_In signal) since the last time the TxOHFrame signal was sampled "High". By doing this the Terminal Equipment will be able to keep track of which overhead bit is being processed by the Transmit Overhead Data Input Interface block at any given time. When the Terminal Equipment knows which overhead bit is being processed at a given TxOHClk period, it knows when to insert a desired overhead bit value into the outbound DS3 data stream. From this, the Terminal Equipment knows when it should assert the TxOHIns input pin and place the appropriate value on the TxOH input pin of the XRT72L50.

Table 18 relates the number of rising clock edges in the TxOHClk signal since the TxOHFrame was sampled "High" to the DS3 Overhead Bit that is being processed.

TABLE 18: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN TXOHCLK SINCE TXOHFRAME WAS LAST SAMPLED "HIGH" TO THE DS3 OVERHEAD BIT THAT IS BEING PROCESSED

NUMBER OF RISING CLOCK EDGES IN TXOHCLK	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
0 (Clock edge is coincident with TxOHFrame being detected "High")	X	Yes
1	F1	No
2	AIC	Yes
3	F0	No
4	NA	Yes
5	F0	No

TABLE 18: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN TXOHCLK SINCE TXOHFRAME WAS LAST SAMPLED "HIGH" TO THE DS3 OVERHEAD BIT THAT IS BEING PROCESSED

NUMBER OF RISING CLOCK EDGES IN TXOHCLK	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
6	FEAC	Yes
7	F1	No
8	X	Yes
9	F1	No
10	UDL	Yes
11	F0	No
12	UDL	Yes
13	F0	No
14	UDL	Yes
15	F1	No
16	P	No
17	F1	No
18	CP	Yes
19	F0	No
20	CP	Yes
21	F0	No
22	CP	Yes
23	F1	No
24	P	No
25	F1	No
26	FEBE	Yes
27	F0	No
28	FEBE	Yes
29	F0	No
30	FEBE	Yes
31	F1	No
32	M0	No
33	F1	No
34	DL	Yes
35	F0	No
36	DL	Yes

TABLE 18: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN TXOHCLK SINCE TXOHFRAME WAS LAST SAMPLED "HIGH" TO THE DS3 OVERHEAD BIT THAT IS BEING PROCESSED

NUMBER OF RISING CLOCK EDGES IN TXOHCLK	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
37	F0	No
38	DL	Yes
39	F1	No
40	M1	No
41	F1	No
42	UDL	Yes
43	FO	No
44	UDL	Yes
45	FO	No
46	UDL	Yes
47	F1	No
48	M0	No
49	F1	No
50	UDL	Yes
51	F0	No
52	UDL	Yes
53	F0	No
54	UDL	Yes
55	F1	No

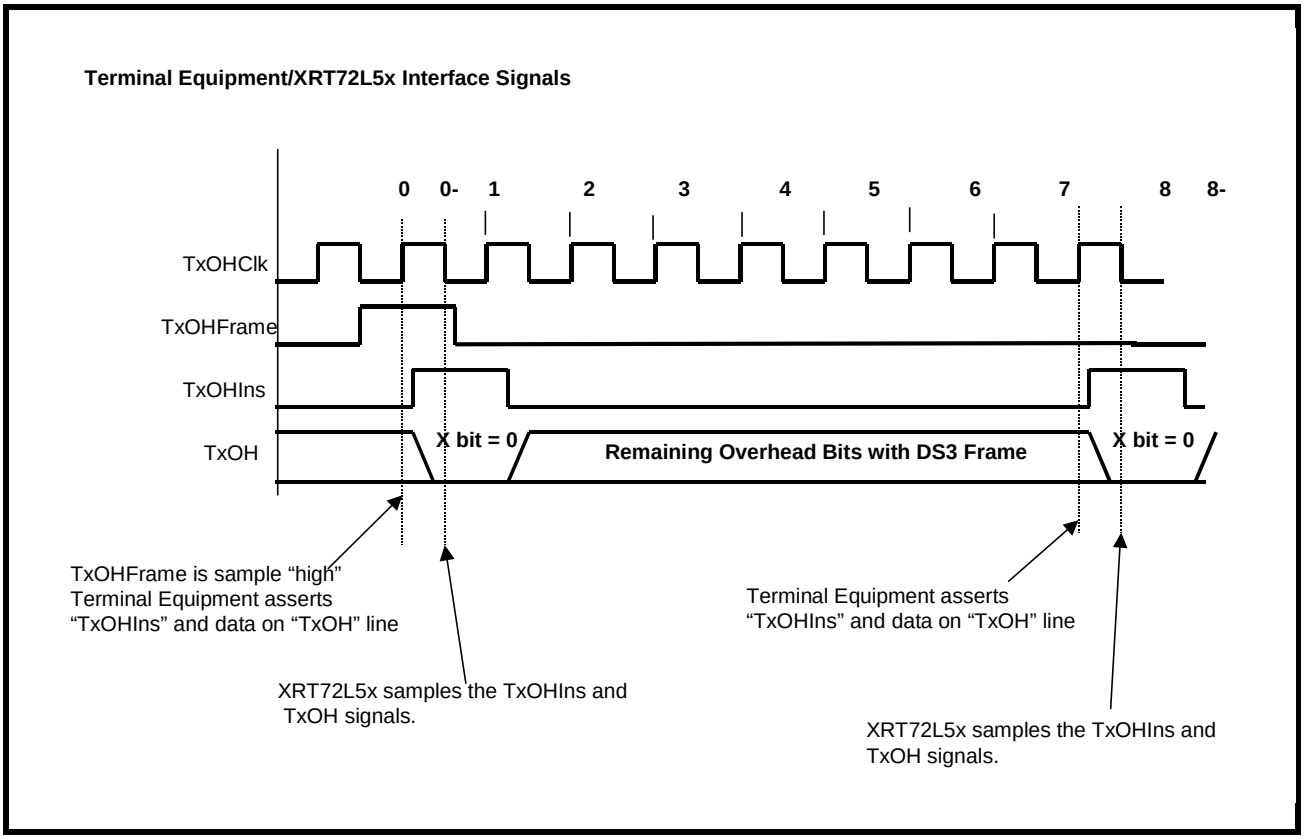
3. After the Terminal Equipment has waited the appropriate number of clock edges from the TxOHFrame signal being sampled "High", it should assert the TxOHIns input signal. Concurrently, the Terminal Equipment should also place the appropriate value of the inserted overhead bit onto the TxOH signal.
4. The Terminal Equipment should hold both the TxOHIns input pin "High" and the value of the TxOH signal stable until the next rising edge of TxOHClk is detected.

Case Study: The Terminal Equipment intends to insert the appropriate overhead bits into the Transmit Overhead Data Input Interface using Method 1 in order to transmit a Yellow Alarm to the remote terminal equipment.

For DS3 Applications, a Yellow Alarm is transmitted by setting both of the X bits within each outbound DS3 frame to “0”.

Assuming that the connection between the Terminal Equipment and the XRT72L50 is as illustrated in Figure 45, then Figure 46 presents an illustration of the signaling that must go on between the Terminal Equipment and the XRT72L50.

FIGURE 46. ILLUSTRATION OF THE SIGNAL THAT MUST OCCUR BETWEEN THE TERMINAL EQUIPMENT AND THE XRT72L50, IN ORDER TO CONFIGURE THE XRT72L50 TO TRANSMIT A YELLOW ALARM TO THE REMOTE TERMINAL EQUIPMENT



In Figure 46 the Terminal Equipment samples the TxOHFrame signal being "High" at the rising clock edge #0. At this point, the Terminal Equipment knows that the XRT72L50 is just about to process the very first overhead bit within a given outbound DS3 frame. The very first overhead bit in Table 18 to be processed is the first X bit. To facilitate the transmission of the Yellow Alarm, the Terminal Equipment must set this X bit to “0”. The Terminal Equipment starts this process by implementing the following steps concurrently.

a. Assert the TxOHIns input pin by setting it "High".

b. Set the TxOH input pin to “0”.

After the Terminal Equipment has applied these signals, the XRT72L50 samples the data on both the TxOHIns and TxOH signals upon the very next falling edge of TxOHClk (designated at 0- in Figure 46). Once the XRT72L50 has sampled this data, it then inserts a "0" into the first X bit position in the outbound DS3 frame.

Upon detection of the very next rising edge of the TxOHClk clock signal (designated as clock edge 1 in Figure 46), the Terminal Equipment negates the TxOHIns signal (e.g., toggles it "Low") and ceases inserting data into the Transmit Overhead Data Input Interface until rising clock edge #8 of the TxOHClk signal. In Table 18 the rising clock edge #8 indicates that the XRT72L50 is just about ready to process the second X bit within the outbound DS3 frame. To facilitate the transmission of the Yellow Alarm, this X Bit must also be set to “0”. The Terminal Equipment implements the following steps concurrently.

a. Assert the TxOHIns input pin by setting it "High".

b. Set the TxOH input to “0”.

After the Terminal Equipment has applied these signals, the XRT72L50 samples the data on both the TxOHIns and TxOH signal upon the very next falling edge of TxOHClk (designated as 8- in Figure 46). Once the XRT72L50 has sampled this data, it inserts a "0" into the second X bit position in the outbound DS3 frame.

4.2.2.2 *Method 2 - Using the TxInClk and TxOHEnable Signals*

When using Method 2, either the TxInClk or RxOutClk signal is used to sample the overhead bits and signals which are input to the Transmit Overhead Data Input Interface. Method 2 involves the use of the following signals:

- TxOH
- TxInClk
- TxOHFrame
- TxOHEnable
- TxOHIns

These signals are described in Table 19.

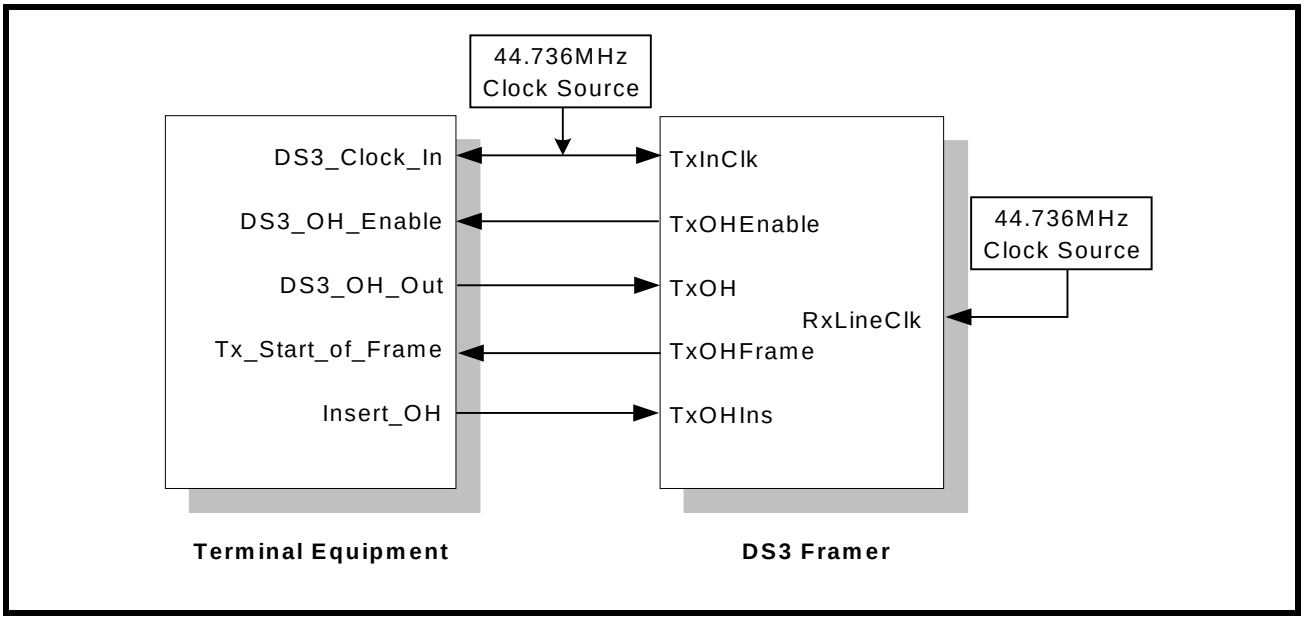
TABLE 19: DESCRIPTION OF METHOD 2 TRANSMIT OVERHEAD INPUT INTERFACE SIGNALS

NAME	TYPE	DESCRIPTION
TxOHEnable	O	**Transmit Overhead Data Enable Output pin** The XRT72L50 asserts this signal for one TxInClk period just prior to the instant that the Transmit Overhead Data Input Interface is processing an overhead bit.
TxInClk	I	**Transmit Section Timing Reference Clock Input pin:** The Transmit Section of the XRT72L50 can be configured to use this clock signal as the Timing Reference. If this configuration is selected, then the XRT72L50 uses this clock signal to sample the data on the TxSer input pin and a DS3 or E3 clock signal must be applied to this pin.
TxOHFrame	O	**Transmit Overhead Input Interface Frame Boundary Indicator Output:** This output signal pulses "High" when the XRT72L50 is processing the last bit within a given DS3 frame.
TxOHIns	I	**Transmit Overhead Data Insert Enable input pin.** Asserting this input signal (e.g., setting it "High") enables the Transmit Overhead Data Input Interface to accept overhead data from the Terminal Equipment. In other words, while this input pin is "High", the Transmit Overhead Data Input Interface samples the data at the TxOH input pin on the falling edge of the TxInClk output signal. Setting this pin "Low" configures the Transmit Overhead Data Input Interface to NOT sample (e.g., ignore) the data at the TxOH input pin on the falling edge of the TxOHClk output signal. If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the Transmit Overhead Data Input Interface (e.g., if the Terminal Equipment asserts the TxOHIns signal at a time when one of these non-insertable overhead bits are being processed), that particular insertion effort is ignored.
TxOH	I	**Transmit Overhead Data Input pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin and inserts into the overhead bit position within the very next outbound DS3 frame. If the TxOHIns pin is pulled "High", the Transmit Overhead Data Input Interface samples the data at this input pin (TxOH) on the falling edge of the TxOHClk output pin. If the TxOHIns pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH) and this data is ignored.

Interfacing the Transmit Overhead Data Input Interface to the Terminal Equipment

Figure 47 illustrates how one should interface the Transmit Overhead Data Input Interface to the Terminal Equipment when using Method 2.

FIGURE 47. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 2)



Method 2 Operation of the Terminal Equipment

If the Terminal Equipment intends to insert any overhead data into the outbound DS3 data stream via the Transmit Overhead Data Input Interface, then it is expected to do the following.

1. To sample the state of both the TxOHFrame and the TxOHEnable input signals via the DS3_Clock_In (e.g., either the TxInClk or the RxOutClk signal of the XRT72L50) signal. If the Terminal Equipment samples the TxOHEnable signal "High", then it knows that the XRT72L50 is about to process an overhead bit. If the Terminal Equipment samples both the TxOHFrame and the TxOHEnable pins "High" at the same time then the Terminal Equipment knows that the XRT72L50 is about to process the first overhead bit within a new DS3 frame.
2. To keep track of the number of times that the TxOHEnable signal has been sampled "High" since the last time both the TxOHFrame and the TxOHEnable signals were sampled "High". By doing this, the Terminal Equipment is able to keep track of which overhead bit the Transmit Overhead Data Input Interface is about to process. From this, the Terminal Equipment knows when it should assert the TxOHIns input pin and place the appropriate value on the TxOH input pins of the XRT72L50.

Table 20 relates the number of TxOHEnable output pulses that have occurred since both the TxOHFrame and TxOHEnable pins were sampled "High", to the DS3 overhead bit that is being processed.

TABLE 20: THE RELATIONSHIP BETWEEN THE NUMBER OF TXOHENABLE PULSES SINCE THE LAST OCCURRENCE OF THE TXOHFRAME PULSE, TO THE DS3 OVERHEAD BIT THAT IS BEING PROCESSED BY THE XRT72L50

NUMBER OF TXOHENABLE PULSES	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
0 (The TxOHEnable and TxOHFrame signals are both sampled "High")	X	Yes
1	F1	No
2	AIC	Yes
3	F0	No
4	NA	Yes

TABLE 20: THE RELATIONSHIP BETWEEN THE NUMBER OF TXOHENABLE PULSES SINCE THE LAST OCCURRENCE OF THE TXOHFRAME PULSE, TO THE DS3 OVERHEAD BIT THAT IS BEING PROCESSED BY THE XRT72L50

NUMBER OF TXOHENABLE PULSES	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
5	F0	No
6	FEAC	Yes
7	F1	No
8	X	Yes
9	F1	No
10	UDL	Yes
11	F0	No
12	UDL	Yes
13	F0	No
14	UDL	Yes
15	F1	No
16	P	No
17	F1	No
18	CP	Yes
19	F0	No
20	CP	Yes
21	F0	No
22	CP	Yes
23	F1	No
24	P	No
25	F1	No
26	FEBE	Yes
27	F0	No
28	FEBE	Yes
29	F0	No
30	FEBE	Yes
31	F1	No
32	M0	No
33	F1	No
34	DL	Yes
35	F0	No

TABLE 20: THE RELATIONSHIP BETWEEN THE NUMBER OF TXOHENABLE PULSES SINCE THE LAST OCCURRENCE OF THE TXOHFRAME PULSE, TO THE DS3 OVERHEAD BIT THAT IS BEING PROCESSED BY THE XRT72L50

NUMBER OF TXOHENABLE PULSES	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
36	DL	Yes
37	F0	No
38	DL	Yes
39	F1	No
40	M1	No
41	F1	No
42	UDL	Yes
43	FO	No
44	UDL	Yes
45	FO	No
46	UDL	Yes
47	F1	No
48	M0	No
49	F1	No
50	UDL	Yes
51	F0	No
52	UDL	Yes
53	F0	No
54	UDL	Yes
55	F1	No

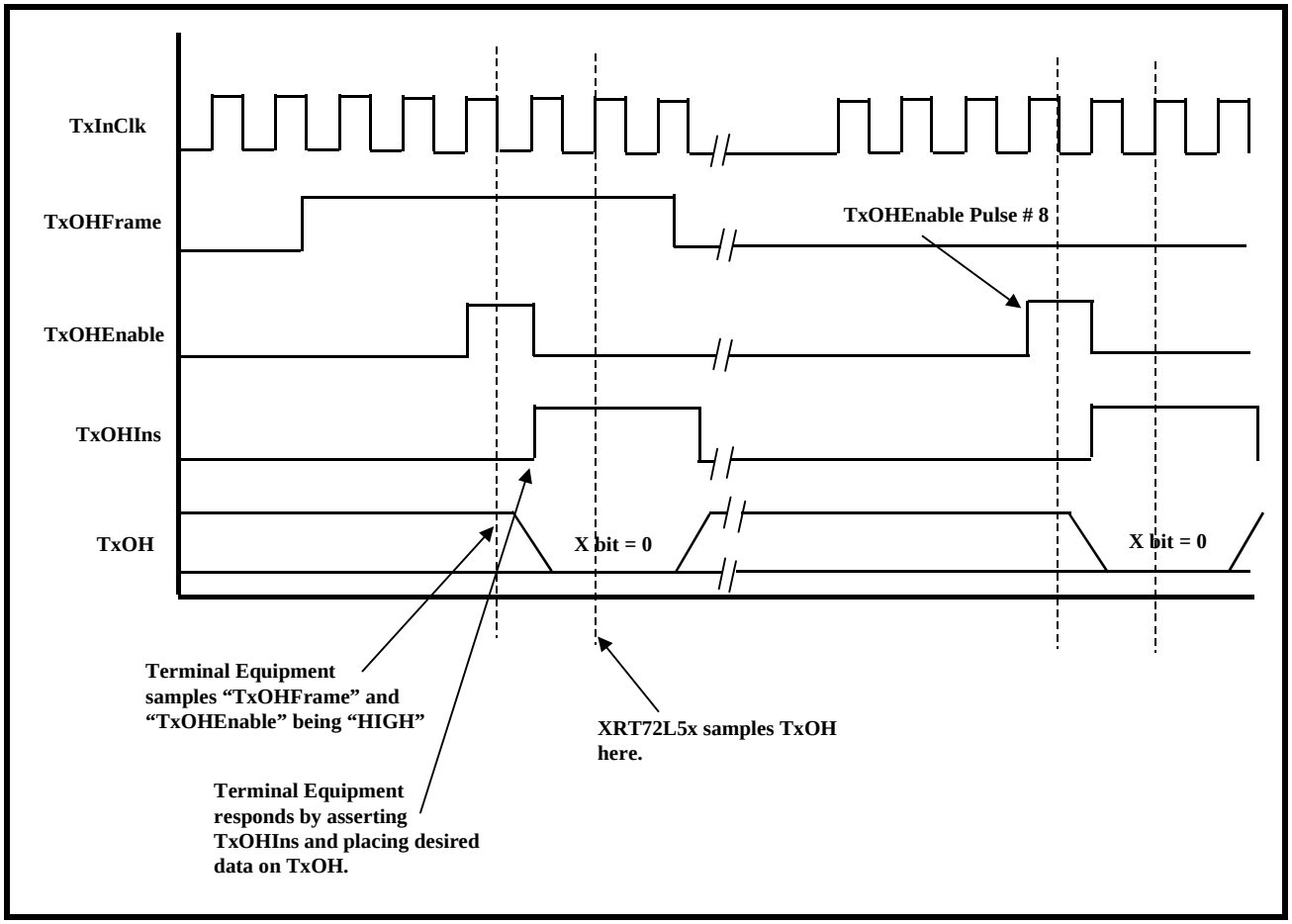
3. After the Terminal Equipment has waited through the appropriate number of pulses via the TxOHEnable pin, it should then assert the TxOHIns input signal. Concurrently, the Terminal Equipment should also place the appropriate value of the inserted overhead bit onto the TxOH signal.
4. The Terminal Equipment should hold both the TxOHIns input pin "High" and the value of the TxOH signal stable until the next TxOHEnable pulse is detected.

Case Study: The Terminal Equipment intends to insert the appropriate overhead bits into the Transmit Overhead Data Input Interface using Method 2 in order to transmit a Yellow Alarm to the remote terminal equipment.

In this case, the Terminal Equipment intends to insert the appropriate overhead bits, into the Transmit Overhead Data Input Interface such that the XRT72L50 transmits a Yellow Alarm to the remote terminal equipment. For DS3 applications, a Yellow Alarm is transmitted by setting all of the X bits to “0”.

If one assumes that the connection between the Terminal Equipment and the XRT72L50 is as illustrated in Figure 47, then Figure 48 presents an illustration of the signaling that must go on between the Terminal Equipment and the XRT72L50.

FIGURE 48. BEHAVIOR OF TRANSMIT OVERHEAD DATA INPUT INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (FOR METHOD 2)



4.2.3 The Transmit DS3 HDLC Controller

The Transmit DS3 HDLC Controller block can be used to transport either Bit-Oriented Signaling (BOS) or Message-Oriented Signaling (MOS) type messages or both types of messages to the remote terminal equipment.

4.2.3.1 *Bit-Oriented Signaling (or FEAC Message) processing via the Transmit DS3 HDLC Controller.*

The Transmit DS3 HDLC Controller block consists of two major blocks:

- The Transmit FEAC Processor.
- The LAPD Transmitter.

If the Transmit DS3 Framer is operating in the C-bit Parity Framing Format then the FEAC (Far-End Alarm & Control) bit-field of the DS3 Frame can be used to transmit the FEAC messages (See Figure 30). The FEAC code word is a 6-bit value which is encapsulated by 10 framing bits, forming a 16-bit FEAC message of the form:

0	d5	d4	d3	d2	d1	d0	0	1	1	1	1	1	1	1	1

where '[d5, d4, d3, d2, d1, d0]' is the FEAC code word. The rightmost bit (e.g., a 1) of the FEAC Message is transmitted first. Since each DS3 frame contains only 1 FEAC bit, 16 DS3 Frames are required to transmit the 16 bit FEAC Code Message, once

The XRT72L50 contains two registers that support FEAC Message Transmission.

- Tx DS3 FEAC Register (Address = 0x32)
- Tx DS3 FEAC Configuration and Status Register (Address = 0x31)

Operating the Transmit FEAC Processor

To transmit a FEAC message to the remote terminal, the following steps must be executed.

STEP 1 - Write the six bit FEAC Codeword (to be sent)

In this step, the µP/µC writes the six bit FEAC code word into the Tx DS3 FEAC Register. The bit format of this register is presented below.

Tx DS3 FEAC Register (Address = 0x32)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	TxFEAC[5]	TxFEAC[4]	TxFEAC[3]	TxFEAC[2]	TxFEAC[1]	TxFEAC[0]	Not Used
RO	R/W	R/W	R/W	R/W	R/W	R/W	R0
0	d5	d4	d3	d2	d1	d0	0

STEP 2 - Enabling the Transmit FEAC Processor

To enable the Transmit FEAC Processor within the Transmit DS3 HDLC Controller block, a “1” must be written into bit 2 (TxFEAC Enable) within the Tx DS3 FEAC Configuration and Status Register, as depicted below.

Transmit DS3 FEAC Configuration and Status Register (Address = 0x31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	Not Used	Not Used	TxFEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC Go	TxFEAC Busy
RO	RO	RO	R/W	RUR	R/W	R/W	R0
x	x	x	x	x	1	X	X

STEP 3 - Initiate the Transmission of the FEAC Message

The transmission of the FEAC code word residing in the Tx DS3 FEAC registe) can be initiated by writing a “1” to bit 1 (TxFEAC Go) within the Tx DS3 FEAC Configuration and Status register, as depicted below.

Transmit DS3 FEAC Configuration and Status Register (Address = 0x31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	Not Used	Not Used	TxFEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC Go	TxFEAC Busy
RO	RO	RO	R/W	RUR	R/W	R/W	R0
x	x	x	x	x	1	1	X

While executing this particular write operation, the binary value, 000xx110b, should be written into the Tx DS3 FEAC Configuration and Status Register. This insures that a “1” is being written to Bit 2 (Tx FEAC Enable) of the register to keep the Transmit FEAC Processor enabled.

Once this step has been completed, the Transmit FEAC Processor proceeds to transmit the 16 bit FEAC code via the outbound DS3 frames. This 16 bit FEAC message must be transmitted repeatedly at least 10 consecutive times requiring a total of 160 DS3 Frames. During this process, Bit 0 (Tx FEAC Busy) is asserted indicating that the Tx FEAC Processor is currently transmitting the FEAC Message to the remote Terminal. This bit-field will toggle to "0" upon completion of the 10th transmission of the FEAC Code Message. The

Transmit FEAC Processor will generate an interrupt (if enabled) to the local µP/µC upon completion of the 10th transmission of the FEAC Message. The purpose of having the Framer generate this interrupt is to let the local µP/µC know that the Transmit FEAC Processor is now available and ready to transmit a new FEAC message.

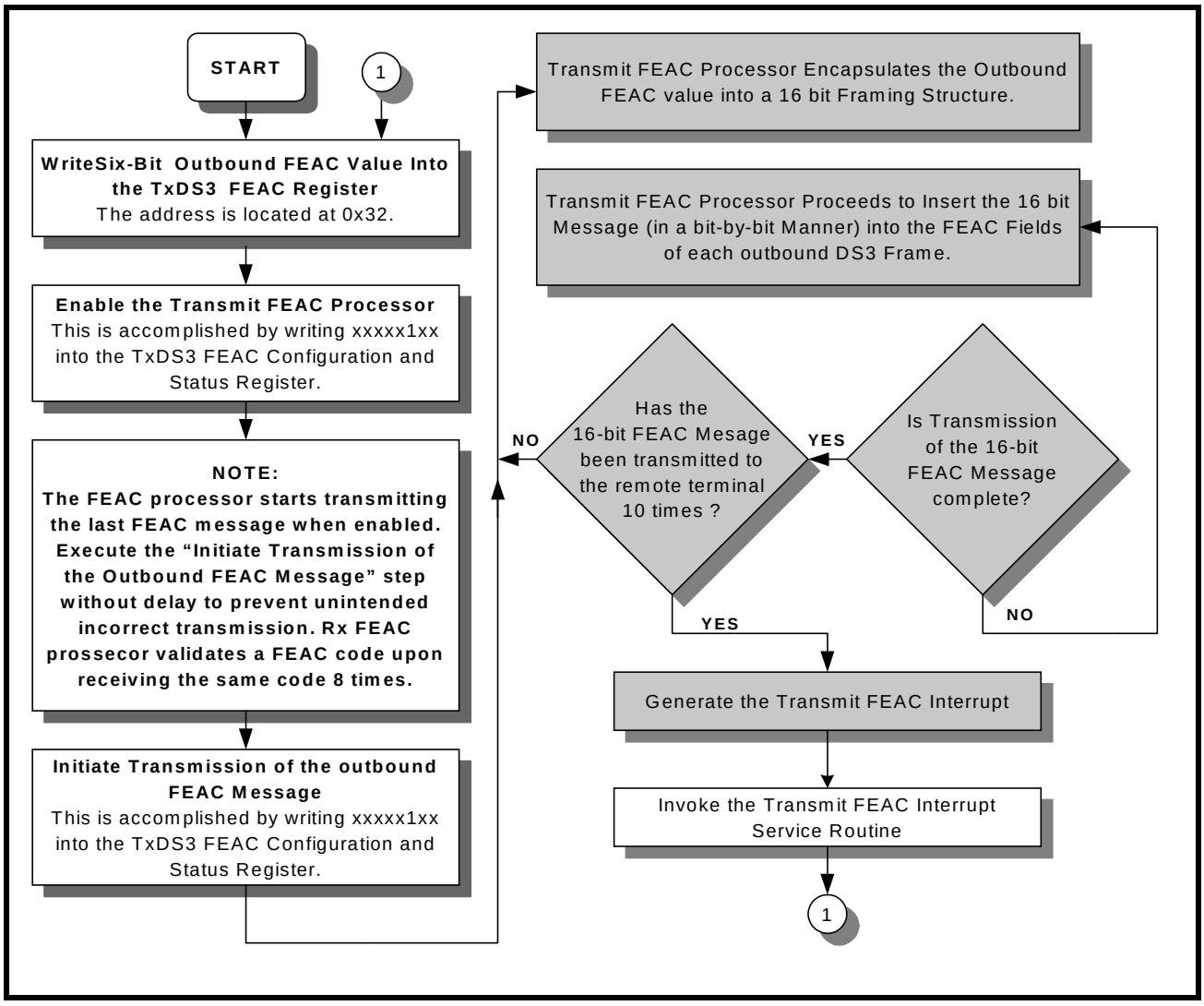
The Transmit FEAC Processor continues to send the FEAC Code Message even after the 10th transmission until the TxFEAC processor is disabled or a new FEAC code transmission is initiated.

If the TxFEAC processor is disabled, the FEAC bit contains a "1" which the remote Rx side interprets as an idle FEAC message.

Figure 49 presents a flow chart depicting how to use the Transmit FEAC Processor.

NOTE: *The FEAC processor starts transmitting the last FEAC message when enabled. Execute the "Initiate Transmission of the Outbound FEAC Message" step without delay to prevent unintended incorrect transmission. Rx FEAC prossecor validates a FEAC code upon receiving the same code 8 times.*

FIGURE 49. A FLOW CHART DEPICTING HOW TO TRANSMIT A FEAC MESSAGE VIA THE FEAC TRANSMITTER



NOTE: *For a detailed description of the Receive FEAC Processor within the Receive DS3 HDLC Controller block, please see* Section 4.3.3.1.

4.2.3.2 *Message-Oriented Signaling (e.g., LAP-D) processing via the Transmit DS3 HDLC Controller*

The LAPD Transmitter within the Transmit DS3 HDLC Controller Block allows the user to transmit Path Maintenance Data Link (PMDL) messages to the remote terminal via the outbound DS3 Frames. The

message bits are inserted into and carried by the 3 DL bit fields of F-Frame #5 within each DS3 M-frame. The on-chip LAPD transmitter supports both the 76 byte and 82 byte length message formats and the Framer allocates 88 bytes of on-chip RAM (e.g., the Transmit LAPD Message buffer) to store the message to be transmitted. The message format complies with ITU-T Q.921 (LAP-D) protocol with different addresses and is presented below in Figure 50.

NOTE: {(Header = 4bytes) + (Payload = 82 bytes max) = 86 bytes + FCS = 2 bytes} = 88 bytes. But, FCS is always computed by the Framer. The user must write a max of 86 bytes only.

FIGURE 50. LAPD MESSAGE FRAME FORMAT

Flag Sequence (8 bits)		
SAPI (6-bits)	C/R	EA
TEI (7 bits)		EA
Control (8-bits)		
76 or 82 Bytes of Information (Payload)		
FCS - MSB		
FCS - LSB		
Flag Sequence (8-bits)		

Where: Flag Sequence = 0x7E

SAPI + CR + EA = 0x3C or 0x3E

TEI + EA = 0x01

Control = 0x03

Comprise the 4 HEADER Bytes

Flag Sequence Byte

The Flag Sequence byte is of the value 0x7E and is used for two purposes

1. To denote the boundaries of the LAPD Message Frame, and
2. To function as the Idle Pattern (e.g., Transmit HDLC Controller block transmits a continuous stream of flag sequence octets whenever no LAPD Message is being transmitted).

The user must write this value (0x7E) at address 0x86.

SAPI - Service Access Point Identifier

The SAPI bit-fields are assigned the value of 001111b or 15 (decimal).

TEI - Terminal Endpoint Identifier

The TEI bit-fields are assigned the value of 0x00. The TEI field is used in N-ISDN systems to identify a terminal out of multiple possible terminal. However, since the Framer IC transmits data in a point-to-point manner, the TEI value is unimportant.

The user must write 0x3C or 0x3E at address 0x87 and 0x01 at address ox88.

Control

The Control identifies the type of frame being transmitted. There are three general types of frame formats: Information, Supervisory, and Unnumbered. The Framer assigns the Control byte the value 0x03. Hence, the Framer will be transmitting and receiving Unnumbered LAPD Message frames.

The user must write 0x03 at address 0x89.

Information Payload

The Information Payload is the 76 bytes or 82 bytes of data (e.g., the PMDL Message) that the has been written into the on-chip Transmit LAPD Message buffer (located at addresses 0x8A through 0xDB).

It is important to write in a specific octet value into the first byte position within the Transmit LAPD Message buffer (located at Address = 0x8A). The value of this octet depends upon the type of LAPD Message frame/ PMDL Message that the user wishes to transmit. Table 21 lists the various types of LAPD Message frames/ PMDL Messages that are supported by the XRT72L50 Framer and the corresponding octet value that must be written into the first octet position within the Transmit LAPD Message buffer.

TABLE 21: THE LAPD MESSAGE TYPE AND THE CORRESPONDING VALUE OF THE FIRST BYTE WITHIN THE INFORMATION PAYLOAD

LAPD MESSAGE TYPE	VALUE OF FIRST BYTE, WITHIN INFORMATION PAYLOAD OF MESSAGE	MESSAGE SIZE
CL Path Identification	0x38	76 bytes
IDLE Signal Identification	0x34	76 bytes
Test Signal Identification	0x32	76 bytes
ITU-T Path Identification	0x3F	82 bytes

Frame Check Sequence Bytes

The 16 bit FCS (Frame Check Sequence) is calculated over the LAPD Message Header and Information Payload bytes by using the CRC-16 polynomial, $x^{16} + x^{12} + x^5 + 1$.

NOTE: *For FCS calculation, Header also includes the starting Flag Sequence byte (0x7E).*

Operation of the LAPD Transmitter

If a message is to be transmitted via the LAPD Transmitter, the information portion (or the body) of the message must be written into the Transmit LAPD Message Buffer located at 0x8A through 0xDB in on-chip RAM via the Microprocessor Interface. Afterwards, three things must be done:

STEP 1 - Specifying the Length of the LAPD Message

One of two different sizes of LAPD Messages can be transmitted. This is accomplish by writing the appropriate data to bit 1 within the Tx DS3 LAPD Configuration Register. The bit-format of this register is presented below.

Transmit DS3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	X	0	X	X

The relationship between the contents of bit-fields 1 and the LAPD Message size is given in Table 22.

TABLE 22: RELATIONSHIP BETWEEN TXLAPD MSG LENGTH AND THE LAPD MESSAGE SIZE

TXLAPD MSG LENGTH	LAPD MESSAGE LENGTH
0	LAPD Message size is 76 bytes
1	LAPD Message size is 82 bytes

The Message Type selected must correspond with the contents of the first byte of the Information (Payload) portion, as presented in Table 21 and written at address 0x8A.

STEP 2 - Enabling the LAPD Transmitter

Prior to the transmission of any data via the LAPD Transmitter, the LAPD Transmitter must be enabled. This is accomplished by writing a “1” to Bit 0 of the Tx DS3 LAPD Configuration Register, as depicted below.

Transmit DS3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	X	0	X	1

Bit 0 - TxLAPD Enable

This bit-field allows the user to enable or disable the LAPD Transmitter in accordance with Table 23.

TABLE 23: RELATIONSHIP BETWEEN TXLAPD MSG LENGTH AND THE LAPD MESSAGE SIZE

TXLAPD ENABLE	RESULTING ACTION OF THE LAPD TRANSMITTER
0	The LAPD Transmitter is disabled and the DL bits, in the DS3 frame, are transmitted as all 1’s.
1	The LAPD Transmitter is enabled and is transmitting a continuous stream of Flag Sequence octets (0x7E).

Prior to executing Step 2, the LAPD Transmitter is disabled and the Transmit DS3 Framer block is setting each of the DL bits within the outbound DS3 data stream to “1”. After this step is executed, the LAPD Transmitter begins transmitting the flag sequence octet (0x7E) via the DL bits.

NOTE: *Upon power up or reset, the LAPD Transmitter is disabled. Therefore, this bit must be set to a "1" in order to enable the LAPD Transmitter.*

STEP 3 - Initiate the Transmission

At this point, the LAPD Transmitter is ready to begin transmission. The user has written the information portion of the PMDL message into the on-chip Transmit LAPD Message buffer. Further, the user has specified the type of LAPD message that is to be transmitted and has enabled the LAPD Transmitter. To initiate the transmission of this message, write a "1" to Bit 3 (TxDL Start) of the Tx DS3 LAPD Status/Interrupt Register. The bit format of this register is presented below.

Transmit DS3 LAPD Status/Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Tx DL Start	Tx DL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	1	X	X	X

A "0" to "1" transition of Bit 3 (TxDL Start) in this register, initiates the transmission of the data link message. While the LAPD transmitter is transmitting the message, Bit 2 (TxDL Busy) is set to “1”. This bit-field allows the user to poll the status of the LAPD Transmitter. Once the message transfer is completed, this bit-field toggles back to “0”.

The LAPD Transmitter can be configured to interrupt the µC/µP upon completion of transmission of the LAPD Message by setting Bit 1 (TxLAPD Interrupt Enable) of the Tx DS3 LAPD Status/Interrupt register to “1”. The purpose of this interrupt is to let the local µC/µP know that the LAPD Transmitter is available and ready to transmit a new message. Bit 0 reflects the interrupt status for the LAPD Transmitter.

NOTE: *This bit-field will be reset on reading this register.*

Details Associated with the Transmission of a PMDL Message

Once the user has invoked the TxDL Start command and written the LAPD Transmitter does the following.

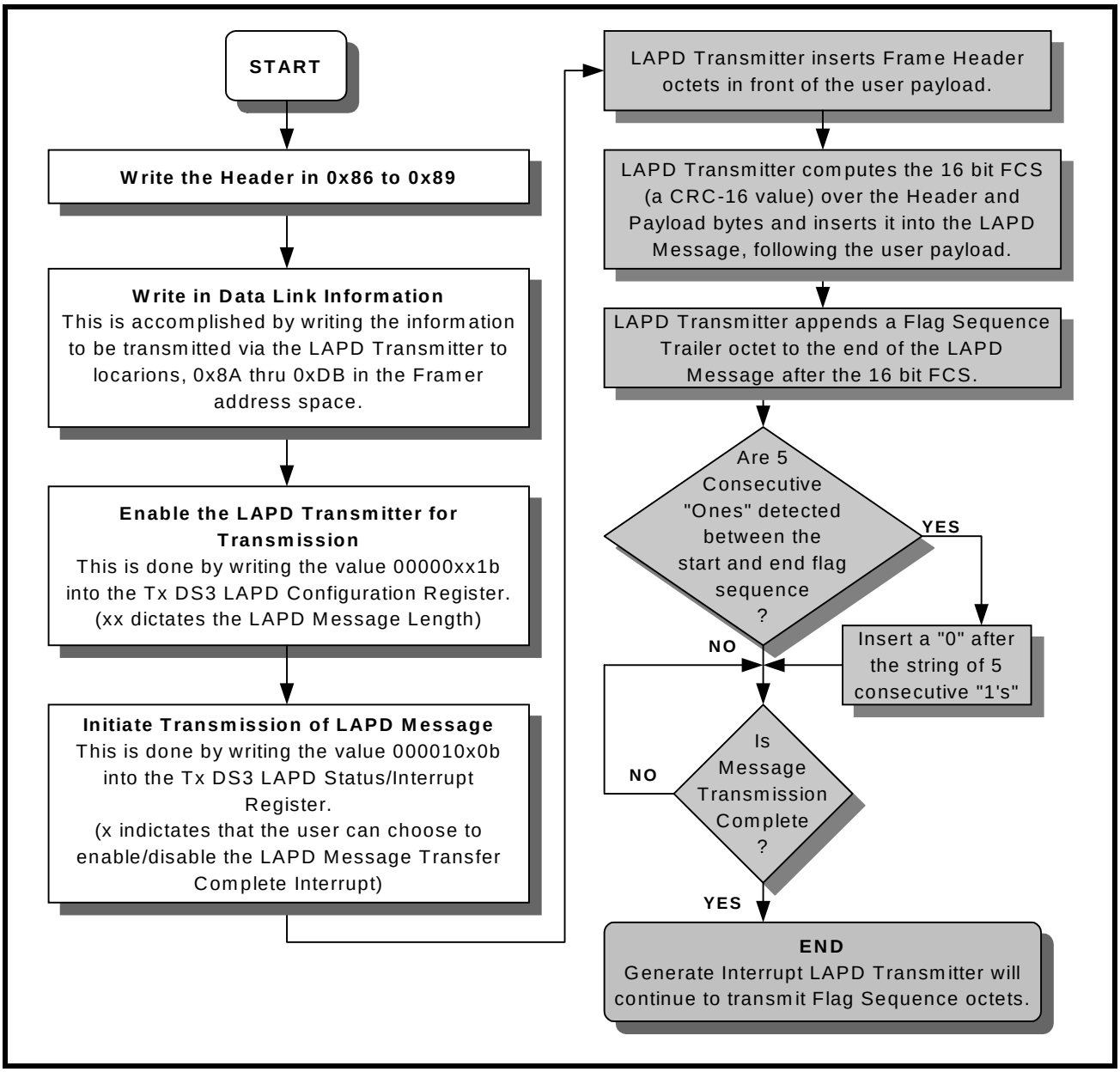
- Depending on the message type, compute the 16 bit Frame Check Sum (FCS) of the LAPD Message Frame (e.g., of the LAPD Message header and information payload) and append this value to the LAPD Message, (at the end of 76 or 82 bytes).
- Append a trailer Flag Sequence octet to the end of the message LAPD following the 16 bit FCS value.
- Serialize the composite LAPD message. Between the two 0x7E flags, ZeroStuff any consecutive five “Ones” by inserting an extra “0”. This insures that any occurrence of 0x7E in the payload does not serve as a terminating flag sequence. Insert the Zero Stuffed LAPD message into the DL bit fields of each outgoing DS3 Frame.
- Complete the transmission of the frame overhead, payload, FCS value, and trailer Flag Sequence octet via the Transmit DS3 Framer.

Once the LAPD Transmitter has completed its transmission of the LAPD Message, the Framer generates an interrupt to the local µC/µP (if enabled). Afterwards, the LAPD Transmitter proceeds to retransmit the LAPD Message repeatedly at one second intervals. During Idle periods (e.g., in between these transmission of the LAPD Message), the LAPD Transmitter will be sending a continuous stream of Flag Sequence Bytes. The LAPD Transmitter continues this behavior until the user has disabled the LAPD Transmitter by writing a "0" to bit 0 (TxLAPD Enable) within the Tx DS3 LAPD Configuration Register. If the LAPD Transmitter is idle, then it will continuously send the Flag Sequence octets (via the DL bits of each outbound DS3 Frame) to the remote terminal equipment.

NOTE: *In order to prevent the user's data (e.g., the payload portion of the LAPD Message Frame) from mimicking the Flag Sequence byte, the LAPD Transmitter will insert a "0" into the LAPD data stream immediately following the detection of five (5) consecutive 1s (this stuffing occurs for all bits between the two flag sequence bytes 0x7E). The 'remote' LAPD Receiver (see Section 4.3.3.2) will have the responsibility of detecting the 5 consecutive 1s and removing the subsequent "0" from the payload portion of the incoming LAPD message.*

Figure 51 presents a flow chart depicting the procedure (in white boxes) that the user should use in order to transmit a LAPD message. This figure also indicates (via the shaded boxes) what the LAPD Transmitter circuitry will do before and during message transmission.

FIGURE 51. FLOW CHART DEPICT HOW TO USE THE LAPD TRANSMITTER



The Mechanics of Transmitting a New LAPD Message

As mentioned above, after the LAPD Transmitter has been enabled, and commanded to transmit the message, residing in the Transmit LAPD Message buffer, it will continue to transmit this message at one-second intervals. If another (e.g., different) PMDL message is to be transmitted to the Remote LAPD Receiver, the new message will have to be written into the Transmit LAPD Message buffer, via the Microprocessor Interface section of the Framer. However, care must be taken when writing in this new message. If this message is written into the Transmit LAPD Message buffer at the wrong time (with respect to these one-second transmissions), the user's action could interfere with these transmissions, thereby causing the LAPD Transmitter to transmit a corrupted message to the Remote LAPD Receiver. In order to avoid this problem, while writing the new message into the Transmit LAPD Message buffer, the following should be done:

1. Configure the Framer to automatically reset activated interrupts

This can be done by writing a "1" into Bit 3 of the Framer Operating Mode Register, as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	1	0	1	X	X	X

This action will prevent the LAPD Transmitter from generating its own one-second interrupts.

2. Enable the One-Second Interrupt

This can be done by writing a "1" into Bit 0 of the Block Interrupt Enable Register, as depicted below.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	0	X

3. Write the new message into the Transmit LAPD Message buffer immediately after the occurrence of the One-Second interrupt.

By timing the writes to the Transmit LAPD Message buffer to occur immediately after the occurrence of the One-Second interrupt, the user avoids conflicting with the one-second transmissions of the LAPD Message, and will transmit the correct messages to the remote LAPD Receiver.

4.2.4 The Transmit DS3 Framer Block

4.2.4.1 *Brief Description of the Transmit DS3 Framer*

The Transmit DS3 Framer block accepts data from any of the following three sources, and uses it to form the DS3 data stream.

- The Transmit Payload Data Input block
- The Transmit Overhead Data Input block
- The Transmit HDLC Controller block
- The Internal Overhead Data Generator

The manner in how the Transmit DS3 Framer block handles data from each of these sources is described below.

Handling of data from the Transmit Payload Data Input Interface

For DS3 applications, all data that is input to the Transmit Payload Data Input Interface will be inserted into the payload bit positions within the outbound DS3 frames.

Handling of data from the Internal Overhead Bit Generator

By default, the Transmit DS3 Framer block will internally generate the overhead bits. However, if the Terminal Equipment inserts its own values for the overhead bits (via the Transmit Overhead Data Input Interface) or, if the user enables and employs the Transmit DS3 HDLC Controller block, then these internally generated overhead bits will be overwritten.

Handling of data from the Transmit Overhead Data Input Interface

For DS3 applications, the Transmit DS3 Framer block automatically generates and inserts the framing alignment bits (e.g., the F and M bits) into the outbound DS3 frames. Further, the Transmit DS3 Framer block will automatically compute and insert the P-bits into the outbound DS3 frames. Hence, the Transmit DS3 Framer block will not accept data from the Transmit OH Data Input Interface block for the F, M and P bits.

However, the Transmit DS3 Framer block will accept (and insert) data from the Transmit Overhead Data Input Interface for the following bit-fields.

- X-bits
- FEBE bits
- FEAC bits
- DL bits
- UDL bits
- CP bits

If the user's local Data Link Equipment activates the Transmit Overhead Data Input Interface block and writes data into this interface for these bits, then the Transmit DS3 Framer block will insert this data into the appropriate overhead bit-fields, within the outbound DS3 frames.

Handling of Data from the Transmit HDLC Controller block

The exact manner in how the Transmit DS3 Framer handles data from the Transmit HDLC Controller block depends upon whether the Transmit HDLC Controller is transmitting BOS (Bit Oriented Signaling) or MOS (Message Oriented Signaling) data.

If the Transmit DS3 HDLC Controller block is not activated, then the Transmit DS3 Framer block will insert a “1” into each FEAC and DL bit-field, within each outbound DS3 frame.

If the Transmit DS3 HDLC Controller block is activated, and is configured to transmit either a BOS or MOS type message, then data will be inserted into the FEAC and DL bit-fields as described in Section 4.2.3.

4.2.4.2 *Detailed Functional Description of the Transmit DS3 Framer Block*

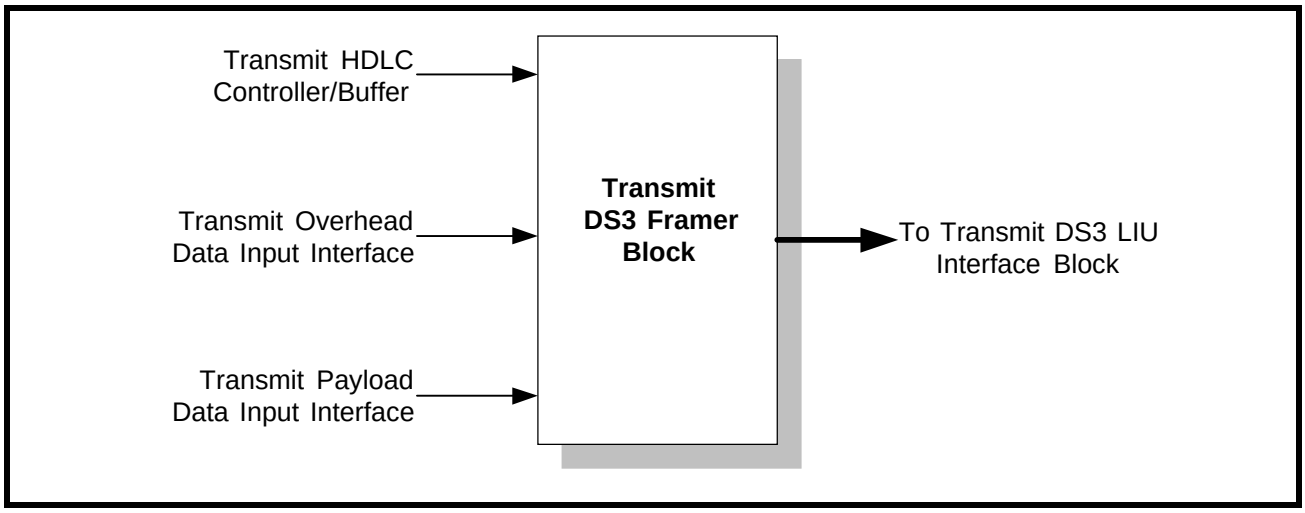
The Transmit DS3 Framer receives data from the following three sources and combines them together to form a DS3 data stream.

- The Transmit Payload Data Input Interface block.
- The Transmit Overhead Data Input Interface block
- The Transmit HDLC Controller block.

Afterwards, this DS3 data stream will be routed to the Transmit DS3 LIU Interface block, for further processing.

Figure 52 presents a simple illustration of the Transmit DS3 Framer block, along with the associated paths to the other functional blocks within the chip.

FIGURE 52. THE TRANSMIT DS3 FRAMER BLOCK AND THE ASSOCIATED PATHS TO OTHER FUNCTIONAL BLOCKS



In addition to taking data from multiple sources and multiplexing them, in appropriate manner, to create the outbound DS3 frames, the Transmit DS3 Framer block has the following roles.

- Generating Alarm Conditions
- Generating Errored Frames (for testing purposes)
- Routing outbound DS3 frames to the Transmit DS3 LIU Interface block

Each of these additional roles are discussed below.

4.2.4.2.1 Generating Alarm Conditions

By writing the appropriate data into the on-chip registers, the Transmit DS3 Framer block permits the user to override the data that is being written into the Transmit Payload Data and Overhead Data Input Interfaces and transmit the following alarm conditions.

- Generate the Yellow Alarms (or FERF indicators)
- Manipulate the X-bit (set them to “1”)
- Generate the AIS Pattern
- Generate the IDLE pattern
- Generate the LOS pattern
- Generate FERF (Yellow) Alarms, in response to detection of a Red Alarm condition (via the Receive Section of the XRT72L50).
- Generate and transmit a desired value for FEBE (Far-End-Block Error).

The procedure and results of generating any of these alarm conditions is presented below.

Each of these options can be exercised by writing the appropriate data to the Tx DS3 Configuration Register (Address = 0x30). The bit format of this register is presented below.

Tx DS3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Tx Yellow Alarm	Tx X-Bit	Tx IDLE Pattern	Tx AIS Pattern	Tx LOS Pattern	FERF on LOS	FERF on OOF	FERF on AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

The role/function of each of these bit-fields within the register, are discussed below.

4.2.4.2.1.1 *Transmit Yellow Alarm - Bit 7*

This read/write bit field permits the user to force the transmission of a Yellow Alarm to the remote terminal equipment via software control. If the user opts to transmit a Yellow Alarm then both of the X-bits, within the outbound DS3 frames will be set to '0'. Table 24 relates the content of this bit field to the Transmit DS3 Framer block's action.

TABLE 24: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 7 (TX YELLOW ALARM) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER BLOCK'S ACTION

BIT 7	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The X-bits are generated by the Transmit DS3 Framer block based upon Near End Receiving Conditions (as detected by the Receive Section of the chip)
1	**Transmit Yellow Alarm:** The Transmit DS3 Framer block will overwrite the X-bits by setting them all to 0. The payload information is not modified and is transmitted as normal.

NOTE: *This bit is ignored when either the TxIDLE, TxAIS, or the TxLOS bit-fields are set.*

4.2.4.2.1.2 *Transmit X-bit - Bit 6*

This bit field functions as the logical complement to Bit 7 (e.g., Tx Yellow Alarm). This read/write bit field permits the user to force all of the X-bits, in the outbound DS3 frames, to "1" and transmit them to the remote terminal equipment. Table 25 relates the content of this bit field to the Transmit DS3 Framer Block's action.

TABLE 25: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 6 (TX X-BITS) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER BLOCK'S ACTION

BIT 6	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The X-bits are generated by the Transmit DS3 Framer block based upon Receiving Conditions (as detected by the Receive Section of the Framer chip).
1	**Set X-bits to 1:** The Transmit DS3 Framer will overwrite the X-bits by setting them to 1. Payload information is not modified and is transmitted as normal.

NOTE: *This bit is ignored when either the Transmit Yellow Alarm, Tx AIS, Tx IDLE, or TxLOS bit is set.*

4.2.4.2.1.3 *Transmit Idle Pattern - Bit 5*

This read/write bit field permits the user to transmit an Idle pattern to the remote terminal equipment upon software control. Table 26 relates the contents of this bit field to the Transmit DS3 Framer's action.

TABLE 26: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 5 (TX IDLE) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER ACTION

BIT 5	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The Overhead bits are either internally generated, or they are inserted via the Transmit Overhead Data Input Interface or the Transmit HDLC Controller blocks. The Payload bits are received from the Transmit Payload Data Input Interface.
1	**Transmit Idle Condition Pattern:** When this command is invoked, the Transmit DS3 Framer will do the following: • Set the X-bits to 1 • Set the CP-Bits (F-Frame #3) to 0 • Generate Valid M, F, and P bits Overwrite the data in the DS3 payload with a repeating 1100... pattern.

NOTE: *This bit is ignored when either the Tx AIS or the Tx LOS bit is set.*

4.2.4.2.1.4 *Transmit AIS Pattern - Bit 4*

This read/write bit field allows the user to transmit an AIS pattern to the remote terminal equipment, upon software control. Table 27 relates the contents of this bit field to the Transmit DS3 Framer block's action.

TABLE 27: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 4 (TX AIS PATTERN) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER BLOCK'S ACTION

BIT 4	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The Overhead bits are either internally generated, or they are inserted via the Transmit Overhead Data Input Interface or the Transmit HDLC Controller blocks. The Payload bits are received from the Transmit Payload Data Input Interface.
1	**Transmit AIS Pattern:** When this command is invoked, the Transmit DS3 Framer block will do the following. • Set the X-bits to 1 • Set all the C-bits to 0 • Generate valid M, F, and P bits Overwrite the data in the DS3 payload with a repeating 1010... pattern

NOTE: *This bit is ignored when the TxLOS bit is set.*

4.2.4.2.1.5 *Transmit LOS Pattern - Bit 3*

This read/write bit field allows the user to transmit an LOS (Loss of Signal) pattern to the remote terminal, upon software control. Table 28 relates the contents of this bit field to the Transmit DS3 Framer block's action.

TABLE 28: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 3 (TX LOS) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER BLOCK'S ACTION

BIT 3	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The Overhead bits are either internally generated, or they are inserted via the Transmit Overhead Data Input Interface or the Transmit HDLC Controller blocks. The Payload bits are received from the Transmit Payload Data Input Interface.
1	**Transmit LOS Pattern:** When this command is invoked the Transmit DS3 Framer will do the following. • Set all of the overhead bits to "0" (including the M, F, and P bits) Overwrite the DS3 payload bits with an all zeros pattern.

NOTE: *When this bit is set, it overrides all of the other bits in this register.*

4.2.4.2.1.6 *FERF (Far-End Receive Failure) on LOS - Bit 2*

This Read/Write bit-field allows the user to configure the Transmit DS3 Framer block to automatically generate a Yellow Alarm if the Near-End Receive Section (of the XRT72L50) detects a LOS (Loss of Signal) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

4.2.4.2.1.7 *FERF (Far-End Receive Failure) on OOF - Bit 1*

This Read/Write bit-field allows the user to configure the Transmit DS3 Framer block to automatically generate a Yellow Alarm if the Near-End Receive Section (of the XRT72L50) detects an OOF (Out-of-Frame) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

4.2.4.2.1.8 *FERF (Far-End Receive Failure) on AIS - Bit 0*

This Read/Write bit-field allows the user to configure the Transmit DS3 Framer block to automatically generate a Yellow Alarm if the Near-End Receive Section (of the XRT72L50) detects an AIS (Alarm Indication Signal) pattern.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

4.2.4.2.1.9 *Transmitting FEBE (Far-End Block Error) Values*

By default, the Transmit DS3 Framer block will set the three (3) FEBE bit-fields to [1, 1, 1] if all of the following conditions are true.

- The Local Receive DS3 Framer block detects no P-Bit Errors.
- The Local Receive DS3 Framer block detects no CP-Bit Errors

Conversely, the Transmit DS3 Framer block will set the three (3) FEBE bit-fields to a value other than [1, 1, 1] if any one of the following conditions are true.

- The Local Receive DS3 Framer block detects a P-bit Error in the most recently received DS3 frame.
- The Local Receive DS3 Framer block detects a CP bit Error in the most recently received DS3 frame.

4.2.4.2.2 Generating Errored DS3 Frames

The Transmit DS3 Framer block permits the user to insert errors into the framing and error detection overhead bits (e.g., the P, M and F-bits) of the outbound DS3 data stream in order to support Far-End Equipment testing. This option can be exercised by writing data to any of the numerous Transmit DS3 Mask Registers. These Mask Registers and their comprising bit-fields are defined below.

Tx DS3 M-Bit Mask Register, Address = 0x35

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
TxFEBE DAT[2]	TxFEBE DAT[1]	TxFEBE DAT[0]	FEBE Reg Enable	TxErr PBit	MBit Mask(2)	MBit Mask(1)	MBit Mask(0)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

The bit-fields of the Tx DS3 M-bit Mask Register, that are relevant to error-insertion are shaded. The remaining bit-fields pertain to the FEBE bit-fields, and are discussed in Section 4.2.4.2.1.9.

The Tx DS3 M-Bit Mask Register serves two purposes

1. It allows user values to be transmited for FEBE (3 bits) - please see Section 4.2.4.2.1.9.
2. It allows the user to transmit errored P-bits.
3. It allows the user to insert errors into the M-bit (framing bits) in order to support equipment testing.

Each of these bit-fields are discussed below.

Bit 3 - Tx Err (Transmit Errored) P-Bit

This bit-field allows the user to insert errors into the P-bits, of each outbound DS3 Frame, for equipment testing purposes. If this bit-field is 0, then the P-Bits are transmitted as calculated from the payload of the previous DS3 frames. However, if this bit-field is 1, then the P-bits are inverted (from their calculated value) prior to transmission.

Bits 2 - 0: M-Bit Mask[2:0]

The Transmit DS3 Framer will automatically perform an XOR operation with the M-bits (in the DS3 data-stream) and the contents of the corresponding bit-field, within this register. The results of this operation will be written back into the M-bit positions within the outbound DS3 Frames. Therefore, to insure that no errors are inserted into the M-bits, make sure that the contents of the M-Bit Mask[2:0] bit-fields are 0.

F-Bit Error Insertion

The remaining mask registers (Tx DS3 F-Bit Mask1 through Mask4 registers) contain bit-fields which correspond to each of the 28 F-bits, within the DS3 frame. Prior to transmission, these bit-fields are automatically XORed with the contents of the corresponding bit fields within these Mask Registers. The result of this XOR operation is written back into the corresponding bit-field, within the outgoing DS3 frame, and is transmitted on the line. Therefore, if none of the bits are to be modified, then these registers must contain all 0s (the default value).

Tx DS3 F-Bit Mask1 Register, Address = 0x36

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Unused	Unused	Unused	Unused	FBit Mask(27)	FBit Mask(26)	FBit Mask(25)	FBit Mask(24)
RO	RO	RO	RO	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Tx DS3 F-Bit Mask2 Register, Address = 0x37

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
FBit Mask(23)	FBit Mask(22)	FBit Mask(21)	FBit Mask(20)	FBit Mask(19)	FBit Mask(18)	FBit Mask(17)	FBit Mask(16)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Tx DS3 F-Bit Mask3 Register, Address = 0x38

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
FBit Mask(15)	FBit Mask(14)	FBit Mask(13)	FBit Mask(12)	FBit Mask(11)	FBit Mask(10)	FBit Mask(9)	FBit Mask(8)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

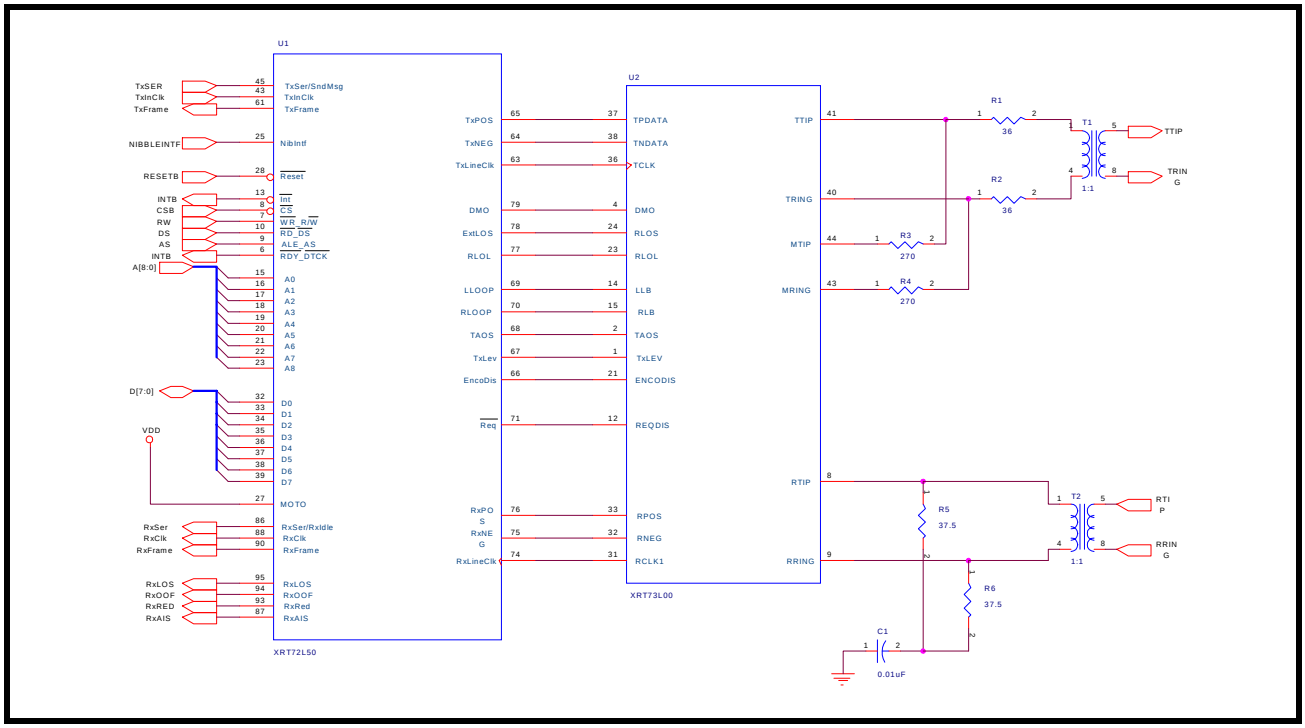
Tx DS3 F-Bit Mask4 Register, Address = 0x39

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
FBit Mask(7)	FBit Mask(6)	FBit Mask(5)	FBit Mask(4)	FBit Mask(3)	FBit Mask(2)	FBit Mask(1)	FBit Mask(0)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

4.2.5 The Transmit DS3 Line Interface Block

The XRT72L50 Framer IC is a digital device that takes DS3 payload and overhead bit information from some terminal equipment, processes this data and ultimately, multiplexes this information into a series of outbound DS3 frames. However, for DS3 coaxial cable applications, the XRT72L50 Framer IC lacks the current drive capability to be able to directly transmit this DS3 data stream through some transformer-coupled coax cable with enough signal strength for it to comply with the Isolated Pulse Template requirements and be received by the remote receiver. Therefore, in order to get around this problem, the Framer IC requires the use of an LIU (Line Interface Unit) IC. An LIU is a device that has sufficient drive capability, along with the necessary pulse-shaping circuitry to be able to transmit a signal through the transmission medium in a manner that it can (1) comply with the DSX-3 Isolated Pulse Template requirements and (2) be reliably received by the Remote Terminal Equipment. Figure 53 presents a circuit drawing depicting the Framer IC interfacing to an LIU (XRT73L00 DS3/E3/STS-1 Transmit LIU).

FIGURE 53. INTERFACING THE XRT72L50 FRAMER IC TO THE XRT73L00 DS3/E3/STS-1 LIU

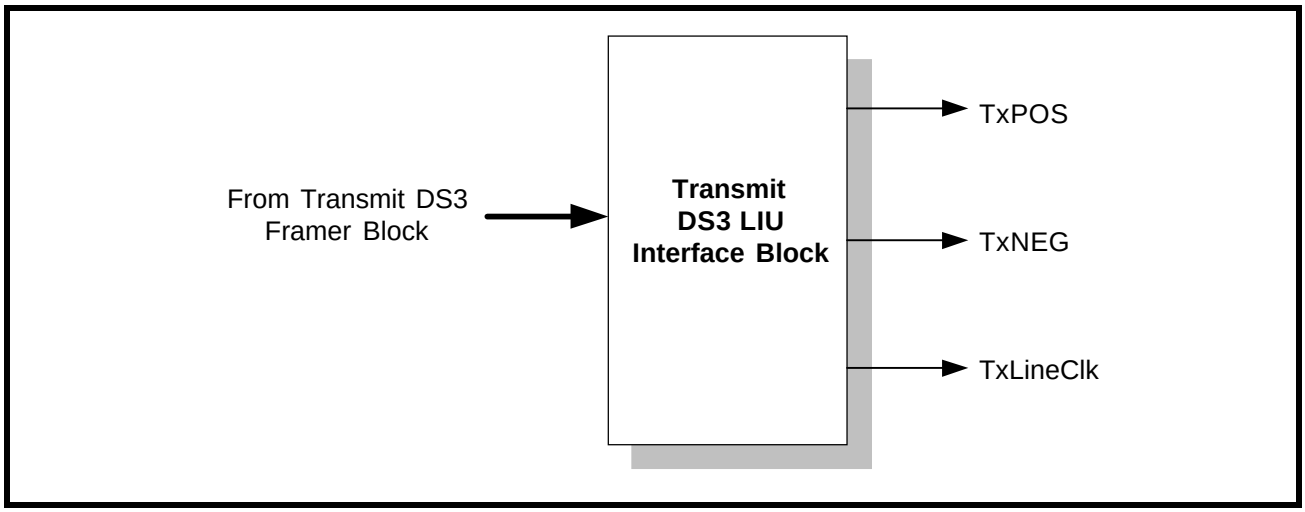


The Transmit Section of the XRT72L50 contains a block which is known as the Transmit DS3 LIU Interface block. The purpose of the Transmit DS3 LIU Interface block is to take the outbound DS3 data stream, from the Transmit DS3 Framer block, and to do the following:

1. Encode this data into one of the following line codes
   a. Unipolar (e.g., Single-Rail)
   b. AMI (Alternate Mark Inversion)
   c. B3ZS (Bipolar 3 Zero Substitution)
2. And to transmit this data to the LIU IC.

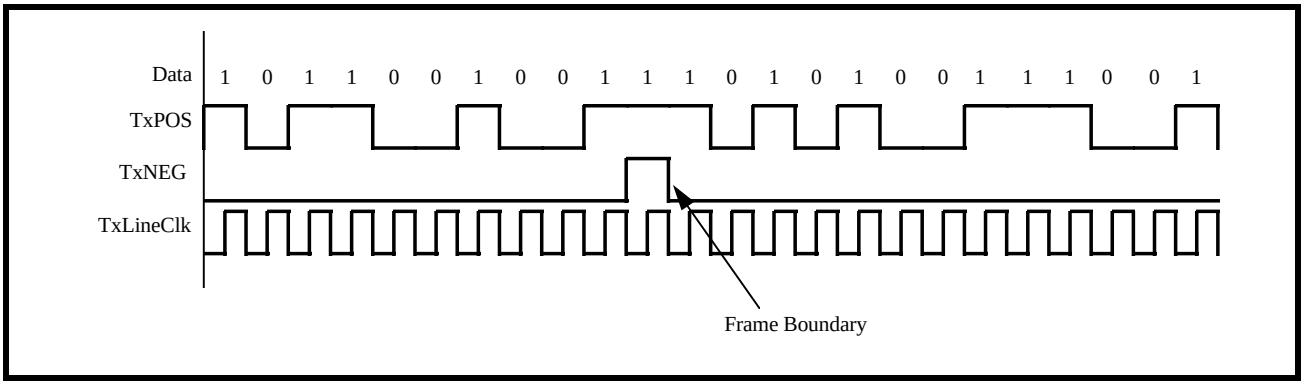
Figure 54 presents a simple illustration of the Transmit DS3 LIU Interface block.

FIGURE 54. THE TRANSMIT DS3 LIU INTERFACE BLOCK



The Transmit DS3 LIU Interface block can transmit data to the LIU IC or other external circuitry via two different output modes: Unipolar or Bipolar. If the Unipolar (or Single Rail) mode is selected, then the contents of the DS3 Frame is output, in a binary (NRZ manner) data stream via the TxPOS pin to the LIU IC. The TxNEG pin will only be used to denote the frame boundaries. TxNEG will pulse "High" for one bit period, at the start of each new DS3 frame, and will remain "Low" for the remainder of the frame. Figure 55 presents an illustration of the TxPOS and TxNEG signals during data transmission while the Transmit DS3 LIU Interface block is operating in the Unipolar mode. This mode is sometimes referred to as Single Rail mode because the data pulses only exist in one polarity: positive.

FIGURE 55. THE BEHAVIOR OF TXPOS AND TXNEG SIGNALS DURING DATA TRANSMISSION WHILE THE TRANSMIT DS3 LIU INTERFACE IS OPERATING IN THE UNIPOLAR MODE



When the Transmit DS3 LIU Interface block is operating in the Bipolar (or Dual Rail) mode, then the contents of the DS3 Frame is output via both the TxPOS and TxNEG pins. If the Bipolar mode is chosen, then the DS3 data to the LIU can be transmitted via one of two different line codes: Alternate Mark Inversion (AMI) or Binary - 3 Zero Substitution (B3ZS). Each one of these line codes will be discussed below. Bipolar mode is sometimes referred to as Dual Rail because the data pulses occur in two polarities: positive and negative. The role of the TxPOS, TxNEG and TxLineClk output pins, for this mode are discussed below.

TxPOS - Transmit Positive Polarity Pulse: The Transmit DS3 LIU Interface block will assert this output to the LIU IC when it desires for the LIU to generate and transmit a positive polarity pulse to the remote terminal equipment.

TxNEG - Transmit Negative Polarity Pulse: The Transmit DS3 LIU Interface block will assert this output to the LIU IC when it desires for the LIU to generate and transmit a negative polarity pulse to the remote terminal equipment.

TxLineClk - Transmit Line Clock: The LIU IC uses this signal from the Transmit DS3 LIU Interface block to sample the state of its TxPOS and TxNEG inputs. The results of this sampling dictates the type of pulse (positive polarity, zero, or negative polarity) that it will generate and transmit to the remote Receive DS3 Framer.

4.2.5.1 *Selecting the various Line Codes*

Either the Unipolar Mode or Bipolar Mode can be selected by writing the appropriate value to Bit 3 of the I/O Control Register (Address = 0x01), as shown below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 29 relates the value of this bit field to the Transmit DS3 LIU Interface Output Mode.

TABLE 29: THE RELATIONSHIP BETWEEN THE CONTENT OF BIT 3 (UNIPOLAR/$\overline{\text{BIPOLAR}}$) WITHIN THE UNI I/O CONTROL REGISTER AND THE TRANSMIT DS3 FRAMER LINE INTERFACE OUTPUT MODE

BIT 3	TRANSMIT DS3 FRAMER LIU INTERFACE OUTPUT MODE
0	**Bipolar Mode:** AMI or B3ZS Line Codes are Transmitted and Received
1	**Unipolar (Single Rail) Mode** of transmission and reception of DS3 data is selected.

NOTES:

1. *The default condition is the Bipolar Mode.*
2. *This selection also effects the operation of the Receive DS3 LIU Interface block*

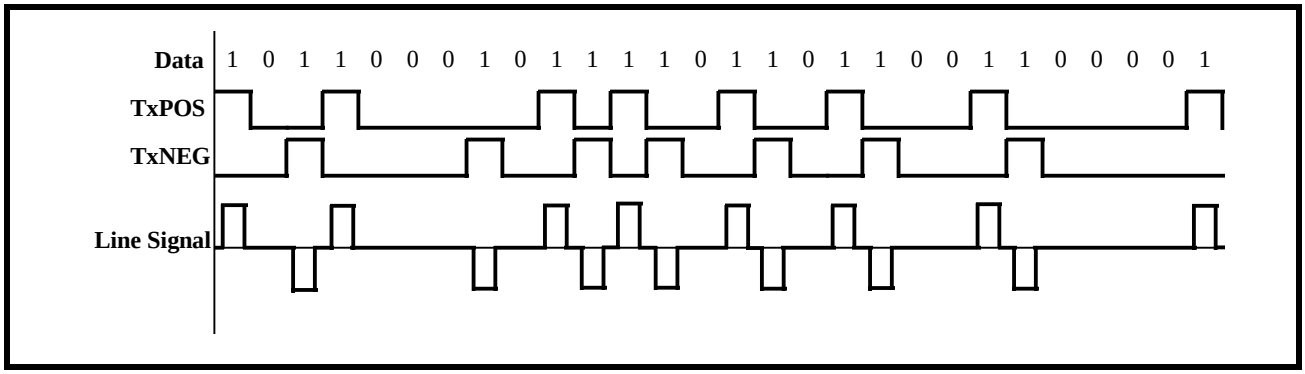
4.2.5.1.1 The Bipolar Mode Line Codes

If framer is to be operated in the Bipolar Mode, then the DS3 data-stream can be transmitted via the AMI (Alternate Mark Inversion) or the B3ZS Line Codes. The definition of AMI and B3ZS line codes follow.

4.2.5.1.1.1 *The AMI Line Code*

AMI or Alternate Mark Inversion, means that consecutive one's pulses (or marks) will be of opposite polarity with respect to each other. The line code involves the use of three different amplitude levels: +1, 0, and -1. +1 and -1 amplitude signals are used to represent one's (or mark) pulses and the "0" amplitude pulses (or the absence of a pulse) are used to represent zeros (or space) pulses. The general rule for AMI is: if a given mark pulse is of positive polarity, then the very next mark pulse will be of negative polarity and vice versa. This alternating-polarity relationship exists between two consecutive mark pulses, independent of the number of 'zeros' that may exist between these two pulses. Figure 56 presents an illustration of the AMI Line Code as would appear at the TxPOS and TxNEG pins of the Framer, as well as the output signal on the line.

FIGURE 56. ILLUSTRATION OF AMI LINE CODE



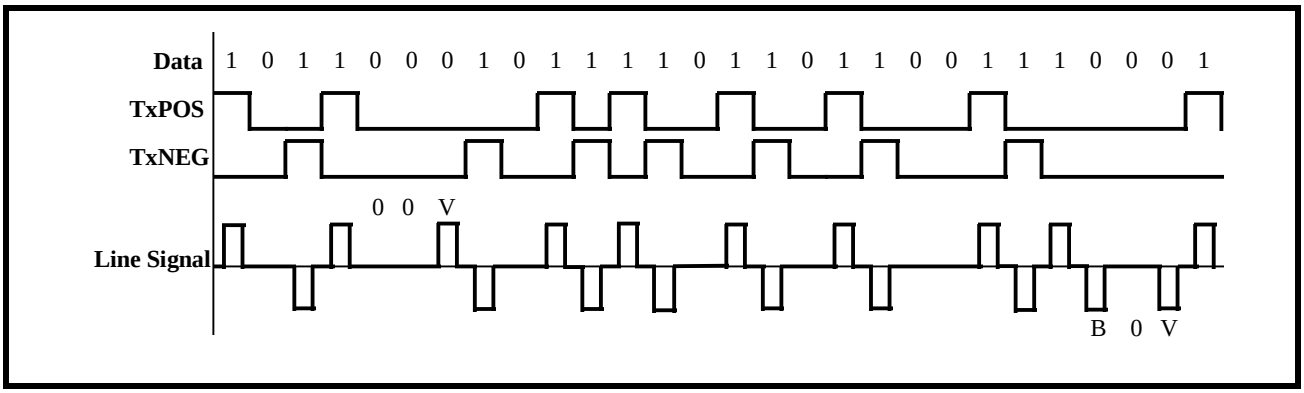
NOTE: *One of the main reasons that the AMI Line Code has been chosen for driving transformer-coupled media is that this line code introduces no dc component, thereby minimizing dc distortion in the line.*

4.2.5.1.1.2 *The B3ZS Line Code*

The Transmit DS3 Framer and the associated LIU IC combine the data and timing information (originating from the TxLineClk signal) into the line signal that is transmitted to the far-end receiver. The far-end receiver has the task of recovering this data and timing information from the incoming DS3 data stream. Many clock and data recovery schemes rely on the use of Phase Locked Loop technology. Phase-Locked-Loop (PLL) technology for clock recovery relies on transitions in the line signal, in order to maintain lock with the incoming DS3 data stream. However, PLL-based clock recovery scheme, are vulnerable to the occurrence of a long stream of consecutive zeros (e.g., the absence of transitions). This scenario can cause the PLL to lose lock with the incoming DS3 data, thereby causing the clock and data recovery process of the receiver to fail. Therefore, some approach is needed to insure that such a long string of consecutive zeros can never happen. One such technique is B3ZS encoding. B3ZS (or Bipolar 3 Zero Substitution) is a form of AMI line coding that implements the following rule.

In general the B3ZS line code behaves just like AMI with the exception of the case when a long string of consecutive zeros occur on the line. Any string of 3 consecutive zeros will be replaced with either a 00V or a B0V where B refers to a Bipolar pulse (e.g., a pulse with a polarity that is compliant with the AMI coding rule). And V refers to a Bipolar Violation pulse (e.g., a pulse with a polarity that violates the alternating polarity scheme of AMI.) The decision between inserting an 00V or a B0V is made to insure that an odd number of Bipolar (B) pulses exist between any two Bipolar Violation (V) pulses. Figure 57 presents a timing diagram that illustrates examples of B3ZS encoding.

FIGURE 57. ILLUSTRATION OF TWO EXAMPLES OF B3ZS ENCODING



The user chooses between AMI or B3ZS line coding by writing to bit 4 of the I/O Control Register (Address = 0x01), as shown below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 30 relates the content of this bit-field to the Bipolar Line Code that DS3 Data will be transmitted and received at.

TABLE 30: THE RELATIONSHIP BETWEEN BIT 4 (AMI/B3ZS*) WITHIN THE I/O CONTROL REGISTER AND THE BIPOLAR LINE CODE THAT IS OUTPUT BY THE TRANSMIT DS3 LIU INTERFACE BLOCK

BIT 4	BIPOLAR LINE CODE
0	B3ZS
1	AMI

NOTES:

1. *This bit is ignored if the Unipolar mode is selected.*
2. *This selection also effects the operation of the Receive DS3 LIU Interface block*

4.2.5.2 *TxLineClk Clock Edge Selection*

The Framer also allows the user to specify whether the DS3 output data (via TxPOS and/or TxNEG output pins) is to be updated on the rising or falling edges of the TxLineClk signal. The purpose of this feature is to insure that the Framer will always be able to output data to the LIU IC, in such a way that the LIU set-up and

hold time requirements can always be met. This selection is made by writing to bit 2 of the I/O Control Register, as depicted below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	X	X	0

Table 31 relates the contents of this bit field to the clock edge of TxClk that DS3 Data is output on the TxPOS and/or TxNEG output pins.

TABLE 31: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 2 (TXLINECLK INV) WITHIN THE I/O CONTROL REGISTER AND THE TXLINECLK CLOCK EDGE THAT TXPOS AND TXNEG ARE UPDATED ON

BIT 2	RESULT
0	**Rising Edge:** Outputs on TxPOS and/or TxNEG are updated on the rising edge of TxLineClk. See Figure 58 for timing relationship between TxLineClk, TxPOS and TxNEG signals, for this selection.
1	**Falling Edge:** Outputs on TxPOS and/or TxNEG are updated on the falling edge of TxLineClk. See Figure 59 for timing relationship between TxLineClk, TxPOS and TxNEG signals, for this selection.

NOTE: *The user will typically make the selection based upon the set-up and hold time requirements of the Transmit LIU IC.*

FIGURE 58. WAVEFORM/TIMING RELATIONSHIP BETWEEN TXLINECLK, TXPOS AND TXNEG - TXPOS AND TXNEG ARE CONFIGURED TO BE UPDATED ON THE RISING EDGE OF TXLINECLK

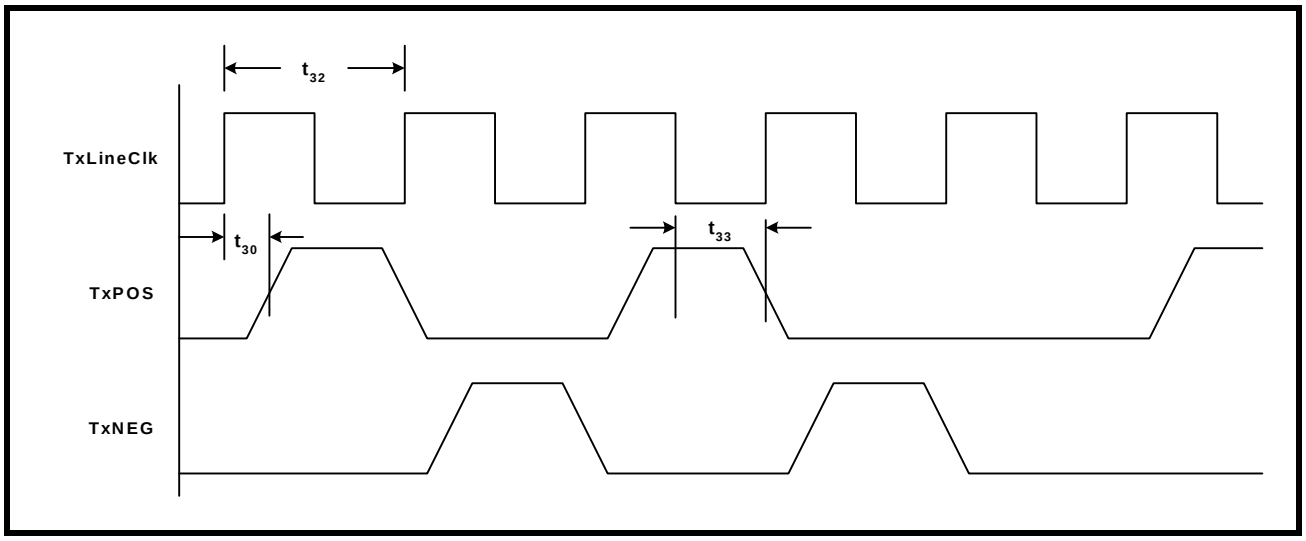
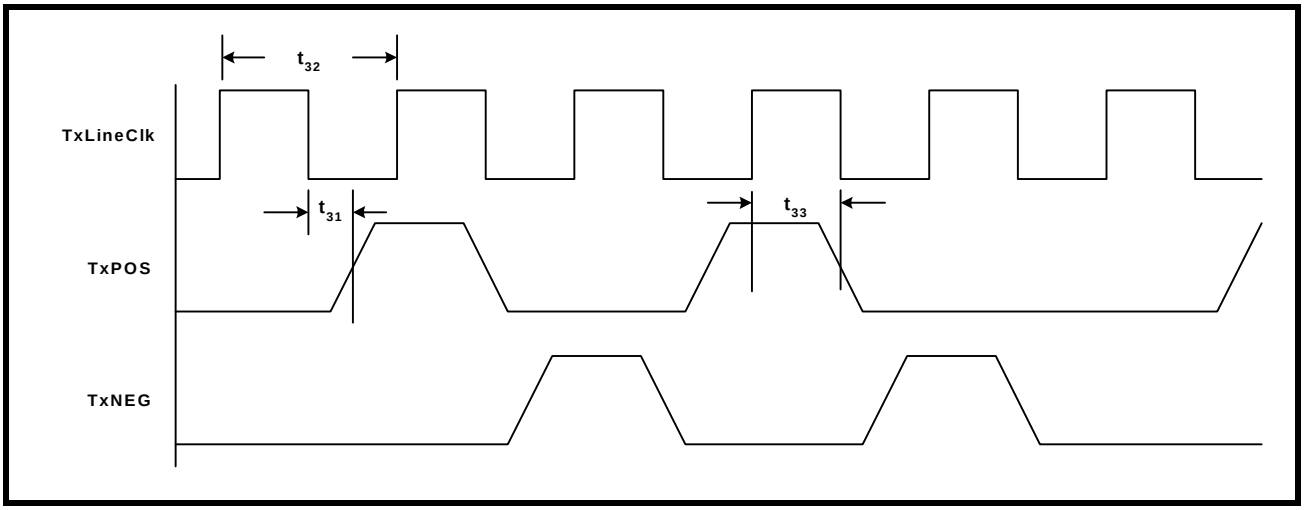


FIGURE 59. WAVEFORM/TIMING RELATIONSHIP BETWEEN TXLINECLK, TXPOS AND TXNEG - TXPOS AND TXNEG ARE CONFIGURED TO BE UPDATED ON THE FALLING EDGE OF TXLINECLK



4.2.6 Transmit Section Interrupt Processing

The Transmit Section of the XRT72L50 can generate an interrupt to the Microcontroller/Microprocessor for the following two reasons.

- Completion of Transmission of FEAC Message
- Completion of Transmission of LAPD Message

4.2.6.1 *Enabling Transmit Section Interrupts*

The Interrupt Structure, within the XRT72L50 contains two hierarchical levels:

- Block Level
- Source Level

The Block Level

The Enable State of the Block Level for the Transmit Section Interrupts dictates whether or not interrupts (if enabled at the source level), are actually enabled.

These Transmit Section interrupts can be enabled or disabled at the Block Level, by writing the appropriate data into Bit 1 (Tx DS3/E3 Interrupt Enable) within the Block Interrupt Enable register (Address = 0x04), as illustrated below.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables the Transmit Section (at the Block Level) for Interrupt Generation. Conversely, setting this bit-field to “0” disables the Transmit Section for interrupt generation.

What does it mean for the Transmit Section Interrupts to be enabled or disabled at the Block Level?

If the Transmit Section is disabled (for interrupt generation) at the Block Level, then ALL Transmit Section interrupts are disabled, independent of the interrupt enable/disable state of the source level interrupts.

If the Transmit Section is enabled (for interrupt generation) at the block level, then a given interrupt will be enabled if, it is also enabled at the source level. Conversely, if the Transmit Section is enabled (for interrupt generation) at the Block level, then a given interrupt will still be disabled, if it is disabled at the source level.

As mentioned earlier, the Transmit Section of the XRT72L50 Framer IC contains the following two interrupts

- Completion of Transmission of FEAC Message Interrupt.
- Completion of Transmission of LAPD Message Interrupt.

The Enabling/Disabling and Servicing of each of these interrupts is described below.

4.2.6.1.1 The Completion of Transmission of FEAC Message Interrupt.

If the Transmit Section interrupts have been enabled at the Block level, then the Completion of Transmission of a FEAC Message Interrupt can be enabled or disabled by writing the appropriate value into Bit 4 (Tx FEAC Interrupt Enable) within the Transmit DS3 FEAC Configuration & Status Register (Address = 0x31) as illustrated below.

Transmit DS3 FEAC Configuration & Status Register (Address = 0x31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			Tx FEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC GO	TxFEAC Busy
RO	RO	RO	R/W	RUR	R/W	R/W	RO
0	0	0	X	0	0	0	0

Setting this bit-field to “1” enables the Completion of Transmission of a FEAC Message Interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

4.2.6.1.2 Servicing the Completion of Transmission of a FEAC Message Interrupt

As mentioned earlier, once the user commands the Transmit FEAC Processor to begin its transmission of a FEAC Message, it will do the following.

1. It will read in the six-bit contents of the Tx DS3 FEAC Register (Address = 0x32) and encapsulate these 6 bits into a 16-bit data structure.
2. The Transmit FEAC Processor will then begin to transmit this 16-bit data structure (to the Remote Terminal Equipment) repeatedly for 10 consecutive times.
3. Upon completion of the 10th transmission, the XRT72L50 Framer IC will generate the Completion of Transmission of a FEAC Message Interrupt to the Microcontroller/Microprocessor. Once the XRT72L50 Framer IC generates this interrupt, it will do the following.

- Assert the Interrupt Output pin ($\overline{Int}$) by toggling it "Low".
- Set Bit 3 (Tx FEAC Interrupt Status) within the Tx DS3 FEAC Configuration & Status Register, as illustrated below.

Transmit DS3 FEAC Configuration & Status Register (Address = 0x31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			Tx FEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC GO	TxFEAC Busy
RO	RO	RO	R/W	RUR	R/W	R/W	RO
0	0	0	1	1	0	0	0

The purpose of this interrupt is to alert the Microcontroller/Microprocessor that the Transmit FEAC Processor has completed its transmission of a given FEAC message and is now ready to transmit the next FEAC Message, to the Remote Terminal Equipment.

4.2.6.1.3 The Completion of Transmission of the LAPD Message Interrupt

If the Transmit Section interrupts have been enabled at the Block level, then the Completion of Transmission of a LAPD Message Interrupt can be enabled or disabled by writing the appropriate value into Bit 1 (TxLAPD Interrupt Enable) within the Tx DS3 LAPD Status & Interrupt Register (Address = 0x34), as illustrated below.

TxDS3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	0

Setting this bit-field to “1’ enables the Completion of Transmission of a LAPD Message Interrupt. Conversely, setting this bit-field to “0” disables the Completion of Transmission of a LAPD Message interrupt.

4.2.6.1.4 Servicing the Completion of Transmission of a LAPD Message Interrupt

As mentioned previously, once the user commands the LAPD Transmitter to begin its transmission of a LAPD Message, it will do the following.

1. It will compute the FCS (Frame Check Sequence) value over the contents of 0x86 through 0xDB and append this 16 bit value to the back-end of the user-message.
2. It will parse through the contents of the Transmit LAPD Message Buffer (located at address locations 0x86 through 0xDB and the FCS bytes) and search for a string of five (5) consecutive “1’s”. If the LAPD Transmitter finds a string of five consecutive “1’s” (within the content of the LAPD Message Buffer, then it will insert a “0” immediately after this string. (Except at 0x86 which should contain the flag sequence byte 0x7E.)
3. It will append a trailing flag sequence byte, 0x7E.
4. Finally, it will begin transmitting the contents of this LAPD Message frame via the DL bits, within each outbound DS3 frame.
5. Once the LAPD Transmitter has completed its transmission of this LAPD Message frame (to the Remote Terminal Equipment), the XRT72L50 Framer IC will generate the Completion of Transmission of a LAPD Message Interrupt to the Microcontroller/Microprocessor. Once the XRT72L50 Framer IC generates this interrupt, it will do the following.

- Assert the Interrupt Output pin ($\overline{\text{Int}}$) by toggling it "Low".

- Set Bit 0 (TxLAPD Interrupt Status) within the TxDS3 LAPD Status and Interrupt Register, as illustrated below.

TxDS3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	1

The purpose of this interrupt is to alert the Microcontroller/MIcroprocessor that the LAPD Transmitter has completed its transmission of a given LAPD (or PMDL) Message, and is now ready to transmit the next PMDL Message, to the Remote Terminal Equipment.

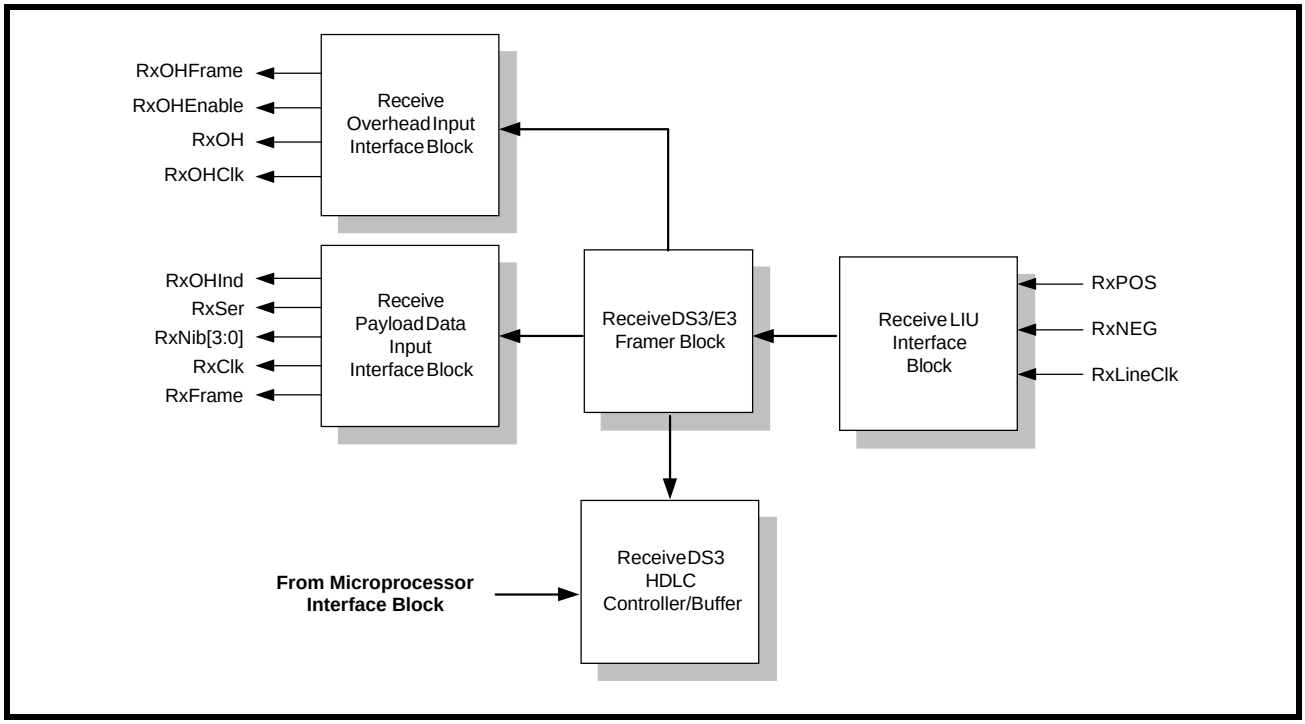
4.3 *The Receive Section of the XRT72L50 (DS3 Mode Operation)*

When the XRT72L50 has been configured to operate in the DS3 Mode, the Receive Section of the XRT72L50 consists of the following functional blocks.

- Receive LIU Interface block
- Receive HDLC Controller block
- Receive DS3 Framer block
- Receive Overhead Data Output Interface block
- Receive Payload Data Output Interface block

Figure 60 presents a simple illustration of the Receive Section of the XRT72L50 Framer IC.

FIGURE 60. THE XRT72L50 RECEIVE SECTION CONFIGURED TO OPERATE IN THE DS3 MODE



Each of these functional blocks will be discussed in detail in this document.

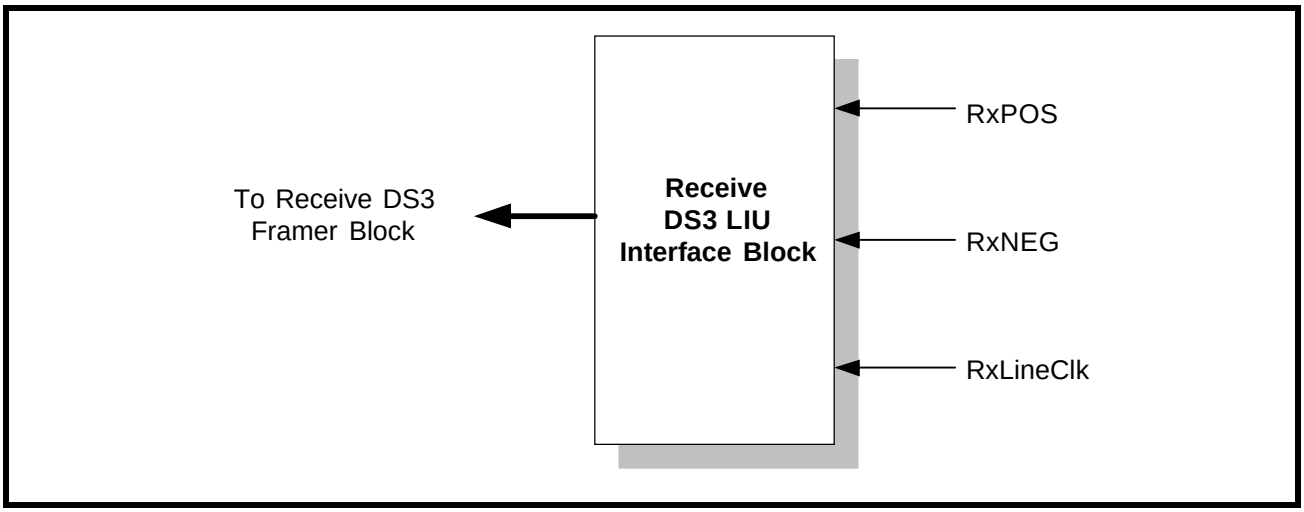
4.3.1 The Receive DS3 LIU Interface Block

The purpose of the Receive DS3 LIU Interface block is two-fold:

1. To receive encoded digital data from the DS3 LIU IC.
2. To decode this data, convert it into a binary data stream and to route this data to the Receive DS3 Framer block.

Figure 61 presents a simple illustration of the Receive DS3 LIU Interface block.

FIGURE 61. THE RECEIVE DS3 LIU INTERFACE BLOCK



The Receive Section of the XRT72L50 will via the Receive DS3 LIU Interface Block receive timing and data information from the incoming DS3 data stream. The DS3 Timing information will be received via the RxLineClk input pin and the DS3 data information will be received via the RxPOS and RxNEG input pins. The Receive DS3 LIU Interface block is capable of receiving DS3 data pulses in unipolar or bipolar format. If the Receive DS3 framer is operating in the bipolar format, then it can be configured to decode either AMI or B3ZS line code data. Each of these input formats and line codes will be discussed in detail, below.

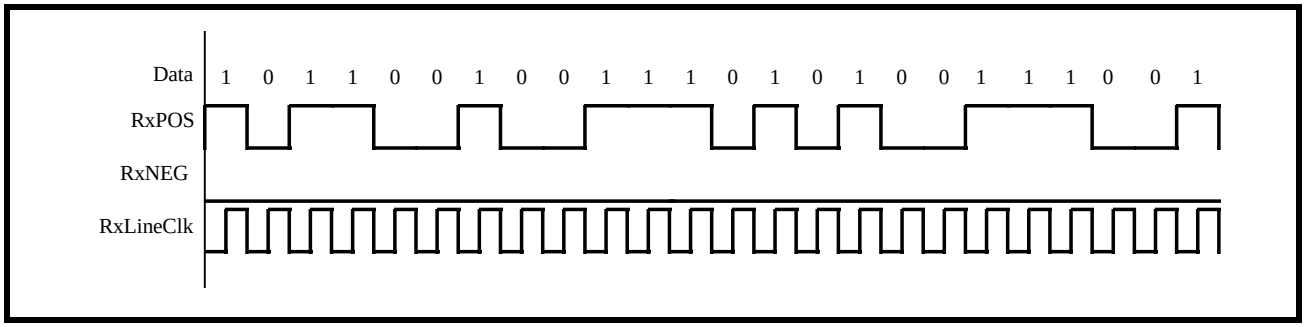
4.3.1.1 *Unipolar Decoding*

If the Receive DS3 LIU Interface block is operating in the Unipolar (single-rail) mode, then it will receive the Single Rail NRZ DS3 data pulses via the RxPOS input pin. The Receive DS3 LIU Interface block will also receive its timing signal via the RxLineClk signal.

NOTE: *The RxLineClk signal will function as the timing source for the entire Receive Section of the XRT72L50.*

No data pulses will be applied to the RxNEG input pin. The Receive DS3 LIU Interface block receives a logic "1" when a logic "1" level signal is present at the RxPOS pin, during the sampling edge of the RxLineClk signal. Likewise, a logic "0" is received when a logic "0" level signal is applied to the RxPOS pin. Figure 62 presents an illustration of the behavior of the RxPOS, RxNEG and RxLineClk input pins when the Receive DS3 LIU Interface block is operating in the Unipolar mode.

FIGURE 62. BEHAVIOR OF THE RXPOS, RXNEG AND RXLINECLK SIGNALS DURING DATA RECEPTION OF UNIPOLAR DATA



The user can configure the Receive DS3 LIU Interface block to operate in either the Unipolar or the Bipolar Mode by writing the appropriate data to the I/O Control Register, as depicted below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 32 relates the value of this bit-field to the Receive DS3 LIU Interface Input Mode.

TABLE 32: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 3 (UNIPOLAR/$\overline{\text{BIPOLAR}}$) WITHIN THE I/O CONTROL REGISTER AND THE TXLINECLK CLOCK EDGE THAT TXPOS AND TXNEG ARE UPDATED ON

BIT 3	RECEIVE DS3 LIU INTERFACE INPUT MODE
0	**Bipolar Mode (Dual Rail):** AMI or B3ZS Line Codes are Transmitted and Received.
1	**Unipolar Mode (Single Rail) Mode** of transmission and reception of DS3 data is selected.

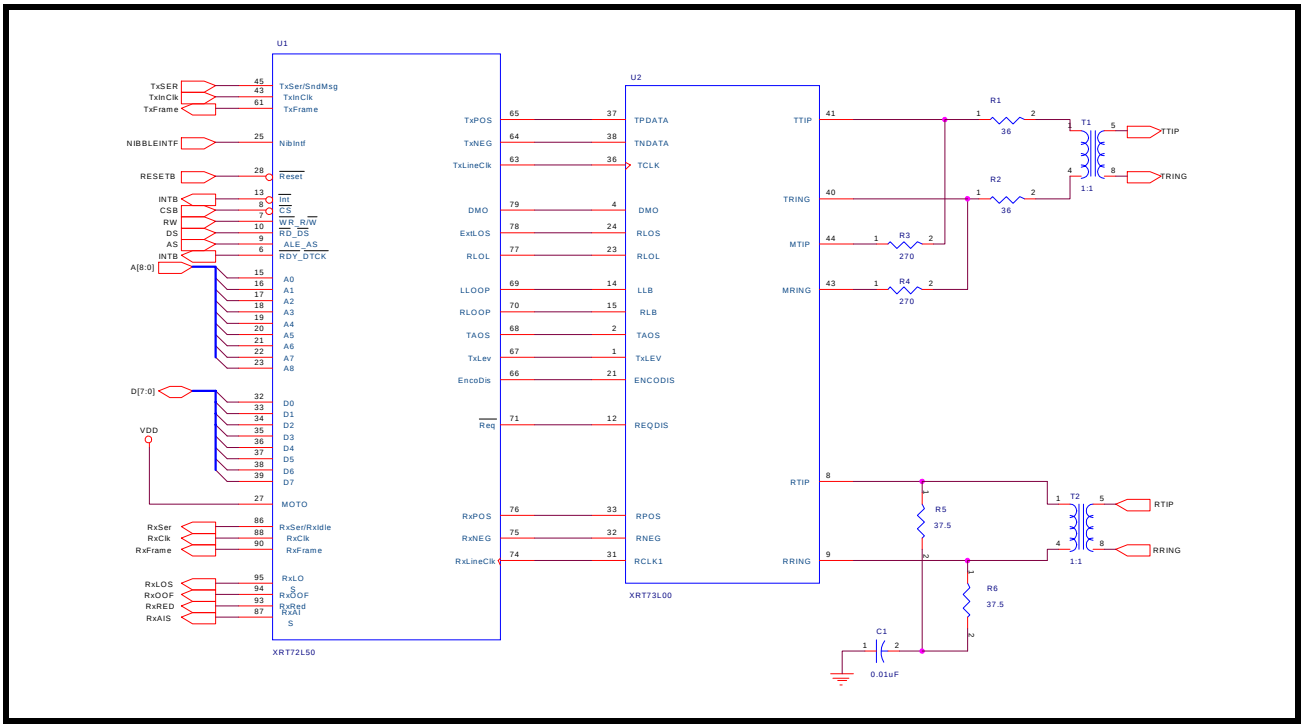
NOTES:

1. *The default condition is the Bipolar Mode.*
2. *This selection also effects the Transmit DS3 Framer Line Interface Output Mode*

4.3.1.2 *Bipolar Decoding*

If the Receive DS3 LIU Interface block is operating in the Bipolar Mode, then it will receive the DS3 data pulses via both the RxPOS, RxNEG, and the RxLineClk input pins. Figure 63 presents a circuit diagram illustrating how the Receive DS3 LIU Interface block interfaces to the Line Interface Unit while the Framer is operating in Bipolar mode. The Receive DS3 LIU Interface block can be configured to decode the incoming data from either the AMI or B3ZS line codes.

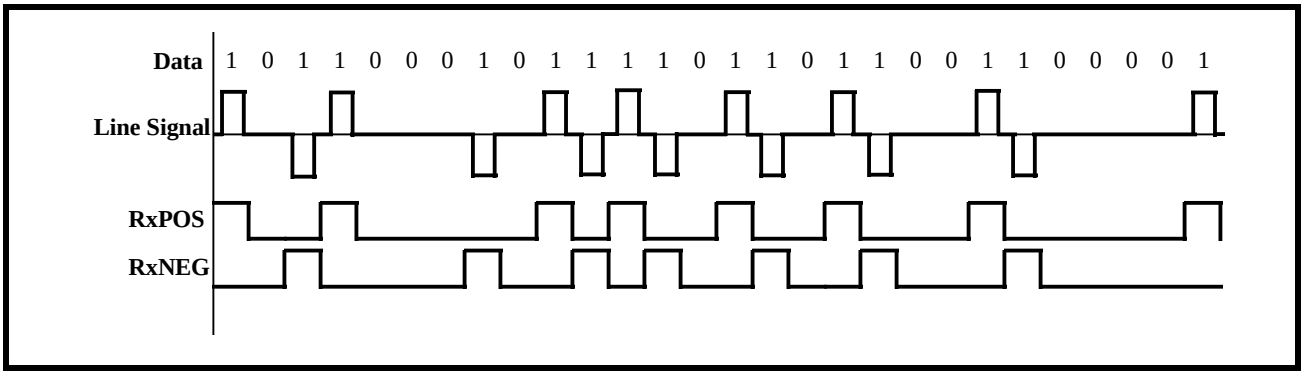
FIGURE 63. IINTERFACING THE XRT72L50 FRAMER IC TO THE XRT73L00 DS3/E3/STS-1 LIU



4.3.1.2.1 AMI Decoding

AMI or Alternate Mark Inversion, means that consecutive one's pulses (or marks) will be of opposite polarity with respect to each other. This line code involves the use of three different amplitude levels: +1, 0, and -1. The +1 and -1 amplitude signals are used to represent one's (or mark) pulses and the "0" amplitude pulses (or the absence of a pulse) are used to represent zeros (or space) pulses. The general rule for the AMI line code is: if a given mark pulse is of positive polarity, then the very next mark pulse will be of negative polarity and vice versa. This alternating-polarity relationship exists between two consecutive mark pulses, independent of the number of zeros that exist between these two pulses. Figure 64 presents an illustration of the AMI Line Code as would appear at the RxPOS and RxNEG input pins of the Framer, as well as the corresponding output signal on the line.

FIGURE 64. AMI LINE CODE



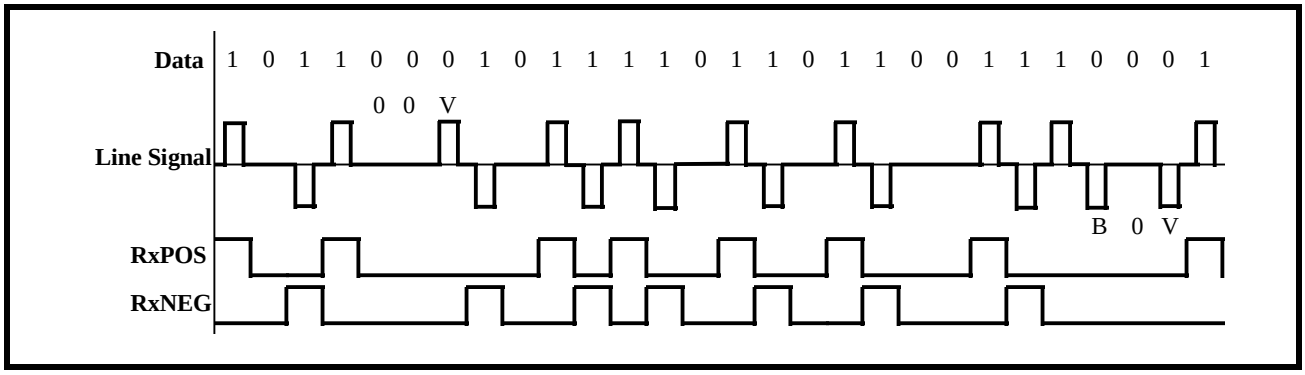
NOTE: *One of the reasons that the AMI Line Code has been chosen for driving copper medium, isolated via transformers, is that this line code has no dc component, thereby eliminating dc distortion in the line.*

4.3.1.2.2 B3ZS Decoding

The Transmit DS3 LIU Interface block and the associated LIU embed and combine the data and clocking information into the line signal that is transmitted to the remote terminal equipment. The remote terminal equipment has the task of recovering this data and timing information from the incoming DS3 data stream. Most clock and data recovery schemes rely on the use of Phase-Locked-Loop technology. One of the problems of using Phase-Locked-Loop (PLL) technology for clock recovery is that it relies on transitions in the line signal, in order to maintain lock with the incoming DS3 data-stream. Therefore, these clock recovery scheme, are vulnerable to the occurrence of a long stream of consecutive zeros (e.g., no transitions in the line). This scenario can cause the PLL to lose lock with the incoming DS3 data, thereby causing the clock and data recovery process of the receiver to fail. Therefore, some approach is needed to insure that such a long string of consecutive zeros can never happen. One such technique is B3ZS (or Bipolar 3 Zero Substitution) encoding.

In general the B3ZS line code behaves just like AMI with the exception of the case when a long string of consecutive zeros occurs on the line. Any 3 consecutive zeros will be replaced with either a 00V or a B0V where B refers to a Bipolar pulse (e.g., a pulse with a polarity that is compliant with the alternating polarity scheme of the AMI coding rule). And V refers to a Bipolar Violation pulse (e.g., a pulse with a polarity that violates the alternating polarity scheme of AMI.) The decision between inserting an 00V or a B0V is made to insure that an odd number of Bipolar (B) pulses exist between any two Bipolar Violation (V) pulses. The Receive DS3 Framer, when operating with the B3ZS Line Code is responsible for decoding the B3ZS-encoded data back into a unipolar (binary-format). For instance, if the Receive DS3 Framer detects a 00V or a B0V pattern in the incoming pattern, the Receive DS3 Framer will replace it with three consecutive zeros. Figure 65 presents a timing diagram that illustrates examples of B3ZS decoding.

FIGURE 65. ILLUSTRATION OF TWO EXAMPLES OF B3ZS DECODING



4.3.1.2.3 Line Code Violations

The Receive DS3 LIU Interface block will also check the incoming DS3 data stream for line code violations. For example, when the Receive DS3 LIU Interface block detects a valid bipolar violation (e.g., in B3ZS line code), it will substitute three zeros into the binary data stream. However, if the bipolar violation is invalid, then an LCV (Line Code Violation) is flagged and the PMON LCV Event Count Register (Address = 0x50 and 0x51) will also be incremented. Additionally, the LCV-One Second Accumulation Registers (Address = 0x6E and 0x6F) will be incremented. For example: If the incoming DS3 data is B3ZS encoded, the Receive DS3 LIU Interface block will also increment the LCV One Second Accumulation Register if three (or more) consecutive zeros are received.

4.3.1.2.4 RxLineClk Clock Edge Selection

The incoming unipolar or bipolar data, applied to the RxPOS and the RxNEG input pins are clocked into the Receive DS3 LIU Interface block via the RxLineClk signal. The Framer IC allows the user to specify which edge (e.g, rising or falling) of the RxLineClk signal will sample and latch the signal at the RxPOS and RxNEG input signals into the Framer IC. This feature was included in the XRT72L50 design to insure that the user can always meet the RxPOS and RxNEG to RxLineClk set-up and hold time requirements. This selection is made by writing the appropriate data to bit 1 of the I/O Control Register, as depicted below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 33 depicts the relationship between the value of this bit-field to the sampling clock edge of RxLineClk.

TABLE 33: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 1 (RXLINECLK INV) OF THE I/O CONTROL REGISTER, AND THE SAMPLING EDGE OF THE RXLINECLK SIGNAL

RXCLKINV (BIT 1)	RESULT
0	**Rising Edge:** RxPOS and RxNEG are sampled at the rising edge of RxLineClk. See Figure 66 for timing relationship between RxLineClk, RxPOS, and RxNEG.
1	**Falling Edge:** RxPOS and RxNEG are sampled at the falling edge of RxLineClk. See Figure 67 for timing relationship between RxLineClk, RxPOS, and RxNEG.

Figure 66 and Figure 67 present the Waveform and Timing Relationships between RxLineClk, RxPOS and RxNEG for each of these configurations.

FIGURE 66. WAVEFORM/TIMING RELATIONSHIP BETWEEN RXLINECLK, RXPOS AND RXNEG - WHEN RXPOS AND RXNEG ARE TO BE SAMPLED ON THE RISING EDGE OF RXLINECLK

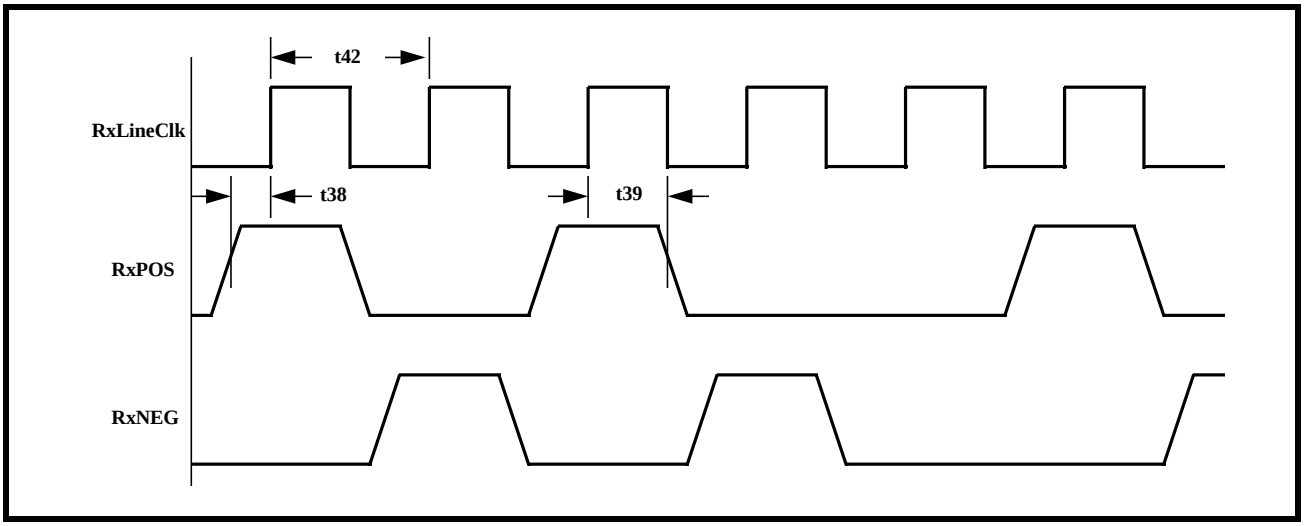
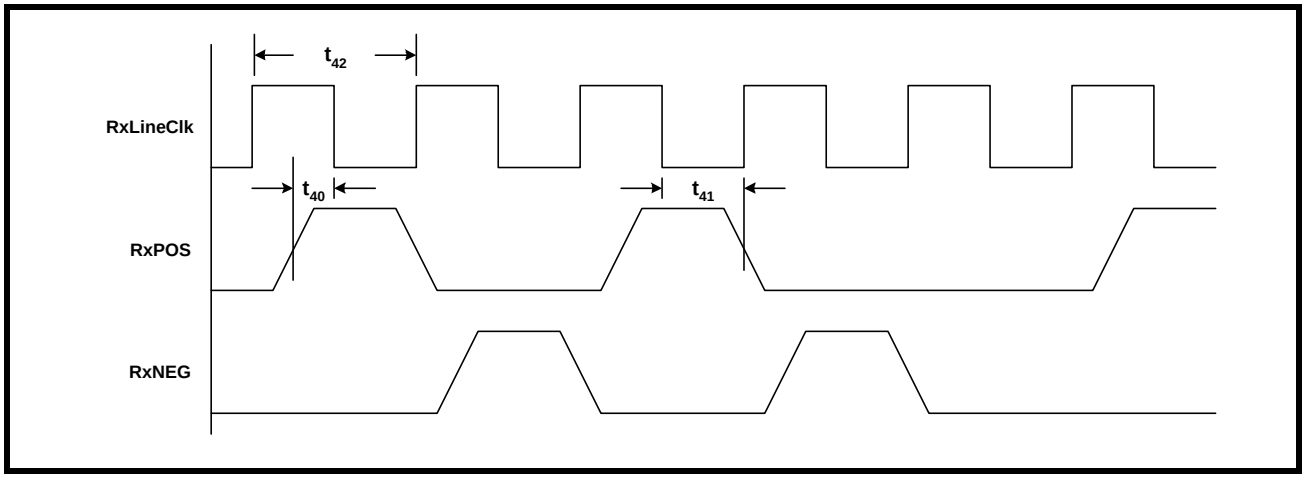


FIGURE 67. WAVEFORM/TIMING RELATIONSHIP BETWEEN RXLINECLK, RXPOS AND RXNEG - WHEN RXPOS AND RXNEG ARE TO BE SAMPLED ON THE FALLING EDGE OF RXLINECLK



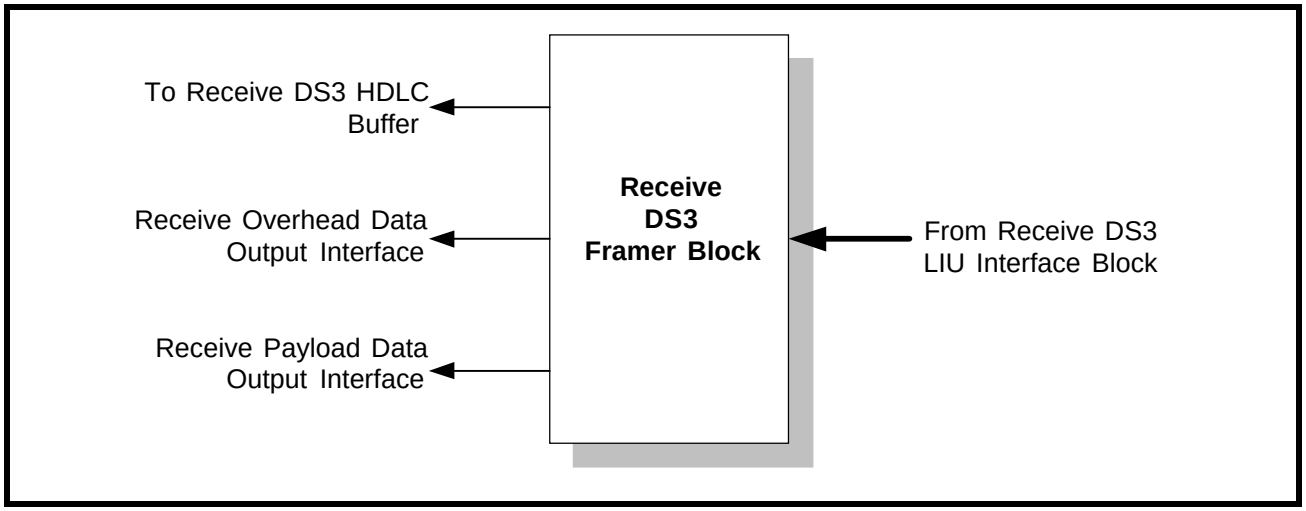
4.3.2 The Receive DS3 Framer Block

The Receive DS3 Framer block accepts decoded DS3 data from the Receive DS3 LIU Interface block, and routes data to the following destinations.

- The Receive Payload Data Output Interface Block
- The Receive Overhead Data Output Interface Block.
- The Receive DS3 HDLC Controller Block

Figure 68 presents a simple illustration of the Receive DS3 Framer block along with the associated paths to the other functional blocks within the Framer chip.

FIGURE 68. THE RECEIVE DS3 FRAMER BLOCK AND THE ASSOCIATED PATHS TO OTHER FUNCTIONAL BLOCKS



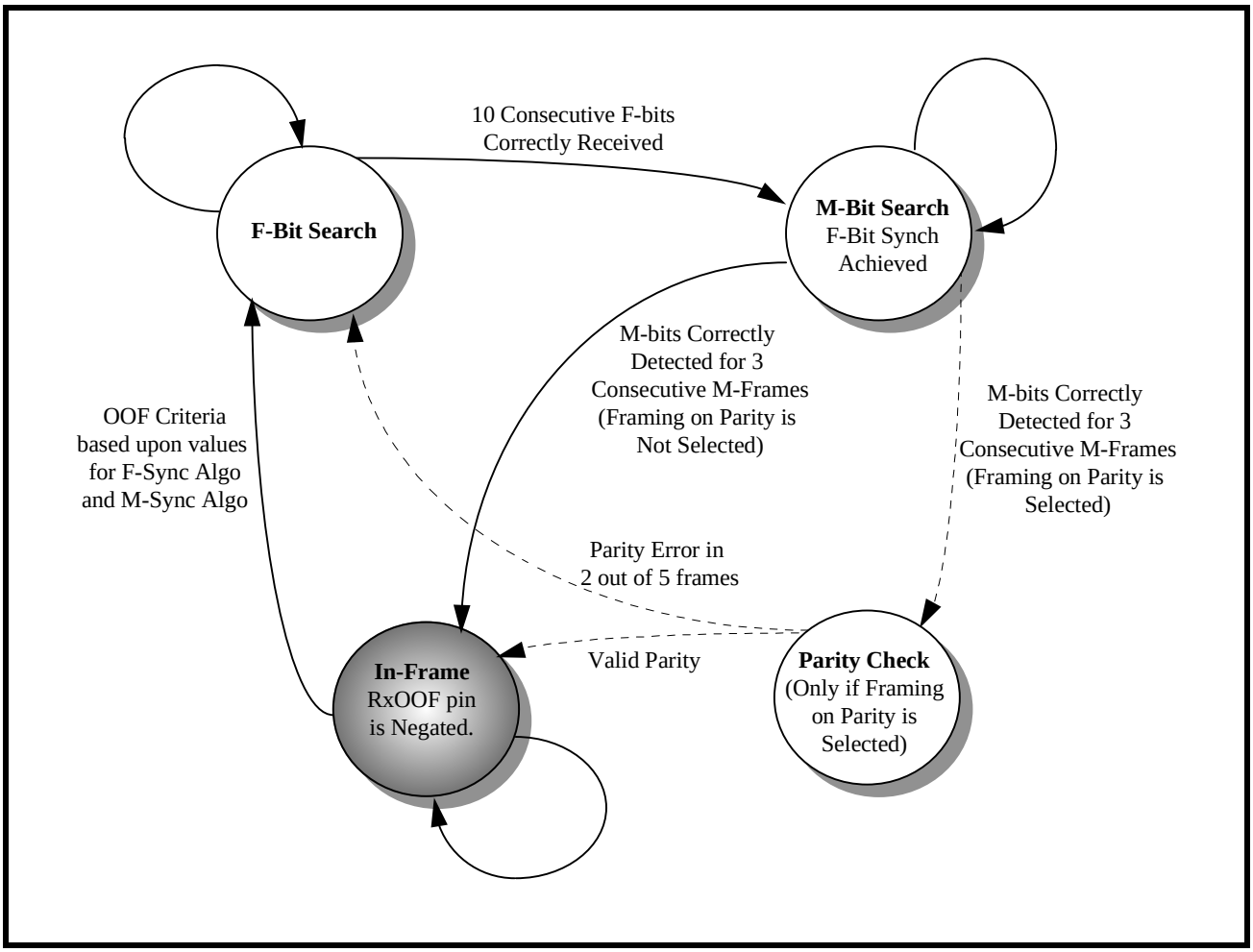
Once the B3ZS (or AMI) encoded data has been decoded into a binary data-stream, the Receive DS3 Framer block will use portions of this data-stream in order to synchronize itself to the remote terminal equipment. At any given time, the Receive DS3 Framer block will be operating in one of two modes.

- **The Frame Acquisition Mode:** In this mode, the Receive DS3 Framer block is trying to acquire synchronization with the incoming DS3 frames, or

- **The Frame Maintenance Mode:** In this mode, the Receive DS3 Framer block is trying to maintain frame synchronization with the incoming DS3 Frames.

Figure 69 presents a State Machine diagram that depicts the Receive DS3 Framer block's DS3 Frame Acquisition/Maintenance Algorithm.

FIGURE 69. THE STATE MACHINE DIAGRAM FOR THE RECEIVE DS3 FRAMER BLOCK'S FRAME ACQUISITION/MAINTENANCE ALGORITHM



4.3.2.1 *Frame Acquisition Mode Operation*

The Receive DS3 Framer block will be performing Frame Acquisition operation while it is operating in any of the following states (per the DS3 Frame Acquisition/Maintenance algorithm State Machine diagram, as depicted in Figure 69.)

- The F-bit Search state
- The M-bit Search state
- The P-Bit Check state (optional)

Once the Receive DS3 Framer block enters the In-Frame state (per Figure 69), then it will begin Frame Maintenance operation.

When the Receive DS3 Framer block is in the frame-acquisition mode, it will begin to look for valid DS3 frames by first searching for the F-bits in the incoming DS3 data stream. At this initial point the Receive DS3 Framer block will be operating in the F-Bit Search state within the DS3 Frame Acquisition/Maintenance algorithm state machine diagram (see Figure 69). Each DS3 F-frame consists of four (4) F-bits that occur in a repeating 1001

pattern. The Receive DS3 Framer block will attempt to locate this F-bit pattern by performing five (5) different searches in parallel. The F-bit search has been declared successful if at least 10 consecutive F-bits are detected. After the F-bit match has been declared, the Receive DS3 Framer block will then transition into the M-Bit Search state within the DS3 Frame Acquisition/Maintenance algorithm (per Figure 69). When the Receive DS3 Framer block reaches this state, it will begin searching for valid M-bits. Each DS3 M-frame consists of three (3) M-bits that occur in a repeating 010 pattern. The M-bit search is declared successful if three consecutive M-frames (or 21 F-frames) are detected correctly. Once this occurs an M-frame lock is declared, and the Receive DS3 Framer block will then transition to the In-Frame state. At this point, the Receive DS3 Framer block will declare itself in the In-Frame condition, and will begin Frame Maintenance operations. The Receive DS3 Framer block will then indicate that it has transitioned from the OOF condition into the In-Frame condition by doing the following.

- Generate a Change in OOF Condition interrupt to the local µP.
- Negate the RxOOF output pin (e.g., toggle it "Low").
- Negate the RxOOF bit-field (Bit 4) within the Receive DS3 Configuration and Status Register.

The Receive DS3 Framer can be configured to operate such that 'valid parity' (P-bits) must also be detected before the Receive DS3 Framer can declare itself In Frame. This configuration is set by writing the appropriate data to the Rx DS3 Configuration and Status Register, as depicted below.

Rx DS3 Configuration and Status Register, (Address = 0x10)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit2	Bit 1	Bit 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Table 34 relates the contents of this bit field to the framing acquisition criteria.

Table 34: The Relationship between the contents of Bit 2 (Framing on Parity) within the Rx DS3 Configuration and Status Register, and the resulting Framing Acquisition Criteria

Framing on Parity (Bit 2)	Framing Acquisition Criteria
0	The In-frame is declared after F-bit synchronization (10 F-bit matches) followed by M-bit synchronization (M-bit matches for 3 DS3 M-frames)
1	The In-frame condition is declared after F-bit synchronization, followed by M-bit synchronization, with valid parity over the frames. Also, the occurrence of parity errors in 2 or more out of 5 frames starts a frame search

Once the Receive DS3 Framer block is operating in the In-Frame condition, normal data recovery and processing of the DS3 data stream begins. The maximum average reframing time is less than 1.5 ms.

4.3.2.2 *Frame Maintenance Mode Operation*

When the Receive DS3 Framer block is operating in the In-Frame state (per Figure 69), it will then begin to perform Frame Maintenance operations, where it will continue to verify that the F- and M-bits are present, at their proper locations. While the Receive DS3 Framer block is operating in the Frame Maintenance mode, it will declare an Out-of-Frame (OOF) condition if 3 or 6 F-bits (depending upon user selection) out of 16 consecutive F-bits are in error. This selection for the OOF Declaration criteria is made by writing the appropriate value to bit 1 (F-Sync Algo) of the Rx DS3 Configuration and Status Register, as depicted below.

Rx DS3 Configuration and Status Register, (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Table 35 relates the contents of this bit-field to the OOF Declaration criteria

TABLE 35: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 1 (F-SYNC ALGO) WITHIN THE RX DS3 CONFIGURATION AND STATUS REGISTER, AND THE RESULTING F-BIT OOF DECLARATION CRITERIA USED BY THE RECEIVE DS3 FRAMER BLOCK

F-SYNC ALGO (BIT 1)	OOF DECLARATION CRITERIA
0	OOF is declared when 6 out of 16 consecutive F-bits are in error.
1	OOF is declared when 3 out of 16 consecutive F-bits are in error.

NOTE: *Once the Receive DS3 Framer block has declared an OOF condition, it will transition back to the F-Bit Search state within the DS3 Frame Acquisition/Maintenance algorithm (per Figure 69).*

In addition to selecting an OOF Declaration criteria for the F-bits, the following options exist for configuring the OOF Declaration criteria based upon M-bits.

1. M-bit errors do not cause a OOF Declaration, or
2. OOF will be declared if 3 out of 4 consecutive M-bits are in error.

The selection between these two options is made by writing the appropriate value to Bit 0 (M-Sync Algo) within the Receive DS3 Configuration and Status Register, as depicted below.

Rx DS3 Configuration and Status Register, (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Table 36 relates the contents of this Bit Field to the M-Bit Error criteria for Declaration of OOF.

TABLE 36: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 0 (M-SYNC ALGO) WITHIN THE RX DS3 CONFIGURATION AND STATUS REGISTER, AND THE RESULTING M-BIT OOF DECLARATION CRITERIA USED BY THE RECEIVE DS3 FRAMER BLOCK

MSYNC ALGO (BIT 0)	OOF DECLARATION CRITERIA
0	M-Bit Errors do not result in the declaration of OOF
1	OOF is declared when 3 out of 4 M-bits are in error.

The Framing on Parity Criteria for OOF Declaration

Finally, the Framer IC offers the Framing on Parity option, which also effects the OOF Declaration criteria. As was mentioned earlier, the Framer IC allows the user to configure the Receive DS3 Framer block to detect

'valid-parity' before declaring itself In-Frame. This same selection also configures the Receive DS3 Framer block to also declare an OOF Condition if a P-bit error is detected in 2 of the last 5 M-frames.

Whenever the Receive DS3 Framer block declares OOF after being in the In-Frame State the following will happen.

- The Receive DS3 Framer will assert the RxOOF output pin (e.g., toggles it "High").
- Bit 4 (RxOOF) within the Rx DS3 Configuration and Status Register will be set to "1" as depicted below.

Rx DS3 Configuration and Status Register, (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
X	X	X	X	X	X	X	X

- The Receive DS3 Framer block will also issue a Change in OOF Status interrupt request, anytime there is a change in the OOF status.

4.3.2.3 *Forcing a Reframe via Software Command*

The Framer IC permits the user to force a reframe procedure of the Receive DS3 Framer block via software command. If a "1" is written into Bit 0 of the I/O Control Register, as depicted below, then the Receive DS3 Framer will be forced into the Frame Acquisition Mode, (or more specifically, in the F-Bit Search State per Figure 69). Afterwards, the Receive DS3 Framer block will begin its search for valid F-Bits. The Framer IC will also respond to this command by asserting the RxOOF output pin, and generating a Change in OOF Status interrupt.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	1

4.3.2.4 *Performance Monitoring of the Receive DS3 Framer block*

The user can monitor the number of framing bit errors (M and F bits) that have been detected by the Receive DS3 Framer block. This is accomplished by periodically reading the PMON Framing Bit Error Count Registers (Address = 0x52 and 0x53), as depicted below.

PMON Framing Bit Error Event Count Register - MSB (Address = 0x52)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
F-Bit Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON Framing Bit Error Event Count Register - LSB (Address = 0x53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
F-Bit Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

When the µP/µC reads these registers, it will read in the number of framing bit errors that have been detected since the last read of these two registers. These registers are reset upon read.

4.3.2.5 *DS3 Receive Alarms*

The Receive DS3 Framer block is capable of detecting any of the following alarm conditions.

- LOS (Loss of Signal)
- AIS (Alarm Indication Signal)
- The Idle Pattern.
- FERF (Far-End Receive Failure) of Yellow Alarm condition.
- FEBE (Far-End-Block Error)
- Change in AIC State

The methods by which the Receive DS3 Framer block uses to detect and declare each of these alarm conditions are described below.

4.3.2.5.1 The Loss of Signal (LOS) Alarm

The Receive DS3 Framer block will declare a Loss of Signal (LOS) state when it detects 180 consecutive incoming “0s” via the RxPOS and RxNEG input pins **OR** if the RLOS input pin (of the XRT73L00 DS3 LIU IC) is asserted (e.g., driven "High" and conneted to the ExtLOS pin78, of the Framer IC). The Receive DS3 Framer block will indicate the occurrence of an LOS condition by:

1. Asserting the RxLOS output pin (e.g., toggles it "High").
2. Setting Bit 6 (RxLOS) within the Rx DS3 Configuration and Status Register to 1, as depicted below.

NOTE: *LOS is always declared if the RLOS input is driven “High”. The 180 consecutive “zero” pulse internal LOS criteria can be disabled by setting bit 5 at 0x00 to “0”*

Rx DS3 Configuration and Status Register, (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
0	1	0	1	x	x	x	x

3. The Receive DS3 Framer block will generate a Change in LOS Status interrupt request.

NOTE: *The Receive DS3 Framer will also declare an OOF condition and perform all of the notification procedures as described in* Section 4.3.2.2*.*

4. Force the on-chip Transmit Section to transmit a FERF (Far-End Receive Failure) indicator back out to the remote terminal.

The Receive DS3 Framer block will clear the LOS condition when at least 60 out of 180 consecutive received bits are 1.

NOTE: *The Receive DS3 Framer block will also generate the Change in LOS Condition interrupt, when it clears the LOS Condition.*

The Framer chip allows the user to modify the LOS Declaration criteria such that an LOS condition is declared only if the RLOS input pin (from the XRT73L00 DS3/E3/STS-1 LIU IC) is asserted. In this case, the internally-generated LOS criteria of 180 consecutive “zeros” will be disabled. This can be accomplished by writing a "0" to bit 5 (Internal LOS Enable) of the Framer Operating Mode Register, as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	1	0	X	X	X	X	X

NOTE: *For more information on the RLOS input pin, please see Section 2.1.*

4.3.2.5.2 The Alarm Indication Signal (AIS)

The Receive DS3 Framer block will identify and declare an AIS condition if it detects all of the following conditions in the incoming DS3 Data Stream:

- Valid M-bits, F-bits and P-bits
- All C-bits are zeros.
- X-bits are set to 1
- The Payload portion of the DS3 Frame exhibits a repeating 1010... pattern.

The Receive DS3 Framer block contains, within its circuitry, an Up/Down Counter that supports the assertion and negation of the AIS condition. This counter begins with the value of 0x00 upon power up or reset. The counter is then incremented anytime the Receive DS3 Framer block detects an AIS Type M-frame. This counter is then decremented, or kept at zero value, when the Receive DS3 Framer block detects a non-AIS type M-frame. The Receive DS3 Framer block will declare an AIS Condition if this counter reaches the value of 63 M-frames or greater. Explained another way, the AIS condition is declared if the number of AIS-type M-frames is detected, such that it meets the following conditions:

NAIS - NVALID $\geq$ 63

where:

NAIS = the number of M-frames containing the AIS pattern.

NVALID = the number of M-frames not containing the AIS pattern

If at anytime, the contents of this Up/Down counter exceeds 63 M-frames, then the Receive DS3 Framer block will:

1. Assert the RxAIS output pin by toggling it "High".
2. Set Bit 7 (RxAIS) within the Rx DS3 Configuration and Status Register, to "1" as depicted below.

Rx DS3 Configuration and Status Register, (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
1	X	X	X	X	X	X	X

3. Generate a Change in AIS Status Interrupt Request to the µP/µC.
4. Force the Transmit Section to transmit a FERF indication back to the remote terminal.

The Receive DS3 Framer block will clear the AIS condition when the following expression is true.

NAIS - NVALID $\leq$ 0.

In other words, once the Receive DS3 Framer block has detected a sufficient number of normal (or Non-AIS) M-frames, such that this Up/Down counter reaches zero, then the Receive DS3 Framer block will clear the AIS Condition indicators. The Receive DS3 Framer block will inform the µC/µP of this negation of the AIS Status by generating a Change in AIS Status interrupt.

4.3.2.5.3 The Idle (Condition) Alarm

The Receive DS3 Framer block will identify and declare an Idle Condition if it receives a sufficient number of M-Frames that meets all of the following conditions.

- Valid M-bits, F-bits, and P-bits
- The 3 CP-bits (in F-Frame #3) are zeros.
- The X-bits are set to 1
- The payload portion of the DS3 Frame exhibits a repeating 1100... pattern.

The Receive DS3 Framer block circuitry includes an Up/Down Counter that is used to track the number of M-frames that have been identified as exhibiting the Idle Condition by the Receive DS3 Framer block. The contents of this counter are set to zero upon reset or power up. This counter is then incremented whenever the Receive DS3 Framer block detects an Idle-type M-frame. The counter is decremented, or kept at zero if a non-Idle M-frame is detected. If the Receive DS3 Framer block detects a sufficient number of Idle-type M-frames, such that the counter reaches the number 63, then the Receive DS3 Framer block will declare the Idle Condition. Explained another way, the Receive DS3 Framer block will declare an Idle Condition if the number of Idle-Pattern M-frames is detected such that it meets the following conditions.

NIDLE - NVALID $\geq$ 63,

where:

NIDLE = the number of M-frames containing the Idle Pattern

NVALID = the number of M-frames not exhibit the Idle Pattern

Anytime the contents of this Up/Down Counter reaches the number 63, then the Receive DS3 Framer block will:

1. Set Bit 5 (RxIdle) within the Rx DS3 Configuration and Status Register, to "1" as depicted below.

Rx DS3 Configuration and Status Register, (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
X	X	1	X	X	X	X	X

2. Generate a Change in Idle Status Interrupt Request to the local µP/µC.

The Receive DS3 Framer block will clear the Idle Condition if it has detected a sufficient number of Non-Idle M-frames, such that this Up/Down Counter reaches the value 0.

4.3.2.5.4 The Detection of (FERF) or Yellow Alarm Condition

The Receive DS3 Framer block will identify and declare a Yellow Alarm condition or a Far-End Receive Failure (FERF) condition, if it starts to receive DS3 frames with both of its X-bits set to 0.

When the Receive DS3 Framer block detects a FERF condition in the incoming DS3 frames, then it will then do the following.

1. It will assert the RxFERF (bit-field 4) within the Rx DS3 Status Register, as depicted below.

Rx DS3 Status Register (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used			Rx FERF	RxAIC	RxFEBE [2]	RxFEBE [1]	RxFEBE [0]
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	1	X	X	X	X

This bit-field will remain asserted for the duration that the Yellow Alarm condition exists.

2. The Receive DS3 Framer block will also generate a Change in FERF Status interrupt to the µP/µC. Consequently, the Receive DS3 Framer block will also assert the FERF Interrupt Status bit, within the Rx DS3 Interrupt Status Register, as depicted below.

Rx DS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	IDLE Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	X	X	X	1	X	X	X

The Receive DS3 Framer block will clear the FERF condition, when it starts to receive Receive DS3 Frames that have its X bits set to 1.

NOTE: *The FERF indicator is frequently referred to as the Yellow Alarm.*

4.3.2.5.5 The Detection of the FEBE Events

As described in Section 4.2.4.2.1.9, a given Terminal Equipment will set the three FEBE (Far-End Block Error) bit-fields to the value [1, 1, 1] (e.g., all of the FEBE bits are set to “1”) within the outbound DS3 frames if, all of the following conditions are true about the incoming DS3 line signal.

- The Receive Circuitry (within the Terminal Equipment) detects no P-Bit Errors.
- The Receive Circuitry (within the Terminal Equipment) detects no CP-Bit Errors.

If the Receive Section of the Terminal Equipment detects any P or CP bit errors, then the Transmit Section of the Terminal Equipment will set the three FEBE bits (within the outbound DS3 data stream) to a value other than [1, 1, 1].

How does the Receive DS3 Framer block (within the XRT72L50) respond when it receives a DS3 frame with all three (3) of its FEBE bit-fields set to “1”?

As mentioned above, the Terminal Equipment will transmit DS3 frames, with the FEBE bits set to [1, 1, 1], during un-erred conditions. Hence, if the Receive DS3 Framer block (within the XRT72L50 Framer IC) receives DS3 frames with the FEBE bits set to [1, 1, 1] it will interpret this event as an un-erred event, and will continue normal operation.

However, if the Receive DS3 Framer block receives a DS3 frame with the FEBE bits set to a value other than [1, 1, 1], then it will increment the PMON FEBE Event Count Registers (which are located at address locations 0x58 and 0x59 within the Framer Address space).

4.3.2.5.6 Detection of Change in the AIC State

Section 4.1 indicates that the AIC (Application Identification Channel) bit-field is the third overhead bit, within F-Frame # 1. This particular bit-field is set to “1” for the C-Bit Parity Framing Format, and is set to “0” for the M13 Framing Format.

Hence, a given Terminal Equipment receiving a DS3 data stream can identify the framing format of this DS3 data stream, by reading the value fo the AIC bit-field. The Receive DS3 Framer block permits the user's Microcontroller/MIcroprocessor to determine the state of the AIC bit-field (within the incoming DS3 data stream) by writing the value of the AIC bit-field, within the most recently received DS3 frame, into bit 3 (RxAIC) within the Rx DS3 Status Register (Address = 0x11), as illustrated below.

RxDS3 Status Register (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			RxFERF	RxAIC	RxFEBE[2:0]		
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

The Receive DS3 Framer block will also generate an interrupt if it detects a change of state in the AIC bit-field (within the incoming DS3 data stream). If this occurs, then the Receive DS3 Framer block will set Bit 2 (AIC Interrupt Status) within the Rx DS3 Interrupt Stauts Register (Address = 0x13) to "1" as illustrated below.

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

4.3.2.6 *Performance Monitoring of the DS3 Transport Medium*

The DS3 Frame consists of some overhead bits that are used to support performance monitoring of the DS3 Transmission Link. These bits are the P-Bits and the CP-Bits.

4.3.2.6.1 P-Bit Checking/Options

The remote Transmit DS3 Framer will compute the even parity of the payload portion of an outbound DS3 Frame and will place the resulting parity bit value in the 2 P-bit-fields within the very next outbound DS3 Frame. The value of these two bits fields is expected to be the identical.

The Receive DS3 Framer block, while receiving each of these DS3 Frames (from the remote Transmit DS3 Framer), will compute the even-parity of the payload portion of the frame. The Receive DS3 Framer block will then compare this locally computed parity value to that of the P-bit fields within the very next DS3 Frame. If the Receive DS3 Framer block detects a parity error, then two things will happen:

1. The Receive DS3 Framer block will inform the µP/µC of this occurrence by generating a Detection of P-Bit Error interrupt,
2. The Receive DS3 Framer block will alter the value of the FEBE bits, (to a pattern other than 111) that the Near-End Transmit DS3 Framer will be transmitting back to the remote Terminal.
3. The XRT72L50 Framer IC will increment the PMON Parity Error Event Count Registers (Address = 0x54 and 0x55) for each detected parity error, in the incoming DS3 data stream. The bit-format of these two registers follows.

PMON Parity Error Event Count Register - MSB (Address = 0x54)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Parity Error Count - High Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

PMON Parity Error Event Count Register - LSB (Address = 0x55)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Parity Error Count - Low Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

When the µP reads these registers, it will read in the number of parity-bit errors that have been detected by the Receive DS3 Framer block, since the last time these registers were read. These registers are reset upon read.

NOTE: *When the Framing with Parity option is selected, the Receive DS3 Framer block will declare an OOF condition if P-bit errors were detected in two out of 5 consecutive DS3 M-frames.*

4.3.2.6.2 CP-Bit Checking/Options

CP-bits are very similar to P-bits except for the following.

1. CP-bits are used to permit performance monitoring over an entire DS3 path (e.g., from the source terminal) through any number of mid-network terminals to the sink terminal).
2. P-bits are used to permit performance monitoring of a DS3 data stream, as it is transmitted from one terminal to an adjacent terminal.

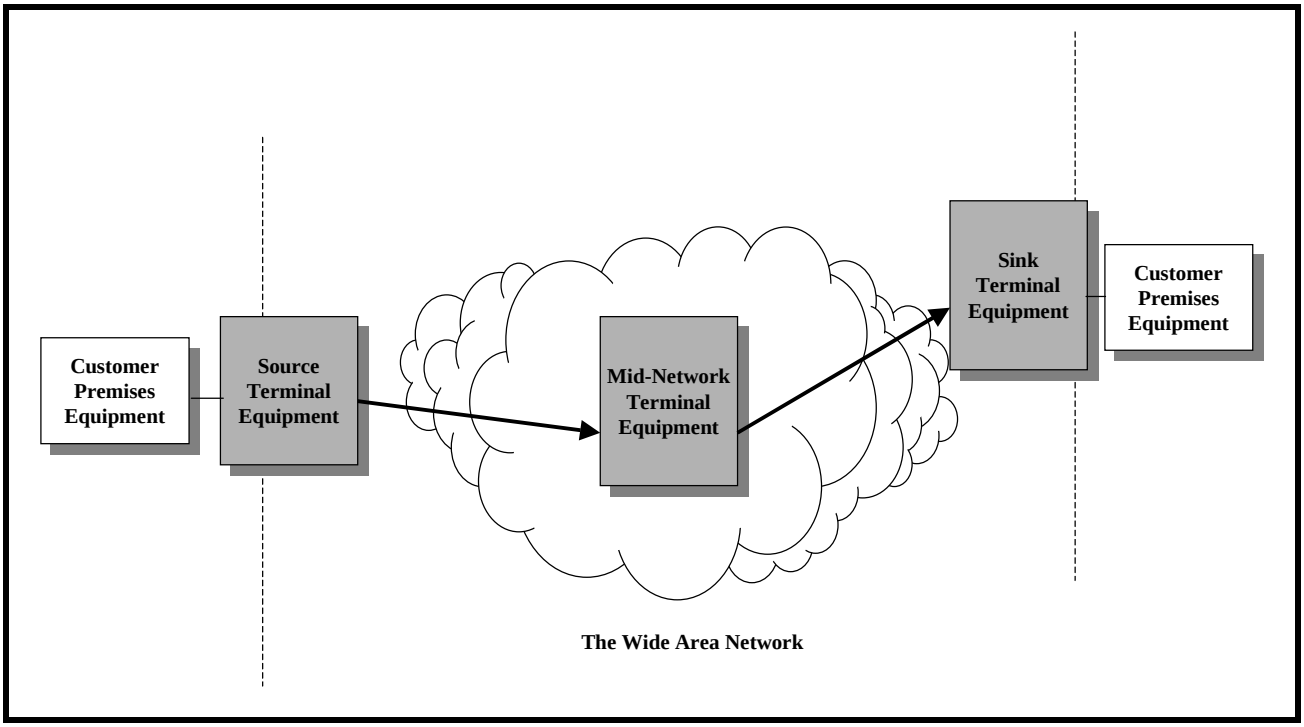
How CP-Bits are Processed

The following section describes how the CP-bits are processed at three locations.

- The Source Terminal Equipment
- The Mid-Network Terminal Equipment
- The Sink Terminal Equipment

Figure 70 presents a simple illustration of the locations of these three types of Terminal Equipment, within the Wide-Area Network.

FIGURE 70. A SIMPLE ILLUSTRATION OF THE LOCATIONS OF THE SOURCE, MID-NETWORK AND SINK TERMINAL EQUIPMENT (FOR CP-BIT PROCESSING)



NOTE: *The use of the terms Source and Sink Terminal Equipment are used to simplify this discussion of CP-Bit Processing. In reality, the Source Terminal Equipment (in Figure 70) will also function as the Sink Terminal Equipment (for DS3 traffic traveling in the opposite direction). Likewise, the Sink Terminal Equipment will also function as the Source Terminal Equipment.*

Processing at the Source Terminal Equipment

The Source Terminal Equipment (located at one edge of the wide-area network) will typically receive its DS3 payload data from some Customer Premise Equipment (CPE). As the Source Terminal Equipment receives this data from the CPE, it will compute the even-parity value over all the payload bits within a given outbound DS3 frame. The Terminal Equipment will then insert this even parity value into both of the P-bit fields and both of the CP-bits fields, within the very next outbound DS3 frame.

Hence, both the P-bit values and CP-bit values will originate at the Source Terminal Equipment.

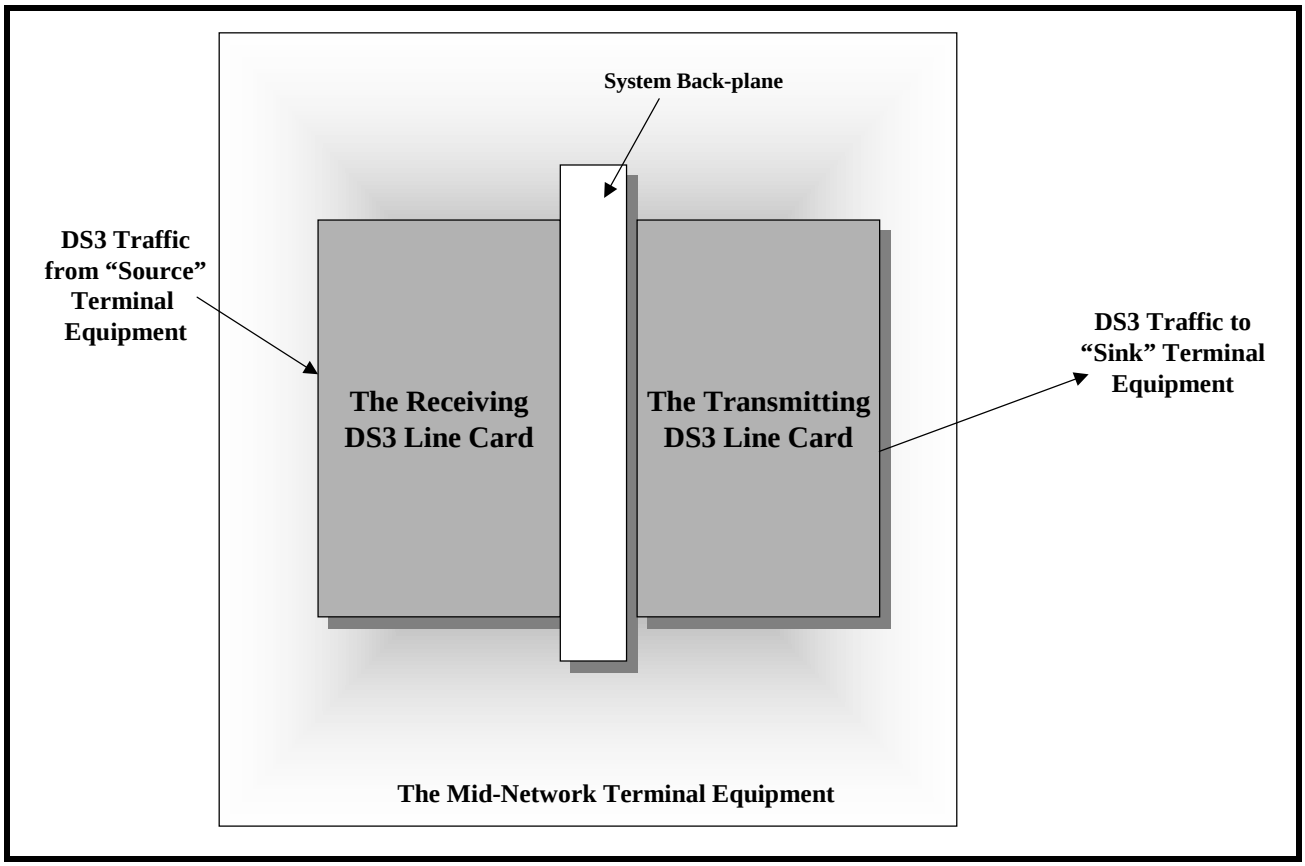
Processing at the Mid-Network Terminal Equipment

The Mid-Network Terminal Equipment has the task of doing the following.

- Receiving a DS3 data stream, via the Receive WAN Interface Line Card.
- Transmitting this same DS3 data stream (out to another Remote Terminal Equipment) via the Transmit WAN Interface Line Card.

Figure 71 presents an illustration of the basic architecture of the Mid-Network Terminal Equipment.

FIGURE 71. ILLUSTRATION OF THE PRESUMED CONFIGURATION OF THE MID-NETWORK TERMINAL EQUIPMENT



Operation of the Receive WAN Interface Line Card

The Receive WAN Interface line card receives a DS3 data stream from some remote Terminal Equipment. As the Receive WAN Interface card does this, it will also do the following:

1. Compute and verify the P-Bits of each inbound DS3 frame.
2. Compute and verify the CP-Bits of each inbound DS3 frame.
3. Output both the payload and overhead bits to the system back-plane.

Operation of the Transmit WAN Interface Line Card

The Transmit WAN Interface Line Card receives the outbound DS3 data stream from the system back-plane. As the Transmit WAN Interface Line Card receives this data it will also do the following.

1. Extract out the CP-bit values, from the Receive WAN Interface line card (via the system back-plane) and insert these values into the CP-bit fields, within the outbound DS3 data stream, via the Transmit Overhead Data Input Interface block of the XRT72L50 Framer IC.
2. Compute the even-parity over all the payload bits, within a given outbound DS3 frame, and insert this value into the P bits within the very next outbound DS3 frame.
3. Transmit this resulting DS3 data stream to the remote terminal equipment.

Processing at the Sink Terminal

The Sink Terminal Equipment (located at the opposite edge of the wide-area-network, from the Source Terminal Equipment) will receive and terminate this DS3 data stream. As the Sink Terminal Equipment receives this DS3 data stream it will also do the following.

1. Compute and verify the P bits within each inbound DS3 frame.
2. Compute and verify the CP bits within each inbound DS3 frame.

4.3.3 The Receive HDLC Controller Block

The Receive DS3 HDLC Controller block can be used to receive either bit-oriented signaling (BOS) or message-oriented signaling (MOS) type data link messages. The Receive DS3 HDLC Controller block can also be configured to receive both types of message from the remote terminal equipment.

Both BOS and MOS types of HDLC message processing are discussed in detail below.

4.3.3.1 *Bit-Oriented Signaling (or FEAC) Processing via the Receive DS3 HDLC Controller.*

The Receive DS3 HDLC Controller block consists of two major sub-blocks

- The Receive FEAC Processor
- The LAPD Receiver

This section describes how to operate the Receive FEAC Processor.

If the Receive DS3 Framer block is operating in the C-bit Parity Framing format, then the FEAC bit-field within the DS3 Frame can be used to receive FEAC (Far End Alarm and Control) messages (See Figure 72). Each FEAC code word is actually six bits in length. However, this six bit FEAC Code word is encapsulated with 10 framing bits to form a 16 bit message of the form:

	FEAC CODE WORD						FRAMING								
0	d5	d4	d3	d2	d1	d0	0	1	1	1	1	1	1	1	1

Where, [d5, d4, d3, d2, d1, d0] is the FEAC Code word. The rightmost bit of the 16-bit data structure (e.g., a 1) will be received first. Since each DS3 Frame contains only 1 FEAC bit-field, 16 DS3 Frames are required to transmit the 16 bit FEAC code message. The six bits, labeled d5 through d0 can represent 64 distinct messages, of which 43 have been defined in the standards.

The Receive FEAC Processor frames and validates the incoming FEAC data from the remote Transmit FEAC Processor via the received FEAC channel. Additionally, the Receive FEAC Processor will write the Received FEAC code words into an 8 bit Rx-FEAC register. Framing is performed by looking for two 0s spaced 6 bits apart preceded by 8 1s. The Receive DS3 HDLC Controller contains two registers that support FEAC Message Reception.

- Rx DS3 FEAC Register (Address = 0x16)
- Rx DS3 FEAC Interrupt Enable/Status Register (Address = 0x17)

The Receive FEAC Processor generates an interrupt upon validation and removal of the incoming FEAC Code words.

Operation of the Receive DS3 FEAC Processor

The Receive FEAC Processor will validate or remove FEAC code words that it receives from the remote Transmit FEAC Processor. The FEAC Code Validation and Removal functions are described below.

FEAC Code Validation

When the remote terminal equipment wishes to send a FEAC message to the Local Receive FEAC Processor, it (the remote terminal equipment) will transmit this 16 bit message, repeatedly for a total of 10 times. The Receive FEAC Processor will frame to this incoming FEAC Code Message, and will attempt to validate this message. Once the Receive FEAC Processor has received the same FEAC code word in at least 8 out of the last 10 received codes, it will validate this code word by writing this 6 bit code word into the Receive DS3 FEAC Register. The Receive FEAC Processor will then inform the µC/µP of this Receive FEAC validation event by generating a Rx FEAC Valid interrupt and asserting the FEAC Valid and the RxFEAC Valid Interrupt Status Bits in the Rx DS3 Interrupt Enable/Status Register, as depicted below. The Bit Format of the Rx DS3 FEAC Register is presented below.

Rx DS3 FEAC Interrupt Enable/Status Register (Address = 0x17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	Not Used	Not Used	FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
X	X	X	1	X	0	1	1

The bit-format of the Rx DS3 FEAC register is presented below. It is important to note that the last validated FEAC code word will be written into the shaded bit-fields below.

Rx DS3 FEAC Register (Address = 0x16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	RxFEAC [5]	RxFEAC [4]	RxFEAC [3]	RxFEAC [2]	RxFEAC [1]	RxFEAC [0]	Not Used
RO	RO	RO	RO	RO	RO	RO	RO
0	d5	d4	d3	d2	d1	d0	0

The purpose of generating an interrupt to the µP, upon FEAC Code Word Validation is to inform the local µP that the Framer has a newly received FEAC message that needs to be read. The local µP would read-in this FEAC code word from the Rx DS3 FEAC Register (Address = 0x16).

FEAC Code Removal

After the 10th transmission of a given FEAC code word, the remote terminal equipment may proceed to transmit a different FEAC code word. When the Receive FEAC processor detects this occurrence, it must Remove the FEAC codeword that is presently residing in the Rx DS3 FEAC Register. The Receive FEAC Processor will remove the existing FEAC code word when it detects that 3 (or more) out of the last 10 received FEAC codes are different from the latest validated FEAC code word. The Receive FEAC Processor will inform the local µP/µC of this removal event by generating a Rx FEAC Removal interrupt, and asserting the RxFEAC Remove Interrupt Status bit in the Rx DS3 Interrupt Enable/Status Register, as depicted below.

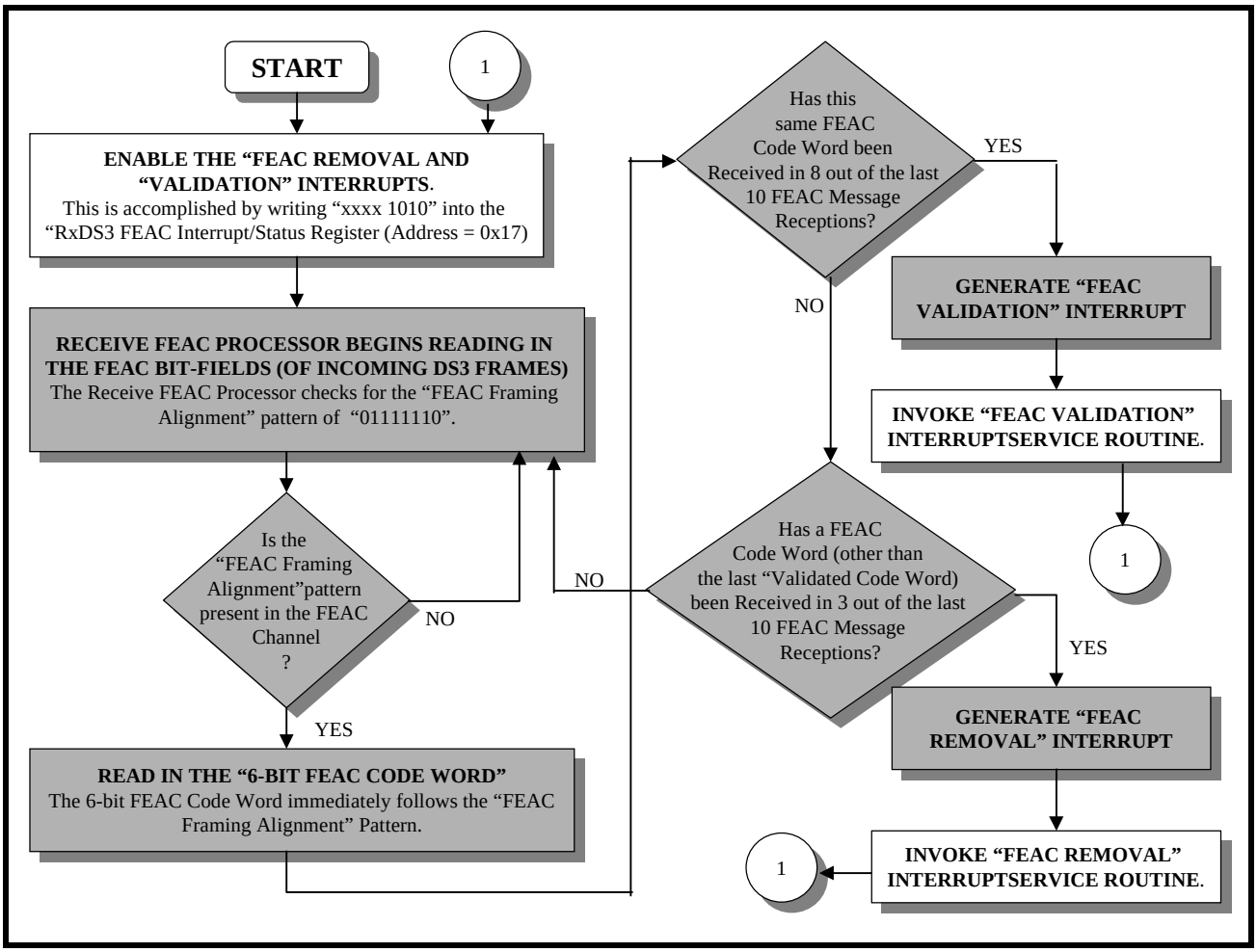
Rx DS3 FEAC Interrupt Enable/Status Register (Address = 0x17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	Not Used	Not Used	FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
X	X	X	0	1	1	X	0

Additionally, the Receive FEAC processor will also denote the removal event by setting the FEAC Valid bit-field (Bit 4), within the Rx DS3 FEAC Interrupt Enable/Status Register to 0, as depicted above.

The description of Bits 0 through 3 within this register, all support Interrupt Processing, and will therefore be presented in Section 4.3.6. Figure 72 presents a flow diagram depicting how the Receive FEAC Processor functions.

FIGURE 72. FLOW DIAGRAM DEPICTING HOW THE RECEIVE FEAC PROCESSOR FUNCTIONS



NOTES:

1. *The white (e.g., unshaded) boxes reflect tasks that the user's system must perform in order to configure the Receive FEAC Processor to receive FEAC messages.*
2. *A brief description of the steps that must exist within the FEAC Validation and FEAC Removal Interrupt Service Routines exists in* Section 4.3.3

4.3.3.2 *The Message Oriented Signaling (e.g., LAP-D) Processing via the Receive DS3 HDLC Controller block*

The LAPD Receiver (within the Receive DS3 HDLC Controller block) allows the user to receive PMDL messages from the remote terminal equipment, via the inbound DS3 frames. In this case, the inbound message bits will be carried by the 3 DL bit-fields of F-Frame 5, within each DS3 M-Frame. The remote LAPD Transmitter will transmit a LAPD Message to the Near-End Receiver via these three bits within each DS3 Frame. The LAPD Receiver will receive and store the information portion of the received LAPD frame into the Receive LAPD Message Buffer, which is located at addresses: 0xDE through 0x135 within the on-chip RAM. The LAPD Receiver has the following responsibilities.

- Framing to the incoming LAPD Messages
- Filtering out stuffed "Zeros" (Between the two flag sequence bytes, 0x7E)
- Storing the Frame Message into the Receive LAPD Message Buffer
- Perform Frame Check Sequence (FCS) Verification
- Provide status indicators for

End of Message (EOM)

Flag Sequence Byte detected

Abort Sequence detected

Message Type

C/R Type

The occurrence of FCS Errors

The LAPD receiver's actions are facilitated via the following two registers.

- Rx DS3 LAPD Control Register
- Rx DS3 LAPD Status Register

Operation of the LAPD Receiver

The LAPD Receiver, once enabled, will begin searching for the boundaries of the incoming LAPD message. The LAPD Message Frame boundaries are delineated via the Flag Sequence octets (0x7E), as depicted in Figure 73.

FIGURE 73. LAPD MESSAGE FRAME FORMAT

Flag Sequence (8 bits)		
SAPI (6-bits)	C/R	EA
TEI (7 bits)		EA
Control (8-bits)		
76 or 82 Bytes of Information (Payload)		
FCS - MSB		
FCS - LSB		
Flag Sequence (8-bits)		

Where: Flag Sequence = 0x7E

SAPI + CR + EA = 0x3C or 0x3E

TEI + EA = 0x01

Control = 0x03

The 16 bit FCS is calculated using CRC-16, x16 + x12 + x5 + 1

The first byte of the information field indicates the type and size of the message being transferred. The value of this information or payload field and the corresponding message type/size follow:

CL Path Identification = 0x38 (76 bytes)

IDLE Signal Identification = 0x34 (76 bytes)

Test Signal Identification = 0x32 (76 bytes)

ITU-T Path Identification = 0x3F (82 bytes)

The LAPD Receiver must be enabled before it can begin receiving any LAPD messages. The LAPD Receiver can be enabled by writing a "1" into Bit 2 (RxLAPD Enable) within the Rx DS3 LAPD Control Register. The bit format of this register is depicted below.

Rx DS3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	Not Used	Not Used	Not Used	Not Used	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	1	X	X

Once the LAPD Receiver has been enabled, it will begin searching for the Flag Sequence octets (0x7E), in the DL bit-fields, within the incoming DS3 frames. When the LAPD Receiver finds the flag sequence byte, it will assert the Flag Present bit (Bit 0) within the Rx DS3 LAPD Status Register, as depicted below.

Rx DS3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	RxAbort	RxLAPD Type[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	X	X	X	1

The receipt of the Flag Sequence octet can mean one of two things.

1. The Flag Sequence byte marks the beginning or end of an incoming LAPD Message.
2. The received Flag Sequence octet could be just one of many Flag Sequence octets that are transmitted via the DS3 Transport Medium, during idle periods between the transmission of LAPD Messages.

The LAPD Receiver will clear the Flag Present bit as soon as it has received an octet that is something other than the Flag Sequence octet. At this point, the LAPD Receiver should be receiving either octet #2 of the incoming LAPD Message, or an Abort Sequence (e.g., a string of seven or more consecutive 1s). If this next set of data is an abort sequence, then the LAPD Receiver will assert the RxAbort bit (Bit 6) within the Rx DS3 LAPD Status Register. However, if this next octet is Octet #2 of an incoming LAPD Message, then the Rx DS3 LAPD Status Register will start de-stuffing “zeros” after any consecutive 5 “Ones” and will begin to present some additional status information on this incoming message. Each of these indicators is presented below in sequential order.

Bit 3 - RxCR Type - C/R (Command/Response) Type

This bit-field reflects the contents of the C/R bit-field within octet #2 of the LAPD Frame Header. When this bit is "0" it means that this message is originating from a customer installation. When this bit is "1" it means that this message is originating from a network terminal.

Bit 4,5 - RxLAPD Type[1, 0] - LAPD Message Type

The combination of these two bit fields indicate the Message Type and the Message Size of the incoming LAPD Message frame. Table 37 relates the values of Bits 4 and 5 to the Incoming LAPD Message Type/Size.

TABLE 37: THE RELATIONSHIP BETWEEN RXLAPDTYPE[1:0] AND THE RESULTING LAPD MESSAGE TYPE AND SIZE

RXLAPD TYPE[1, 0]	MESSAGE TYPE	MESSAGE SIZE
00	CL Path Identification	76 bytes
01	Idle Signal Identification	76 bytes

TABLE 37: THE RELATIONSHIP BETWEEN RXLAPDTYPE[1:0] AND THE RESULTING LAPD MESSAGE TYPE AND SIZE

RXLAPD TYPE[1, 0]	MESSAGE TYPE	MESSAGE SIZE
10	Test Signal Identification	76 bytes
11	TU-T Path Identification	82 bytes

NOTE: The Message Size pertains to the size of the Information portion of the LAPD Message Frame (as presented in Figure 73).

Bit 3 - Flag Present

The LAPD Receiver should receive another Flag Sequence octet, which marks the End of the Message. Therefore, this bit field should be asserted once again.

Bit 1 - EndOfMessage - End of LAPD Message Frame

Upon receiving a valid header, the EOM bit will be set “Low” (if “High” from a previous valid LAPD message reception).

Upon receipt of the closing Flag Sequence octet, this bit-field should be asserted. The assertion of this bit-field indicates that a LAPD Message Frame has been completely received. Additionally, if this newly received LAPD Message is different from the previous message, then the LAPD Receiver will inform the µC/µP of the EndOfMessage event by generating an interrupt.

Bit 2 - RxFCSErr - Frame Check Sequence Error Indicator

The LAPD Receiver will take the incoming (“Zero” de-stuffed) LAPD Message and compute its own version of the Frame Check Sequence (FCS) word. Afterwards, the LAPD Receiver will compare its computed value with that it has received from the remote LAPD Transmitter. If these two values match, then the LAPD Receiver will presume that the LAPD Message has been properly received and the contents of the Received LAPD Message (payload portion) will be retained at locations 0xDE through 0x135 in on-chip RAM. The LAPD Receiver will indicate an error-free reception of the LAPD Message by keeping this bit field negated (Bit 2 = 0). However, if these two FCS values do not match, then the received LAPD Message is corrupted and the user is advised not to process this erroneous information. The LAPD Receiver will indicate an erred receipt of this message by setting this bit-field to 1.

NOTE: The Receive DS3 HDLC Controller block will not generate an interrupt to the µP due to the detection of an FCS error. Therefore, the user is advised to validate each and every received LAPD message by checking this bit-field prior to processing the LAPD message.

Removal of Stuff Bits from the Payload Portion of the incoming LAPD Message

While the LAPD Receiver is receiving a LAPD Message, it has the responsibility of removing all of the "0" stuff bits from the Payload Portion of the incoming LAPD Message Frame. Recall that the text in Section 4.2.3.2 indicated that the LAPD Transmitter (at the remote terminal) will insert a "0" immediately following a string of 5 consecutive “1s” within the payload portion of the LAPD Message frame. The LAPD Transmitter performs this bit-stuffing procedure in order to prevent the user data from mimicking the Flag Sequence octet (0x7E) or the ABORT sequence. Therefore, in order to recover the user data to its original content (prior to the bit-stuffing), the LAPD Receiver will remove the "0" that immediately follows a string of 5 consecutive 1s.

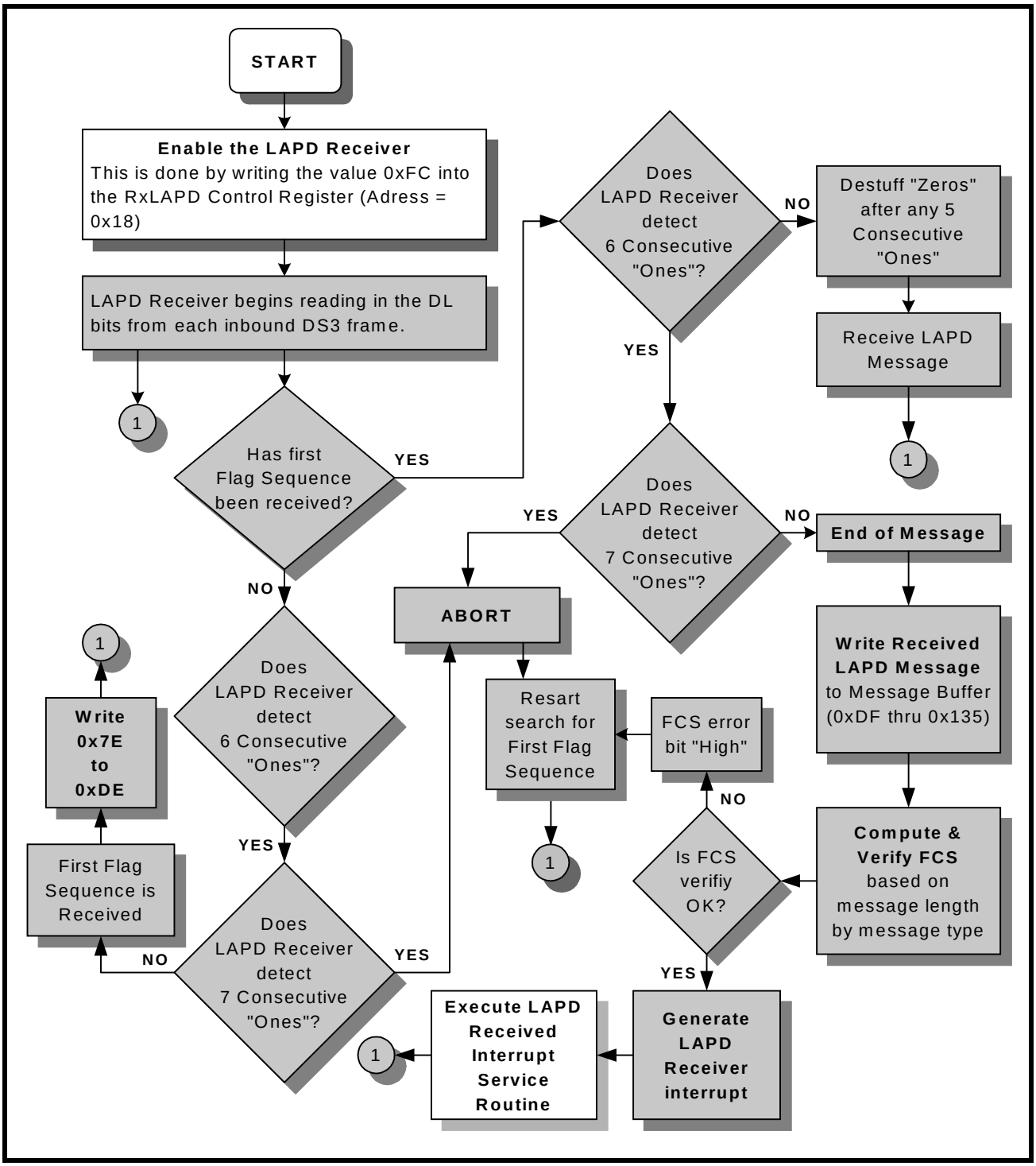
Writing the Incoming LAPD Message into the Receive LAPD Message Buffer

The LAPD receiver will obtain the LAPD Message frame from the incoming DS3 data-stream. In addition to processing the framing overhead octets, performing error checking (via FCS) and removing the stuffed 0s from the user payload data. The LAPD Receiver will also write the payload portion of the LAPD Frame into the Receive LAPD Message buffer at locations 0xDE through 0x135 in on-chip RAM.

Therefore, the local µP/µC must read this location when it wishes to process this newly received LAPD Message. Location 0xDE will contain the flag sequence 0x7E, which is the first header byte.

Figure 74 presents a flow chart depicting how the LAPD Receiver works.

FIGURE 74. FLOW CHART DEPICTING THE FUNCTIONALITY OF THE LAPD RECEIVER



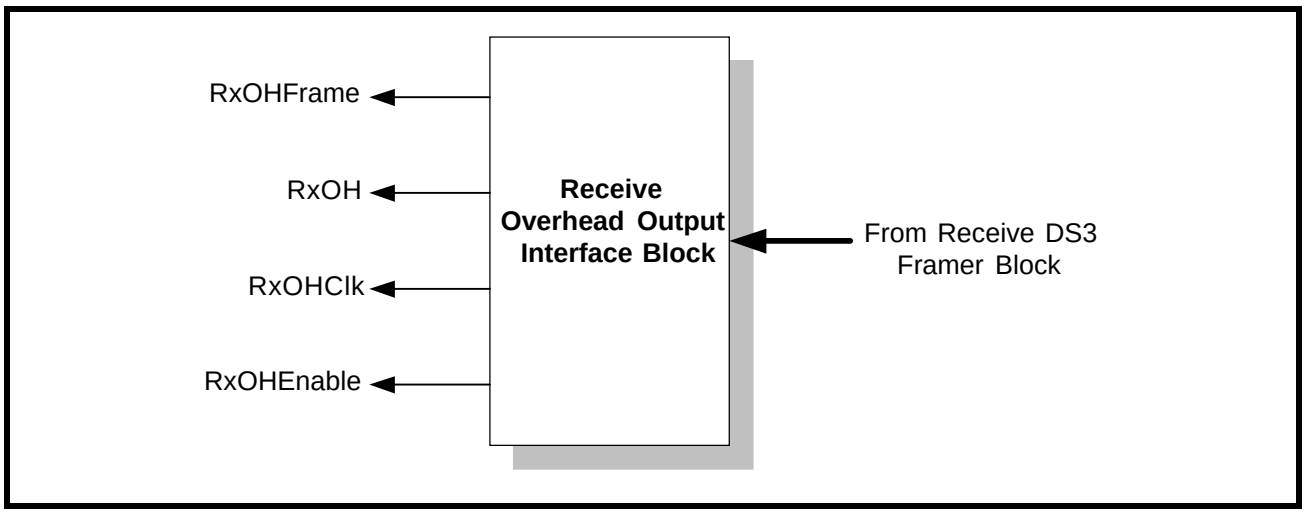
NOTES:

1. *The white (e.g., unshaded) boxes reflect tasks that the user's system must perform in order to configure the LAPD Receiver to receive LAPD Messages.*
2. *A brief description of the steps that must exist within the Receive LAPD Interrupt Service routine exists in* Section 4.3.6

4.3.4 The Receive Overhead Data Output Interface

Figure 75 presents a simple illustration of the Receive Overhead Data Output Interface block within the XRT72L50.

FIGURE 75. THE RECEIVE OVERHEAD OUTPUT INTERFACE BLOCK



The DS3 frame consists of 4760 bits. Of these bits, 4704 bits are payload bits and the remaining 56 bits are overhead bits. The XRT72L50 has been designed to handle and process both the payload type and overhead type bits for each DS3 frame.

The Receive Payload Data Output Interface block, within the Receive Section of the XRT72L50, has been designed to handle the payload bits. Likewise, the Receive Overhead Data Output Interface block has been designed to handle and process the overhead bits.

The Receive Overhead Data Output Interface block unconditionally outputs the contents of all overhead bits within the incoming DS3 data stream. The XRT72L50 does not offer the user a means to shut off this transmission of data. However, the Receive Overhead Output Interface block does provide the user with the appropriate output signals for external Data Link Layer equipment to sample and process these overhead bits, via the following two methods.

- Method 1- Using the RxOHClk clock signal.
- Method 2 - Using the RxClk and RxOHEnable output signals.

Each of these methods are described below.

4.3.4.1 *Method 1 - Using the RxOHClk Clock signal*

The Receive Overhead Data Output Interface block consists of four (4) signals. Of these four signals, the following three signals are to be used when sampling the DS3 overhead bits via Method 1.

- RxOH
- RxOHClk
- RxOHFrame

Each of these signals are listed and described below in Table 38.

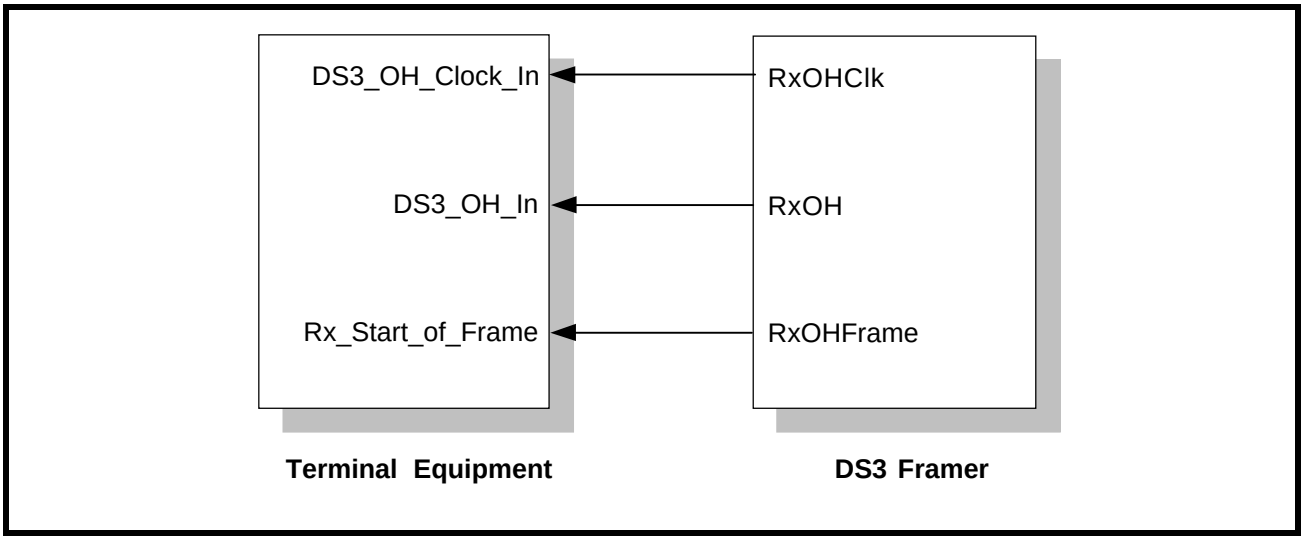
TABLE 38: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK

SIGNAL NAME	TYPE	DESCRIPTION
RxOH	Output	**Receive Overhead Data Output pin:** The XRT72L50 will output the overhead bits, within the incoming DS3 frames, via this pin. The Receive Overhead Data Output Interface block will output a given overhead bit, upon the falling edge of RxOHClk. Hence, the external data link equipment should sample the data, at this pin, upon the rising edge of RxOHClk. The XRT72L50 will always output the DS3 Overhead bits via this output pin. There are no external input pins or register bit settings available that will disable this output pin.
RxOHClk	Output	**Receive Overhead Data Output Interface Clock Signal:** The XRT72L50 will output the Overhead bits (within the incoming DS3 frames), via the RxOH output pin, upon the falling edge of this clock signal. As a consequence, the user's data link equipment should use the rising edge of this clock signal to sample the data on both the RxOH and RxOHFrame output pins. This clock signal is always active.
RxOHFrame	Output	**Receive Overhead Data Output Interface - Start of Frame Indicator:** The XRT72L50 will drive this output pin "High" (for one period of the RxOHClk signal), whenever the first overhead bit within a given DS3 frame is being driven onto the RxOH output pin.

Interfacing the Receive Overhead Data Output Interface block to the Terminal Equipment (Method 1)

Figure 76 illustrates how one should interface the Receive Overhead Data Output Interface block to the Terminal Equipment when using Method 1 to sample and process the overhead bits from the inbound DS3 data stream.

FIGURE 76. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (METHOD 1)



Method 1 Operation of the Terminal Equipment

If the Terminal Equipment intends to sample any overhead data from the inbound DS3 data stream (via the Receive Overhead Data Output Interface block) then it is expected to do the following:

1. Sample the state of the RxOHFrame signal (e.g., the Rx_Start_of_Frame input signal) on the rising edge of the RxOHClk (e.g., the DS3_OH_Clock_In) signal.
2. Keep track of the number of rising clock edges that have occurred in the RxOHClk (e.g., the DS3_OH_Clock_In) signal, since the last time the RxOHFrame signal was sampled "High". By doing this,

the Terminal Equipment will be able to keep track of which overhead bit is being output via the RxOH output pin. Based upon this information, the Terminal Equipment will be able to derive some meaning from these overhead bits.

Table 39 relates the number of rising clock edges (in the RxOHClk signal, since the RxOHFrame signal was last sampled "High") to the DS3 Overhead bit that is being output via the RxOH output pin.

TABLE 39: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN RXOHCLK, (SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

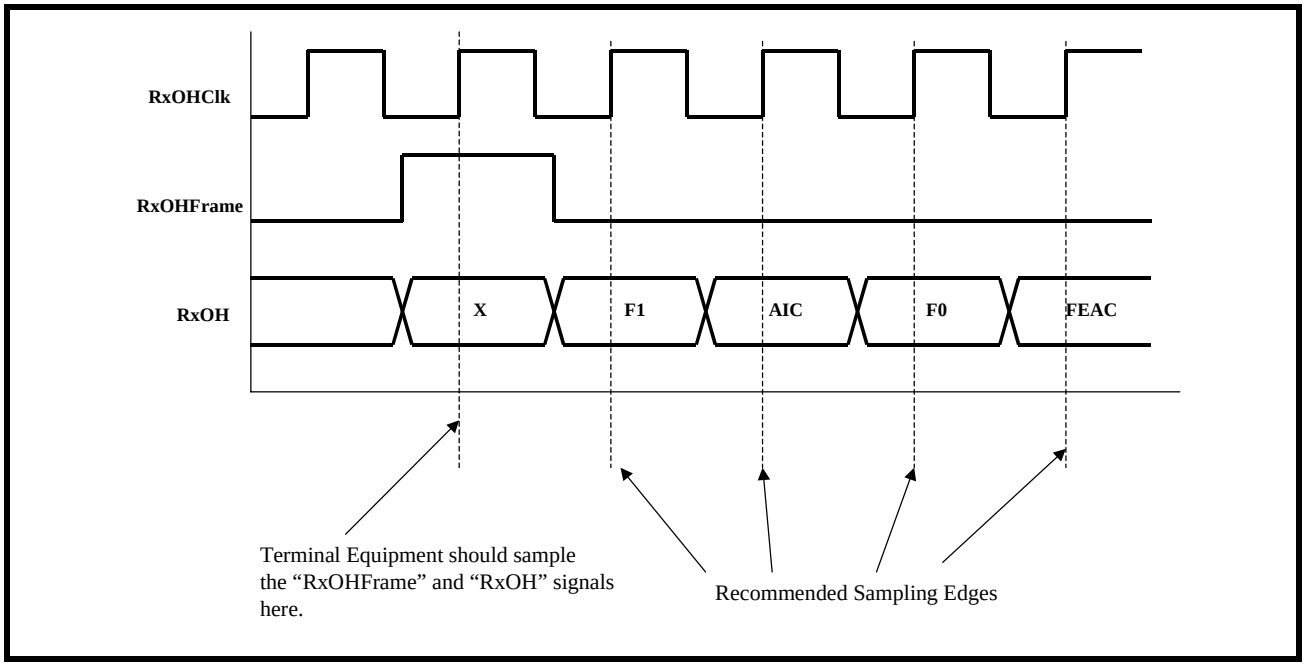
NUMBER OF RISING CLOCK EDGES IN RXOHCLK	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
0 (Clock edge is coincident with RxOHFrame being detected "High")	X
1	F1
2	AIC
3	F0
4	NA
5	F0
6	FEAC
7	F1
8	X
9	F1
10	UDL
11	F0
12	UDL
13	F0
14	UDL
15	F1
16	P
17	F1
18	CP
19	F0
20	CP
21	F0
22	CP
23	F1
24	P
25	F1

TABLE 39: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN RXOHCLK, (SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

NUMBER OF RISING CLOCK EDGES IN RXOHCLK	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
26	FEBE
27	F0
28	FEBE
29	F0
30	FEBE
31	F1
32	M0
33	F1
34	DL
35	F0
36	DL
37	F0
38	DL
39	F1
40	M1
41	F1
42	UDL
43	FO
44	UDL
45	FO
46	UDL
47	F1
48	M0
49	F1
50	UDL
51	F0
52	UDL
53	F0
54	UDL
55	F1

Figure 77 presents the typical behavior of the Receive Overhead Data Output Interface block, when Method 1 is being used to sample the incoming DS3 overhead bits.

FIGURE 77. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE OVERHEAD OUTPUT INTERFACE (FOR METHOD 1).



Method 2 - Using RxOutClk and the RxOHEnable signals

Method 1 requires that the Terminal Equipment be able to handle an additional clock signal, RxOHClk. However, there may be a situation in which the Terminal Equipment circuitry does not have the means to accommodate and process this extra clock signal, in order to use the Receive Overhead Data Output Interface. Hence, Method 2 is available. Method 2 involves the use of the following signals.

- RxOH
- RxOutClk
- RxOHEnable
- RxOHFrame

Each of these signals are listed and described below in Table 40.

TABLE 40: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (METHOD 2)

SIGNAL NAME	TYPE	DESCRIPTION
RxOH	Output	**Receive Overhead Data Output pin:** The XRT72L50 will output the overhead bits, within the incoming DS3 frames, via this pin. The Receive Overhead Output Interface will pulse the RxOHEnable output pin (for one RxOutClk period) at approximately the middle of the RxOH bit period. The user is advised to design the Terminal Equipment to latch the contents of the RxOH output pin, whenever the RxOHEnable output pin is sampled "High" on the falling edge of RxOutClk.
RxOHEnable	Output	**Receive Overhead Data Output Enable - Output pin:** The XRT72L50 will assert this output signal for one RxOutClk period when it is safe for the Terminal Equipment to sample the data on the RxOH output pin.

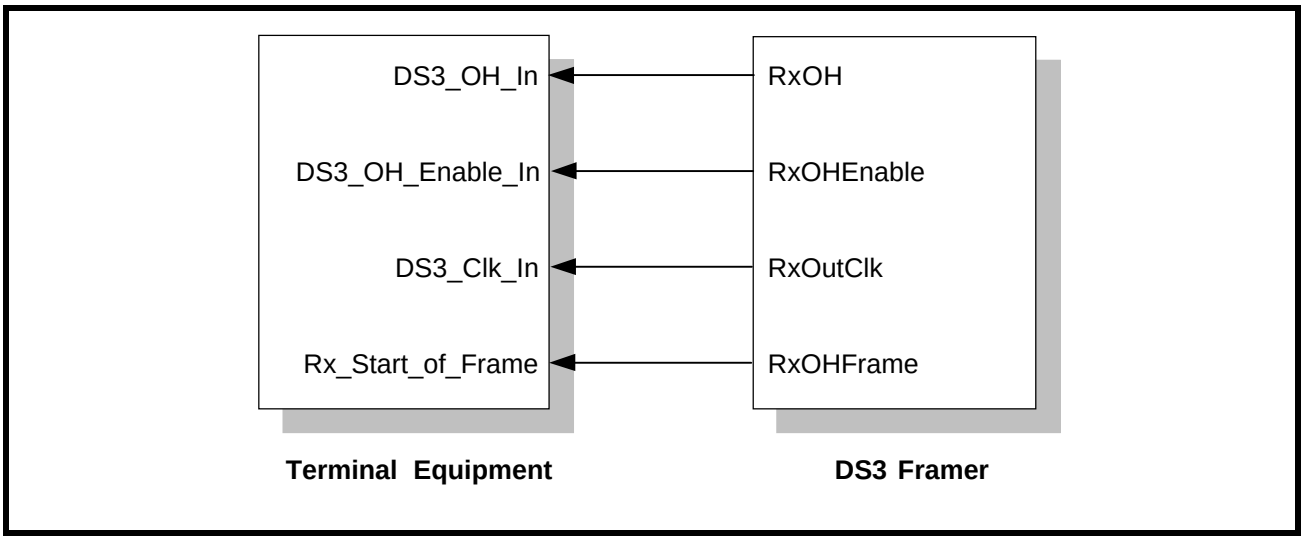
TABLE 40: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (METHOD 2)

SIGNAL NAME	TYPE	DESCRIPTION
RxOHFrame	Output	**Receive Overhead Data Output Interface - Start of Frame Indicator:** The XRT72L50 will drive this output pin "High" (for one period of the RxOH signal), whenever the first overhead bit, within a given DS3 frame is being driven onto the RxOH output pin.
RxOutClk	Output	**Receive Section Output Clock Signal:** This clock signal is derived from the RxLineClk signal (from the LIU) for loop-timing applications, and the TxInClk signal (from a local oscillator) for local-timing applications. For DS3 applications, this clock signal will operate at 44.736MHz. The user is advised to design the Terminal Equipment to latch the contents of the RxOH pin, anytime the RxOHEnable output signal is sampled "High" on the falling edge of this clock signal.

Interfacing the Receive Overhead Data Output Interface block to the Terminal Equipment (Method 2)

Figure 78 illustrates how one should interface the Receive Overhead Data Output Interface block to the Terminal Equipment, when using Method 2 to sample and process the overhead bits from the inbound DS3 data stream.

FIGURE 78. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE (METHOD 2)



Method 2 Operation of the Terminal Equipment

If the Terminal Equipment intends to sample any overhead data from the inbound DS3 data stream (via the Receive Overhead Data Output Interface), then it is expected to do the following.

1. Sample the state of the RxOHFrame signal (e.g., the Rx_Start_of_Frame input) on the falling edge of the RxOutClk clock signal, whenever the RxOHEnable output signal is also sampled "High".
2. Keep track of the number of times that the RxOHEnable signal has been sampled "High" since the last time the RxOHFrame was also sampled "High". By doing this, the Terminal Equipment will be able to keep track of which overhead bit is being output via the RxOH output pin. Based upon this information, the Terminal Equipment will be able to derive some meaning from these overhead bits.
3. Table 41 relates the number of RxOHEnable output pulses (that have occurred since both the RxOHFrame and the RxOHEnable pins were both sampled "High") to the DS3 overhead bit that is being output via the RxOH output pin.

TABLE 41: THE RELATIONSHIP BETWEEN THE NUMBER OF RXOHENABLE OUTPUT PULSES ((SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

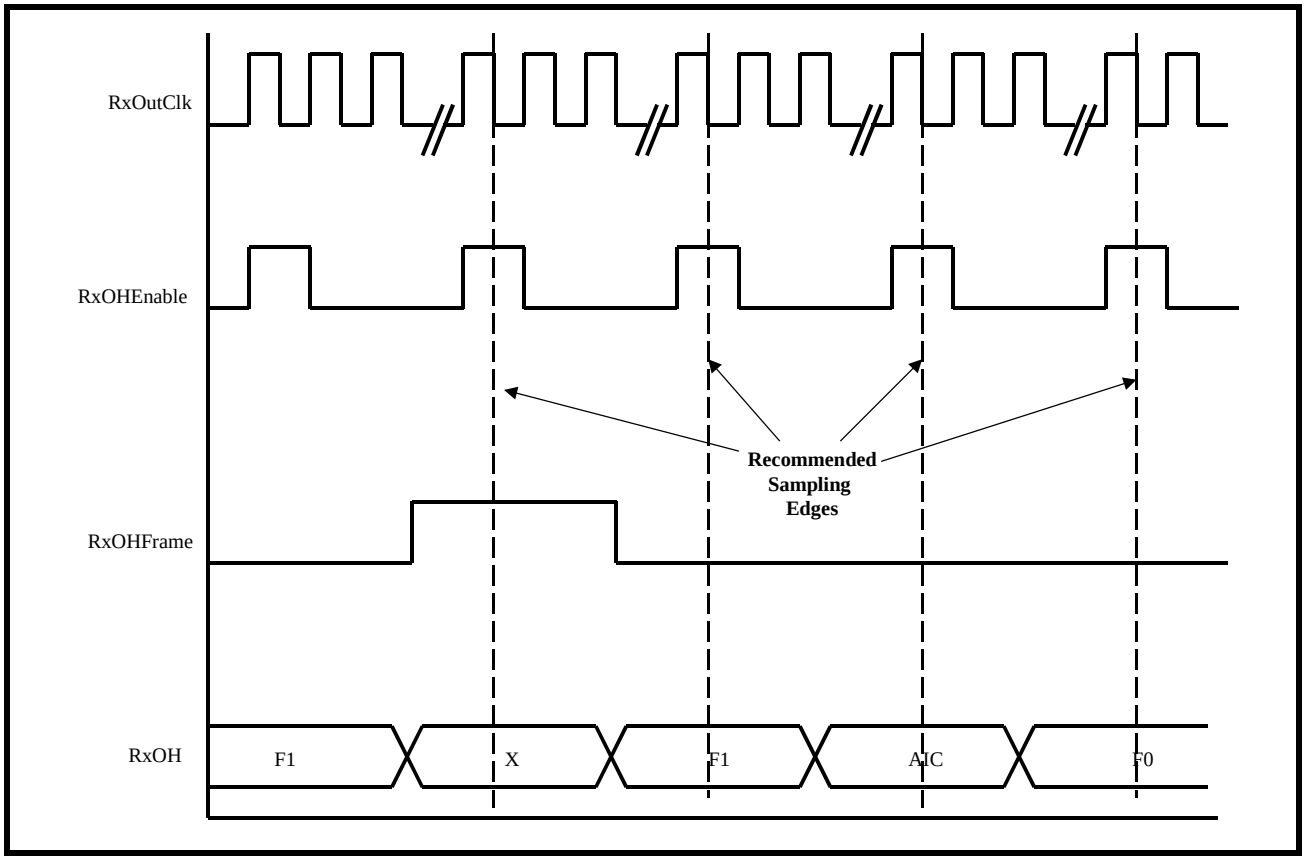
NUMBER OF RXOHENABLE OUTPUT PULSES	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
0 (The RxOHEnable and RxOHFrame signals are both sampled "High")	X
1	F1
2	AIC
3	F0
4	NA
5	F0
6	FEAC
7	F1
8	X
9	F1
10	UDL
11	F0
12	UDL
13	F0
14	UDL
15	F1
16	P
17	F1
18	CP
19	F0
20	CP
21	F0
22	CP
23	F1
24	P
25	F1
26	FEBE
27	F0
28	FEBE
29	F0
30	FEBE

TABLE 41: THE RELATIONSHIP BETWEEN THE NUMBER OF RXOHENABLE OUTPUT PULSES ((SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

NUMBER OF RXOHENABLE OUTPUT PULSES	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
31	F1
32	M0
33	F1
34	DL
35	F0
36	DL
37	F0
38	DL
39	F1
40	M1
41	F1
42	UDL
43	FO
44	UDL
45	FO
46	UDL
47	F1
48	M0
49	F1
50	UDL
51	F0
52	UDL
53	F0
54	UDL
55	F1

Figure 79 presents the typical behavior of the Receive Overhead Data Output Interface block, when Method 2 is being used to sample the incoming DS3 overhead bits.

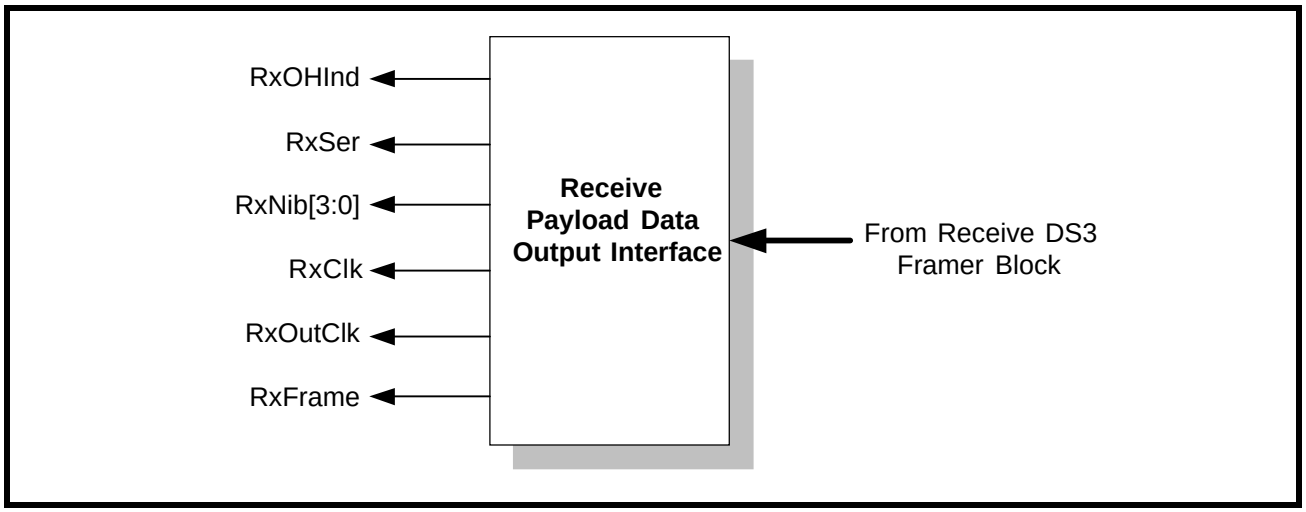
FIGURE 79. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (FOR METHOD 2).



4.3.5 The Receive Payload Data Output Interface

Figure 80 presents a simple illustration of the Receive Payload Data Output Interface block.

FIGURE 80. THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK



Each of the output pins of the Receive Payload Data Output Interface block are listed in Table 42 and described below. The exact role that each of these output pins assume, for a variety of operating scenarios are described throughout this section.

TABLE 42: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

SIGNAL NAME	TYPE	DESCRIPTION
RxSer	Output	**Receive Serial Payload Data Output pin:** If the XRT72L50 is operated in the serial mode, then the chip will output the payload data, of the incoming DS3 frames, via this pin. The XRT72L50 will output this data upon the rising edge of RxClk. The user is advised to design the Terminal Equipment such that it will sample this data on the falling edge of RxClk. ***NOTE:*** *This signal is only active if the NibIntf input pin is pulled "Low".*
RxNib[3:0]	Output	**Receive Nibble-Parallel Payload Data Output pins:** If the XRT72L50 is operated in the nibble-parallel mode, then the chip will output the payload data, of the incoming DS3 frames, via these pins. The XRT72L50 will output data via these pins, upon the falling edge of the RxClk output pin. The user is advised to design the Terminal Equipment such that it will sample this data upon the rising edge of RxClk. ***NOTE:*** *These pins are only active if the NibIntf input pin is pulled "High".*
RxClk	Output	**Receive Payload Data Output Clock pin:** The exact behavior of this signal depends upon whether the XRT72L50 is operating in the Serial or in the Nibble-Parallel-Mode. **Serial Mode Operation** In the serial mode, this signal is a 44.736MHz clock output signal. The Receive Payload Data Output Interface will update the data via the RxSer output pin, upon the rising edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxSer pin, upon the falling edge of this clock signal. **Nibble-Parallel Mode Operation** In this Nibble-Parallel Mode, the XRT72L50 will derive this clock signal, from the RxLineClk signal. The XRT72L50 will pulse this clock 1176 times for each inbound DS3 frame. The Receive Payload Data Output Interface will update the data, on the RxNib[3:0] output pins upon the falling edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxNib[3:0] output pins, upon the rising edge of this clock signal
RxOHInd	Output	**Receive Overhead Bit Indicator Output:** This output pin will pulse "High" whenever the Receive Payload Data Output Interface outputs an overhead bit via the RxSer output pin. The purpose of this output pin is to alert the Terminal Equipment that the current bit, (which is now residing on the RxSer output pin), is an overhead bit and should not be processed by the Terminal Equipment. The XRT72L50 will update this signal, upon the rising edge of the RxClk signal. The user is advised to design (or configure) the Terminal Equipment to sample this signal (along with the data on the RxSer output pin) on the falling edge of the RxClk signal. For DS3 applications, this output pin is only active if the XRT72L50 is operating in the Serial Mode. This output pin will be "Low" if the device is operating in the Nibble-Parallel Mode.
RxFrame	Output	**Receive Start of Frame Output Indicator:** The exact behavior of this pin, depends upon whether the XRT72L50 has been configured to operate in the Serial Mode or the Nibble-Parallel Mode. **Serial Mode Operation:** The Receive Section of the XRT72L50 will pulse this output pin "High" (for one bit period) when the Receive Payload Data Output Interface block is driving the very first bit of a given DS3 frame, onto the RxSer output pin. **Nibble-Parallel Mode Operation:** The Receive Section of the XRT72L50 will pulse this output pin "High" (for one nibble period), when the Receive Payload Data Output Interface is driving the very first nibble of a given DS3 frame, onto the RxNib[3:0] output pins.

Operation of the Receive Payload Data Output Interface block

The Receive Payload Data Output Interface permits the user to read out the payload data of inbound DS3 frames, via either of the following modes.

- Serial Mode
- Nibble-Parallel Mode

Each of these modes are described in detail, below.

4.3.5.1 *Serial Mode Operation*

Behavior of the XRT72L50

If the XRT72L50 has been configured to operate in the Serial mode, then the XRT72L50 will behave as follows.

Payload Data Output

The XRT72L50 will output the payload data, of the incoming DS3 frames via the RxSer output, upon the rising edge of RxClk.

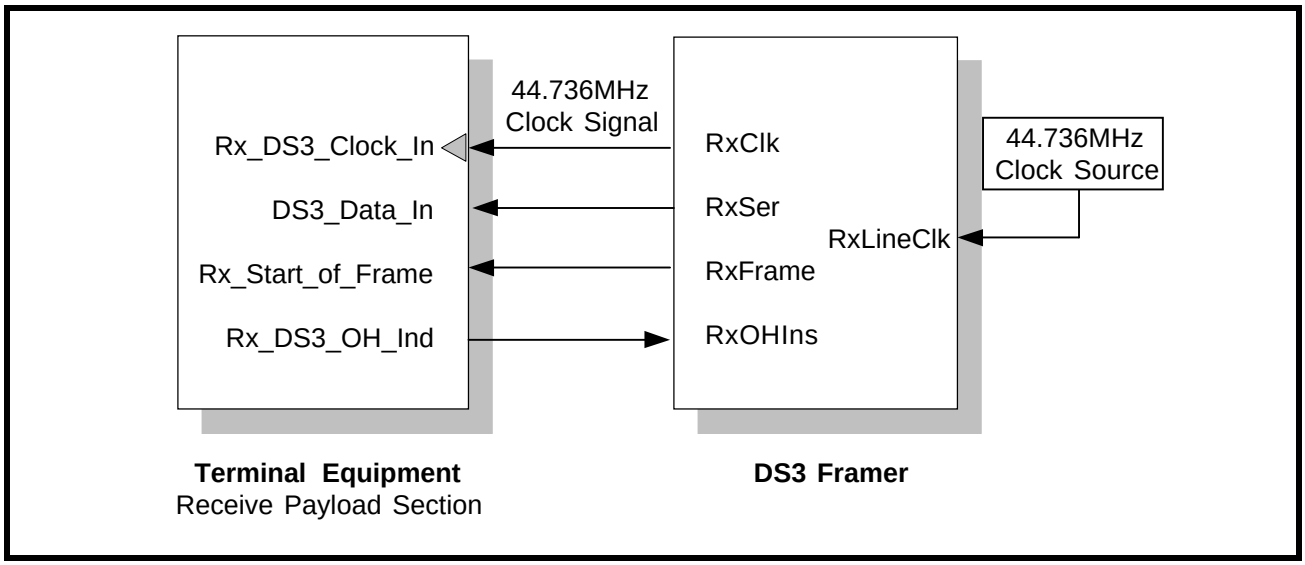
Delineation of inbound DS3 Frames

The XRT72L50 will pulse the RxFrame output pin "High" for one bit-period, coincident with it driving the first bit within a given DS3 frame, via the RxSer output pin.

Interfacing the XRT72L50 to the Receive Terminal Equipment

Figure 81 presents a simple illustration as how the user should interface the XRT72L50 to that terminal equipment which processes Receive Direction payload data.

FIGURE 81. THE XRT72L50 DS3/E3 FRAMER IC BEING INTERFACED TO THE RECEIVE TERMINAL EQUIPMENT (SERIAL MODE OPERATION)



Required Operation of the Terminal Equipment

The XRT72L50 will update the data on the RxSer output pin, upon the rising edge of RxClk. However, because the rising edge of RxClk to data delay is between 14ns to 16ns, the Terminal Equipment should sample the data on the RxSer output pin (or the DS3_Data_In pin at the Terminal Equipment) upon the rising edge of RxClk. This will still permit the Terminal Equipment with a RxSer to RxClk set-up time of approximately 6ns and a hold time of 14 to 16ns. As the Terminal Equipment samples RxSer with each rising edge of RxClk it should also be sampling the following signals.

- RxFrame
- RxOHInd

The Need for sampling RxFrame

The XRT72L50 will pulse the RxFrame output pin "High" coincident with it driving the very first bit of a given DS3 frame onto the RxSer output pin. If knowledge of the DS3 Frame Boundaries is important for the operation of the Terminal Equipment, then this is a very important signal for it to sample.

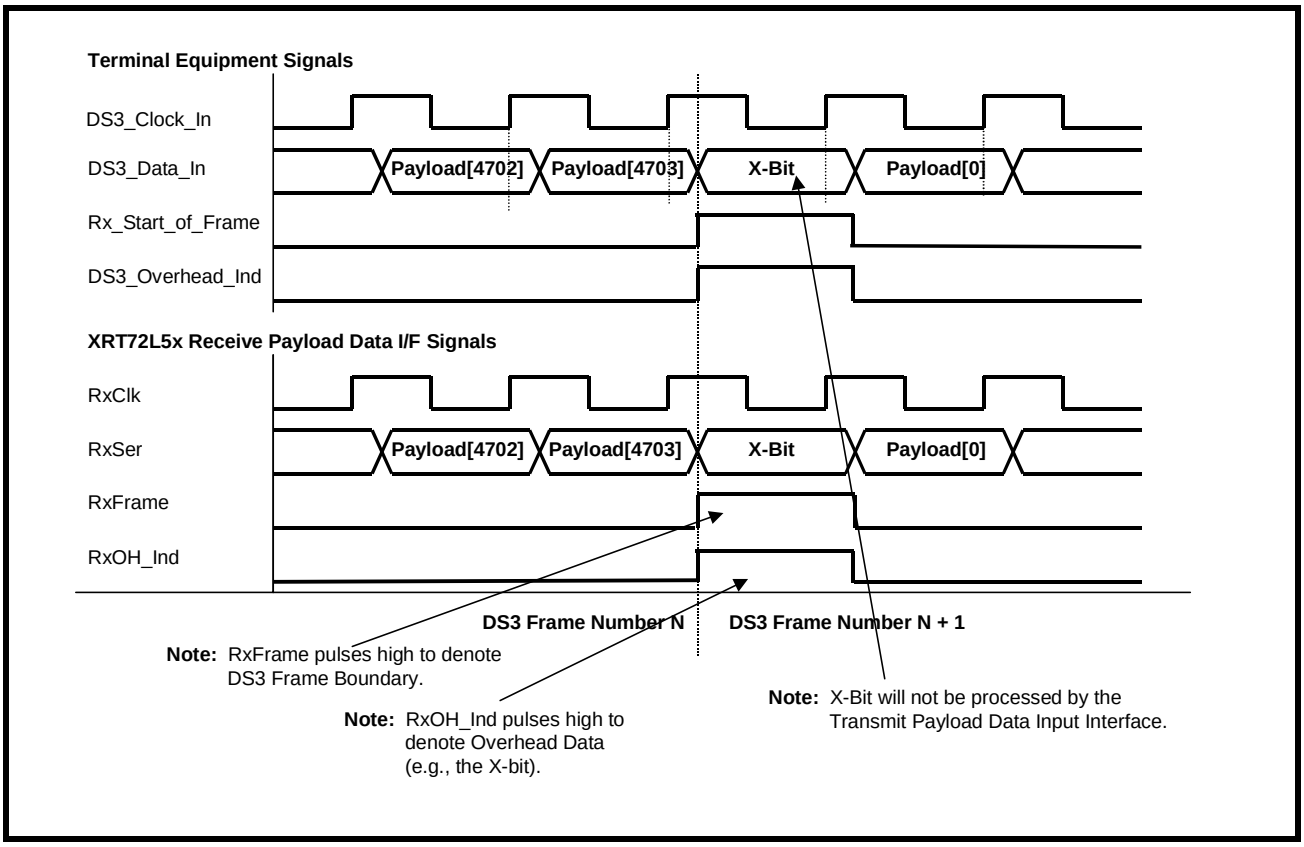
The Need for sampling RxOHInd

The XRT72L50 will indicate that it is currently driving an overhead bit onto the RxSer output pin, by pulsing the RxOHInd output pin "High". If the Terminal Equipment samples this signal "High", then it should know that the bit, that it is currently sampling via the RxSer pin is an overhead bit and should not be processed.

The Behavior of the Signals between the Receive Payload Data Output Interface block and the Terminal Equipment

The behavior of the signals between the XRT72L50 and the Terminal Equipment for DS3 Serial Mode Operation is illustrated in Figure 82.

FIGURE 82. AN ILLUSTRATION OF THE BEHAVIOR OF THE SIGNALS BETWEEN THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK OF THE XRT72L50 AND THE TERMINAL EQUIPMENT (SERIAL MODE OPERATION)



4.3.5.2 *Nibble-Parallel Mode Operation*

Behavior of the XRT72L50

If the XRT72L50 has been configured to operate in the Nibble-Parallel Mode, then the XRT72L50 will behave as follows.

Payload Data Output

The XRT72L50 will output the payload data of the incoming DS3 frames, via the RxNib[3:0] output pins, upon the falling edge of RxClk.

NOTES:

1. *In this case, RxClk will function as the Nibble Clock signal between the XRT72L50 the Terminal Equipment. The XRT72L50 will pulse the RxClk output signal "High" 1176 times, for each inbound DS3 frame.*
2. *Unlike Serial Mode operation, the duty cycle of RxClk, in Nibble-Parallel Mode operation is approximately 25%.*

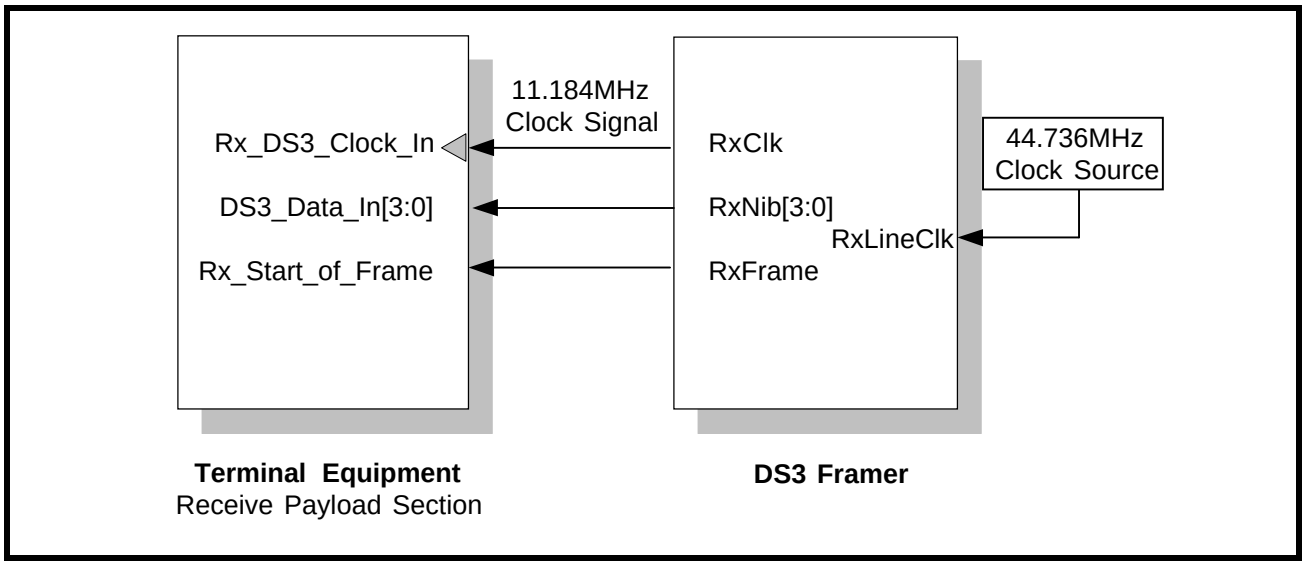
Delineation of Inbound DS3 Frames

The XRT72L50 will pulse the RxFrame output pin "High" for one nibble-period coincident with it driving the very first nibble, within a given inbound DS3 frame, via the RxNib[3:0] output pins.

Interfacing the XRT72L50 the Terminal Equipment.

Figure 83 presents a simple illustration as how the user should interface the XRT72L50 to that terminal equipment which processes Receive Direction payload data.

FIGURE 83. THE XRT72L50 DS3/E3 FRAMER IC BEING INTERFACED TO THE RECEIVE SECTION OF THE TERMINAL EQUIPMENT (NIBBLE-PARALLEL MODE OPERATION)



Required Operation of the Terminal Equipment

The XRT72L50 will update the data on the RxNib[3:0] line, upon the falling edge of RxClk. Hence, the Terminal Equipment should sample the data on the RxNib[3:0] output pins (or the DS3_Data_In[3:0] input pins at the Terminal Equipment) upon the rising edge of RxClk. As the Terminal Equipment samples RxSer with each rising edge of RxClk it should also be sampling the RxFrame signal.

The Need for Sampling RxFrame

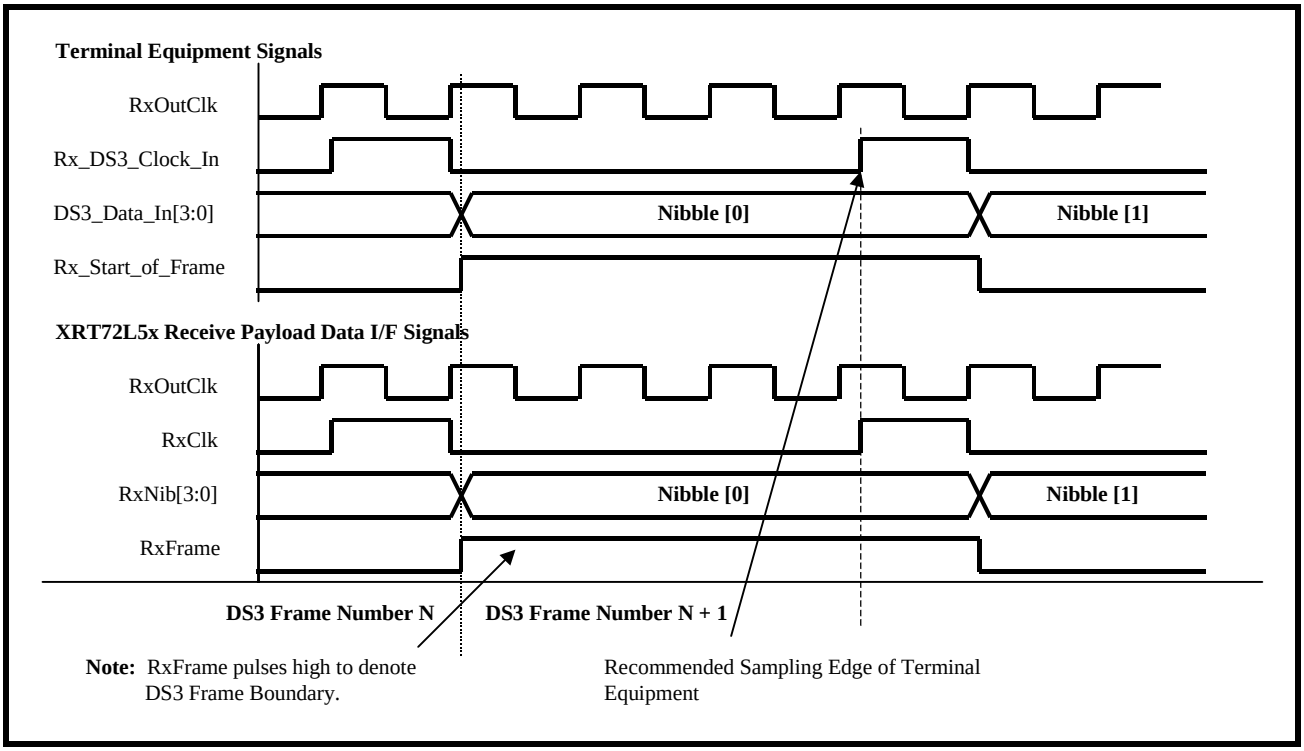
The XRT72L50 will pulse the RxFrame output pin "High" coincident with it driving the very first nibble of a given DS3 frame, onto the RxNib[3:0] output pins. If knowledge of the DS3 Frame Boundaries is important for the operation of the Terminal Equipment, then this is a very important signal for it to sample.

NOTE: *For DS3/Nibble-Parallel Mode Operation, none of the Overhead bits will be output via the RxNib[3:0] output pins. Hence, the RxOH_Ind output pin will be in-active in this mode.*

The Behavior of the Signals between the Receive Payload Data Output Interface block and the Terminal Equipment

The behavior of the signals between the XRT72L50 and the Terminal Equipment for DS3 Nibble-Mode operation is illustrated in Figure 84.

FIGURE 84. AN ILLUSTRATION OF THE BEHAVIOR OF THE SIGNALS BETWEEN THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK OF THE XRT72L50 AND THE TERMINAL EQUIPMENT (NIBBLE-MODE OPERATION).



4.3.6 Receive Section Interrupt Processing

The Receive Section of the XRT72L50 can generate an interrupt to the Microcontroller/Microprocessor for the following reasons.

- Change of State of Receive LOS (Loss of Signal) condition
- Change of State of Receive OOF (Out of Frame) condition
- Change of State of Receive AIS (Alarm Indicator Signal) condition
- Change of State of Receive Idle Condition.
- Change of State of Receive FERF (Far-End Receive Failure) condition.
- Change of State of AIC (Application Identification Channel) bit.
- Detection of P-Bit Error in a DS3 frame
- Detection of CP-Bit Error in a DS3 frame
- The Receive FEAC Message - Validation Interrupt
- The Receive FEAC Message - Removal Interrupt
- Completion of Reception of a LAPD Message

4.3.6.1 *Enabling Receive Section Interrupts*

The Interrupt Structure, within the XRT72L50 contains two hierarchical levels.

- Block Level
- Source Level

The Block Level

The Enable state of the Block level for the Receive Section Interrupts dictates whether or not interrupts (if enabled at the source level), are actually enabled.

These Receive Section interrupts can be enabled or disabled at the Block Level, by writing the appropriate data into Bit 7 (Rx DS3/E3 Interrupt Enable) within the Block Interrupt Enable register (Address = 0x04), as illustrated below.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
X	0	0	0	0	0	0	0

Setting this bit-field to “1” enables the Receive Section (at the Block Level) for interrupt generation. Conversely, setting this bit-field to “0” disables the Receive Section for interrupt generation.

4.3.6.2 *Enabling/Disabling and Servicing Receive Section Interrupts*

The Receive Section of the XRT72L50 Framer IC contains numerous interrupts. The Enabling/Disabling and Servicing of each of these interrupts is described below.

4.3.6.2.1 The Change of State on Receive LOS Interrupt

If the Change of State on Receive LOS (Loss of Signal) Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an LOS (Loss of Signal) condition, and
2. When the XRT72L50 Framer IC clears the LOS (Loss of Signal) condition.

Conditions causing the XRT72L50 Framer IC to declare an LOS condition

- If the XRT73L00 LIU IC declares an LOS condition, and drives the RLOS input pin (of the XRT72L50 Framer IC) "High".
- If the XRT72L50 Framer IC detects a 180 consecutive “0’s”, via the RxPOS and RxNEG input pins and Internal LOS is enabled, (Address 0x00, bit 5).

Conditions causing the XRT72L50 Framer IC to clear the LOS condition.

- When the XRT73L00 LIU IC ceases declaring an LOS condition and drives the RLOS input pin (of the XRT72L50 Framer IC) "Low".
- When the XRT72L50 Framer IC detects at least 60 marks (via the RxPOS and RxNEG input pins) out of 180 bit-periods and Internal LOS is enabled, (Address 0x00, bit 5).

Enabling and Disabling the Change of State on Receive LOS Interrupt:

The Change of State on Receive LOS Interrupt can be enabled or disabled by writing the appropriate value into Bit 6 (LOS Interrupt Enable) within the RxDS3 Interrupt Enable Register, as illustrated below.

RxDS3 Interrupt Enable Register (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change of State on Receive LOS Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$) by driving this pin "Low".
- It will set Bit 6 (LOS Interrupt Status) within the RxDS3 Interrupt Status register to “1”, as illustrated below.

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	1	0	0	0	0	0	0

Whenever the user’s system encounters the Change of LOS on Receive Interrupt, then it should do the following.

1. It should determine the current state of the LOS condition. Recall, that this interrupt can generated, whenever the XRT72L50 Framer declares or clears the LOS defects. Hence, the current state of the LOS defect can be determined by reading the state of Bit 6 (RxLOS), within the RxDS3 Configuration & Status Registers, as illustrated below.

RxDS3 Configuration & Status Register (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
0	1	0	0	X	0	0	0

If the LOS State is TRUE

1. It should transmit a FERF (Far-End Receive Failure) to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-LOS feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the Remote Terminal, indicating that a Loss of Signal condition has been declared.

If the LOS State is FALSE

1. It should cease transmitting a FERF indicator to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-LOS feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the Remote Terminal Equipment, indicating that the Loss of Signal condition has been cleared.

4.3.6.2.2 The Change of State on Receive OOF Interrupt

If the Change of State on Receive OOF (Out-of-Frame) Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an OOF (Out of Frame) condition, and
2. When the XRT72L50 Framer IC clears the OOF (Out of Frame) condition.

Conditions causing the XRT72L50 Framer IC to declare an OOF condition

- If the Receive DS3 Framer block (within the XRT72L50 Framer IC) detects at least either 3 or 6 F-bit errors, in the last 16 F-bits.

Conditions causing the XRT72L50 Framer IC to clear the OOF condition.

- Whenever, the Receive DS3 Framer block transitions from the M-Bit Search into the In-Frame state (within the Frame Acquisition/Maintenance State Machine Diagram).

Enabling and Disabling the Change of State on Receive OOF Interrupt:

The Change of State on Receive OOF Interrupt can be enabled or disabled by writing the appropriate value into Bit 1 (OOF Interrupt Enable) within the RxDS3 Interrupt Enable Register, as illustrated below.

RxDS3 Interrupt Enable Register (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change of State on Receive OOF Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$) by driving this pin "Low".
- It will set Bit 1 (OOF Interrupt Status), within the RxDS3 Interrupt Status Register to “1”, as indicated below.

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	1	0

Whenever the Terminal Equipment encounters a Change in OOF on Receive Interrupt, then it should do the following.

1. It should determine the current state of the OOF condition. Recall, that this interrupt can generated, whenever the XRT72L50 Framer declares or clears the OOF defects. Hence, the current state of the OOF defect can be determined by reading the state of Bit 4 (RxOOF), within the RxDS3 Configuration & Status Registers, as illustrated below.

RxDS3 Configuration & Status Register (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
0	0	0	0	X	0	0	0

If OOF is TRUE.

1. It should transmit a FERF (Far-End Receive Failure) to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-OOF feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the Remote Terminal, indicating that a Service Affecting condition has been detected in the Local Terminal Equipment.

if OOF is FALSE

1. It should cease transmitting a FERF (Far-End Receive Failure) indicator to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-OOF feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the Remote Terminal Equipment, indicating that the Service Affecting condition has been cleared.

4.3.6.2.3 The Change of State of Receive AIS Interrupt

If the Change of State on Receive AIS (Alarm Indication Signal) Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC detects an AIS pattern, in the incoming DS3 data stream, and
2. When the XRT72L50 Framer IC no longer detects the AIS pattern in the incoming DS3 data stream.

Conditions causing the XRT72L50 Framer IC to declare an AIS condition

- If the Receive DS3 Framer block (within the XRT72L50 Framer IC) detects at least 63 DS3 frames, which contains the AIS pattern.

Conditions causing the XRT72L50 Framer IC to clear the AIS condition.

- Whenever, the Receive DS3 Framer block detects 63 DS3 frames, which do not contain the AIS pattern.

Enabling and Disabling the Change of State on Receive AIS Interrupt:

The Change of State on Receive AIS Interrupt can be enabled or disabled by writing the appropriate value into Bit 5 (AIS Interrupt Enable) within the RxDS3 Interrupt Enable Register, as illustrated below.

RxDS3 Interrupt Enable Register (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change of State on Receive AIS Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$) by driving it "Low".
- It will set Bit 5 (AIS Interrupt Status) within the RxDS3 Interrupt Status Register, to “1”, as indicated below.

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	1	0	0	0	0	0

Whenever the Terminal Equipment encounters a Change in AIS on Receive interrupt, it should do the following.

1. It should determine the current state of the AIS condition. Recall, that this interrupt can generated, whenever the XRT72L50 Framer declares or clears the AIS defects. Hence, the current state of the AIS defect can be determined by reading the state of Bit 7 (RxAIS), within the RxDS3 Configuration & Status Registers, as illustrated below

RxDS3 Configuration & Status Register (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
0	0	0	0	X	0	0	0

If the AIS Condition is TRUE

1. The Local Terminal Equipment should transmit a FERF (Far-End Receive Failure) to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-AIS feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the Remote Terminal, indicating that a Service Affecting condition has been detected in the Local Terminal Equipment.

If the AIS Condition is FALSE

1. The Local Terminal Equipment should cease transmitting a FERF (Far-End Receive Failure) indicator to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-AIS feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE) to the Remote Terminal, indicates that the Service Affecting condition no longer exists.

4.3.6.2.4 The Change of State of Receive Idle Interrupt

If the Change of State on Receive Idle Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC detects an Idle pattern, in the incoming DS3 data stream, and
2. When the XRT72L50 Framer IC no longer detects the Idle pattern in the incoming DS3 data stream.

Conditions causing the XRT72L50 Framer IC to declare an Idle condition

- If the Receive DS3 Framer block (within the XRT72L50 Framer IC) detects at least 63 DS3 frames, which contains the Idle pattern.

Conditions causing the XRT72L50 Framer IC to clear the Idle condition.

- Whenever, the Receive DS3 Framer block detects 63 DS3 frames, which do not contain the Idle pattern.

Enabling and Disabling the Change of State on Receive Idle Interrupt:

To enable or disable the Change of State on Receive Idle Interrupt, write the appropriate value into Bit 4 (Idle Interrupt Enable) within the RxDS3 Interrupt Enable Register, as illustrated below.

RxDS3 Interrupt Enable Register (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change of State on Receive Idle Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request Output pin ($\overline{Int}$) by driving it "Low".
- It will set Bit 4 (Idle Interrupt Status), within the Rx DS3 Interrupt Status Register to “1”, as indicated below.

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	1	0	0	0	0

Whenever the Terminal Equipment encounters the Change in Idle Condition Receive Interrupt, it should do the following.

1. It should determine the current state of the Idle condition. Recall, that this interrupt can generated, whenever the XRT72L50 Framer declares or clears the Idle condition. Hence, the current state of the Idle condition can be determined by reading the state of Bit 5 (RxIdle), within the RxDS3 Configuration & Status Registers, as illustrated below

RxDS3 Configuration & Status Register (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
RO	RO	RO	RO	RO	R/W	R/W	R/W
0	0	0	0	X	0	0	0

4.3.6.2.5 The Change of State of Receive FERF Interrupt

If the Change of State on Receive FERF Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC detects the FERF indicator, in the incoming DS3 data stream, and
2. When the XRT72L50 Framer IC no longer detects the FERF indicator, in the incoming DS3 data stream.

Conditions causing the XRT72L50 Framer IC to declare an FERF (Far-End-Receive Failure) condition

- If the Receive DS3 Framer block (within the XRT72L50 Framer IC) detects some incoming DS3 frames with both of the X bits set to “0”.

Conditions causing the XRT72L50 Framer IC to clear the FERF condition.

- Whenever, the Receive DS3 Framer block starts to detect some incoming DS3 frames, in which the X bits are not set to “0”.

Enabling and Disabling the Change of State on Receive FERF Interrupt:

To enable or disable the Change of State on Receive FERF Interrupt, write the appropriate value into Bit 3 (FERF Interrupt Enable) within the RxDS3 Interrupt Enable Register, as illustrated below.

RxDS3 Interrupt Enable Register (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change of State on Receive FERF Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request Output pin ($\overline{\text{Int}}$) by driving it "High".
- It will set Bit 3 (FERF Interrupt Status), within the Rx DS3 Interrupt Status Register, to “1”, as indicated below.

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

Whenever the Terminal Equipment encounters a Change in FERF Condition on Receive Interrupt, it should do the following.

1. It should determine the current state of the FERF condition. Recall, that this interrupt can generated, whenever the XRT72L50 Framer declares or clears the FERF condition. Hence, to determine the current

state of the FERF condition read the state of Bit 4 (RxFERF), within the RxDS3 Status Registers, as illustrated below

RxDS3 Status Register (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			RxFERF	RxAIC	RxFEBE[2:0]		
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

4.3.6.2.6 The Change of State of Receive AIC Interrupt

If the Change of State of Receive AIC Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt, anytime the Receive DS3 Framer block has detected a change in the value of the AIC bit, within the incoming DS3 data stream.

Enabling and Disabling the Change of State of Receive AIC Interrupt:

To enable or disable the Change of State on Receive AIC Interrupt, write the appropriate value into Bit 2 (AIC Interrupt Enable) within the RxDS3 Interrupt Enable Register, as illustrated below.

RxDS3 Interrupt Enable Register (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change of State on Receive AIC Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request Output pin ($\overline{Int}$) by driving it "High".
- It will set Bit 2 (AIC Interrupt Status), within the Rx DS3 Interrupt Status Register, to “1”, as indicated below.

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

Whenever the Terminal Equipment encounters this interrupt, it should do the following.

- It should continue to check the state of the AIC bit, in order to see if this change is constant.
- If this change is constant, then the user should configure the XRT72L50 Framer IC to operate in the M13 framing format, if the AIC bit-field is “0”.

- Conversely, if the AIC bit-field is “1”, then the user should configure the XRT72L50 Framer IC to operate in the C-bit Parity framing format.

4.3.6.2.7 The Detection of P-Bit Error Interrupt

If the Detection of P-Bit Error Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt, anytime the Receive DS3 Framer block has detected a P-bit error, within the incoming DS3 data stream.

Enabling and Disabling the Detection of P-Bit Error Interrupt:

The Detection of P-Bit Error Interrupt can be enabled or disabled by writing the appropriate value into Bit 0 (P-Bit Error Interrupt Enable) within the RxDS3 Interrupt Enable Register, as illustrated below.

RxDS3 Interrupt Enable Register (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Detection of P-Bit Error Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$) by driving it "High".
- It will set Bit 0 (P-Bit Error Interrupt Status) within the Rx DS3 Interrupt Status Register, to “1”, as indicated below.

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	1

Whenever the Terminal Equipment encounters the Detection of P-bit Error Interrupt, It should read the contents of PMON Parity Error Count Register (located at 0x54 and 0x55), in order to determine the number of P-bit errors recently received.

4.3.6.2.8 The Detection of CP-Bit Error Interrupt

If the Detection of CP-Bit Error Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt, anytime the Receive DS3 Framer block has detected a CP-bit error, within the incoming DS3 data stream.

Enabling and Disabling the Detection of CP-Bit Error Interrupt:

To enable or disable the Detection of CP-Bit Error Interrupt, write the appropriate value into Bit 7 (CP-Bit Error Interrupt Enable) within the RxDS3 Interrupt Enable Register, as illustrated below.

RxDS3 Interrupt Enable Register (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Detection of CP-Bit Error Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$) by driving it "High".
- It will set Bit 7 (CP-Bit Error Interrupt Status) within the Rx DS3 Interrupt Status Register, to “1”, as indicated below.

RxDS3 Interrupt Status Register (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
1	0	0	0	0	0	0	1

Whenever the Terminal Equipment encounters the Detection of CP-bit Error Interrupt, it should do the following.

- It should read contents of PMON Frame CP-Bit Error Count Register (located at 0x72 and 0x73), in order to determine the number of CP-bit errors recently received.

4.3.6.2.9 The Receive FEAC Message - Validation Interrupt

If the Receive FEAC Message - Validation Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt any time the Receive FEAC Processor validates a new FEAC (Far-End Alarm & Control) Message.

In particular, the Receive FEAC Processor will validate a FEAC Message, if that same FEAC Message has been received in 8 of the last 10 FEAC Message receptions.

Enabling/Disabling the Receive FEAC Message - Validation Interrupt

To enable or disable the Receive FEAC Message - Validation Interrupt, write the appropriate data into Bit 1 (RxFEAC Valid Interrupt Enable) within the RxDS3 FEAC Interrupt Enable/Status Register, as indicated below.

RxDS3 FEAC Interrupt Enable/Status Register (Address = 0x17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
0	0	0	0	0	0	X	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Receive FEAC Message - Validation Interrupt.

Whenever the XRT72L50 Framer IC generates this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$) by driving it "Low".
- It will set Bit 0 (RxFEAC Valid Interrupt Status), within the RxDS3 FEAC Interrupt Enable/Status Register to “1”, as indicated below.

RxDS3 FEAC Interrupt Enable/Status Register (Address = 0x17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
0	0	0	0	0	0	1	1

- It will write the contents of this validated FEAC Message into the Rx DS3 FEAC Register, as indicated below.

RXDS3 FEAC REGISTER (ADDRESS = 0X16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxFEAC[5:0]						Not Used
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Whenever the Terminal Equipment encounters the Receive FEAC Message - Validation Interrupt, then it should do the following.

- It should read the contents of the High RxDS3 FEAC Register, and respond accordingly.

4.3.6.2.10 The Receive FEAC Message - Removal Interrupt

if the Receive FEAC Message - Removal Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt any time the High Receive FEAC Processor removes a new FEAC (Far-End Alarm & Control) Message.

In particular, the Receive FEAC Processor will remove a FEAC Message if it has received a different FEAC Message (from the most recently validated message) in 3 of the last 10 FEAC Message receptions.

Enabling/Disabling the Receive FEAC Message - Removal Interrupt

To enable or disable the Receive FEAC Message - Removal Interrupt, write the appropriate data into Bit 3 (RxFEAC Remove Interrupt Enable) within the RxDS3 FEAC Interrupt Enable/Status Register, as indicated below.

RxDS3 FEAC Interrupt Enable/Status Register (Address = 0x17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
0	0	0	0	X	0	X	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Receive FEAC Message - Validation Interrupt.

Whenever the XRT72L50 Framer IC generates this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$) by driving it "Low".
- It will set Bit 2 (RxFEAC Remove Interrupt Status), within the RxDS3 FEAC Interrupt Enable/Status Register to “1”, as indicated below.

RxDS3 FEAC Interrupt Enable/Status Register (Address = 0x17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
0	0	0	0	0	0	1	1

- It will delete the contents of the most recently validated FEAC Message from the Rx DS3 FEAC Register, as indicated below.

RXDS3 FEAC REGISTER (ADDRESS = 0X16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxFEAC[5:0]						Not Used
RO	RO	RO	RO	RO	RO	RO	RO
0	X	X	X	X	X	X	0

4.3.6.2.11 The Completion of Reception of a LAPD Message Interrupt

If the Completion of Reception of a LAPD Message interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt anytime the Receive HDLC Controller block has received a new LAPD Message buffer, from the Remote Terminal Equipment, and has stored the contents of this message in the Receive LAPD Message Buffer.

Enabling/Disable the Receive LAPD Message Interrupt

To enable or disable the Receive LAPD Message Interrupt, write the appropriate data into Bit 1 (RxLAPD Interrupt Enable) within the RxDS3 LAPD Control Register, as indicated below.

RxDS3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	X	0

Writing a “1” into this bit-field enables the Receive LAPD Message Interrupt. Conversely, writing a “0” into this bit-field disables the Receive LAPD Message interrupt.

Servicing the Receive LAPD Message Interrupt

Whenever the XRT72L50 Framer IC generates this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$) by driving it "Low".
- It will set Bit 0 (RxLAPD Interrupt Status), within the Rx DS3 LAPD Control Register to “1”, as indicated below.

RxDS3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	1	1

- It will write the contents of this newly Received LAPD Message into the Receive LAPD Message buffer (located at 0xDE through 0x135).

Whenever the Terminal Equipment encounters the Receive LAPD Interrupt, then it should read out the contents of the Receive LAPD Message buffer, and respond accordingly.

5.0 E3/ITU-T G.751 OPERATION OF THE XRT72L50

The XRT72L50 can be configured to operate in the E3/ITU-T G.751 Mode by writing a “0” into bit-field 6 and a “0” into bit-field 2, within the Framer Operating Mode register, as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	0	x	0	x	0	x	x

5.1 *Description of the E3, ITU-T G.751 Frames and Associated Overhead Bits*

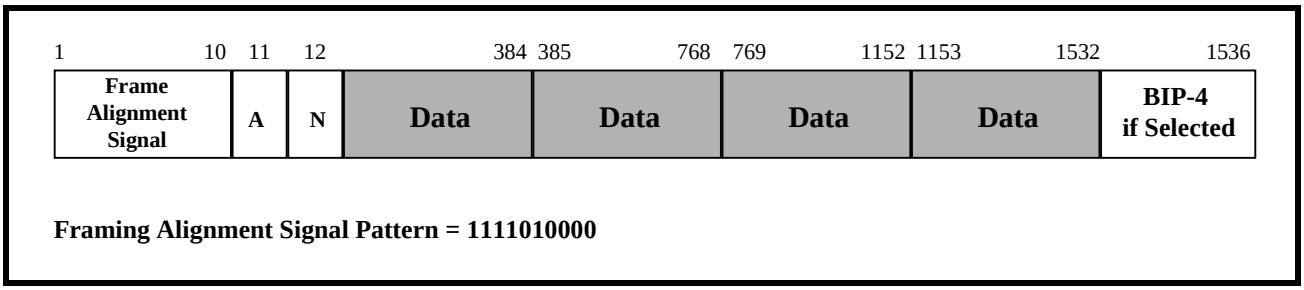
The E3, ITU-T G.751 Frame contains 1536 bits, of which 12 bits are overhead and the remaining 1524 bits are payload bits.

Each E3, ITU-T G.751 Frame consists of the following 12 overhead bits.

- A 10 bit FAS (Framing Alignment Signal) pattern. This pattern is assigned the constant pattern of, 1111010000, and is used by the Receive E3 Framer block to acquire and maintain Frame Synchronization with the incoming E3 frames.
- The A (or Alarm) Bit.
- The N (or National) Bit.
- The BIP-4 Bits (if configured).

The frame repetition rate for this type of E3 frame is 22375 times per second, thereby resulting in the standard E3 bit rate of 34.368 Mbps. Figure 85 presents an illustration of the E3, ITU-T G.751 Frame Format.

FIGURE 85. ILLUSTRATION OF THE E3, ITU-T G.751 FRAMING FORMAT.



5.1.1 Definition of the Overhead Bits

Each of these Overhead Bits are further defined below.Frame Alignment Signaling (FAS) Pattern Bits

The first 10 bits, within each E3, ITU-T G.751 frame are known as the FAS (or Framing Alignment Signaling) bits. The Receive E3 Framer block, while trying to acquire or maintain framing synchronization with its incoming E3 frames, will attempt to locate the FAS bits. The FAS pattern is assigned the value, 1111010000.

5.1.1.1 *The A (Alarm) Bit*

The A bit typically functions as a FERF (Far-End Receive Failure) indicator bit. However, if the user configures the XRT72L50 Framer IC to transmit and receive E3 frames which are carrying the BIP-4 value (located at the end of a given E3 frame), then this bit will also function as the FEBE indicator bit. A detailed discussion on the practical use of the A bit is presented in Section 5.0. Each of these roles of the A bit are briefly discussed below.

The A Bit Functioning as the FERF bit-field

If the Receive E3 Framer block (at a Local Terminal) is experiencing problems receiving E3 frame data from a Remote Terminal (e.g., an LOS, OOF or AIS condition), then it will inform the Remote Terminal Equipment of this fact by commanding the Local Transmit E3 Framer block to set the A bit-field, within the next outbound E3 frame, to “1”. The Local Transmit E3 Framer block will continue to set the A bit-field (within the subsequent outbound E3 frames) to “1” until the Receive E3 Framer block no longer experiences problems in receiving the E3 frame data. If the Remote Terminal Equipment receives a certain number of consecutive E3 frames, with the A bit-field set to “1”, then the Remote Terminal Equipment will interpret this signaling as an indication of a Far-End Receive Failure (e.g., a problem with the Local Terminal Equipment).

Conversely, if the Receive E3 Framer block (at a Local Terminal Equipment) is not experiencing any problems receiving E3 frame data from a Remote Terminal Equipment, then it will also inform the Remote Terminal Equipment of this fact by commanding the Local Transmit E3 Framer block to set the A bit-field within an outbound E3 frame (which is destined for the Remote Terminal) to “0”. The Remote Terminal Equipment will interpret this form of signaling as an indication of a normal operation.

A detailed discussion into the practical use of the A bit-field is presented in Section 5.0.

5.1.1.2 *The N Bit*

The N bit is typically used to transport PMDL (Path Maintenance Data Link) information, from one terminal to the next. However, the N bit-field can also be used to transport a proprietary data link, if configured according.

A detailed discussion into the practical use of the N-bit field is presented in Section 5.0.

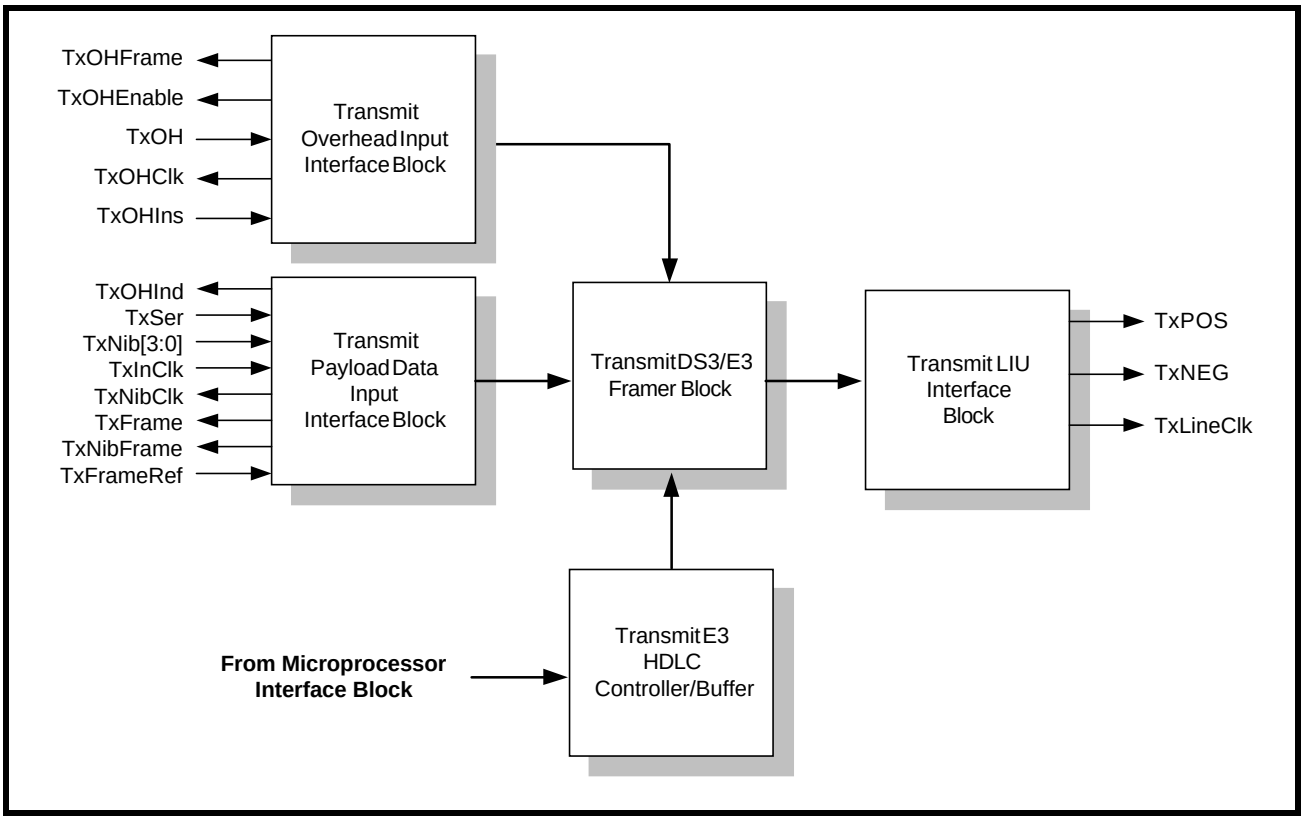
5.2 *The Transmit Section of the XRT72L50 (E3, ITU-T G.751 Mode Operation)*

When the XRT72L50 has been configured to operate in the E3, ITU-T G.751 Mode, the Transmit Section of the XRT72L50 consists of the following functional blocks.

- Transmit Payload Data Input Interface block
- Transmit Overhead Data Input Interface block
- Transmit E3 Framer block
- Transmit HDLC Controller block
- Transmit LIU Interface block

Figure 86 presents a simple illustration of the Transmit Section of the XRT72L50 Framer IC.

FIGURE 86. THE XRT72L50 TRANSMIT SECTION CONFIGURED TO OPERATE IN THE E3 MODE

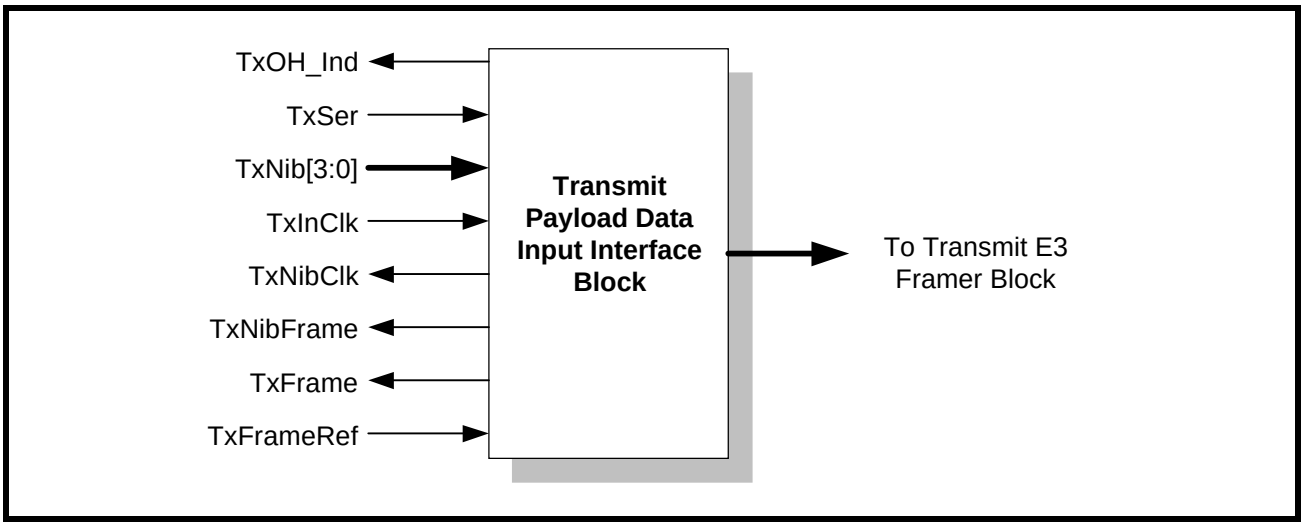


Each of these functional blocks will be discussed in detail in this document.

5.2.1 The Transmit Payload Data Input Interface Block

Figure 87 presents a simple illustration of the Transmit Payload Data Input Interface block.

FIGURE 87. THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK



Each of the input and output pins of the Transmit Payload Data Input Interface are listed in Table 43 and described below. The exact role that each of these inputs and output pins assume, for a variety of operating scenarios are described throughout this section.

TABLE 43: LISTING AND DESCRIPTION OF THE PINS ASSOCIATED WITH THE TRANSMIT PAYLOAD DATA INPUT INTERFACE

SIGNAL NAME	TYPE	DESCRIPTION
TxSer	Input	**Transmit Serial Payload Data Input Pin:** If the user opts to operate the XRT72L50 in the serial mode, then the Terminal Equipment is expected to apply the payload data (that is to be transported via the outbound E3 data stream) to this input pin. The XRT72L50 will sample the data that is at this input pin upon the rising edge of either the RxOutClk or the TxInClk signal (whichever is appropriate). ***NOTE:*** *This signal is only active if the NibIntf input pin is pulled "Low".*
TxNib[3:0]	Input	**Transmit Nibble-Parallel Payload Data Input pins:** If the user opts to operate the XRT72L50 in the Nibble-Parallel mode, then the Terminal Equipment is expected to apply the payload data (that is to be transported via the outbound E3 data stream) to these input pins. The XRT72L50 will sample the data that is at these input pins upon the rising edge of the TxNibClk signal. ***NOTE:*** *These pins are only active if the NibIntf input pin is pulled "High".*
TxInClk	Input	**Transmit Section Timing Reference Clock Input pin:** The Transmit Section of the XRT72L50 can be configured to use this clock signal as the Timing Reference. If the user has made this configuration selection, then the XRT72L50 will use this clock signal to sample the data on the TxSer input pin. ***NOTE:*** *If this configuration is selected, then a 34.368 MHz clock signal must be applied to this input pin.*
TxNibClk	Output	**Transmit Nibble Mode Output** If the user opts to operate the XRT72L50 in the Nibble-Parallel mode, then the XRT72L50 will derive this clock signal from the selected Timing Reference for the Transmit Section of the chip (e.g., either the TxInClk or the RxLineClk signals). The XRT72L50 will use this signal to sample the data on the TxNib[3:0] input pins.
TxOHInd	Output	**Transmit Overhead Bit Indicator Output:** This output pin will pulse "High" one-bit period prior to the time that the Transmit Section of the XRT72L50 will be processing an Overhead bit. The purpose of this output pin is to warn the Terminal Equipment that, during the very next bit-period, the XRT72L50 is going to be processing an Overhead bit and will be ignoring any data that is applied to the TxSer input pin.
TxFrame	Output	**Transmit End of Frame Output Indicator:** The Transmit Section of the XRT72L50 will pulse this output pin "High" (for one bit-period), when the Transmit Payload Data Input Interface is processing the last bit of a given E3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new E3 frame to the XRT72L50 (e.g., to permit the XRT72L50 to maintain Transmit E3 framing alignment control over the Terminal Equipment).
TxFrameRef	Input	**Transmit Frame Reference Input:** The XRT72L50 permits the user to configure the Transmit Section to use this input pin as a frame reference. If the user makes this configuration selection, then the Transmit Section will initiate its transmission of a new E3 frame, upon the rising edge of this signal. The purpose of this input pin is to permit the Terminal Equipment to maintain Transmit E3 Framing alignment control over the XRT72L50.
TxNibFrame	Output	**Transmit Frame Boundary Indicator - Nibble/Parallel Interface:** This output pin pulses "High" when the last nibble of a given DS3 or E3 frame is expected at the TxNib[3:0] input pins. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame to the XRT72L50.

Operation of the Transmit Payload Data Input Interface

The Transmit Terminal Input Interface is extremely flexible, in that it permits the user to make the following configuration options.

- The Serial or the Nibble-Parallel Interface Mode

- The Loop-Timing or the TxInClk (Local Timing) Mode

Further, if the XRT72L50 has been configured to operate in the Local-Timing mode, then the user has two additional options.

- The XRT72L50 is the Frame Master (e.g., it dictates when the Terminal Equipment will initiate the transmission of data within a new E3 frame).
- The XRT72L50 is the Frame Slave (e.g., the Terminal Equipment will dictate when the XRT72L50 initiates the transmission of a new E3 frame).

Given these three set of options, the Transmit Terminal Input Interface can be configured to operate in one of the six (6) following modes.

- Mode 1 - Serial/Loop-Timed Mode
- Mode 2 - Serial/Local-Timed/Frame Slave Mode
- Mode 3 - Serial/Local-Timed/Frame Master Mode
- Mode 4 - Nibble/Loop-Timed Mode
- Mode 5 - Nibble/Local-Timed/Frame Slave Mode
- Mode 6 - Nibble/Local-Timed/Frame Master Mode

Each of these modes are described, in detail, below.

5.2.1.1 *Mode 1 - The Serial/Loop-Timing Mode The Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will behave as follows.

A. Loop-Timing (Uses the RxLineClk signal as the Timing Reference)

Since the XRT72L50 is configured to operate in the loop-timed mode, the Transmit Section of the XRT72L50 will use the RxLineClk input clock signal (e.g., the Recovered Clock signal, from the LIU) as its timing source. When the XRT72L50 is operating in this mode it will do the following.

1. It will ignore any signal at the TxInClk input pin.
2. The XRT72L50 will output a 34.368MHz clock signal via the RxOutClk output pin. This clock signal functions as the Transmit Payload Data Input Interface block clock signal.
3. The XRT72L50 will use the rising edge of the RxOutClk signal to latch in the data residing on the TxSer input pin.

B. Serial Mode

The XRT72L50 will accept the E3 payload data from the Terminal Equipment, in a serial-manner, via the TxSer input pin The Transmit Payload Data Input Interface will latch this data into its circuitry, on the rising edge of the RxOutClk output clock signal.

C. Delineation of outbound E3 frames

The XRT72L50 will pulse the TxFrame output pin "High" for one bit-period coincident with the XRT72L50 processing the last bit of a given E3 frame.

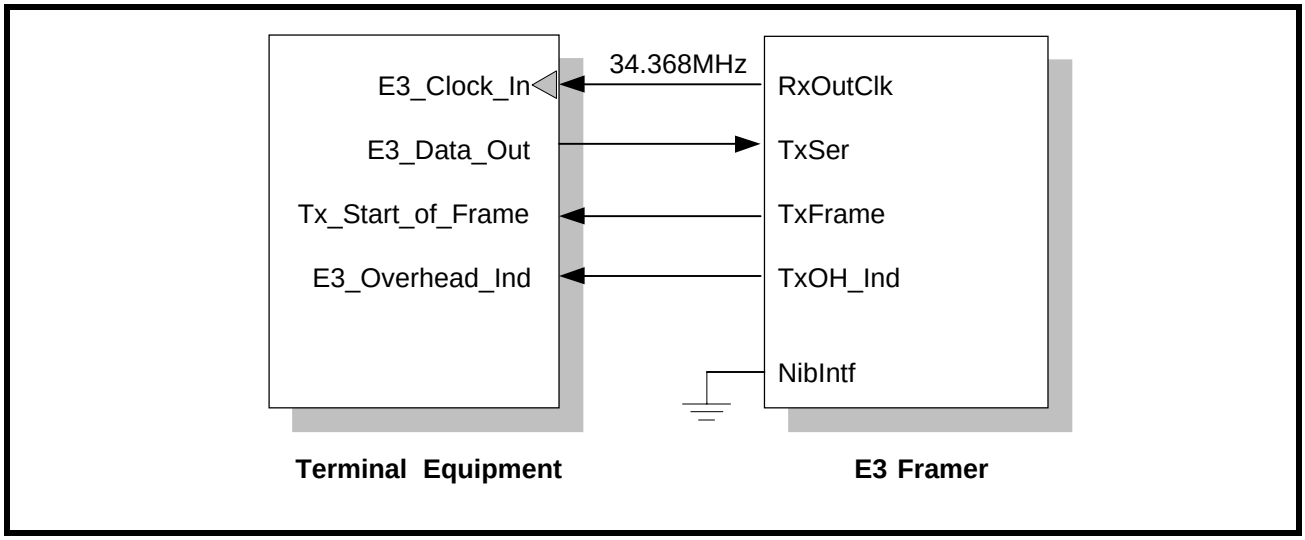
D. Sampling of Payload Data, from the Terminal Equipment

In Mode 1, the XRT72L50 will sample the data at the TxSer input, on the rising edge of RxOutClk.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 1 Operation

Figure 88 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 1 operation.

FIGURE 88. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 1 (SERIAL/LOOP-TIMED) OPERATION



Mode 1 Operation of the Terminal Equipment

When the XRT72L50 is operating in this mode, it will function as the source of the 34.368MHz clock signal. This clock signal will be used as the Terminal Equipment Interface clock by both the XRT72L50 IC and the Terminal Equipment.

The Terminal Equipment will serially output the payload data of the outbound E3 data stream via its E3_Data_Out pin. The Terminal Equipment will update the data on the E3_Data_Out pin upon the rising edge of the 34.368 MHz clock signal, at its E3_Clock_In input pin (as depicted in Figure 88 and Figure 89).

The XRT72L50 will latch the outbound E3 data stream (from the Terminal Equipment) on the rising edge of the RxOutClk signal.

The XRT72L50 will indicate that it is processing the last bit, within a given outbound E3 frame, by pulsing its TxFrame output pin "High" for one bit-period. When the Terminal Equipment detects this pulse at its Tx_Start_of_Frame input, it is expected to begin transmission of the very next outbound E3 frame to the XRT72L50 via the E3_Data_Out (or TxSer pin).

Finally, the XRT72L50 will indicate that it is about to process an overhead bit by pulsing the TxOH_Ind output pin "High" one bit period prior to its processing of an OH (Overhead) bit. In Figure 88, the TxOH_Ind output pin is connected to the E3_Overhead_Ind input pin of the Terminal Equipment. Whenever the E3_Overhead_Ind pin is pulsed "High" the Terminal Equipment is expected to not transmit a E3 payload bit upon the very next clock edge. Instead, the Terminal Equipment is expected to delay its transmission of the very next payload bit, by one clock cycle.

The behavior of the signals, between the XRT72L50 and the Terminal Equipment, for E3 Mode 1 operation is illustrated in Figure 88.

Inserting the A and N bits into the outbound E3 frames via the Transmit Payload Data Input Interface block

The XRT72L50 DS3/E3 Framer permits the Terminal Equipment to insert its own values for the A and/or N bits, into the outbound E3 frame, via the Transmit Payload Data Input Interface block. If the user desires to do this, the XRT72L50 Framer IC must be configured to accept the Terminal Equipment's value for the A and N bits, by writing to appropriate data into the TxASourceSel[1:0] and TxNSourceSel[1:0] bit-fields, within the TxE3 Configuration Register (Address =0x30), as illustrated below.

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx BIP-4 Enable	TxASourceSel[1:0]		TxNSourceSel[1:0]		Tx AIS Enable	Tx LOS Enable	Tx FAS Source Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	X	X	X	X	0	0	0

Configuring the Transmit Payload Data Input Interface block to accept the A Bits from the Terminal Equipment

If the user wishes to configure the Transmit Payload Data Input Interface block to accept the A bits from the Terminal Equipment, then the user must write the value “10” into the TxASourceSel[1:0] bit-fields. Once the user does this, then any value, which resides on the TxSer input pin, when the A bit is being processed by the Transmit Section will be inserted into the A bit-field within the very next outbound E3 frame.

For completeness, the relationship between the contents of the TxASourceSel[1:0] bits and the resulting source of the A bit is listed below.

Bit 6, 5, TxASourceSel[1:0]

These two Read/Write bit-fields combine to specify the source of the A-bit, within each outbound E3 frame. The relationship between these two bit-fields and the resulting source of the A Bit is tabulated below.

TXASOURCESEL[1:0]	SOURCE OF A BIT
00	TxE3 Service Bits Register (Address = 0x35)
01	Transmit Overhead Data Input Interface
10	Transmit Payload Data Input Interface
11	Functions as a FEBE (Far-End-Block Error) bit-field. This bit-field is set to "0", if the Near-End Receive Section (within this chip) detects no BIP-4 Errors within the incoming E3 frames. This bit-field is set to "1", if the Near-End Receive Section (within this chip) detects a BIP-4 Error within the incoming E3 frame.

Configuring the Transmit Payload Data Input Interface block to accept the N Bits from the Terminal Equipment, then the user must write the value “11” into the TxNSourceSel[1:0] bit-fields. Once the user does this, then any value, which resides on the TxSer input pin, when the N bit is being processed by the Transmit Section will be inserted into the N bit-field within the very next outbound E3 frame.

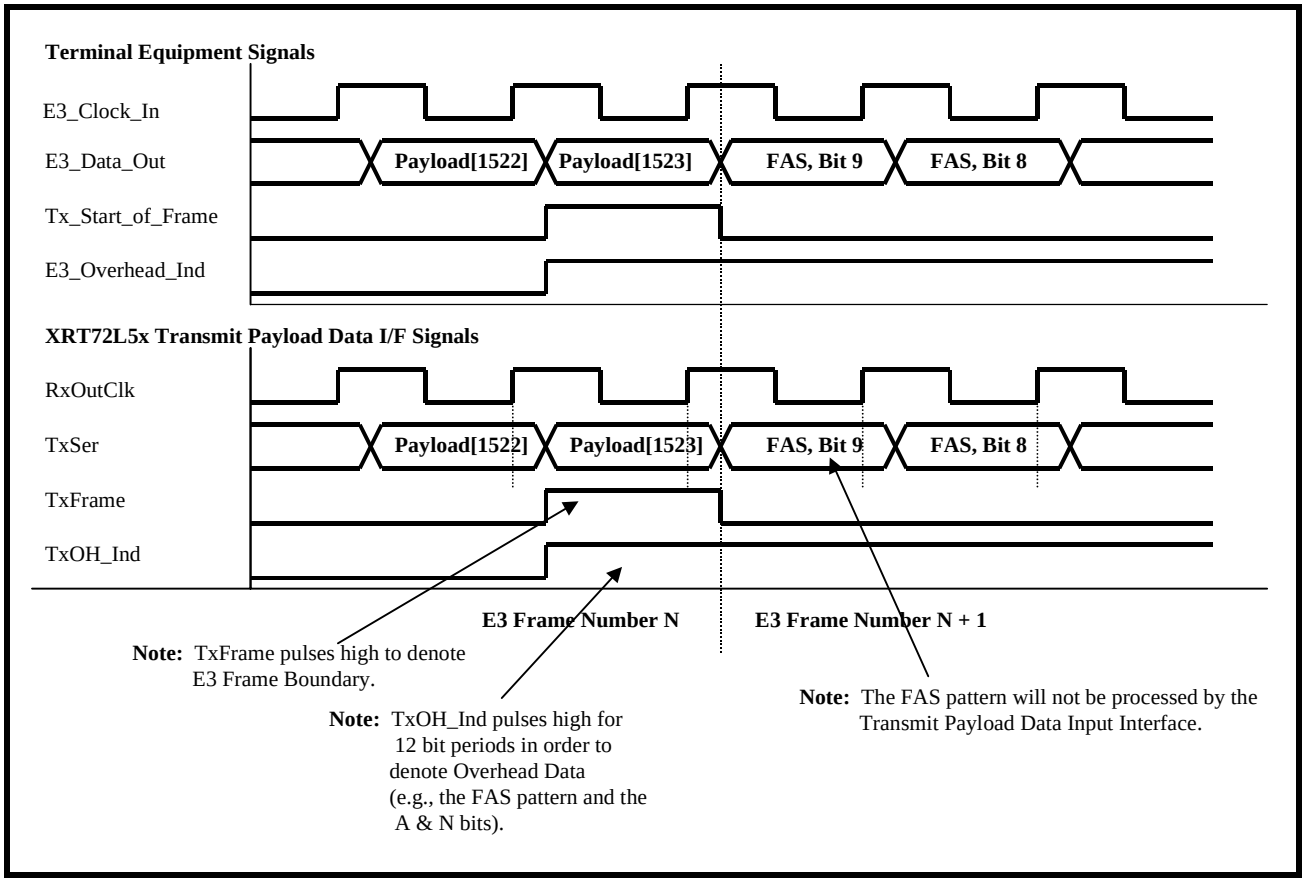
For completeness, the relationship between the contents of the TxNSourceSel[1:0] bits and the resulting source of the N bit is listed below.

Bits 4, 3, TxNSourceSel[1:0]

These two Read/Write bit-fields combine to specify the source of the N-bit, within each outbound E3 frame. The relationship between these two bit-fields and the resulting source of the N Bit is tabulated below.

TxNSourceSel[1:0]	Source of N Bit
00	TxE3 Service Bits Register (Address = 0x35)
01	Transmit Overhead Data Input Interface
10	Transmit LAPD Controller
11	Transmit Payload Data Input Interface.

Figure 89. Behavior of the Terminal Interface signals between the XRT72L50 Transmit Payload Data Input Interface block and the Terminal Equipment (for Mode 1 Operation)



How to configure the XRT72L50 into the Serial/Loop-Timed/Non-Overhead Interface Mode

1. Set the NibIntf input pin "Low".
2. Set the TimRefSel[1:0] bit fields (within the Framer Operating Mode Register) to "00", as illustrated below.

Framer Operating Mode Register (Address = 0x00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit2	Bit 1	Bit 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	0

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 88.

5.2.1.2 *Mode 2 - The Serial/Local-Timed/Frame-Slave Mode Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will function as follows.

A. Local-Timed - Uses the TxInClk signal as the Timing Reference

In this mode, the Transmit Section of the XRT72L50 will use the TxInClk signal as its timing reference.

B. Serial Mode

The XRT72L50 will receive the E3 payload data, in a serial manner, via the TxSer input pin. The Transmit Payload Data Input Interface (within the XRT72L50) will latch this data into its circuitry, on the rising edge of the TxInClk input clock signal.

C. Delineation of outbound E3 frames (Frame Slave Mode)

The Transmit Section of the XRT72L50 will use the TxInClk input as its timing reference, and will use the TxFrameRef input signal as its framing reference. In other words, the Transmit Section of the XRT72L50 will initiate frame generation upon the rising edge of the TxFrameRef input signal).

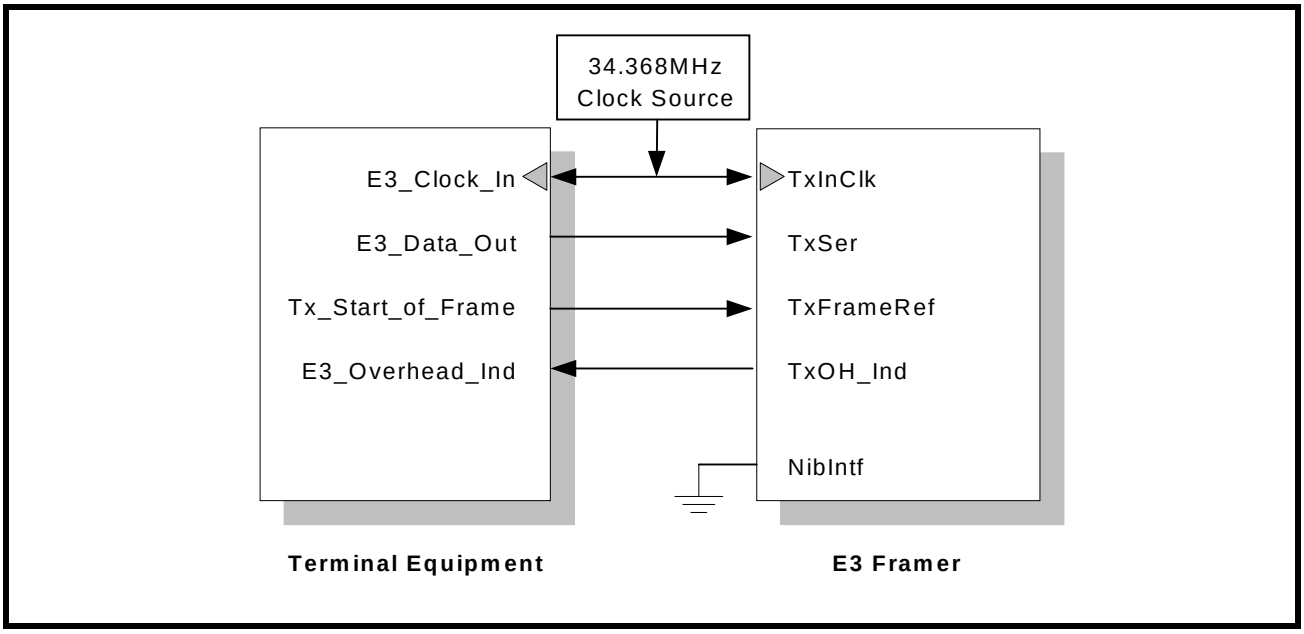
D. Sampling of payload data, from the Terminal Equipment

In Mode 2, the XRT72L50 will sample the data, at the TxSer input pin, on the rising edge of TxInClk.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 2 Operation

Figure 90 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 2 operation.

FIGURE 90. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 2 (SERIAL/LOCAL-TIMED/FRAME-SLAVE) OPERATION



Mode 2 Operation of the Terminal Equipment

As shown in Figure 90, both the Terminal Equipment and the XRT72L50 will be driven by an external 34.368MHz clock signal. The Terminal Equipment will receive the 34.368MHz clock signal via its E3_Clock_In input pin, and the XRT72L50 Framer IC will receive the 34.368MHz clock signal via the TxInClk input pin.

The Terminal Equipment will serially output the payload data of the outbound E3 data stream, via the E3_Data_Out output pin, upon the rising edge of the signal at the E3_Clock_In input pin.

NOTE: *The E3_Data_Out output pin of the Terminal Equipment is electrically connected to the TxSer input pin*

The XRT72L50 Framer will latch the data residing on the TxSer input line on the rising edge of the TxInClk signal.

In this case, the Terminal Equipment has the responsibility of providing the framing reference signal by pulsing its Tx_Start_of_Frame output signal (and in turn, the TxFrameRef input pin of the XRT72L50), "High" for one-bit period, coincident with the first bit of a new E3 frame. Once the XRT72L50 detects the rising edge of the input at its TxFrameRef input pin, it will begin generation of a new E3 frame.

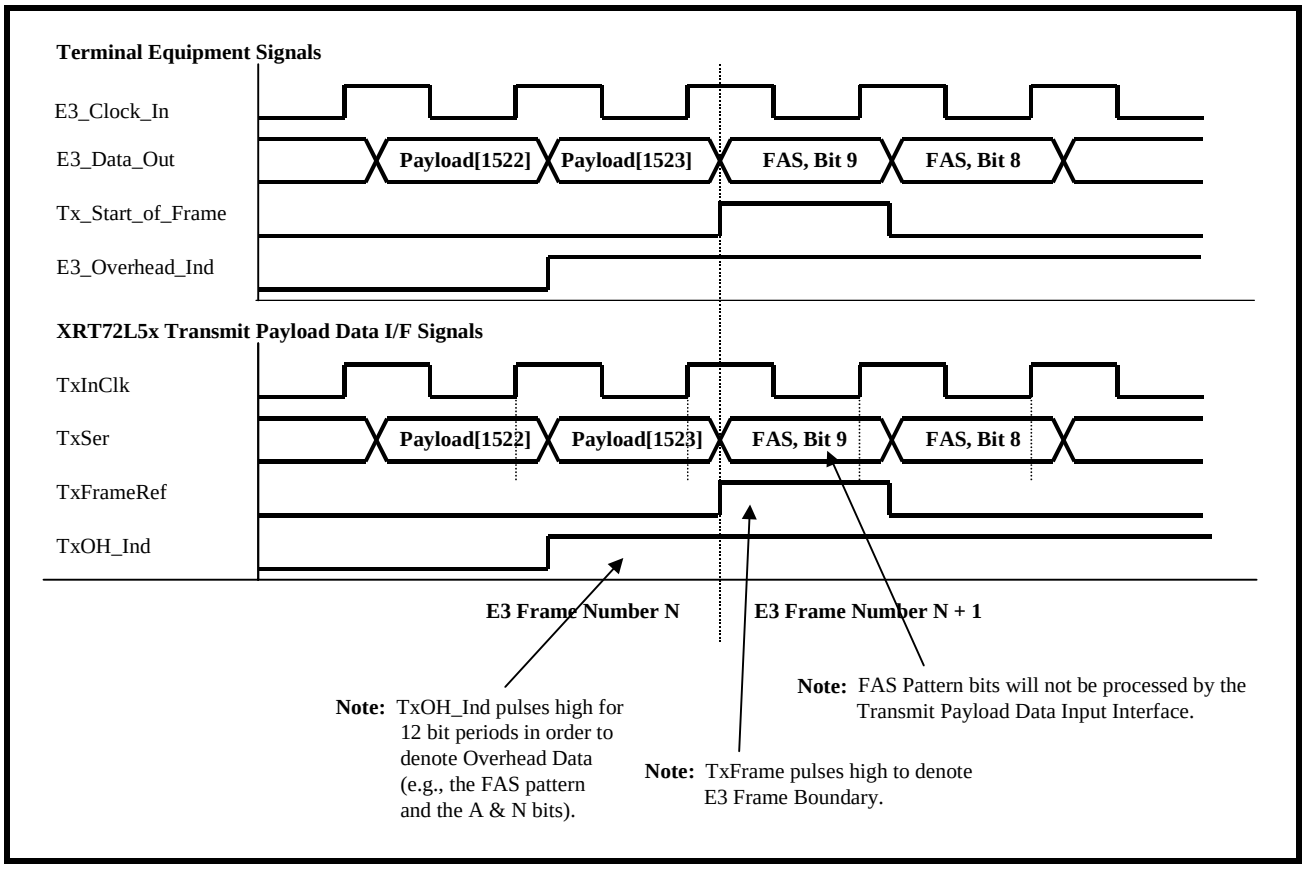
NOTES:

1. *In this case, the Terminal Equipment is controlling the start of Frame Generation, and is therefore referred to as the Frame Master. Conversely, since the XRT72L50 does not control the generation of a new E3 frame, but is rather driven by the Terminal Equipment, the XRT72L50 is referred to as the Frame Slave.*
2. *If the user opts to configure the XRT72L50 to operate in Mode 2, it is imperative that the Tx_Start_of_Frame (or TxFrameRef) signal is synchronized to the TxInClk input clock signal.*

Finally, the XRT72L50 will pulse its TxOH_Ind output pin, one bit-period prior to it processing a given overhead bit, within the outbound E3 frame. Since the TxOH_Ind output pin of the XRT72L50 is electrically connected to the E3_Overhead_Ind whenever the XRT72L50 pulses the TxOH_Ind output pin "High", it will also be driving the E3_Overhead_Ind input pin (of the Terminal Equipment) "High". Whenever the Terminal Equipment detects this pin toggling "High", it should delay transmission of the very next E3 frame payload bit by one clock cycle.

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Mode 2 Operation is illustrated in Figure 91.

FIGURE 91. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (MODE 2 OPERATION)



How to configure the XRT72L50 to operate in this mode.

1. Set the NibIntf input pin "Low".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "01" as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	1

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 90.

5.2.1.3 *Mode 3 - The Serial/Local-Timed/Frame-Master Mode Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will function as follows.

A. Local-Timed - Uses the TxInClk signal as the Timing Reference

In this mode, the Transmit Section of the XRT72L50 will use the TxInClk signal as its timing reference.

B. Serial Mode

The XRT72L50 will receive the E3 payload data, in a serial manner, via the TxSer input pin. The Transmit Payload Data Input Interface (within the XRT72L50) will latch this data into its circuitry, on the rising edge of the TxInClk input clock signal.

C. Delineation of outbound E3 frames (Frame Master Mode)

The Transmit Section of the XRT72L50 will use the TxInClk signal as its timing reference, and will initiate E3 frame generation, asynchronously with respect to any externally applied signal. The XRT72L50 will pulse its TxFrame output pin "High" whenever its it processing the very last bit-field within a given E3 frame.

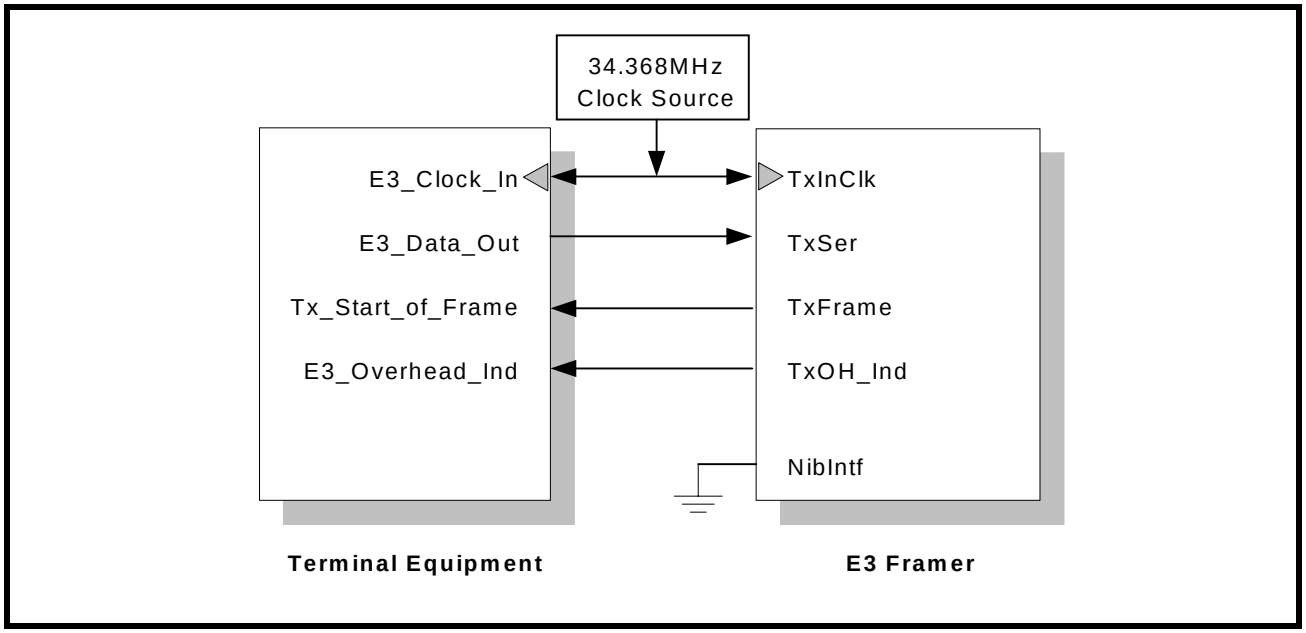
D. Sampling of payload data, from the Terminal Equipment

In Mode 3, the XRT72L50 will sample the data, at the TxSer input pin, on the rising edge of TxInClk.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 3 Operation

Figure 92 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 3 operation.

FIGURE 92. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 3 (SERIAL/LOCAL-TIMED/FRAME-MASTER) OPERATION



Mode 3 Operation of the Terminal Equipment

In Figure 92, both the Terminal Equipment and the XRT72L50 are driven by an external 34.368 MHz clock signal. This clock signal is connected to the E3_Clock_In input of the Terminal Equipment and the TxInClk input pin of the XRT72L50.

The Terminal Equipment will serially output the payload data on its E3_Data_Out output pin, upon the rising edge of the signal at the E3_Clock_In input pin. Similarly, the XRT72L50 will latch the data, residing on the TxSer input pin, on the rising edge of TxInClk.

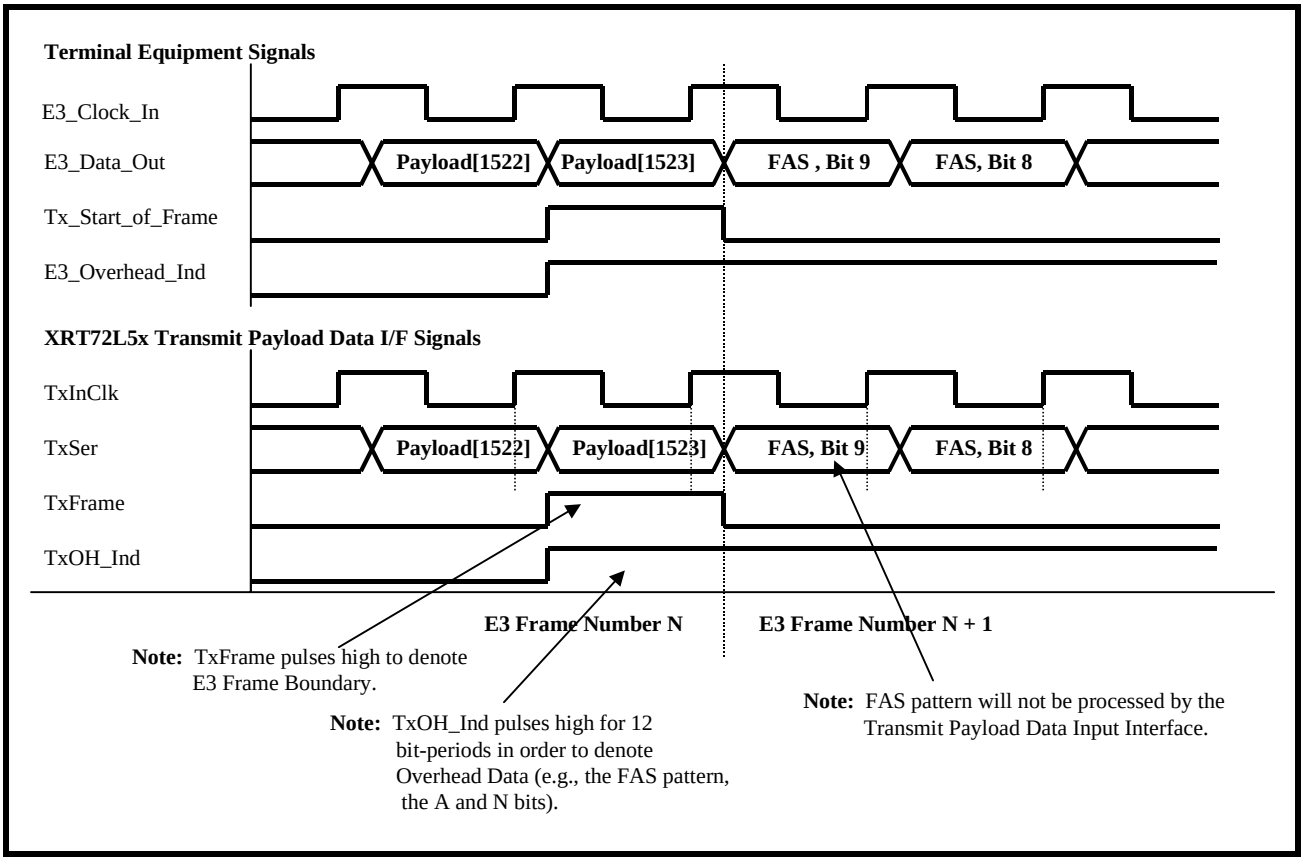
The XRT72L50 will pulse the TxFrame output pin "High" for one bit-period, coincident while it is processing the last bit-field within a given outbound E3 frame. The Terminal Equipment is expected to monitor the TxFrame signal (from the XRT72L50) and to place the first bit, within the very next outbound E3 frame on the TxSer input pin.

NOTE: *In this case, the XRT72L50 dictates exactly when the very next E3 frame will be generated. The Terminal Equipment is expected to respond appropriately by providing the XRT72L50 with the first bit of the new E3 frame, upon demand. Hence, in this mode, the XRT72L50 is referred to as the Frame Master and the Terminal Equipment is referred to as the Frame Slave.*

Finally, the XRT72L50 will pulse its TxOH_Ind output pin, one bit-period prior to it processing a given overhead bit, within the outbound E3 frame. Since the TxOH_Ind output pin (of the XRT72L50) is electrically connected to the E3_Overhead_Ind whenever the XRT72L50 pulses the TxOH_Ind output pin "High", it will also be driving the E3_Overhead_Ind input pin (of the Terminal Equipment) "High". Whenever the Terminal Equipment detects this pin toggling "High", it should delay transmission of the very next E3 frame payload bit by one clock cycle.

The behavior of the signal between the XRT72L50 and the Terminal Equipment for E3 Mode 3 Operation is illustrated in Figure 93.

FIGURE 93. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (E3 MODE 3 OPERATION)



How to configure the XRT72L50 to operate in this mode.

1. Set the NibIntf input pin "Low".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "01" as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	1

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 92.

5.2.1.4 *Mode 4 - The Nibble-Parallel/Loop-Timed Mode Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will behave as follows.

A. Looped Timing (Uses the RxLineClk as the Timing Reference)

In this mode, the Transmit Section of the XRT72L50 will use the RxLineClk signal as its timing reference. When the XRT72L50 is operating in the Nibble-Mode, it will internally divide the RxLineClk signal, by a factor of four (4) and will output this signal via the TxNibClk output pin.

B. Nibble-Parallel Mode

The XRT72L50 will accept the E3 payload data, from the Terminal Equipment in a nibble-parallel manner, via the TxNib[3:0] input pins. The Transmit Terminal Equipment Input Interface block will latch this data into its circuitry, on the rising edge of the TxNibClk output signal.

C. Delineation of the outbound E3 frames

The XRT72L50 will pulse the TxNibFrame output pin "High" for one bit-period coincident with the XRT72L50 processing the last nibble of a given E3 frame.

D. Sampling of payload data, from the Terminal Equipment

In Mode 4, the XRT72L50 will sample the data, at the TxNib[3:0] input pins, on the third rising edge of the RxOutClk clock signal, following a pulse in the TxNibClk signal (see Figure 95).

NOTE: *The TxNibClk signal, from the XRT72L50 operates nominally at 8.592 MHz (e.g., 34.368 MHz divided by 4).*

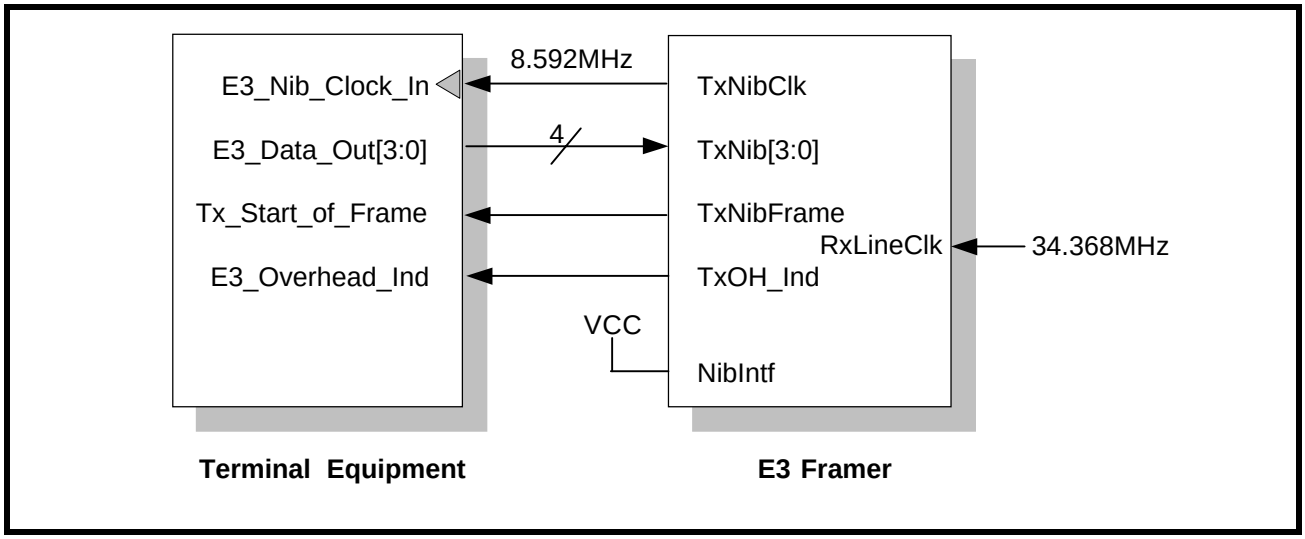
The E3 Frame consists of 1536 bits or 384 nibbles. Therefore, the XRT72L50 will supply 384 TxNibClk pulses between the rising edges of two consecutive TxNibFrame pulses. The E3 Frame repetition rate is 22.375kHz. Hence, 384 TxNibClk pulses for each E3 frame period amounts to TxNibClk running at approximately 8.592 MHz. The method by which the 384 TxNibClk pulses are distributed throughout the E3 frame period is presented below.

Nominally, the Transmit Section within the XRT72L50 will generate a TxNibClk pulse for every 4 RxOutClk (or TxInClk) periods.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 4 Operation

Figure 94 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 4 Operation.

FIGURE 94. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 4 (NIBBLE-PARALLEL/LOOP-TIMED) OPERATION



Mode 4 Operation of the Terminal Equipment

When the XRT72L50 is operating in this mode, it will function as the source of the 8.592MHz (e.g., the 34.368MHz clock signal divided by 4) clock signal, that will be used as the Terminal Equipment Interface clock by both the XRT72L50 and the Terminal Equipment.

The Terminal Equipment will output the payload data of the outbound E3 data stream via its E3_Data_Out[3:0] pins on the rising edge of the 8.592MHz clock signal at the E3_Nib_Clock_In input pin.

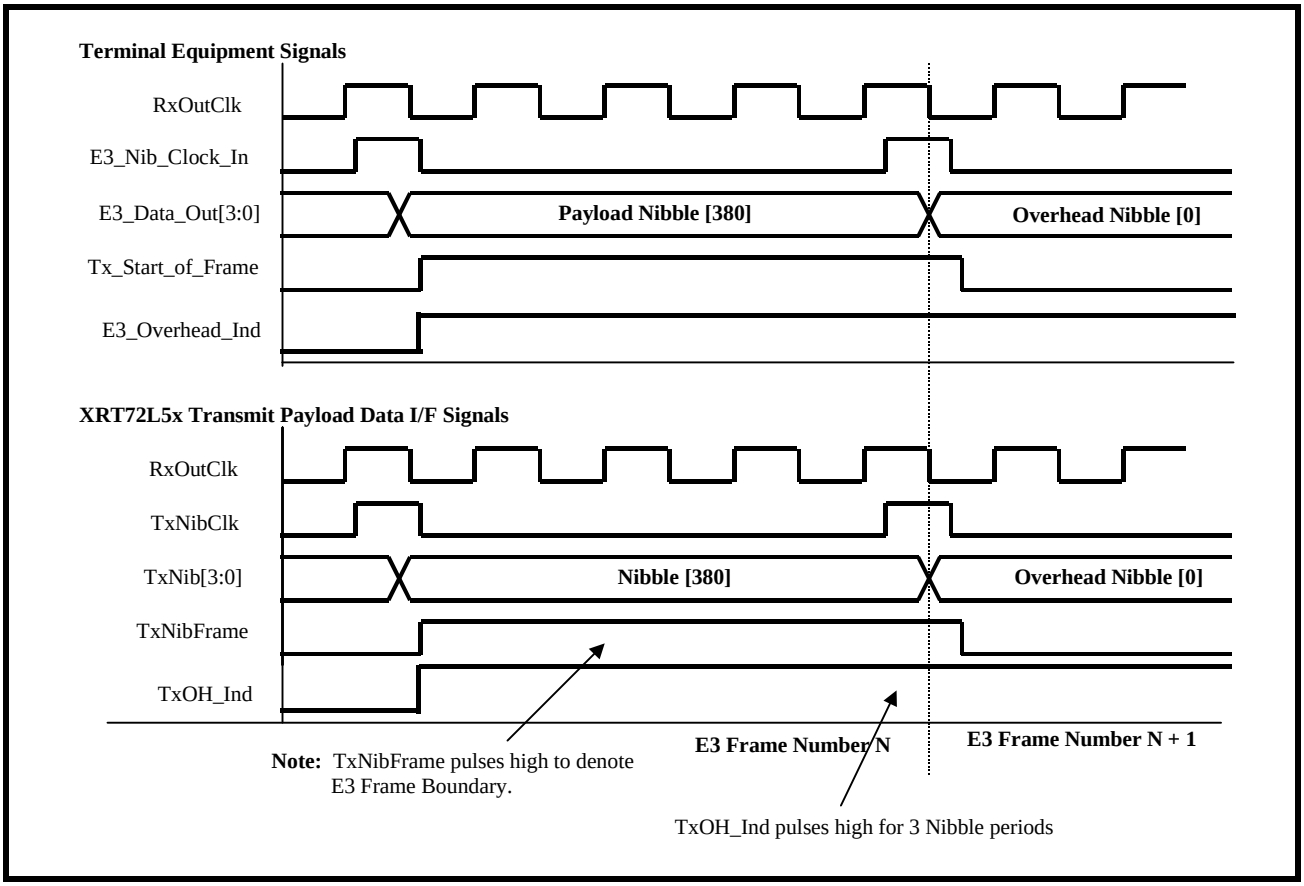
The XRT72L50 will latch the outbound E3 data stream (from the Terminal Equipment) on the rising edge of the TxNibClk output clock signal. The XRT72L50 will indicate that it is processing the last nibble, within a given E3

frame, by pulsing its TxNibFrame output pin "High" for one TxNibClk clock period. When the Terminal Equipment detects a pulse at its Tx_Start_of_Frame input pin, it is expected to transmit the first nibble, of the very next outbound E3 frame to the XRT72L50 via the E3_Data_Out[3:0] (or TxNib[3:0] pins).

Finally, for the Nibble-Parallel Mode operation, the XRT72L50 will pulse the TxOHInd output pin "High" for 3 nibble-periods (e.g., the 3 nibbles consisting of the 10 bit FAS pattern, the A and the N bits). The TxOHInd output pin will remain "Low" for the remainder of the frame period. The TxOHInd output pin will toggle "High" one-nibble period before the Transmit Section (of the Framer IC) processes the first four bits of the FAS pattern.

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Mode 4 Operation is illustrated in Figure 95.

FIGURE 95. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (MODE 4 OPERATION)



How to configure the XRT72L50 into Mode 4

1. Set the NibIntf input pin "High".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "00" as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	0

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 94.

NOTE: *The XRT72L50 Framer IC cannot support the Framer Local Loop-back Mode of operation, while operating in Mode 4. The user must configure the XRT72L50 Framer IC into any of the following modes prior to configuring the Framer Local Loop-back Mode operation.*

- Mode 2 - Serial/Local-Timed/Frame-Slave Mode
- Mode 3 - Serial/Local-Timed/Frame-Master Mode
- Mode 5 - Nibble-Parallel/Local-Timed/Frame-Slave Mode
- Mode 6 - Nibble-Parallel/Local-Timed/Frame-Master Mode.

For more detailed information on the Framer Local Loop-back Mode, please see Section 7.0.

5.2.1.5 *Mode 5 - The Nibble-Parallel/Local-Timed/Frame-Slave Interface Mode Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will function as follows:

A. Local-Timed - Uses the TxInClk signal as the Timing Reference

In this mode, the Transmit Section of the XRT72L50 will use the TxInClk signal at its timing reference. Further, the chip will internally divide the TxInClk clock signal by a factor of 4 and will output this divided clock signal via the TxNibClk output pin. The Transmit Terminal Equipment Input Interface block (within the XRT72L50) will use the rising edge of the TxNibClk signal, to latch the data, residing on the TxNib[3:0] into its circuitry.

B. Nibble-Parallel Mode

The XRT72L50 will accept the E3 payload data, from the Terminal Equipment, in a parallel manner, via the TxNib[3:0] input pins. The Transmit Terminal Equipment Input Interface will latch this data into its circuitry, on the rising edge of the TxNibClk output signal.

C. Delineation of outbound E3 Frames

The Transmit Section will use the TxInClk input signal as its timing reference and will use the TxFrameRef input signal as its Framing Reference (e.g., the Transmit Section of the XRT72L50 initiates frame generation upon the rising edge of the TxFrameRef signal).

D. Sampling of payload data, from the Terminal Equipment

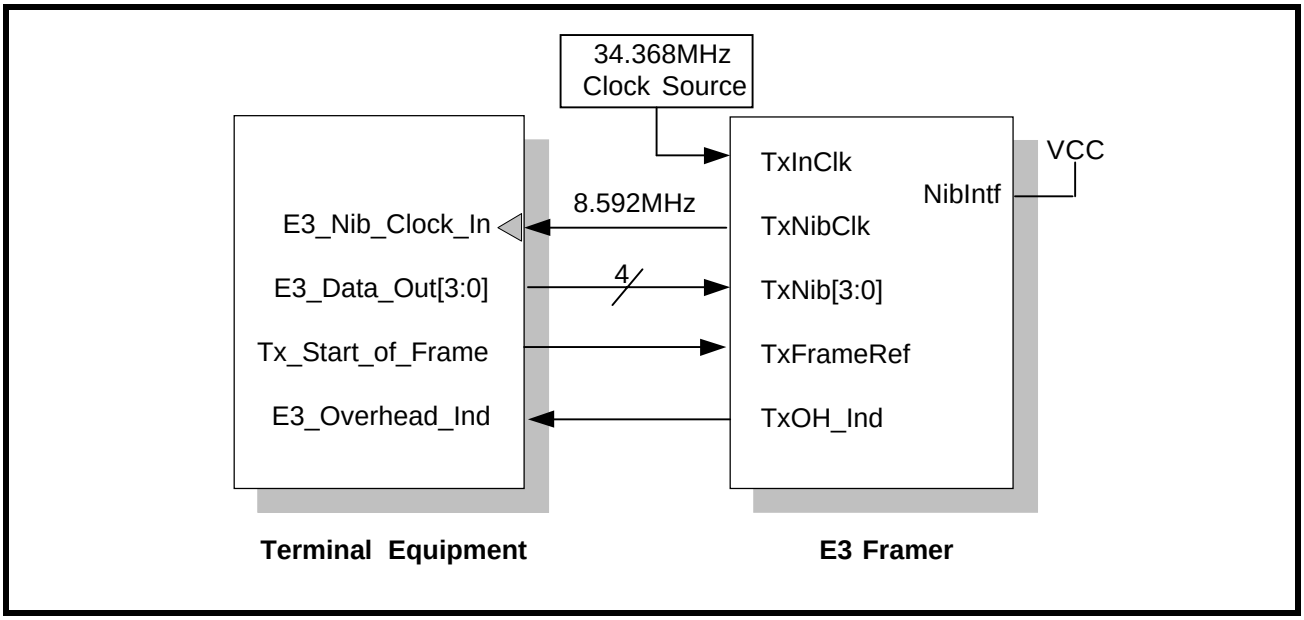
In Mode 5, the XRT72L50 will sample the data, at the TxNib[3:0] input pins, on the third rising edge of the TxInClk clock signal, following a pulse in the TxNibClk signal (see Figure 96).

NOTE: *The TxNibClk signal, from the XRT72L50 operates nominally at 8.592 MHz (e.g., 34.368 MHz divided by 4).*

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 5 Operation

Figure 96 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 5 Operation.

FIGURE 96. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 5 (NIBBLE-PARALLEL/LOCAL-TIMED/FRAME-SLAVE) OPERATION



Mode 5 Operation of the Terminal Equipment

In Figure 96 both the Terminal Equipment and the XRT72L50 will be driven by an external 8.592MHz clock signal. The Terminal Equipment will receive the 8.592MHz clock signal via the E3_Nib_Clock_In input pin. The XRT72L50 will output the 8.592MHz clock signal via the TxNibClk output pin.

The Terminal Equipment will serially output the data on the E3_Data_Out[3:0] pins, upon the rising edge of the signal at the E3_Clock_In input pin.

NOTE: *The E3_Data_Out[3:0] output pins of the Terminal Equipment is electrically connected to the TxNib[3:0] input pins.*

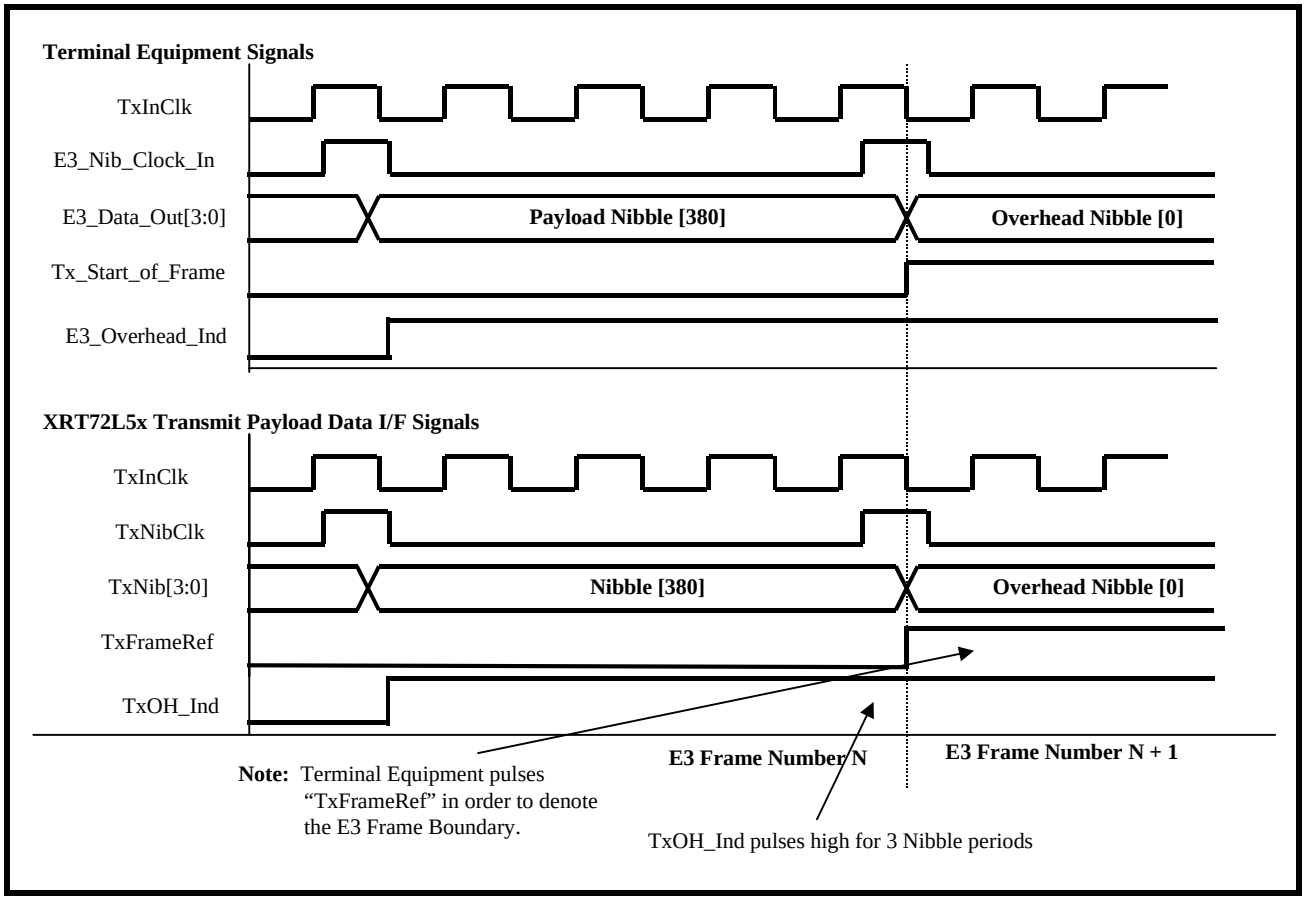
The XRT72L50 will latch the data, residing on the TxNib[3:0] input pins, on the rising edge of the TxNibClk signal.

In this case, the Terminal Equipment has the responsibility of providing the framing reference signal by pulsing the Tx_Start_of_Frame output pin (and in turn, the TxFrameRef input pin of the XRT72L50) "High" for one bit-period, coincident with the first bit of a new E3 frame. Once the XRT72L50 detects the rising edge of the input at its TxFrameRef input pin, it will begin generation of a new E3 frame.

Finally, the XRT72L50 will always internally generate the Overhead bits, when it is operating in both the E3 and Nibble-parallel modes. The XRT72L50 will pull the TxOHInd input pin "Low".

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Mode 5 Operation is illustrated in Figure 97.

FIGURE 97. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (E3, MODE 5 OPERATION)



How to configure the XRT72L50 into Mode 5

1. Set the NibIntf input pin "High".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "01" as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	1

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 96.

5.2.1.6 *4.2.1.6 Mode 6 - The Nibble-Parallel/Local-Timed/Frame-Master Interface Mode Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will function as follows:

A. Local-Timed - Uses the TxInClk signal as the Timing Reference

In this mode, the Transmit Section of the XRT72L50 will use the TxInClk signal at its timing reference. Further, the chip will internally divide the TxInClk clock signal by a factor of 4 and will output this divided clock signal via

the TxNibClk output pin. The Transmit Terminal Equipment Input Interface block (within the XRT72L50) will use the rising edge of the TxNibClk signal, to latch the data, residing on the TxNib[3:0] into its circuitry.

B. Nibble-Parallel Mode

The XRT72L50 will accept the E3 payload data, from the Terminal Equipment, in a parallel manner, via the TxNib[3:0] input pins. The Transmit Terminal Equipment Input Interface will latch this data into its circuitry, on the rising edge of the TxNibClk output signal.

C. Delineation of outbound E3 Frames

The Transmit Section will use the TxInClk input signal as its timing reference and will initiate the generation of E3 frames, asynchronous with respect to any external signal. The XRT72L50 will pulse the TxFrame output pin "High" whenever it is processing the last bit, within a given outbound E3 frame.

D. Sampling of payload data, from the Terminal Equipment

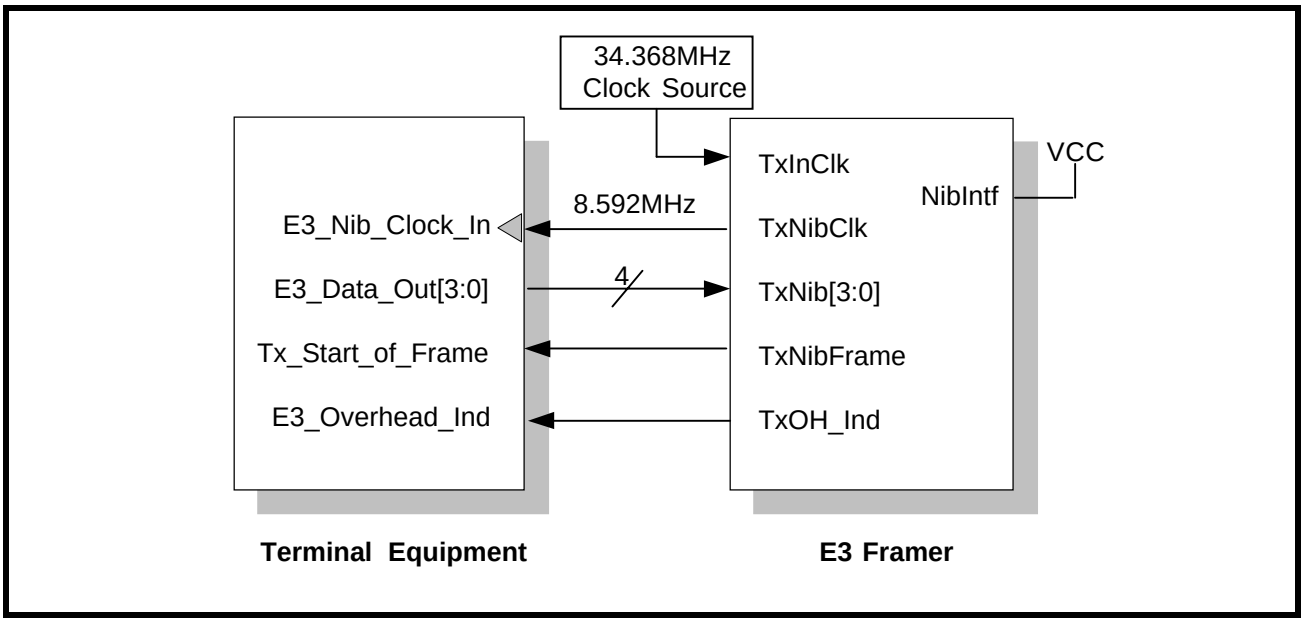
In Mode 6, the XRT72L50 will sample the data, at the TxNib[3:0] input pins, on the third rising edge of the TxInClk clock signal, following a pulse in the TxNibClk signal (see Figure 99).

NOTE: *The TxNibClk signal, from the XRT72L50 operates nominally at 8.592 MHz (e.g., 34.368 MHz divided by 4).*

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 6 Operation

Figure 98 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 6 Operation.

FIGURE 98. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 6 (NIBBLE-PARALLEL/LOCAL-TIMED/FRAME-MASTER) OPERATION



Mode 6 Operation of the Terminal Equipment

In Figure 98 both the Terminal Equipment and the XRT72L50 will be driven by an external 8.592MHz clock signal. The Terminal Equipment will receive the 8.592MHz clock signal via the E3_Nib_Clock_In input pin. The XRT72L50 will output the 8.592MHz clock signal via the TxNibClk output pin.

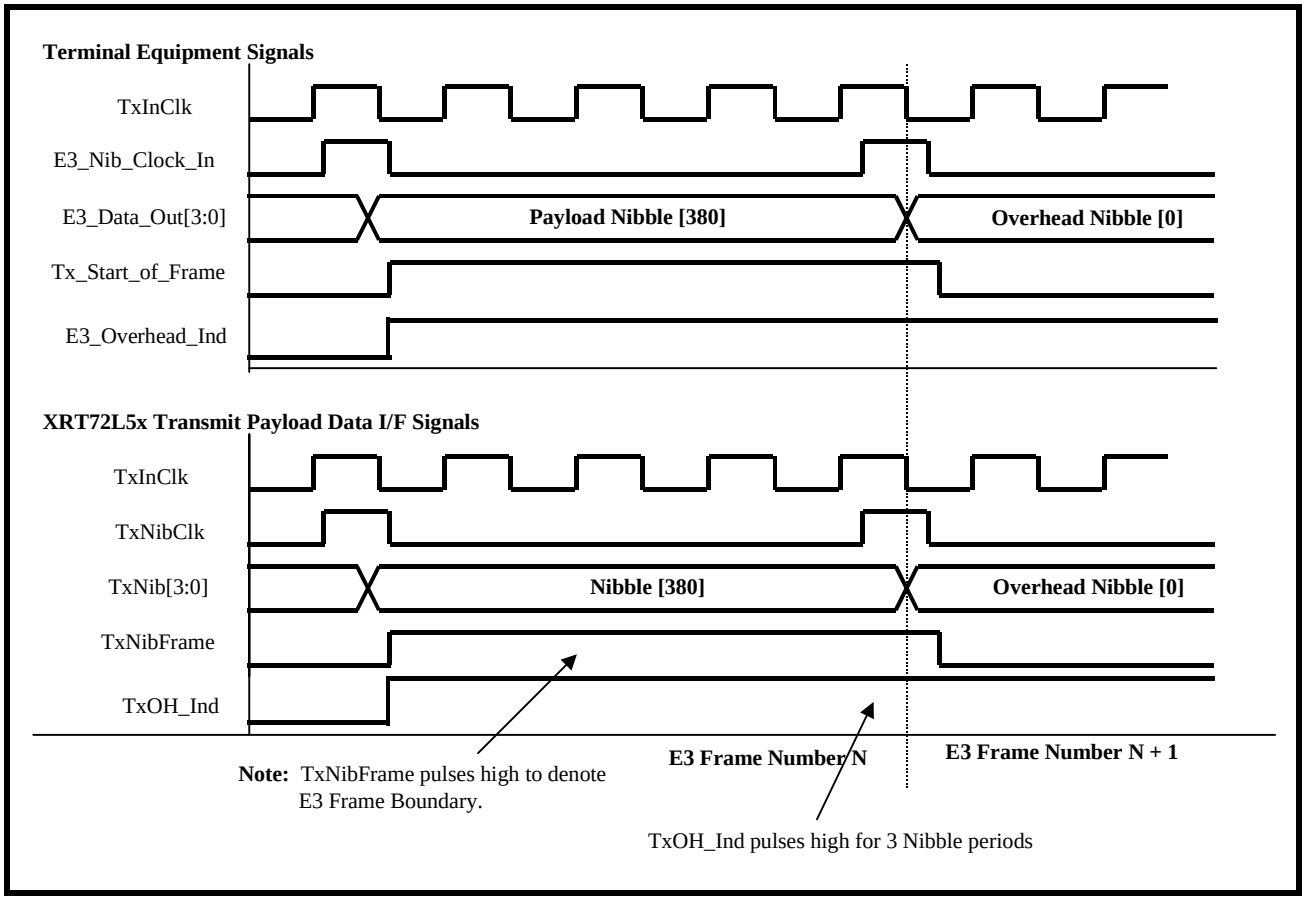
The Terminal Equipment will serially output the data on the E3_Data_Out[3:0] pins upon the rising edge of the signal at the E3_Clock_In input pin. The XRT72L50 will latch the data, residing on the TxNib[3:0] input pins, on the rising edge of the TxNibClk signal.

In this case the XRT72L50 has the responsibility of providing the framing reference signal by pulsing the TxFrame output pin (and in turn the Tx_Start_of_Frame input pin of the Terminal Equipment) "High" for one bit-period, coincident with the last bit within a given E3 frame.

Finally, the XRT72L50 will always internally generate the Overhead bits, when it is operating in both the E3 and Nibble-parallel modes. The XRT72L50 will pull the TxOHInd input pin "Low".

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Mode 6 Operation is illustrated in Figure 99.

FIGURE 99. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (E3 MODE 6 OPERATION)



How to configure the XRT72L50 into Mode 6

1. Set the NibIntfinput pin "High".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "1X" as illustrated below.

Framer Operating Mode Register (Address = 0x00)

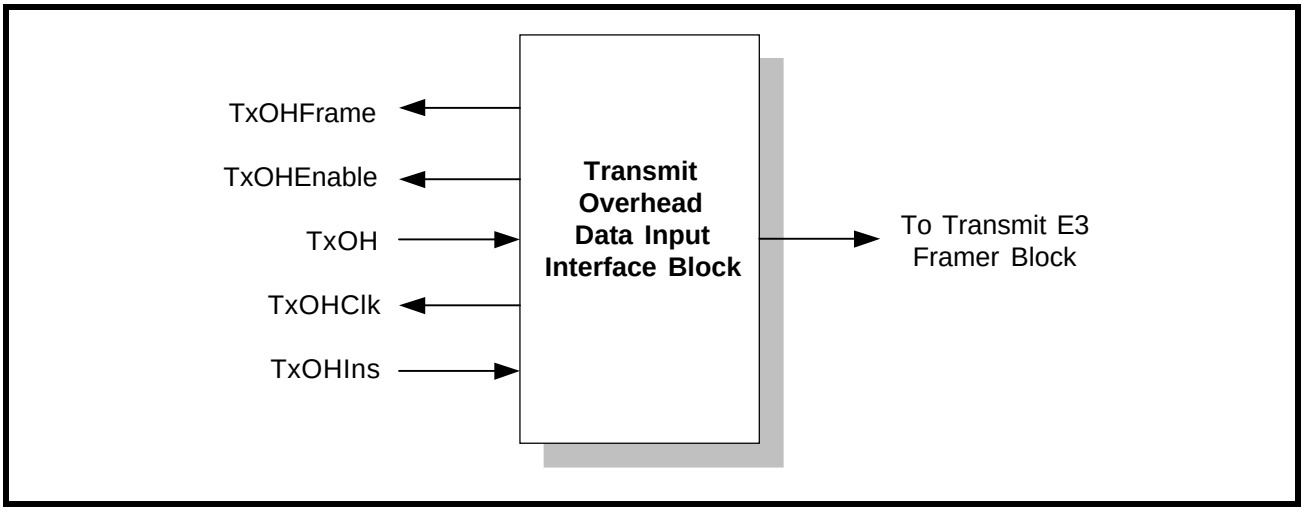
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	x

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 98.

5.2.2 The Transmit Overhead Data Input Interface

Figure 100 presents a simple illustration of the Transmit Overhead Data Input Interface block within the XRT72L50.

FIGURE 100. THE TRANSMIT OVERHEAD DATA INPUT INTERFACE BLOCK



The E3, ITU-T G.751 Frame consists of 1536 bits. Of these bits, 1524 are payload bits and the remaining 12 are overhead bits. The XRT72L50 has been designed to handle and process both the payload type and overhead type bits for each E3 frame. Within the Transmit Section within the XRT72L50, the Transmit Payload Data Input Interface has been designed to handle the payload data. Likewise, the Transmit Overhead Input Interface has been designed to handle and process the overhead bits.

The Transmit Section of the XRT72L50 generates or processes the various overhead bits within the E3 frame, in the following manner.

The Frame Alignment Signaling (FAS) Overhead Bits

The FAS (Framing Alignment Signaling) bits are always internally generated by the Transmit Section of the XRT72L50. Hence, the user cannot insert his/her value for the FAS bits into the outbound E3 data stream, via the Transmit Overhead Data Input Interface.

The A (Alarm) Overhead bit

The A bit is used to transport the FERF (Far-End Receive Failure) condition. This bit-field can be either internally generated by the Transmit Section within the XRT72L50, or can be externally generated and inserted into the outbound E3 data stream, via the Transmit Overhead Data Input Interface.

The N (National) Overhead bit

The E3 frame structure also contains the N bit which can be used to transport a proprietary User Data Link information and or Path Maintenance Data Link information. The UDL (User Data Link) bits are only accessible via the Transmit Overhead Data Input Interface. The Path Maintenance Data Link (PMDL) bits can either be sourced from the Transmit LAPD Controller/Buffer or via the Transmit Overhead Data Input Interface.

Table 44 lists the Overhead Bits within the E3 frame. In addition, this table also indicates whether or not these overhead bits can be sourced by the Transmit Overhead Data Input Interface.

TABLE 44: A LISTING OF THE OVERHEAD BITS WITHIN THE E3 FRAME, AND THEIR POTENTIAL SOURCES, WITHIN THE XRT72L50 IC

OVERHEAD BIT	INTERNALLY GENERATED	ACCESSIBLE VIA THE TRANSMIT OVERHEAD DATA INPUT INTERFACE	BUFFER/REGISTER ACCESSIBLE
FAS Signal - Bit 9	Yes	No	Yes
FAS Signal - Bit 8	Yes	No	Yes
FAS Signal - Bit 7	Yes	No	Yes
FAS Signal - Bit 6	Yes	No	Yes
FAS Signal - Bit 5	Yes	No	Yes
FAS Signal - Bit 4	Yes	No	Yes
FAS Signal - Bit 3	Yes	No	Yes
FAS Signal - Bit 2	Yes	No	Yes
FAS Signal - Bit 1	Yes	No	Yes
FAS Signal - Bit 0	Yes	No	Yes
A Bit	Yes	Yes	Yes
N Bit	Yes	Yes	Yes

NOTES:

1. *The XRT72L50 contains mask register bits that permit the user to alter the state of the internally generated value for these bits.*
2. *The Transmit LAPD Controller/Buffer can be configured to be the source of the N bits, within the outbound E3 data stream.*

The Transmit Overhead Data Input Interface permits the user to insert overhead data into the outbound E3 frames via the following two different methods.

- Method 1 - Using the TxOHClk clock signal
- Method 2 - Using the TxInClk and the TxOHEnable signals.

Each of these methods are described below.

5.2.2.1 *Method 1 - Using the TxOHClk Clock Signal*

The Transmit Overhead Data Input Interface consists of the five signals. Of these five (5) signals, the following four (4) signals are to be used when implementing Method 1.

- TxOH
- TxOHClk
- TxOHFrame
- TxOHIns

Each of these signals are listed and described below.

Table 45.

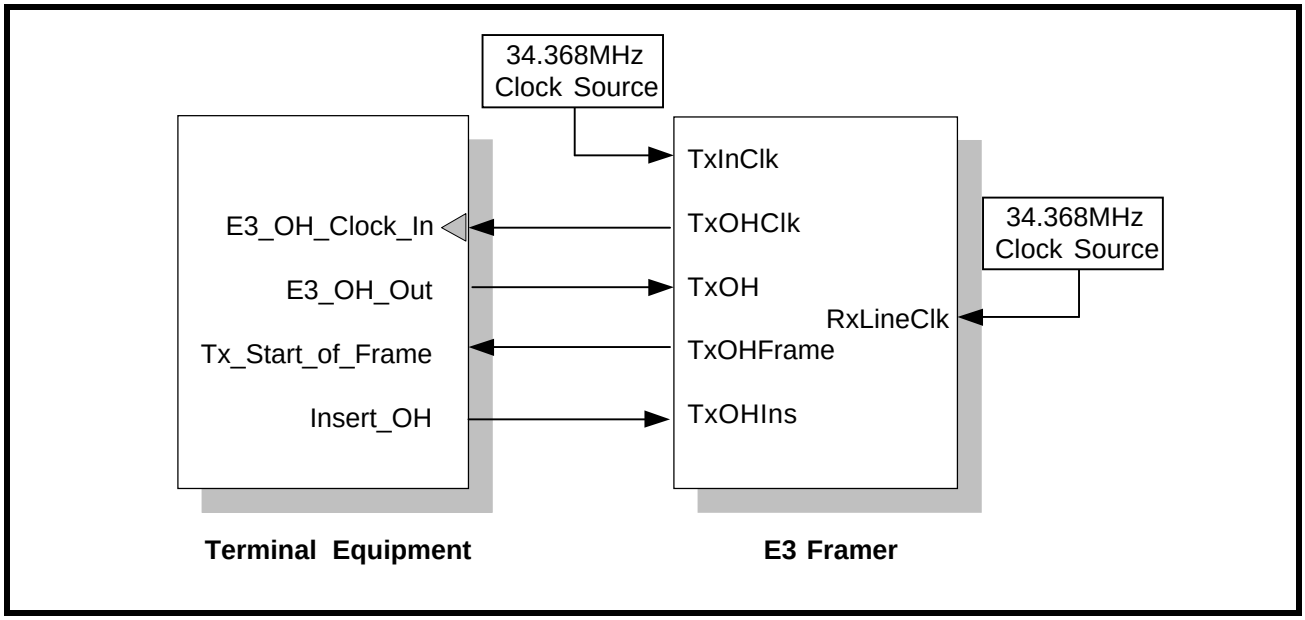
TABLE 45: DESCRIPTION OF METHOD 1 TRANSMIT OVERHEAD INPUT INTERFACE SIGNALS

NAME	TYPE	DESCRIPTION
TxOHIns	Input	**Transmit Overhead Data Insert Enable input pin.** Asserting this input signal (e.g., setting it "High") enables the Transmit Overhead Data Input Interface to accept overhead data from the Terminal Equipment. In other words, while this input pin is "High", the Transmit Overhead Data Input Interface will sample the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. Conversely, setting this pin "Low" configures the Transmit Overhead Data Input Interface to NOT sample (e.g., ignore) the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. ***NOTE:*** *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the Transmit Overhead Data Input Interface (e.g., if the Terminal Equipment asserts the TxOHIns signal, at a time when one of these non-insertable overhead bits are being processed), that particular insertion effort will be ignored.*
TxOH	Input	**Transmit Overhead Data Input pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the overhead bit position within the very next outbound E3 frame. If the TxOHIns pin is pulled "High", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the TxOHClk output pin. Conversely, if the TxOHIns pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.
TxOHClk	Output	**Transmit Overhead Input Interface Clock Output signal:** This output signal serves two purposes: 1. The Transmit Overhead Data Input Interface will provide a rising clock edge on this signal, one bit-period prior to the instant that the Transmit Overhead Data Input Interface is processing an overhead bit. 2. The Transmit Overhead Data Input Interface will sample the data at the TxOH input, on the falling edge of this clock signal (provided that the TxOHIns input pin is "High"). ***NOTE:*** *The Transmit Overhead Data Input Interface will supply a clock edge for all overhead bits within the E3 frame (via the TxOHClk output signal). This includes those overhead bits that the Transmit Overhead Data Input Interface will not accept from the Terminal Equipment.*
TxOHFrame	Output	**Transmit Overhead Input Interface Frame Boundary Indicator Output:** This output signal pulses "High" when the XRT72L50 is processing the last bit within a given E3 frame. The purpose of this output signal is to alert the Terminal Equipment that the Transmit Overhead Data Input Interface block is about to begin processing the overhead bits for a new E3 frame.

Interfacing the Transmit Overhead Data Input Interface to the Terminal Equipment.

Figure 101 illustrates how one should interface the Transmit Overhead Data Input Interface to the Terminal Equipment, when using Method 1.

FIGURE 101. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 1)



Method 1 Operation of the Terminal Equipment

If the Terminal Equipment intends to insert any overhead data into the outbound E3 data stream, (via the Transmit Overhead Data Input Interface), then it is expected to do the following.

1. To sample the state of the TxOHFrame signal (e.g., the Tx_Start_of_Frame input signal) on the rising edge of the TxOHClk (e.g., the E3_OH_Clock_In signal).
2. To keep track of the number of rising clock edges that have occurred, via the TxOHClk (e.g., the E3_OH_Clock_In signal) since the last time the TxOHFrame signal was sampled "High". By doing this the Terminal Equipment will be able to keep track of which overhead bit is being processed by the Transmit Overhead Data Input Interface block at any given time. When the Terminal Equipment knows which overhead bit is being processed, at a given TxOHClk period, it will know when to insert a desired overhead bit value into the outbound E3 data stream. From this, the Terminal Equipment will know when it should assert the TxOHIns input pin and place the appropriate value on the TxOH input pin (of the XRT72L50).

Table 46 relates the number of rising clock edges (in the TxOHClk signal, since TxOHFrame was sampled "High") to the E3 Overhead Bit, that is being processed.

TABLE 46: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN TXOHCLK, (SINCE TXOHFRAME WAS LAST SAMPLED "HIGH") TO THE E3 OVERHEAD BIT, THAT IS BEING PROCESSED

NUMBER OF RISING CLOCK EDGES IN TXOHCLK	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
0 (Clock edge is coincident with TxOHFrame being detected "High")	FAS Signal - Bit 9	No
1	FAS Signal - Bit 8	No
2	FAS Signal - Bit 7	No
3	FAS Signal - Bit 6	No
4	FAS Signal - Bit 5	No
5	FAS Signal - Bit 4	No
6	FAS Signal - Bit 3	No
7	FAS Signal - Bit 2	No
8	FAS Signal - Bit 1	No
9	FAS Signal - Bit 0	No
10	A Bit	Yes
11	N Bit	Yes

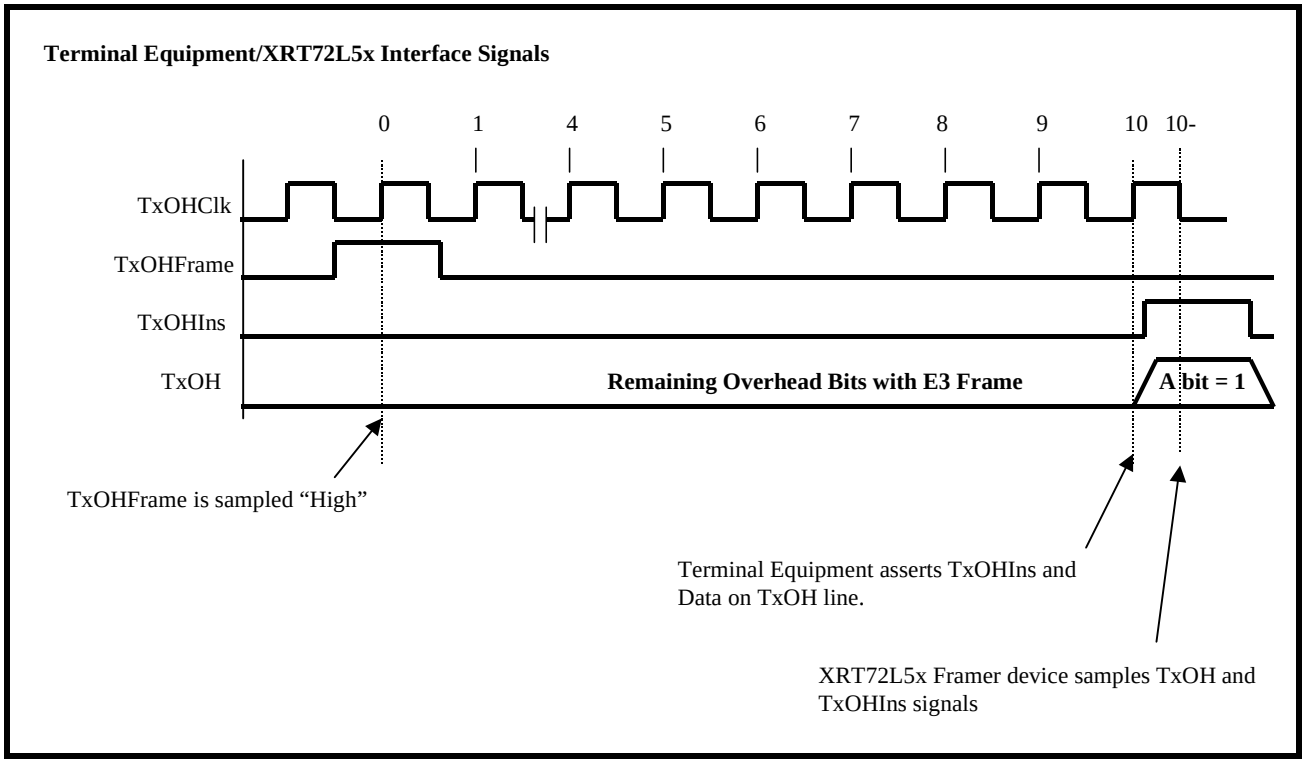
3. After the Terminal Equipment has waited the appropriate number of clock edges (from the TxOHFrame signal being sampled "High"), it should assert the TxOHIns input signal. Concurrently, the Terminal Equipment should also place the appropriate value (of the inserted overhead bit) onto the TxOH signal.
4. The Terminal Equipment should hold both the TxOHIns input pin "High" and the value of the TxOH signal, stable until the next rising edge of TxOHClk is detected.

Case Study: The Terminal Equipment intends to insert the appropriate overhead bits into the Transmit Overhead Data Input Interface (using Method 1) in order to transmit a Yellow Alarm to the remote terminal equipment.

In this example, the Terminal Equipment intends to insert the appropriate overhead bits, into the Transmit Overhead Data Input Interface, such that the XRT72L50 will transmit a Yellow Alarm to the remote terminal equipment. Recall that, for E3, ITU-T G.751 Applications, a Yellow Alarm is transmitted by setting the "A" bit to "1".

If one assumes that the connection between the Terminal Equipment and the XRT72L50 are as illustrated in Figure 101 then Figure 102 presents an illustration of the signaling that must go on between the Terminal Equipment and the XRT72L50.

FIGURE 102. ILLUSTRATION OF THE SIGNAL THAT MUST OCCUR BETWEEN THE TERMINAL EQUIPMENT AND THE XRT72L50 IN ORDER TO CONFIGURE THE XRT72L50 TO TRANSMIT A YELLOW ALARM TO THE REMOTE TERMINAL EQUIPMENT



In Figure 102 the Terminal Equipment samples the TxOHFrame signal being "High" at rising clock edge # 0. From this point, the Terminal Equipment will wait until it has detected the 10th rising edge of the TxOHClk signal. At this point, the Terminal Equipment knows that the XRT72L50 is just about to process the A bit within a given outbound E3 frame. Additionally, according to Table 46, the 10th overhead bit to be processed is the "A" bit. In order to facilitate the transmission of the Yellow Alarm, the Terminal Equipment must set this "A" bit to "1". Hence, the Terminal Equipment starts this process by implementing the following steps concurrently.

a. Assert the TxOHIns input pin by setting it "High".

b. Set the TxOH input pin to "1".

After the Terminal Equipment has applied these signals, the XRT72L50 will sample the data on both the TxOHIns and TxOH signals upon the very next falling edge of TxOHClk (designated as "10-" in Figure 102). Once the XRT72L50 has sampled this data, it will then insert a "1" into the "A" bit position, in the outbound E3 frame.

Upon detection of the very next rising edge of the TxOHClk clock signal (designated as clock edge 1 in Figure 102, the Terminal Equipment will negate the TxOHIns signal (e.g., toggles it "Low") and will cease inserting data into the Transmit Overhead Data Input Interface.

After the Terminal Equipment has performed this insertion procedure, it leaves the remaining overhead bits (within this particular outbound E3 frame) in-tact, by terminating this Overhead Bit Insertion procedure. The Terminal Equipment should now terminate this overhead bit insertion, by doing the following.

a. Assert the TxOHIns input pin by setting it "High".

b. Set the TxOH input to "0".

If the Terminal Equipment wishes to continue its transmission of the Yellow Alarm condition to the Remote Terminal Equipment, then it should resume the Overhead Bit Insertion procedure (as described above), at the beginning of each outbound E3 frame (or each time TxOHFrame is sampled "High").

5.2.2.2 *Method 2 - Using the TxInClk and TxOHEnable Signals*

Method 1 requires the use of an additional clock signal, TxOHClk. However, there may be a situation in which the user does not wish to add this extra clock signal to their design, in order to use the Transmit Overhead Data Input Interface. Hence, Method 2 is available. When using Method 2, either the TxInClk or RxOutClk signal is used to sample the overhead bits and signals which are input to the Transmit Overhead Data Input Interface. Method 2 involves the use of the following signals:

- TxOH
- TxInClk
- TxOHFrame
- TxOHEnable

Each of these signals are listed and described in Table 47.

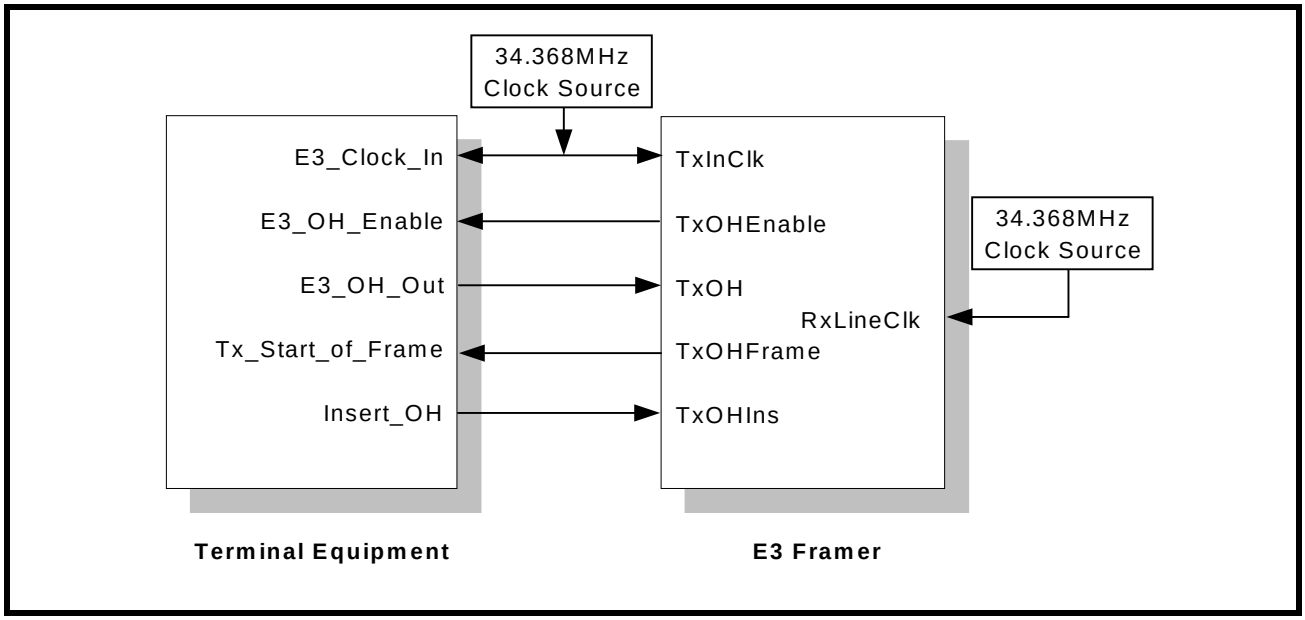
TABLE 47: DESCRIPTION OF METHOD 2 TRANSMIT OVERHEAD INPUT INTERFACE SIGNALS

NAME	TYPE	DESCRIPTION
TxOHEnable	Output	**Transmit Overhead Data Enable Output pin** The XRT72L50 will assert this signal, for one TxInClk period, just prior to the instant that the Transmit Overhead Data Input Interface is processing an overhead bit.
TxOHFrame	Output	**Transmit Overhead Input Interface Frame Boundary Indicator Output:** This output signal pulses "High" when the XRT72L50 is processing the last bit within a given E3 frame.
TxOHIns	Input	**Transmit Overhead Data Insert Enable input pin.** Asserting this input signal (e.g., setting it "High") enables the Transmit Overhead Data Input Interface to accept overhead data from the Terminal Equipment. In other words, while this input pin is "High", the Transmit Overhead Data Input Interface will sample the data at the TxOH input pin, on the falling edge of the TxInClk output signal. Conversely, setting this pin "Low" configures the Transmit Overhead Data Input Interface to NOT sample (e.g., ignore) the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. ***NOTE:*** *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the Transmit Overhead Data Input Interface (e.g., if the Terminal Equipment asserts the TxOHIns signal, at a time when one of these non-insertable overhead bits are being processed), that particular insertion effort will be ignored.*
TxOH	Input	**Transmit Overhead Data Input pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the overhead bit position within the very next outbound E3 frame. If the TxOHIns pin is pulled "High", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the TxOHClk output pin. Conversely, if the TxOHIns pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.

Interfacing the Transmit Overhead Data Input Interface to the Terminal Equipment

Figure 103 illustrates how one should interface the Transmit Overhead Data Input Interface to the Terminal Equipment when using Method 2.

FIGURE 103. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 2)



Method 2 Operation of the Terminal Equipment

If the Terminal Equipment intends to insert any overhead data into the outbound E3 data stream (via the Transmit Overhead Data Input Interface), then it is expected to do the following.

1. To sample the state of both the TxOHFrame and the TxOHEnable input signals, via the E3_Clock_In (e.g., either the TxInClk or the RxOutClk signal of the XRT72L50) signal. If the Terminal Equipment samples the TxOHEnable signal "High", then it knows that the XRT72L50 is about to process an overhead bit. Further, if the Terminal Equipment samples both the TxOHFrame and the TxOHEnable pins "High" (at the same time) then the Terminal Equipment knows that the XRT72L50 is about to process the first overhead bit, within a new E3 frame.
2. To keep track of the number of times that the TxOHEnable signal has been sampled "High" since the last time both the TxOHFrame and the TxOHEnable signals were sampled "High". By doing this, the Terminal Equipment will be able to keep track of which overhead bit the Transmit Overhead Data Input Interface is about ready to process. From this, the Terminal Equipment will know when it should assert the TxOHIns input pin and place the appropriate value on the TxOH input pins of the XRT72L50.

Table 48 also relates the number of TxOHEnable output pulses (that have occurred since both the TxOHFrame and TxOHEnable pins were sampled "High") to the E3 overhead bit, that is being processed.

TABLE 48: THE RELATIONSHIP BETWEEN THE NUMBER OF TXOHENABLE PULSES (SINCE THE LAST OCCURRENCE OF THE TXOHFRAME PULSE) TO THE E3 OVERHEAD BIT, THAT IS BEING PROCESSED BY THE XRT72L50

NUMBER OF TXOHENABLE PULSES	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
0 (Clock edge is coincident with TxOHFrame being detected "High")	FAS Signal - Bit 9	No
1	FAS Signal - Bit 8	No
2	FAS Signal - Bit 7	No
3	FAS Signal - Bit 6	No
4	FAS Signal - Bit 5	No
5	FAS Signal - Bit 4	No
6	FAS Signal - Bit 3	No
7	FAS Signal - Bit 2	No
8	FAS Signal - Bit 1	No
9	FAS Signal - Bit 0	No
10	A Bit	Yes
11	N Bit	Yes

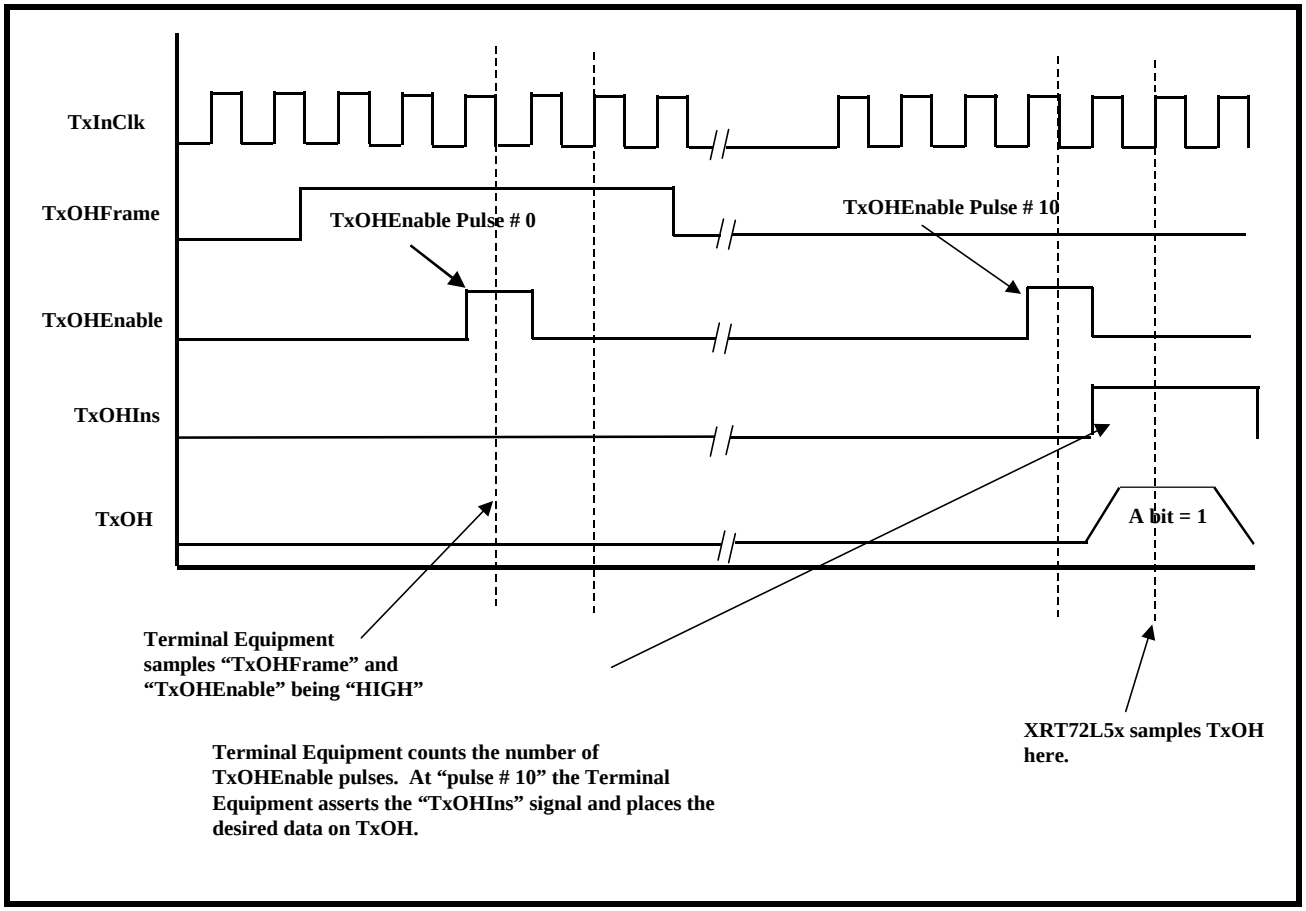
3. After the Terminal Equipment has waited through the appropriate number of pulses via the TxOHEnable pin, it should then assert the TxOHIns input signal. Concurrently, the Terminal Equipment should also place the appropriate value (of the inserted overhead bit) onto the TxOH signal.
4. The Terminal Equipment should hold both the TxOHIns input pin "High" and the value of the TxOH signal stable, until the next TxOHEnable pulse is detected.

Case Study: The Terminal Equipment intends to insert the appropriate overhead bits into the Transmit Overhead Data Input Interface (using Method 2) in order to transmit a Yellow Alarm to the remote terminal equipment.

In this case, the Terminal Equipment intends to insert the appropriate overhead bits, into the Transmit Overhead Data Input Interface such that the XRT72L50 will transmit a Yellow Alarm to the remote terminal equipment. Recall that, for E3, ITU-T G.751 applications, a Yellow Alarm is transmitted by setting the A bit to “1".

If one assumes that the connection between the Terminal Equipment and the XRT72L50 is as illustrated in Figure 103 then, Figure 104 presents an illustration of the signaling that must go on between the Terminal Equipment and the XRT72L50.

FIGURE 104. BEHAVIOR OF TRANSMIT OVERHEAD DATA INPUT INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (FOR METHOD 2)



5.2.3 The Transmit E3 HDLC Controller

The Transmit E3 HDLC Controller block can be used to transport Message-Oriented Signaling (MOS) type messages to the remote terminal equipment as discussed in detail below.

5.2.3.1 *Message-Oriented Signaling (e.g., LAP-D) processing via the Transmit E3 HDLC Controller*

The LAPD Transmitter (within the Transmit E3 HDLC Controller Block) allows the user to transmit path maintenance data link (PMDL) messages to the remote terminal via the outbound E3 Frames. In this case the message bits are inserted into and carried by the N bit, within the outbound E3 frames. The on-chip LAPD transmitter supports both the 76 byte and 82 byte length message formats, and the Framer IC allocates 88 bytes of on-chip RAM (e.g., the Transmit LAPD Message buffer) to store the message to be transmitted. The message format complies with ITU-T Q.921 (LAP-D) protocol with different addresses and is presented below in Figure 105 .

NOTE: {(Header = 4bytes) + (Payload = 82 bytes max) = 86 bytes + FCS = 2 bytes} = 88 bytes. But, FCS is always computed by the Framer. The user must write a max of 86 bytes only.

FIGURE 105. LAPD MESSAGE FRAME FORMAT

Flag Sequence (8 bits)		
SAPI (6-bits)	C/R	EA
TEI (7 bits)		EA
Control (8-bits)		
76 or 82 Bytes of Information (Payload)		
FCS - MSB		
FCS - LSB		
Flag Sequence (8-bits)		

Where: Flag Sequence = 0x7E

SAPI + CR + EA = 0x3C or 0x3E

TEI + EA = 0x01

Control = 0x03

Comprise the 4 HEADER Bytes

The following sections defines each of these bit/byte-fields within the LAPD Message Frame Format.

Flag Sequence Byte

The Flag Sequence byte is of the value 0x7E, and is used to denote the boundaries of the LAPD Message Frame.

The user must write this value (0x7E) at address 0x86.

SAPI - Service Access Point Identifier

The SAPI bit-fields are assigned the value of "001111b" or 15 (decimal).

TEI - Terminal Endpoint Identifier

The TEI bit-fields are assigned the value of 0x00. The TEI field is used in N-ISDN systems to identify a terminal out of multiple possible terminal. However, since the Framer IC transmits data in a point-to-point manner, the TEI value is unimportant.

The user must write 0x3C or 0x3E at address 0x87 and 0x01 at address ox88

Control

The Control identifies the type of frame being transmitted. There are three general types of frame formats: Information, Supervisory, and Unnumbered. The Framer assigned the Control byte the value 03h. Hence, the Framer will be transmitting and receiving Unnumbered LAPD Message frames.

The user must write 0x03 at address 0x89.

Information Payload

The Information Payload is the 76 bytes or 82 bytes of data (e.g., the PMDL Message) that the user has written into the on-chip Transmit LAPD Message buffer (which is located at addresses 0x8A through 0xDB).

It is important to note that the user must write in a specific octet value into the first byte position within the Transmit LAPD Message buffer (located at Address = 0x8A). The value of this octet depends upon the type of LAPD Message frame/PMDL Message that the user wishes to transmit. Table 49 presents a list of the various types of LAPD Message frames/PMDL Messages that are supported by the XRT72L50 Framer and the corresponding octet value that the user must write into the first octet position within the Transmit LAPD Message buffer.

TABLE 49: THE LAPD MESSAGE TYPE AND THE CORRESPONDING VALUE OF THE FIRST BYTE, WITHIN THE INFORMATION PAYLOAD

LAPD MESSAGE TYPE	VALUE OF FIRST BYTE, WITHIN INFORMATION PAYLOAD OF MESSAGE	MESSAGE SIZE
CL Path Identification	0x38	76 bytes
IDLE Signal Identification	0x34	76 bytes
Test Signal Identification	0x32	76 bytes
ITU-T Path Identification	0x3F	82 bytes

Frame Check Sequence Bytes

The 16 bit FCS (Frame Check Sequence) is calculated over the LAPD Message Header and Information Payload bytes, by using the CRC-16 polynomial, $x^{16} + x^{12} + x^5 + 1$.

NOTE: *For FCS calculation, Header also includes the starting Flag Sequence byte (0x7E).*

Operation of the LAPD Transmitter

If the user wishes to transmit a message via the LAPD Transmitter, the information portion (or the body) of the message must be written into the Transmit LAPD Message Buffer, which is located at 0x8A through 0xDB in on-chip RAM via the Microprocessor Interface. Afterwards, the user must do five things:

1. Configure the source of the N bit (within each outbound E3 frame, to be the LAPD Transmitter.
2. Specify the length of LAPD message to be transmitted.
3. Specify whether the LAPD Transmitter should transmit this LAPD Message frame only once, or an indefinite number of times at One-Second intervals.
4. Enable the LAPD Transmitter.
5. Initiate the Transmission of the PMDL Message.

Each of these steps will be discussed in detail.

STEP 1 - Configure the source of the N bit (within each outbound E3 frame, to be the LAPD Transmitter.

This is accomplished by writing the appropriate data into the TxNSourceSel[1:0] bit-fields, within the TxE3 Configuration Register, as illustrated below.

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx BIP-4 Enable	TxASourceSel[1:0]		TxNSourceSel[1:0]		Tx AIS Enable	Tx LOS Enable	Tx FAS Source Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting TxNSourceSel[1:0] to “10” configures the Transmit E3 Framer block to use the LAPD Transmitter as the data source for the N bits. Hence, the N bit, (within each outbound E3 frame) is now carrying LAPD Messages to the remote terminal equipment.

STEP 2 - Specify the type of LAPD Message frame to be Transmitted (within the Transmit LAPD Message Buffer)

The user must write in a specific octet value into the first octet position within the Transmit LAPD Buffer (e.g., at Address Location 0x8A). This octet is referred to as the LAPD Message Frame ID octet. The value of this octet must correspond to the type of LAPD Message frame that is desired to be transmitted. This octet will

ultimately be used by the Remote Terminal Equipment in order to help it identify the type of LAPD message frame that it is receiving. Table 49 lists these octets and the corresponding LAPD Message types.

STEP 3 - Write the PMDL Message into the remaining part of the Transmit LAPD Message Buffer.

The user must now write in the PMDL Message into the remaining portion of the Transmit LAPD Message buffer (e.g., addresses 0x8B through 0xDB).

STEP 4 - Specifying the Length of the LAPD Message

One of two different sizes of LAPD Messages can be transmitted. This can be accomplished by writing the appropriate data to bit 1 within the Tx E3 LAPD Configuration Register. The bit-format of this register is presented below.

Transmit E3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	X	0	X	X

The relationship between the contents of bit-fields 1 and the LAPD Message size is given in Table 50.

TABLE 50: RELATIONSHIP BETWEEN TXLAPD MSG LENGTH AND THE LAPD MESSAGE SIZE

TXLAPD MESSAGE LENGTH	LAPD MESSAGE LENGTH
0	LAPD Message size is 76 bytes
1	LAPD Message size is 82 bytes

NOTE: *The Message Type selected must correspond with the contents of the first byte of the Information (Payload) portion, as presented in* Table 49*.*

STEP 5 - Specify whether the LAPD Transmitter should transmit the LAPD Message frame only once, or an indefinite number of times at one-second intervals.

The Transmit E3 HDLC Control block allows the user to configure the LAPD Transmitter to transmit this LAPD Message frame only once, or an indefinite number of times at one-second intervals. The user implements this configuration by writing the appropriate value into Bit 3 (Auto Retransmit) within the Tx E3 LAPD Configuration Register (Address = 0x33), as depicted below.

TxE3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	1	0	0	0

If the user writes a “1” into this bit-field, then the LAPD Transmitter will transmit the LAPD Message frame repeatedly at one-second intervals until the LAPD Transmitter is disabled.

If the user writes a “0” into this bit-field, then the LAPD Transmitter will transmit the LAPD Message frame only once. Afterwards, the LAPD Transmitter will halt its transmission until the user invokes the Transmit LAPD Message frame command, once again.

STEP 5 - Enabling the LAPD Transmitter

Prior to the transmission of any data via the LAPD Transmitter, the LAPD Transmitter must be enabled. This is accomplished by writing a "1" to bit 0 (TxLAPD Enable) of the Tx E3 LAPD Configuration Register, as depicted below.

Transmit E3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	X	0	X	1

If the user writes a “0” into this bit-field, then the LAPD Transmitter will be enabled, and the LAPD Transmitter will immediately begin to transmit a continuous stream of Flag Sequence octets (0x7E), via the N bit-field of each outbound E3 frame.

Conversely, if the user writes a “1” into this bit-field, then the LAPD Transmitter will be disabled. The Transmit E3 Framer block will automatically insert a “1” into the N bit-field, within each outbound E3 frame. No transmission of PMDL data will occur.

STEP 7 - Initiate the Transmission

At this point, the user should have written the PMDL message into the on-chip Transmit LAPD Message buffer and the type of LAPD Message that is desired to be transmitted should have been specified. Finally, the user should have enabled the LAPD Transmitter. The only remaining to do is initiate the transmission of this message. This process is initiated by writing a “1” to Bit 3 (Tx DL Start) within the Tx E3 LAPD Status and Interrupt Register (Address = 0x34), as depicted below.

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	0

A “0” to “1” transition in Bit 3 (Tx DL Start) in this register, initiates the transmission of LAPD Message frames. At this point, the LAPD Transmitter will begin to search through the PMDL message, which is residing within the Transmit LAPD Message buffer. It will compute and append to the 2 byte FCS value If the LAPD Transmitter finds any string of five (5) consecutive “1’s” in the PMDL Message then the LAPD Transmitter will insert a “0” immediately following these strings of consecutive “1’s”. This procedure is known as stuffing. The purpose of PMDL Message stuffing is to insure that the user’s PMDL Message does not contain strings of data that mimic the Flag Sequence octet (e.g., six consecutive “1’s”) or the ABORT Sequence octet (e.g., seven consecutive “1’s”). Afterwards, the LAPD Transmitter will begin to encapsulate the PMDL Message, residing in the Transmit LAPD Message buffer, into a LAPD Message frame. Finally, the LAPD Transmitter will fragment the outbound LAPD Message frame into bits and will begin to transport these bits via the N bit-field within each outbound E3 frame.

While the LAPD Transmitter is transmitting this LAPD Message frame, the TxDL Busy bit-field (Bit 2) within the Tx E3 LAPD Status and Interrupt Register, will be set to “1”. This bit-field allows the user to poll the status of the LAPD Transmitter. Once the LAPD Transmitter has completed the transmission of the LAPD Message, then this bit-field will toggle back to “0”.

The user can configure the LAPD Transmitter to interrupt the local Microprocessor/Microcontroller upon completion of transmission of the LAPD Message frame, by setting bit-field "1" (TxLAPD Interrupt Enable) within the Tx E3 LAPD Status and Interrupt register (Address = 0x34). to "1" as depicted below.

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	X	X	1	X

'The purpose of t his interrupt is to let the Microprocessor/Microcontroller know that the LAPD Transmitter is available and ready to transmit a LAPD Message frame (which contains a new PMDL Message) to the remote terminal equipment. Bit 0 (Tx LAPD Interrupt Status) within the Tx E3 LAPD Status and Interrupt Register will reflect the status for the Transmit LAPD Interrupt.

NOTE: *This bit-field will be reset upon reading this register.*

Summary of Operating the LAPD Transmitter

Once the user has invoked the TxDL Start command, the LAPD Transmitter will do the following.

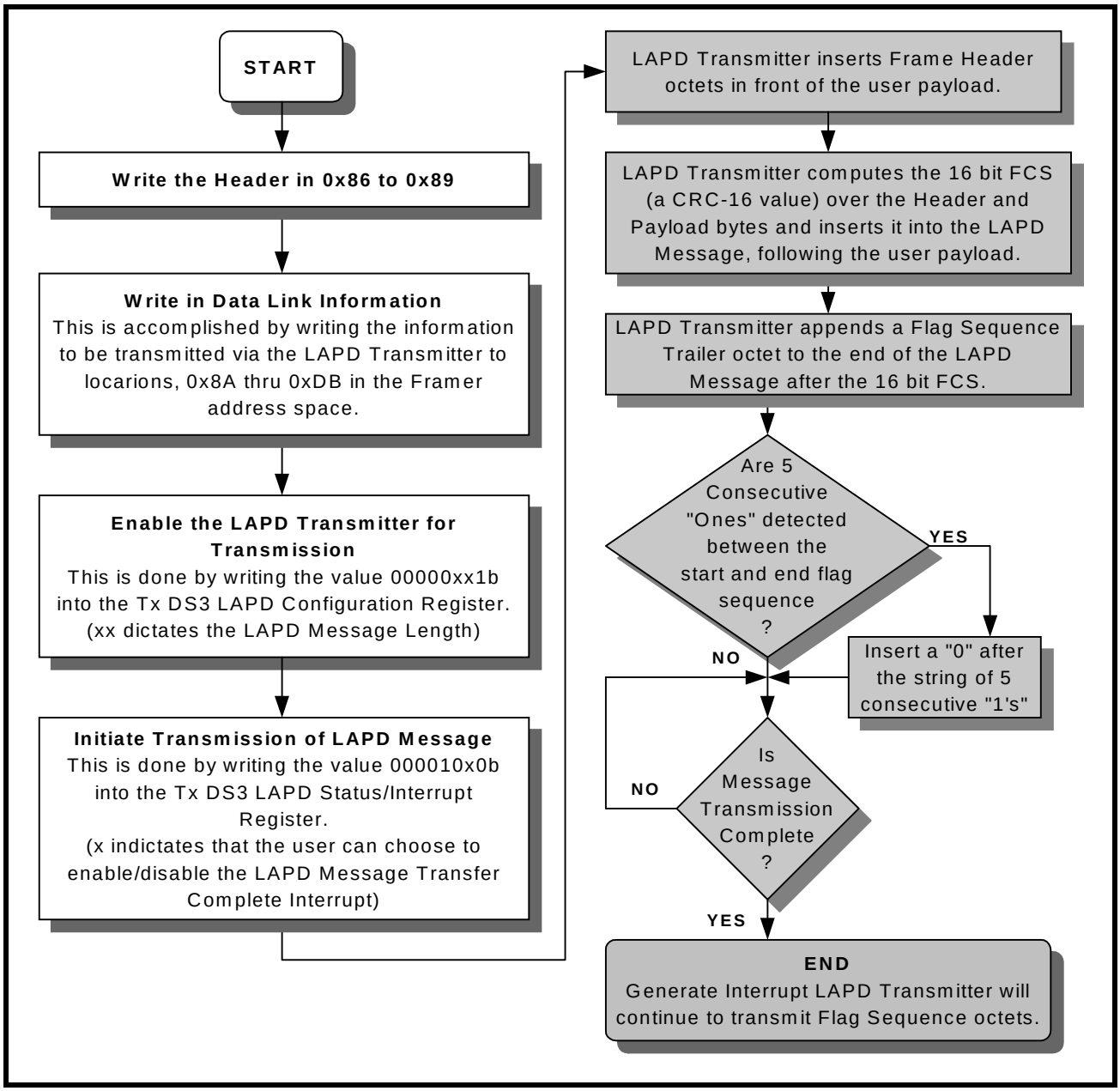
- Compute the 16 bit Frame Check Sum (FCS) of the LAPD Message Frame (e.g., of the LAPD Message header and information payload) and append this value to the LAPD Message, (at the end of 76 or 82 bytes).
- Append a trailer Flag Sequence octet to the end of the message LAPD following the 16 bit FCS value.
- Serialize the composite LAPD message. Between the two 0x7E flags, ZeroStuff any consecutive five "Ones" by inserting an extra "0". This insures that any occurrence of 0x7E in the payload does not serve as a terminating flag sequence. Insert the Zero Stuffed LAPD message into the N bit-field of each outgoing E3 Frame.
- Complete the transmission of the frame overhead, payload, FCS value, and trailer Flag Sequence octet via the Transmit DS3 Framer.

Once the LAPD Transmitter has completed its transmission of the LAPD Message frame, the Framer will generate an Interrupt to the MIcroprocessor/Microcontroller (if enabled). Afterwards, the LAPD Transmitter will either halt its transmission of LAPD Message frames or will proceed to retransmit the LAPD Message frame, repeatedly at one-second intervals. In between these transmissions of the LAPD Message frames, the LAPD Transmitter will be sending a continuous stream of Flag Sequence bytes. The LAPD Transmitter will continue this behavior until the user has disabled the LAPD Transmitter by writing a "1" into bit 3 (No Data Link) within the Tx E3 Configuration register.

NOTE: *In order to prevent the user's data (e.g., the PMDL Message within the LAPD Message frame) from mimicking the Flag Sequence byte or an ABORT Sequence, the LAPD Transmitter will parse through the PMDL Message data and insert a "0" into this data, immediately following the detection of five (5) consecutive "1's" (this stuffing occurs while the PMDL message data is being read in from the Transmit LAPD Message frame. The Remote LAPD Receive (See Section 5.3.3 will have the responsibility of checking the newly received PMDL messages for a string of five (5) consecutive "1's" and removing the subsequent "0" from the payload portion of the incoming LAPD Message.*

Figure 106 presents a flow chart diagram. Figure 106 depicts the procedure (in white boxes) that the user should use in order to transmit a PMDL message via the LAPD Transmitter, when the LAPD Transmitter is configured to retransmit the LAPD Message frame, repeatedly at One-Second intervals. This figure also indicates (via the Shaded boxes) what the LAPD Transmitter circuitry will do before and during message transmission.

FIGURE 106. FLOW CHART DEPICTING HOW TO USE THE LAPD TRANSMITTER



NOTE: *In Figure 106, the unshaded boxes depict the tasks that the user must perform. The shaded boxes present the resulting tasks that the Transmit HDLC Controller block will perform.*

The Mechanics of Transmitting a New LAPD Message frame, if the LAPD Transmitter has been configured to re-transmit the LAPD Message frame, repeatedly, at One-Second intervals.

If the LAPD Transmitter has been configured to retransmit the LAPD Message frame repeatedly at one-second intervals, then it will repeatedly transmit the LAPD Message frame to the Remote Terminal Equipment at one second intervals.

If another (e.g., a different) PMDL Message is to be transmitted to the Remote Terminal Equipment, this new message will have to be written into the Transmit LAPD Message buffer, via the Microprocessor Interface block of the Framer IC. However, care must be taken when writing this new PMDL message. If this message is written into the Transmit LAPD Message buffer at the wrong time (with respect to these One-second LAPD Message frame transmissions), the user's action could interfere with these transmissions, thereby causing the

LAPD Transmitter to transmit a corrupted message to the Remote Terminal Equipment. In order to avoid this problem, while writing the new message into the Transmit LAPD Message buffer, the user should do the following.

1. Configure the Framer to automatically reset activated interrupts.

The user can do this by writing a "1" into Bit 3 within the Framer Operating Mode register (Address = 0x00), as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	1

This action will prevent the LAPD Transmitter from generating its own One-Second interrupt (following each transmission of the LAPD Message frame).

2. Enable the One-Second Interrupt

This can be done by writing a "1" into Bit 0 (One-Second Interrupt Enable) within the Block Interrupt Enable Register, as depicted below.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One-Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	0	1

3. Write the new message into the Transmit LAPD Message buffer immediately after the occurrence of the One-Second Interrupt

By synchronizing the writes to the Transmit LAPD Message buffer to occur immediately after the occurrence of the One-Second Interrupt, the user avoids conflicting with the One-Second transmission of the LAPD Message frame, and will transmit the correct (uncorrupted) PMDL Message to the Remote LAPD Receiver.

5.2.4 The Transmit E3 Framer Block

5.2.4.1 *Brief Description of the Transmit E3 Framer*

The Transmit E3 Framer block accepts data from any of the following four sources, and uses it to form the E3 data stream.

- The Transmit Payload Data Input block
- The Transmit Overhead Data Input block
- The Transmit HDLC Controller block
- The Internal Overhead Data Generator

The manner in how the Transmit E3 Framer block handles data from each of these sources is described below.

Handling of data from the Transmit Payload Data Input Interface

For E3 applications, all data that is input to the Transmit Payload Data Input Interface will be inserted into the payload bit positions within the outbound E3 frames.

Handling of data from the Internal Overhead Bit Generator

By default, the Transmit E3 Framer block will internally generate the overhead bytes. However, if the Terminal Equipment inserts its own values for the overhead bits or bytes (via the Transmit Overhead Data Input Interface) or if the user enables and employs the Transmit E3 HDLC Controller block, then these internally generated overhead bytes will be overwritten.

Handling of data from the Transmit Overhead Data Input Interface

For E3 applications, the Transmit E3 Framer block automatically generates and inserts the framing alignment bytes (e.g., the 10 bit FAS framing alignment signal) into the outbound E3 frames. Hence, the Transmit E3 Framer block will not accept data from the Transmit OH Data Input Interface block for the FAS signal.

However, the Transmit E3 Framer block will accept (and insert) data from the Transmit Overhead Data Input Interface for both the A and N bit-fields.

If the user's local Data Link Equipment activates the Transmit Overhead Data Input Interface block and writes data into this interface for these bits or bytes, then the Transmit E3 Framer block will insert this data into the appropriate overhead bit/byte-fields, within the outbound E3 frames.

Handling of data from the Transmit HDLC Controller Block

The exact manner in how the Transmit E3 Framer handles data from the Transmit HDLC Controller block depends upon whether the Transmit HDLC Controller is activated or not. If the Transmit DS3 HDLC Controller block is not activated, then the Transmit E3 Framer block will insert a “1” into each N bit-field, within each outbound E3 frame.

If the Transmit E3 HDLC Controller block is activated, then data will be inserted into the N bit-fields as described in Section 4.2.3.

5.2.4.2 *Detailed Functional Description of the Transmit E3 Framer Block*

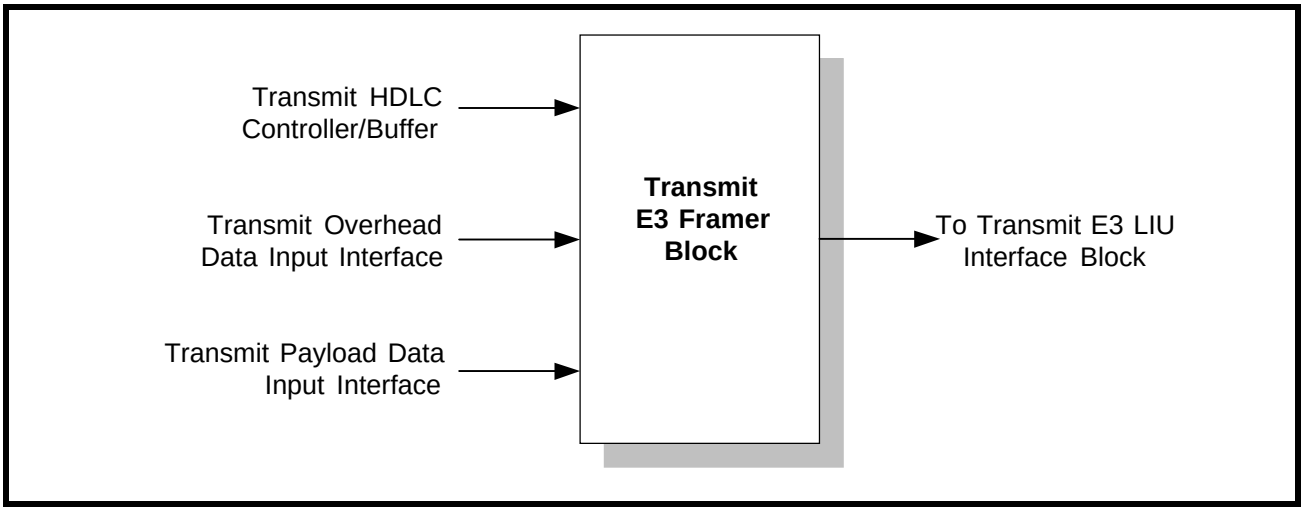
The Transmit E3 Framer receives data from the following four sources and combines them together to form the E3 data stream.

- The Transmit Payload Data Input Interface block.
- The Transmit Overhead Data Input Interface block
- The Transmit HDLC Controller block.
- The Internal Overhead Data Generator.

Afterwards, this E3 data stream will be routed to the Transmit E3 LIU Interface block, for further processing.

Figure 107 presents a simple illustration of the Transmit E3 Framer block, along with the associated paths to the other functional blocks within the chip.

FIGURE 107. THE TRANSMIT E3 FRAMER BLOCK AND THE ASSOCIATED PATHS TO OTHER FUNCTIONAL BLOCKS



In addition to taking data from multiple sources and multiplexing them, in appropriate manner, to create the outbound E3 frames, the Transmit E3 Framer block has the following roles.

- Generating Alarm Conditions
- Generating Errored Frames (for testing purposes)
- Routing outbound E3 frames to the Transmit E3 LIU Interface block

Each of these additional roles are discussed below.

5.2.4.2.1 Generating Alarm Conditions

The Transmit E3 Framer block permits the user to, by writing the appropriate data into the on-chip registers, to override the data that is being written into the Transmit Payload Data and Overhead Data Input Interfaces and transmit the following alarm conditions.

- Generate the Yellow Alarms (or FERF indicators)
- Manipulate the A-bit, by forcing it to “0”.
- Generate the AIS Pattern
- Generate the LOS pattern
- Generate FERF (Yellow) Alarms, in response to detection of a Red Alarm condition (via the Receive Section of the XRT72L50).

The procedure and results of generating any of these alarm conditions is presented below.

The user can exercise each of these options by writing the appropriate data to the Tx E3 Configuration Register (Address = 0x30). The bit format of this register is presented below.

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx BIP-4 Enable	TxASourceSel[1:0]		TxNSourceSel[1:0]		Tx AIS Enable	Tx LOS Enable	Tx FAS Source Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit-fields 1 and 2 permit the user to transmit various alarm conditions to the remote terminal equipment. The role/function of each of these two bit-fields within the register, are discussed below.

5.2.4.2.1.1 *Tx AIS Enable - Bit 2*

This read/write bit field permits the user to force the transmission of an AIS (Alarm Indication Signal) pattern to the remote terminal equipment via software control. If the user opts to transmit an AIS pattern, then the Transmit Section of the Framer IC will begin to transmit an unframed all ones pattern to the remote terminal equipment. Table 51 presents the relationship between the contents of this bit-field, and the resulting Framer action.

TABLE 51: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 2 (TX AIS ENABLE) WITHIN THE TX E3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT E3 FRAMER BLOCK'S ACTION

BIT 2	TRANSMIT E3 FRAMER'S ACTION
0	**Normal Operation:** The Transmit Section of the XRT72L50 Framer IC will transmit E3 traffic based upon data that it accepts via the Transmit Payload Data Input Interface block, the Transmit Overhead Data Input Interface block, the Transmit HDLC Controller block and internally generated overhead bytes.
1	**Transmit AIS Pattern:** The Transmit E3 Framer block will overwrite the E3 traffic, within an Unframed “All Ones” pattern.

NOTE: *This bit is ignored whenever the TxLOS bit-field is set.*

5.2.4.2.1.2 *Transmit LOS Enable - Bit 1*

This read/write bit field allows the user to transmit an LOS (Loss of Signal) pattern to the remote terminal, upon software control. Table 52 relates the contents of this bit field to the Transmit E3 Framer block's action.

TABLE 52: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 1 (TX LOS) WITHIN THE TX E3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT E3 FRAMER BLOCK'S ACTION

BIT 1	TRANSMIT E3 FRAMER'S ACTION
0	**Normal Operation:** The Overhead bits are either internally generated, or they are inserted via the Transmit Overhead Data Input Interface or the Transmit HDLC Controller blocks. The Payload bits are received from the Transmit Payload Data Input Interface.
1	**Transmit LOS Pattern:** When this command is invoked the Transmit E3 Framer will do the following. • Set all of the overhead bytes to "0" (including the FA1 and FA2 bytes) Overwrite the E3 payload bits with an "all zeros" pattern.

NOTE: *When this bit is set, it overrides all of the other bits in this register.*

5.2.4.2.1.3 *Transmitting FERF (Far-End Receive Failure) Indicator or Yellow Alarm*

The XRT72L50 Framer IC permits the user to control the state of the A bit-field, within each outbound E3 frame. This can be achieved by writing the appropriate data into the TxASource[1:0] bit-fields within the Tx E3 Configuration Register, as illustrated below.

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx BIP-4 Enable	TxASourceSel[1:0]		TxNSourceSel[1:0]		Tx AIS Enable	Tx LOS Enable	Tx FAS Source Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	X	X	0	0	0	0	0

The following table presents the relationship between the contents of TxASource[1:0] and the resulting source of the A bit.

TXASOURCESEL[1:0]	SOURCE OF A BIT
00	TxE3 Service Bits Register (Address = 0x35)
01	Transmit Overhead Data Input Interface
10	Transmit Payload Data Input Interface
11	Functions as a FEBE (Far-End-Block Error) bit-field. This bit-field is set to "0", if the Near-End Receive Section (within this chip) detects no BIP-4 Errors within the incoming E3 frames. This bit-field is set to "1", if the Near-End Receive Section (within this chip) detects a BIP-4 Error within the incoming E3 frame.

Hence, if a Yellow Alarm condition needs to be transmitted to the Remote Terminal Equipment, this can be accomplished by executing the following steps.

STEP 1 - Write a “1” into Bit 1 (A Bit) within the Tx E3 Service Bits Register, as indicated below.

TxE3 Service Bits Register (Address = 0x35)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used						A Bit	N Bit
RO	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	1	0

STEP 2 - Write the value “00” into the TxASource[1:0] bit-fields within the Tx E3 Configuration Register, as indicated below.

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx BIP-4 Enable	TxASourceSel[1:0]		TxNSourceSel[1:0]		Tx AIS Enable	Tx LOS Enable	Tx FAS Source Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	0	0	X	X	X	X	X

These two steps will cause the Transmit E3 Framer block to read in the contents of Bit 1 (within the Tx E3 Service Bit register) and insert it into the A bit-field within the outbound E3 data stream. Hence, the A bit will be set to “1”, which will be interpreted as an Alarm Condition, by the Remote Terminal Equipment.

5.2.4.2.2 Configuring the Transmit E3 Framer block to insert the BIP-4 nibble into each outbound E3 frame.

The XRT72L50 Framer IC permits the user to (1) configure the Transmit Section of the device to insert the BIP-4 value into each outbound E3 frame and (2) to configure the Receive Section of the device to compute and verify the BIP-4 value, within each inbound' E3 frame.

These two configurations are accomplished by setting bit 7 (Tx BIP-4 Enable), within the Tx E3 Configuration Register, to "1", as indicated below.

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx BIP-4 Enable	TxASourceSel[1:0]		TxNSourceSel[1:0]		Tx AIS Enable	Tx LOS Enable	Tx FAS Source Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	X	X	X	X	X	X

Setting this bit-field to "1" accomplishes the following.

- It configures the Transmit E3 Framer block to compute the BIP-4 value of a given E3 frame, and insert in to the very last nibble, within the very next outbound E3 frame. (Hence, bits 1533 through 1536, within each E3 frame, will function as the BIP-4 value)
- It configures the Receive E3 Framer block to compute and verify the BIP-4 value of each incoming E3 frame.

5.2.4.2.3 Generating Errored E3 Frames

The Transmit E3 Framer block permits the user to insert errors into the framing and error detection overhead bites (e.g., the FAS pattern, and the BIP-4 nibble) of the outbound E3 data stream in order to support Remote Terminal Equipment testing. The user can exercise this option by writing data into any of the following registers.

- TxE3 FAS Error Mask Register - 0
- TxE3 FAS Error Mask Register - 1
- TxE3 BIP-4 Error Mask Register

Inserting Errors into the FAS pattern of the outbound' E3 frames.

The user can insert errors into the FAS pattern bits, of each outbound E3 frame, by writing the appropriate data into either the TxE3 FAS Error Mask Register - 0 or TxE3 FAS Error Mask Register - 1.

As the Transmit E3 Framer block formulates the outbound E3 frames, the contents of the FAS pattern bits are automatically XORed with the contents of these two registers. The results of this XOR operation is written back into the corresponding bit-field within the outbound E3 frame, and is transmitted to the Remote Terminal Equipment. Therefore, if the user does not wish to modify any of these bits, then these registers must contain all "0's" (the default value).

TxE3 FAS Error Mask Register - 0 (Address = 0x48)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			TxFAS_Error_Mask_Upper[4:0]				
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	X	X	X	X	X

TxE3 FAS Error Mask Register - 1 (Address = 0x49)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			TxFAS_Error_Mask_Lower[4:0]				
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	X	X	X	X	X

Inserting Errors into the BIP-4 nibble, within each outbound E3 frame.

The user can insert errors into the BIP-4 nibble, within each outbound E3 frame, by writing the appropriate data into the TxE3 BIP-4 Error Mask Register.

As the Transmit E3 Framer block formulates the outbound E3 frames, the contents of the BIP-4 bits are automatically XORed with the contents of this register. The results of this XOR operation is written back into the corresponding bit-field within the outbound E3 frame, and is transmitted to the Remote Terminal Equipment. Therefore, if the user does not wish to modify any of these bits, then this register must contain all "0's" (the default value).

NOTE: *This register is only active if the XRT72L50 Framer IC has been configured to insert the BIP-4 nibble into each outbound E3 frame.*

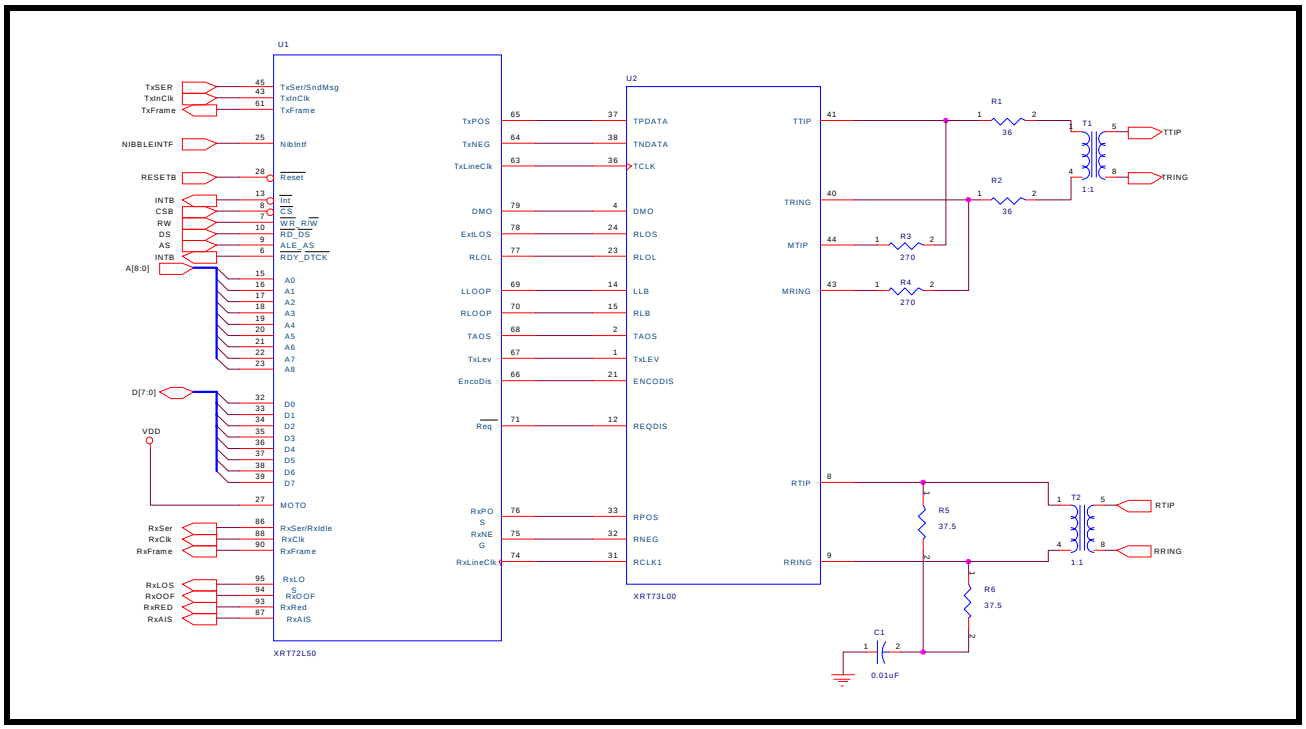
TxE3 BIP-4 Error Mask Register (Address = 0x4A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxBIP-4 Mask[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

5.2.5 The Transmit E3 Line Interface Block

The XRT72L50 Framer IC is a digital device that takes E3 payload and overhead bit information from some terminal equipment, processes this data and ultimately, multiplexes this information into a series of outbound E3 frames. However, the XRT72L50 Framer IC lacks the current drive capability to be able to directly transmit this E3 data stream through some transformer-coupled coax cable with enough signal strength for it to be received by the remote receiver. Therefore, in order to get around this problem, the Framer IC requires the use of an LIU (Line Interface Unit) IC. An LIU is a device that has sufficient drive capability, along with the necessary pulse-shaping circuitry to be able to transmit a signal through the transmission medium in a manner that it can be reliably received by the far-end receiver. Figure 108 presents a circuit drawing depicting the Framer IC interfacing to an LIU (XRT73L00 DS3/E3/STS-1 Transmit LIU).

FIGURE 108. INTERFACING THE XRT72L50 FRAMER IC TO THE XRT73L00 DS3/E3/STS-1 LIU

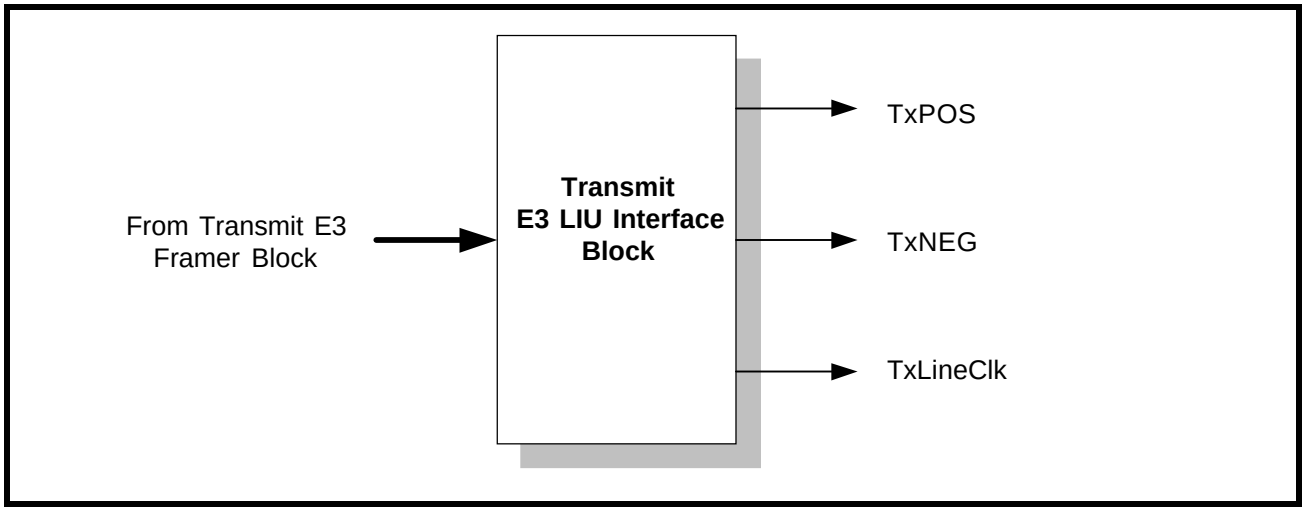


The Transmit Section of the XRT72L50 contains a block which is known as the Transmit E3 LIU Interface block. The purpose of the Transmit E3 LIU Interface block is to take the outbound E3 data stream, from the Transmit E3 Framer block, and to do the following:

1. Encode this data into one of the following line codes
   a. Unipolar (e.g., Single-Rail)
   b. AMI (Alternate Mark Inversion)
   c. HDB3 (High Density Bipolar - 3)
2. And to transmit this data to the LIU IC.

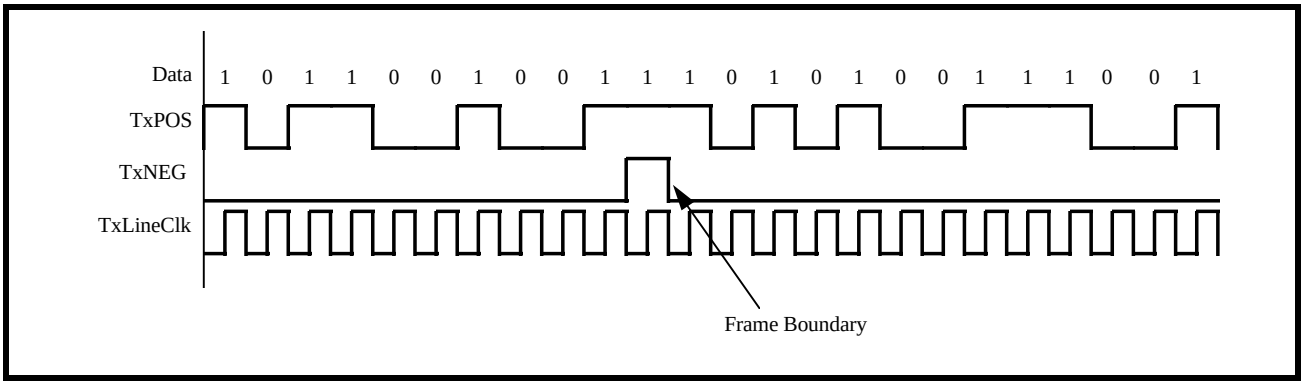
Figure 109 presents a simple illustration of the Transmit E3 LIU Interface block.

FIGURE 109. THE TRANSMIT E3 LIU INTERFACE BLOCK



The Transmit E3 LIU Interface block can transmit data to the LIU IC or other external circuitry via two different output modes: Unipolar or Bipolar. If the user selects Unipolar (or Single Rail) mode, then the contents of the E3 Frame is output, in a binary (NRZ manner) data stream via the TxPOS pin to the LIU IC. The TxNEG pin will only be used to denote the frame boundaries. TxNEG will pulse "High" for one bit period, at the start of each new E3 frame, and will remain "Low" for the remainder of the frame. Figure 110 presents an illustration of the TxPOS and TxNEG signals during data transmission while the Transmit E3 LIU Interface block is operating in the Unipolar mode. This mode is sometimes referred to as Single Rail mode because the data pulses only exist in one polarity: positive.

FIGURE 110. THE BEHAVIOR OF TXPOS AND TXNEG SIGNALS DURING DATA TRANSMISSION WHILE THE TRANSMIT E3 LIU INTERFACE IS OPERATING IN THE UNIPOLAR MODE



When the Transmit E3 LIU Interface block is operating in the Bipolar (or Dual Rail) mode, then the contents of the E3 Frame is output via both the TxPOS and TxNEG pins. If the Bipolar mode is chosen, then E3 data can be transmitted to the LIU via one of two different line codes: Alternate Mark Inversion (AMI) or High Density Bipolar -3 (HDB3). Each one of these line codes will be discussed below. Bipolar mode is sometimes referred to as Dual Rail because the data pulses occur in two polarities: positive and negative. The role of the TxPOS, TxNEG and TxLineClk output pins, for this mode are discussed below.

TxPOS - Transmit Positive Polarity Pulse: The Transmit E3 LIU Interface block will assert this output to the LIU IC when it desires for the LIU to generate and transmit a positive polarity pulse to the remote terminal equipment.

TxNEG - Transmit Negative Polarity Pulse: The Transmit E3 LIU Interface block will assert this output to the LIU IC when it desires for the LIU to generate and transmit a negative polarity pulse to the remote terminal equipment.

TxLineClk - Transmit Line Clock: The LIU IC uses this signal from the Transmit E3 LIU Interface block to sample the state of its TxPOS and TxNEG inputs. The results of this sampling dictates the type of pulse (positive polarity, zero, or negative polarity) that it will generate and transmit to the remote Receive E3 Framer.

5.2.5.1 *Selecting the various Line Codes*

The user can select either the Unipolar Mode or Bipolar Mode by writing the appropriate value to Bit 3 of the I/O Control Register (Address = 0x01), as shown below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 53 relates the value of this bit field to the Transmit E3 LIU Interface Output Mode.

TABLE 53: THE RELATIONSHIP BETWEEN THE CONTENT OF BIT 3 (UNIPOLAR/$\overline{\text{BIPOLAR}}$) WITHIN THE UNI I/O CONTROL REGISTER AND THE TRANSMIT E3 FRAMER LINE INTERFACE OUTPUT MODE

BIT 3	TRANSMIT E3 FRAMER LIU INTERFACE OUTPUT MODE
0	**Bipolar Mode:** AMI or HDB3 Line Codes are Transmitted and Received
1	**Unipolar (Single Rail) Mode** of transmission and reception of E3 data is selected.

NOTES:

1. *The default condition is the Bipolar Mode.*
2. *This selection also effects the operation of the Receive E3 LIU Interface block*

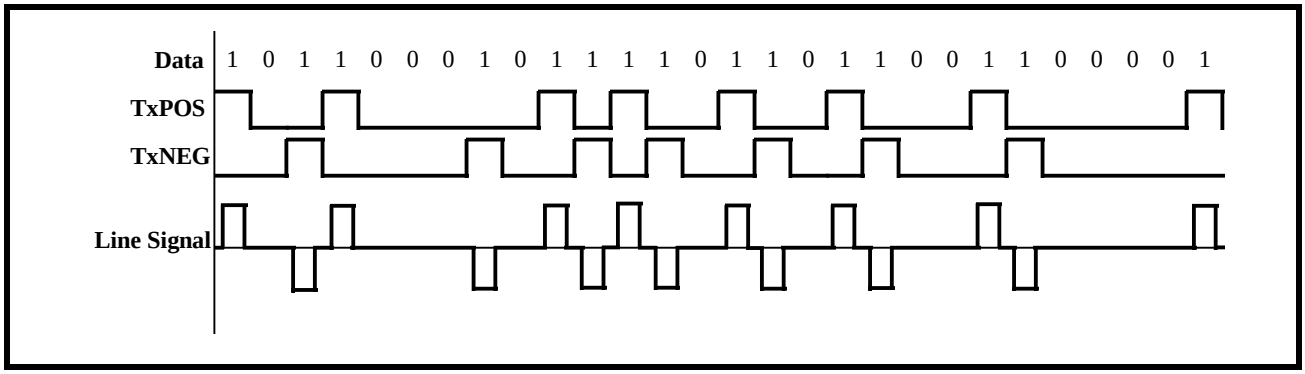
5.2.5.1.1 The Bipolar Mode Line Codes

If the Framer is choosen to operate in the Bipolar Mode, then the E3 data-stream can be choosen to be transmitted via the AMI (Alternate Mark Inversion) or the HDB3 Line Codes. The definition of AMI and HDB3 line codes follow.

5.2.5.1.1.1 *The AMI Line Code*

AMI or Alternate Mark Inversion, means that consecutive "one's" pulses (or marks) will be of opposite polarity with respect to each other. The line code involves the use of three different amplitude levels: +1, 0, and -1. +1 and -1 amplitude signals are used to represent one's (or mark) pulses and the "0" amplitude pulses (or the absence of a pulse) are used to represent zeros (or space) pulses. The general rule for AMI is: if a given mark pulse is of positive polarity, then the very next mark pulse will be of negative polarity and vice versa. This alternating-polarity relationship exists between two consecutive mark pulses, independent of the number of 'zeros' that may exist between these two pulses. Figure 111 presents an illustration of the AMI Line Code as would appear at the TxPOS and TxNEG pins of the Framer, as well as the output signal on the line.

FIGURE 111. ILLUSTRATION OF AMI LINE CODE



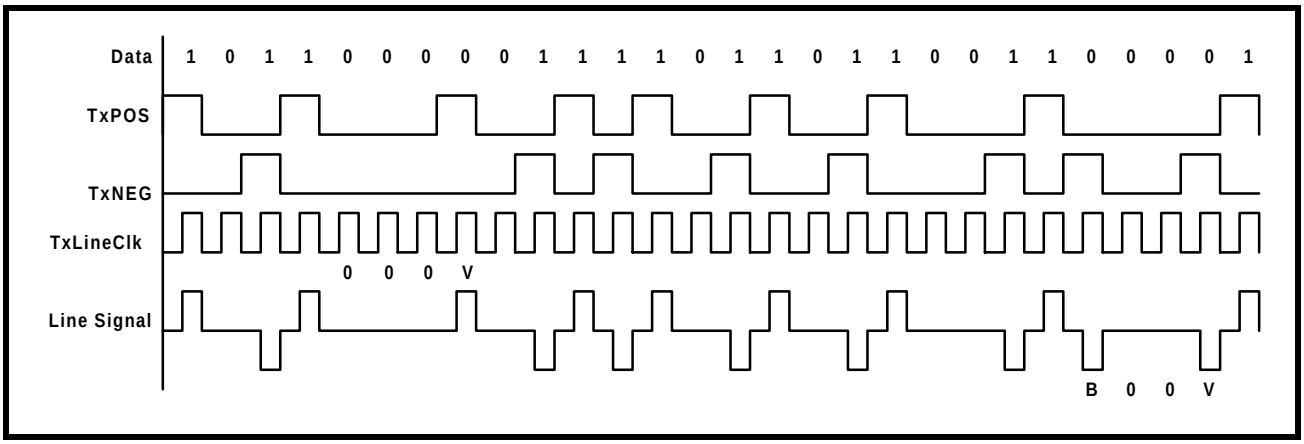
NOTE: *One of the main reasons that the AMI Line Code has been chosen for driving transformer-coupled media is that this line code introduces no dc component, thereby minimizing dc distortion in the line.*

5.2.5.1.1.2 *The HDB3 Line Code*

The Transmit E3 Framer and the associated LIU IC combine the data and timing information (originating from the TxLineClk signal) into the line signal that is transmitted to the remote receiver. The remote receiver has the task of recovering this data and timing information from the incoming E3 data stream. Many clock and data recovery schemes rely on the use of Phase Locked Loop technology. Phase-Locked-Loop (PLL) technology for clock recovery relies on transitions in the line signal, in order to maintain lock with the incoming E3 data stream. However, PLL-based clock recovery scheme, are vulnerable to the occurrence of a long stream of consecutive zeros (e.g., the absence of transitions). This scenario can cause the PLL to lose lock with the incoming E3 data, thereby causing the clock and data recovery process of the receiver to fail. Therefore, some approach is needed to insure that such a long string of consecutive zeros can never happen. One such technique is HDB3 encoding. HDB3 (or High Density Bipolar - 3) is a form of AMI line coding that implements the following rule.

In general the HDB3 line code behaves just like AMI with the exception of the case when a long string of consecutive zeros occur on the line. Any string of 4 consecutive zeros will be replaced with either a "000V" or a "B00V" where "B" refers to a Bipolar pulse (e.g., a pulse with a polarity that is compliant with the AMI coding rule). And "V" refers to a Bipolar Violation pulse (e.g., a pulse with a polarity that violates the alternating polarity scheme of AMI.) The decision between inserting an "000V" or a "B00V" is made to insure that an odd number of Bipolar (B) pulses exist between any two Bipolar Violation (V) pulses. Figure 112 presents a timing diagram that illustrates examples of HDB3 encoding.

FIGURE 112. ILLUSTRATION OF TWO EXAMPLES OF HDB3 ENCODING



The user chooses between AMI or HDB3 line coding by writing to bit 4 of the I/O Control Register (Address = 0x01), as shown below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ZeroSup*	Unipolar/ Bipolar*	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 54 relates the content of this bit-field to the Bipolar Line Code that E3 Data will be transmitted and received at.

TABLE 54: THE RELATIONSHIP BETWEEN BIT 4 (AMI/HDB3*) WITHIN THE I/O CONTROL REGISTER AND THE BIPOLAR LINE CODE THAT IS OUTPUT BY THE TRANSMIT E3 LIU INTERFACE BLOCK

BIT 4	BIPOLAR LINE CODE
0	HDB3
1	AMI

NOTES:

1. *This bit is ignored if the Unipolar mode is selected.*
2. *This selection also effects the operation of the Receive E3 LIU Interface block*

5.2.5.2 *TxLineClk Clock Edge Selection*

The Framer also allows the user to specify whether the E3 output data (via TxPOS and/or TxNEG output pins) is to be updated on the rising or falling edges of the TxLineClk signal. This selection is made by writing to bit 2 of the I/O Control Register, as depicted below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ZeroSup*	Unipolar/ Bipolar*	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 55 relates the contents of this bit field to the clock edge of TxClk that E3 Data is output on the TxPOS and/or TxNEG output pins.

TABLE 55: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 2 (TXLINECLK INV) WITHIN THE I/O CONTROL REGISTER AND THE TXLINECLK CLOCK EDGE THAT TXPOS AND TXNEG ARE UPDATED ON

BIT 2	RESULT
0	**Rising Edge:** Outputs on TxPOS and/or TxNEG are updated on the rising edge of TxLineClk. See Figure 113 for timing relationship between TxLineClk, TxPOS and TxNEG signals, for this selection.
1	**Falling Edge:** Outputs on TxPOS and/or TxNEG are updated on the falling edge of TxLineClk. See Figure 114 for timing relationship between TxLineClk, TxPOS and TxNEG signals, for this selection.

NOTE: *The user will typically make the selection based upon the set-up and hold time requirements of the Transmit LIU IC.*

FIGURE 113. WAVEFORM/TIMING RELATIONSHIP BETWEEN TXLINECLK, TXPOS AND TXNEG - TXPOS AND TXNEG ARE CONFIGURED TO BE UPDATED ON THE RISING EDGE OF TXLINECLK

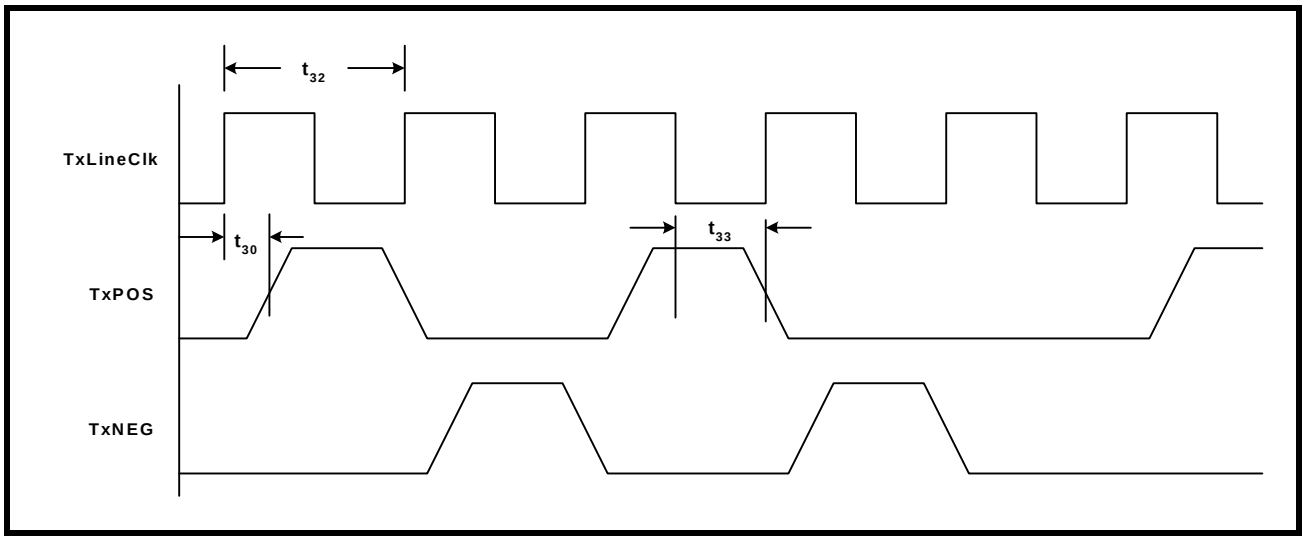
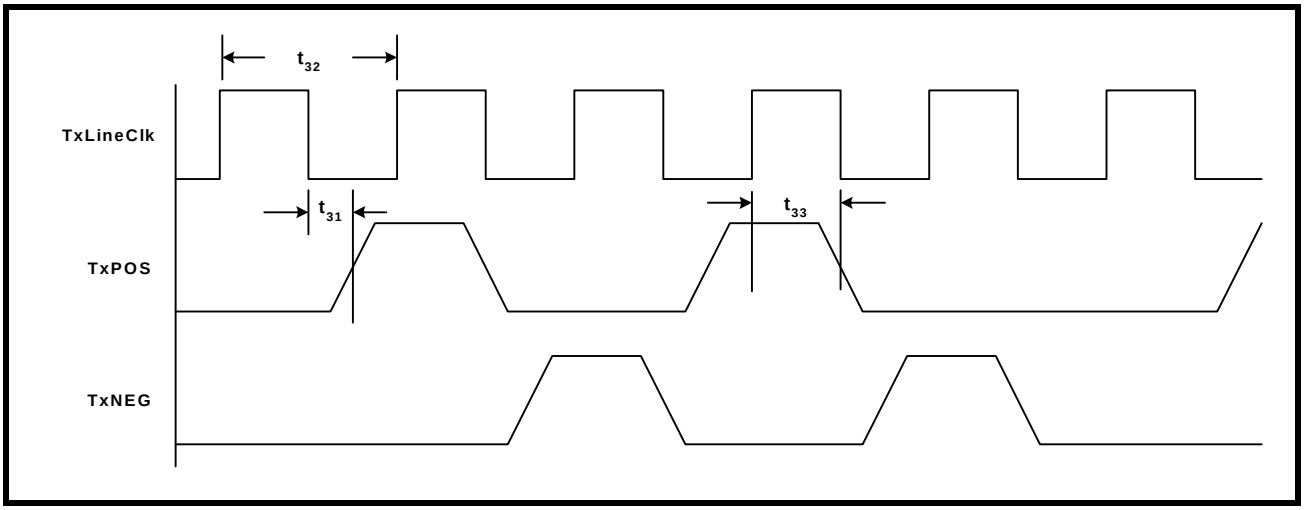


FIGURE 114. WAVEFORM/TIMING RELATIONSHIP BETWEEN TXLINECLK, TXPOS AND TXNEG - TXPOS AND TXNEG ARE CONFIGURED TO BE UPDATED ON THE FALLING EDGE OF TXLINECLK



5.2.6 Transmit Section Interrupt Processing

The Transmit Section of the XRT72L50 can generate an interrupt to the Microprocessor/Microcontroller for the following reasons.

- Completion of Transmission of LAPD Message

5.2.6.1 *Enabling Transmit Section Interrupts*

The Interrupt Structure, within the XRT72L50 contains two hierarchical levels:

- Block Level
- Source Level

The Block Level

The Enable State of the Block Level for the Transmit Section Interrupts dictates whether or not interrupts (enabled) at the source level, are actually enabled.

The user can enable or disable these Transmit Section interrupts, at the Block Level by writing the appropriate data into Bit 1 (Tx DS3/E3 Interrupt Enable) within the Block Interrupt Enable register (Address = 0x04), as illustrated below.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One-Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables the Transmit Section (at the Block Level) for Interrupt Generation. Conversely, setting this bit-field to “0” disables the Transmit Section for interrupt generation.

What does it mean for the Transmit Section Interrupts to be enabled or disabled at the Block Level?

If the Transmit Section is disabled (for interrupt generation) at the Block Level, then ALL Transmit Section interrupts are disabled, independent of the interrupt enable/disable state of the source level interrupts.

If the Transmit Section is enabled (for interrupt generation) at the block level, then a given interrupt will be enabled if it is also enabled at the source level. Conversely, if the Transmit Section is enabled (for interrupt generation) at the Block level, then a given interrupt will still be disabled, if it is disabled at the source level.

As mentioned earlier, the Transmit Section of the XRT72L50 Framer IC contains the Completion of Transmission of LAPD Message Interrupt.

The Enabling/Disabling and Servicing of this interrupt is presented below.

5.2.6.1.1 The Completion of Transmission of the LAPD Message Interrupt

If the Transmit Section interrupts have been enabled at the Block level, then the user can enable or disable the Completion of Transmission of a LAPD Message Interrupt, by writing the appropriate value into Bit 1 (TxLAPD Interrupt Enable) within the Tx E3 LAPD Status & Interrupt Register (Address = 0x34), as illustrated below.

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TXDL Start	TXDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	X	0

Setting this bit-field to “1’ enables the Completion of Transmission of a LAPD Message Interrupt. Conversely, setting this bit-field to “0” disables the Completion of Transmission of a LAPD Message interrupt.

5.2.6.1.2 Servicing the Completion of Transmission of a LAPD Message Interrupt

As mentioned previously, once the user commands the LAPD Transmitter to begin its transmission of a LAPD Message, it will do the following.

1. It will compute the FCS (Frame Check Sequence) value over the contents of 0x86 through 0xDB and append this 16 bit value to the back-end of the user-message.
2. It will parse through the contents of the Transmit LAPD Message Buffer (located at address locations 0x86 through 0xDB and the FCS bytes) and search for a string of five (5) consecutive “1’s”. If the LAPD Transmitter finds a string of five consecutive “1’s” (within the content of the LAPD Message Buffer, then it will insert a “0” immediately after this string. (Except at 0x86 which should contain the flag sequence byte 0x7E.)
3. It will append a trailing flag sequence byte, 0x7E.
4. Finally, it will begin transmitting the contents of this LAPD Message frame via the N bits, within each outbound E3 frame.
5. Once the LAPD Transmitter has completed its transmission of this LAPD Message frame (to the Remote Terminal Equipment), the XRT72L50 Framer IC will generate the Completion of Transmission of a LAPD Message Interrupt to the Microcontroller/Microprocessor. Once the XRT72L50 Framer IC generates this interrupt, it will do the following.

- Assert the Interrupt Output pin ($\overline{\text{Int}}$) by toggling it "Low".
- Set Bit 0 (TxLAPD Interrupt Status) within the TxE3 LAPD Status and Interrupt Register, to “1” as illustrated below.

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TXDL Start	TXDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	1

The purpose of this interrupt is to alert the Microcontroller/MIcroprocessor that the LAPD Transmitter has completed its transmission of a given LAPD (or PMDL) Message, and is now ready to transmit the next PMDL Message, to the Remote Terminal Equipment.

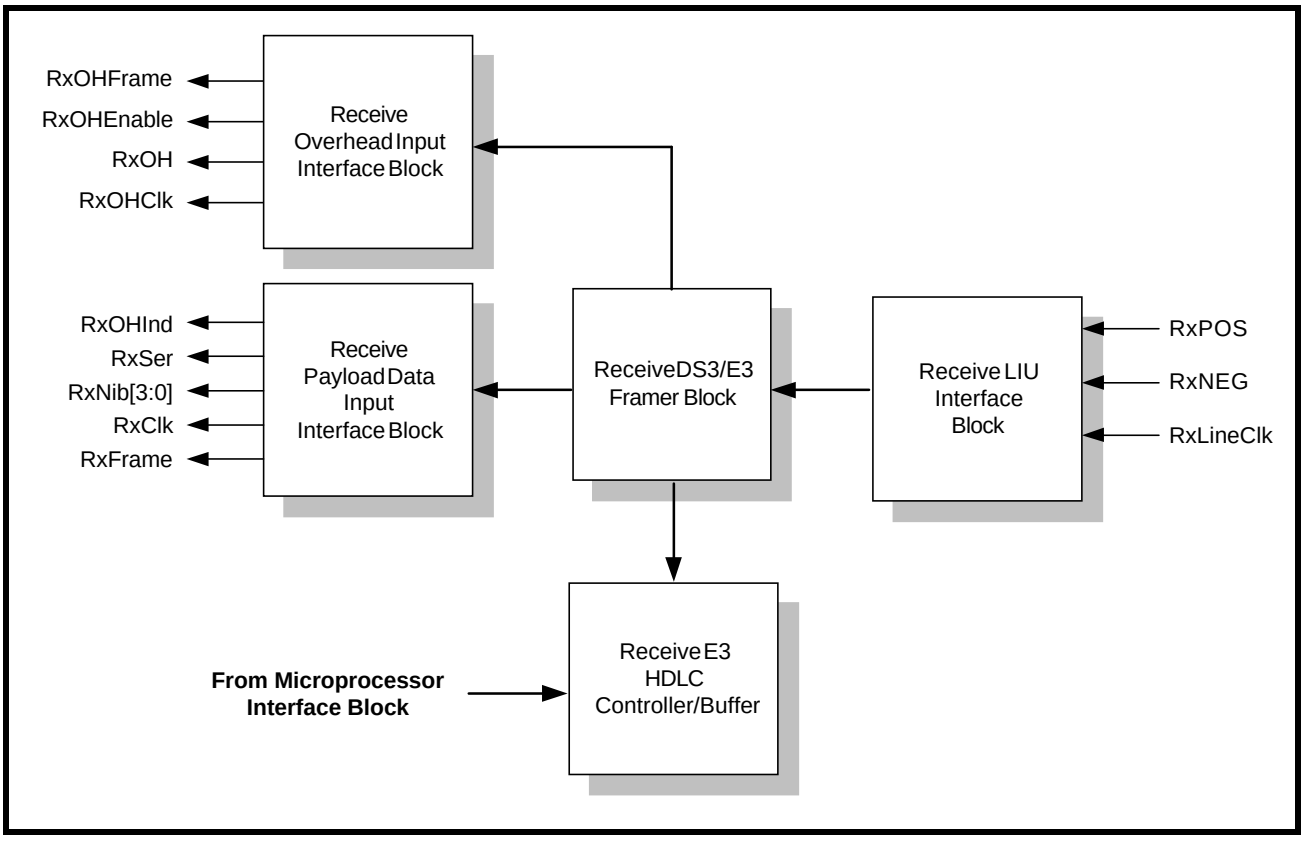
5.3 *The Receive Section of the XRT72L50 (E3 Mode Operation)*

When the XRT72L50 has been configured to operate in the E3 Mode, the Receive Section of the XRT72L50 consists of the following functional blocks.

- Receive LIU Interface block
- Receive HDLC Controller block
- Receive E3 Framer block
- Receive Overhead Data Output Interface block
- Receive Payload Data Output Interface block

Figure 115 presents a simple illustration of the Receive Section of the XRT72L50 Framer IC.

FIGURE 115. THE XRT72L50 RECEIVE SECTION CONFIGURED TO OPERATE IN THE E3 MODE



Each of these functional blocks will be discussed in detail in this document.

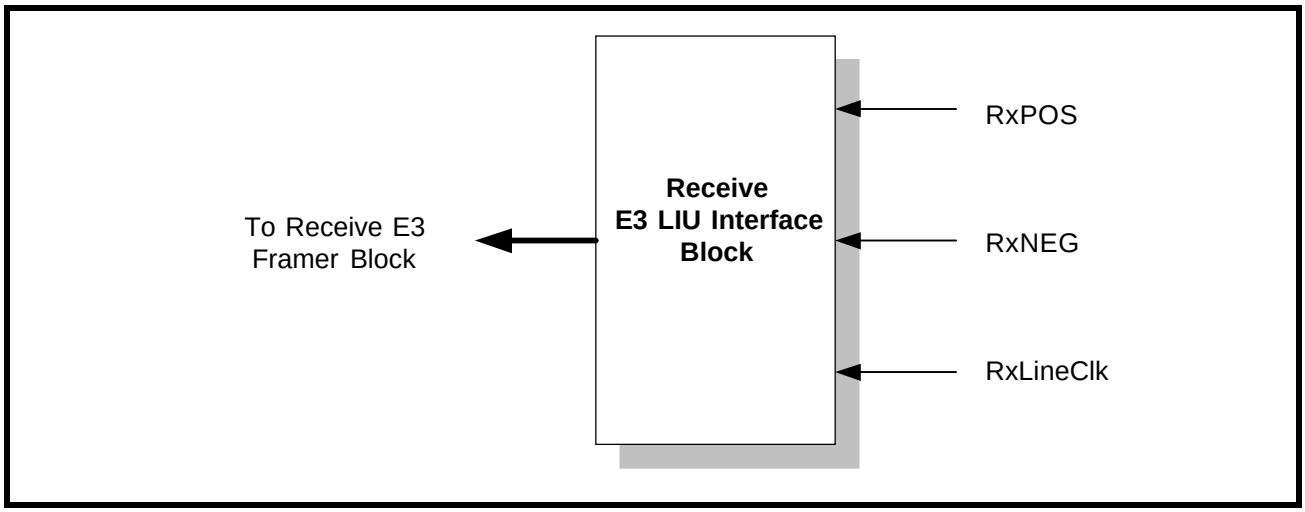
5.3.1 The Receive E3 LIU Interface Block

The purpose of the Receive E3 LIU Interface block is two-fold:

1. To receive encoded digital data from the E3 LIU IC.
2. To decode this data, convert it into a binary data stream and to route this data to the Receive E3 Framer block.

Figure 116 presents a simple illustration of the Receive E3 LIU Interface block.

FIGURE 116. THE RECEIVE E3 LIU INTERFACE BLOCK



The Receive Section of the XRT72L50 will via the Receive E3 LIU Interface Block receive timing and data information from the incoming E3 data stream. The E3 Timing information will be received via the RxLineClk input pin and the E3 data information will be received via the RxPOS and RxNEG input pins. The Receive E3 LIU Interface block is capable of receiving E3 data pulses in unipolar or bipolar format. If the Receive E3 framer is operating in the bipolar format, then it can be configured to decode either AMI or HDB3 line code data. Each of these input formats and line codes will be discussed in detail, below.

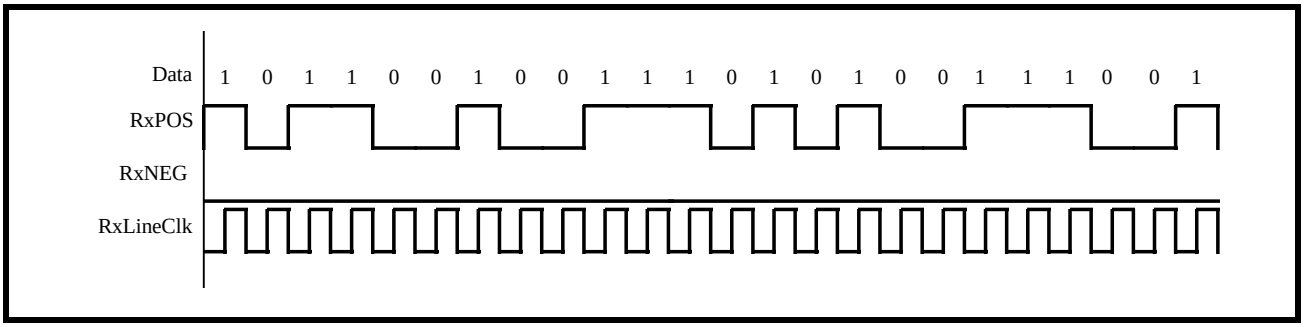
5.3.1.1 *Unipolar Decoding*

If the Receive E3 LIU Interface block is operating in the Unipolar (single-rail) mode, then it will receive the Single Rail NRZ E3 data pulses via the RxPOS input pin. The Receive E3 LIU Interface block will also receive its timing signal via the RxLineClk signal.

NOTE: *The RxLineClk signal will function as the timing source for the entire Receive Section of the XRT72L50.*

No data pulses will be applied to the RxNEG input pin. The Receive E3 LIU Interface block receives a logic "1" when a logic "1" level signal is present at the RxPOS pin, during the sampling edge of the RxLineClk signal. Likewise, a logic "0" is received when a logic "0" level signal is applied to the RxPOS pin. Figure 117 presents an illustration of the behavior of the RxPOS, RxNEG and RxLineClk input pins when the Receive E3 LIU Interface block is operating in the Unipolar mode.

FIGURE 117. BEHAVIOR OF THE RXPOS, RXNEG AND RXLINECLK SIGNALS DURING DATA RECEPTION OF UNIPOLAR DATA



The user can configure the Receive E3 LIU Interface block to operate in either the Unipolar or the Bipolar Mode by writing the appropriate data to the I/O Control Register, as depicted below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ZeroSup*	Unipolar/ Bipolar*	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 56 relates the value of this bit-field to the Receive E3 LIU Interface Input Mode.

TABLE 56: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 2 (TXLINECLK INV) WITHIN THE I/O CONTROL REGISTER AND THE TXLINECLK CLOCK EDGE THAT TXPOS AND TXNEG ARE UPDATED ON

BIT 3	RECEIVE E3 LIU INTERFACE INPUT MODE
0	**Bipolar Mode (Dual Rail):** AMI or HDB3 Line Codes are Transmitted and Received.
1	**Unipolar Mode (Single Rail) Mode** of transmission and reception of E3 data is selected.

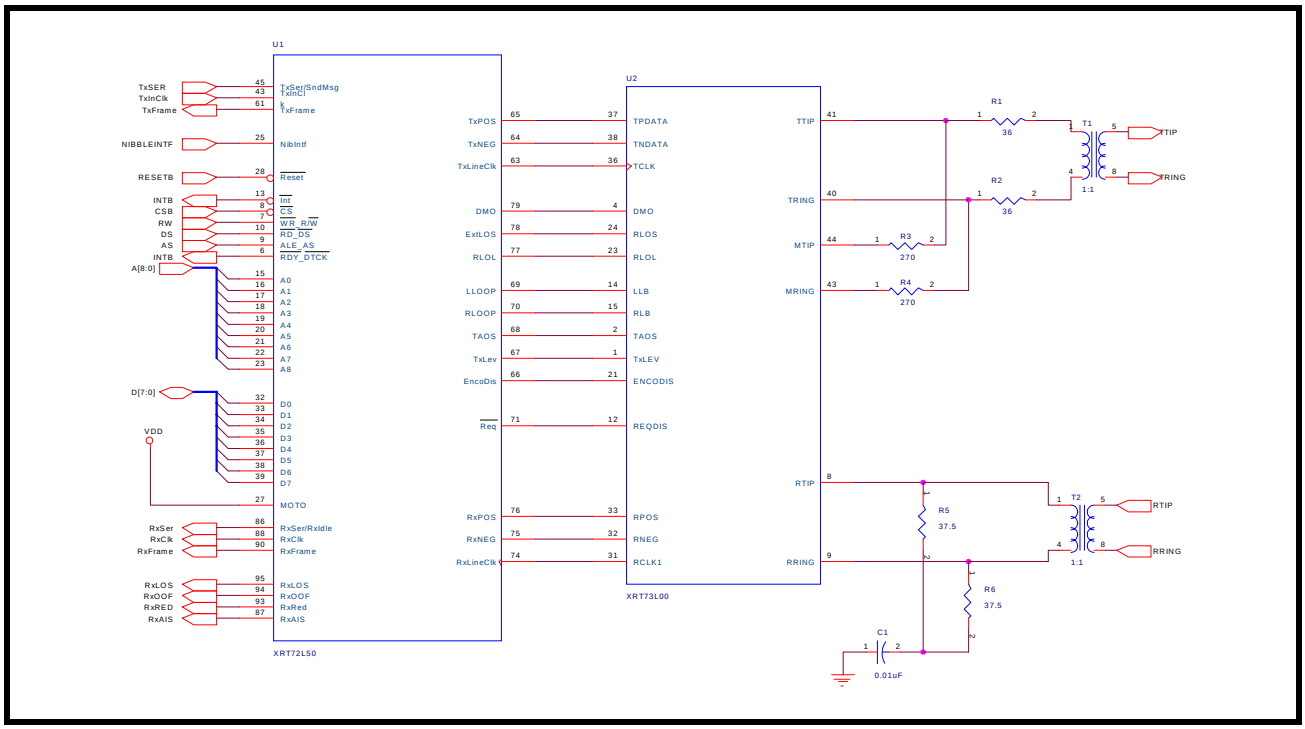
NOTES:

1. *The default condition is the Bipolar Mode.*
2. *This selection also effects the Transmit E3 Framer Line Interface Output Mode*

5.3.1.2 *Bipolar Decoding*

If the Receive E3 LIU Interface block is operating in the Bipolar Mode, then it will receive the E3 data pulses via both the RxPOS, RxNEG, and the RxLineClk input pins. Figure 118 presents a circuit diagram illustrating how the Receive E3 LIU Interface block interfaces to the Line Interface Unit while the Framer is operating in Bipolar mode. The Receive E3 LIU Interface block can be configured to decode either the AMI or HDB3 line codes.

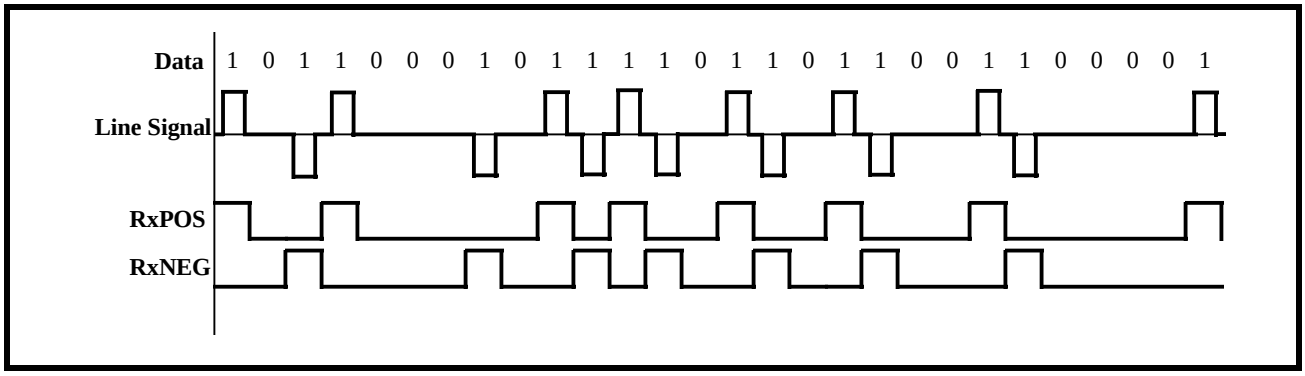
FIGURE 118. INTERFACING THE XRT72L50 FRAMER IC TO THE XRT73L00 DS3/E3/STS-1 LIU



5.3.1.2.1 AMI Decoding

AMI or Alternate Mark Inversion, means that consecutive "one's" pulses (or marks) will be of opposite polarity with respect to each other. This line code involves the use of three different amplitude levels: +1, 0, and -1. The +1 and -1 amplitude signals are used to represent one's (or mark) pulses and the "0" amplitude pulses (or the absence of a pulse) are used to represent zeros (or space) pulses. The general rule for AMI is: if a given mark pulse is of positive polarity, then the very next mark pulse will be of negative polarity and vice versa. This alternating-polarity relationship exists between two consecutive mark pulses, independent of the number of zeros that exist between these two pulses. Figure 119 presents an illustration of the AMI Line Code as would appear at the RxPOS and RxNEG pins of the Framer, as well as the output signal on the line.

FIGURE 119. ILLUSTRATION OF AMI LINE CODE



NOTE: *One of the reasons that the AMI Line Code has been chosen for driving copper medium, isolated via transformers, is that this line code has no dc component, thereby eliminating dc distortion in the line.*

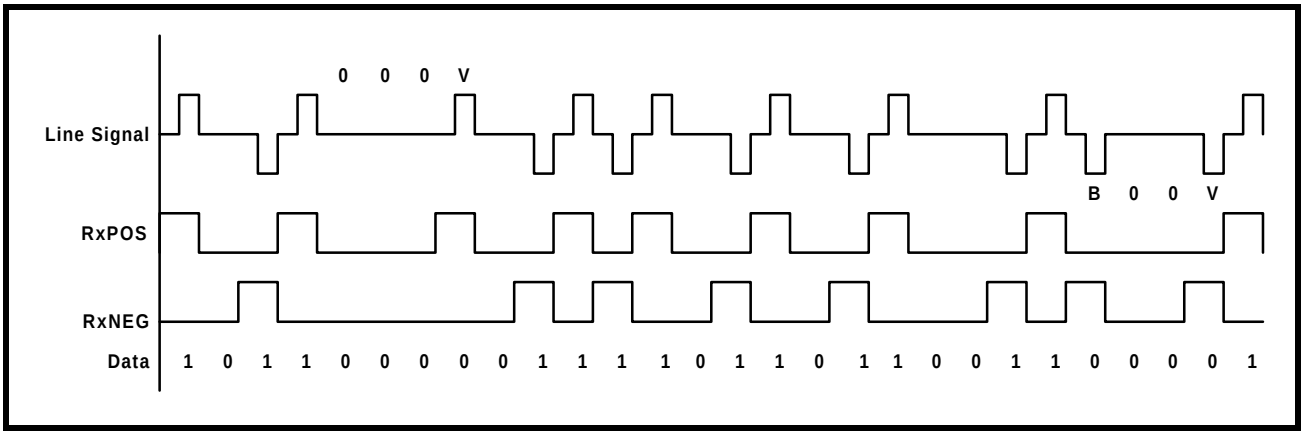
5.3.1.2.2 HDB3 Decoding

The Transmit E3 LIU Interface block and the associated LIU embed and combine the data and clocking information into the line signal that is transmitted to the remote terminal equipment. The remote terminal

equipment has the task of recovering this data and timing information from the incoming E3 data stream. Most clock and data recovery schemes rely on the use of Phase-Locked-Loop technology. One of the problems of using Phase-Locked-Loop (PLL) technology for clock recovery is that it relies on transitions in the line signal, in order to maintain lock with the incoming E3 data-stream. Therefore, these clock recovery scheme, are vulnerable to the occurrence of a long stream of consecutive zeros (e.g., no transitions in the line). This scenario can cause the PLL to lose lock with the incoming E3 data, thereby causing the clock and data recovery process of the receiver to fail. Therefore, some approach is needed to insure that such a long string of consecutive zeros can never happen. One such technique is HDB3 (or High Density Bipolar -3) encoding.

In general the HDB3 line code behaves just like AMI with the exception of the case when a long string of consecutive zeros occurs on the line. Any 4 consecutive zeros will be replaced with either a "000V" or a "B00V" where "B" refers to a Bipolar pulse (e.g., a pulse with a polarity that is compliant with the AMI coding rule). And "V" refers to a Bipolar Violation pulse (e.g., a pulse with a polarity that violates the alternating polarity scheme of AMI.) The decision between inserting an "000V" or a "B00V" is made to insure that an odd number of Bipolar (B) pulses exist between any two Bipolar Violation (V) pulses. The Receive E3 LIU Interface block, when operating with the HDB3 Line Code is responsible for decoding the HD-encoded data back into a unipolar (binary-format). For instance, if the Receive E3 LIU Interface block detects a "000V" or a "B00V" pattern in the incoming pattern, the Receive E3 LIU Interface block will replace it with four (4) consecutive zeros. Figure 120 presents a timing diagram that illustrates examples of HDB3 decoding.

FIGURE 120. ILLUSTRATION OF TWO EXAMPLES OF HDB3 DECODING



5.3.1.2.3 Line Code Violations

The Receive E3 LIU Interface block will also check the incoming E3 data stream for line code violations. For example, when the Receive E3 LIU Interface block detects a valid bipolar violation (e.g., in HDB3 line code), it will substitute four zeros into the binary data stream. However, if the bipolar violation is invalid, then an LCV (Line Code Violation) is flagged and the PMON LCV Event Count Register (Address = 0x50 and 0x51) will also be incremented. Additionally, the LCV-One-Second Accumulation Registers (Address = 0x6E and 0x6F) will be incremented. For example: If the incoming E3 data is HDB3 encoded, the Receive E3 LIU Interface block will also increment the LCV One-Second Accumulation Register if three (or more) consecutive zeros are received.

5.3.1.2.4 RxLineClk Clock Edge Selection

The incoming unipolar or bipolar data, applied to the RxPOS and the RxNEG input pins are clocked into the Receive E3 LIU Interface block via the RxLineClk signal. The Framer IC allows the user to specify which edge (e.g, rising or falling) of the RxLineClk signal will sample and latch the signal at the RxPOS and RxNEG input signals into the Framer IC. The user can make this selection by writing the appropriate data to bit 1 of the I/O Control Register, as depicted below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 57 depicts the relationship between the value of this bit-field to the sampling clock edge of RxLineClk.

TABLE 57: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 1 (RXLINECLK INV) OF THE I/O CONTROL REGISTER, AND THE SAMPLING EDGE OF THE RXLINECLK SIGNAL

RXCLKINV (BIT 1)	RESULT
0	**Rising Edge:** RxPOS and RxNEG are sampled at the rising edge of RxLineClk. See Figure 121 for timing relationship between RxLineClk, RxPOS, and RxNEG.
1	**Falling Edge:** RxPOS and RxNEG are sampled at the falling edge of RxLineClk. See Figure 122 for timing relationship between RxLineClk, RxPOS, and RxNEG.

Figure 121 and Figure 122 present the Waveform and Timing Relationships between RxLineClk, RxPOS and RxNEG for each of these configurations.

FIGURE 121. WAVEFORM/TIMING RELATIONSHIP BETWEEN RXLINECLK, RXPOS AND RXNEG - WHEN RXPOS AND RXNEG ARE TO BE SAMPLED ON THE RISING EDGE OF RXLINECLK

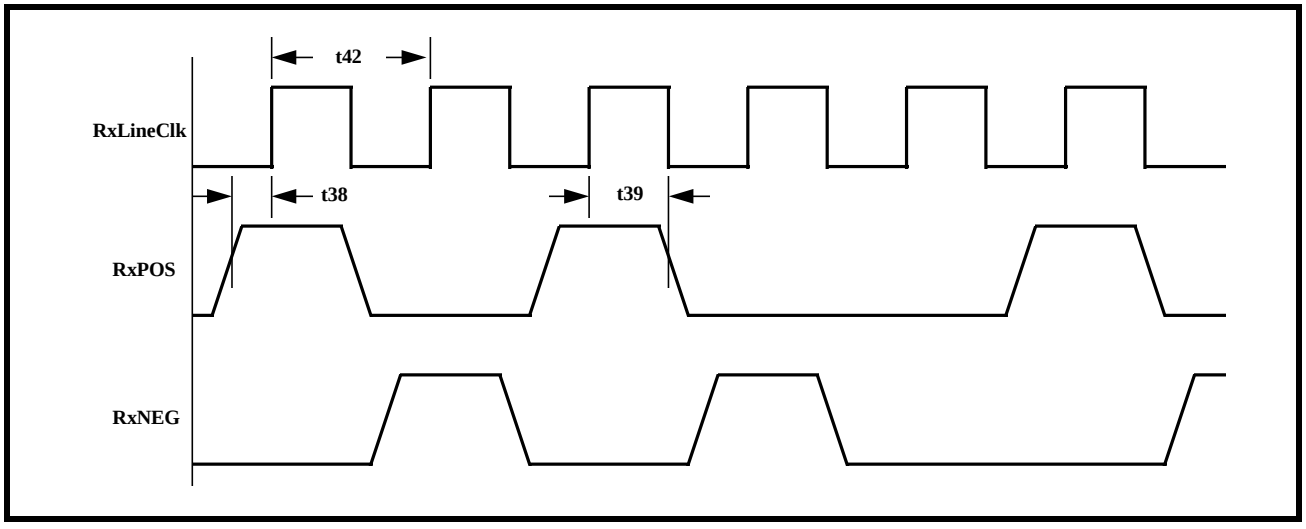
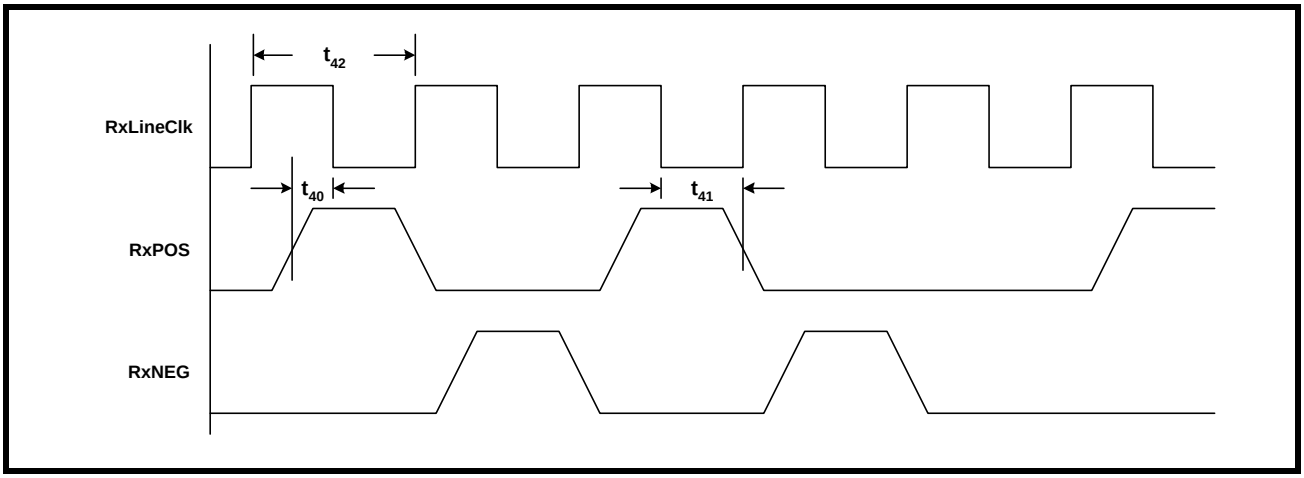


FIGURE 122. WAVEFORM/TIMING RELATIONSHIP BETWEEN RXLINECLK, RXPOS AND RXNEG - WHEN RXPOS AND RXNEG ARE TO BE SAMPLED ON THE FALLING EDGE OF RXLINECLK



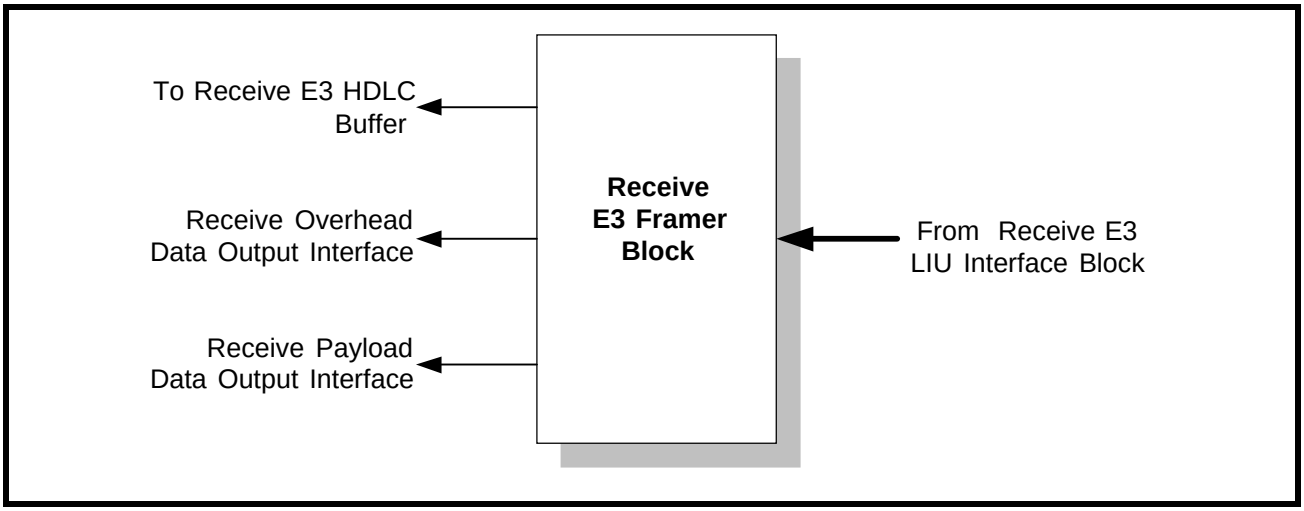
5.3.2 The Receive E3 Framer Block

The Receive E3 Framer block accepts decoded E3 data from the Receive E3 LIU Interface block, and routes data to the following destinations.

- The Receive Payload Data Output Interface Block
- The Receive Overhead Data Output Interface Block.
- The Receive E3 HDLC Controller Block

Figure 123 presents a simple illustration of the Receive E3 Framer block along with the associated paths to the other functional blocks within the Framer chip.

FIGURE 123. THE RECEIVE E3 FRAMER BLOCK AND THE ASSOCIATED PATHS TO OTHER FUNCTIONAL BLOCKS



Once the HDB3 (or AMI) encoded data has been decoded into a binary data-stream, the Receive E3 Framer block will use portions of this data-stream in order to synchronize itself to the remote terminal equipment. At any given time, the Receive E3 Framer block will be operating in one of two modes.

- **The Frame Acquisition Mode:** In this mode, the Receive E3 Framer block is trying to acquire synchronization with the incoming E3 frame, or

- **The Frame Maintenance Mode:** In this mode, the Receive E3 Framer block is trying to maintain frame synchronization with the incoming E3 Frames.

Figure 124 presents a State Machine diagram that depicts the Receive E3 Framer block's E3/ITU-T G.751 Frame Acquisition/Maintenance Algorithm.

5.3.2.1 *The Framing Acquisition Mode*

The Receive E3 Framer block is considered to be operating in the Frame Acquisition Mode, if it is operating in any one of the following states within the E3 Frame Acquisition/Maintenance Algorithm per Figure 124.

- FAS Pattern Search State
- FAS Pattern Verification State
- OOF Condition State
- LOF Condition State

Each of these Framing Acquisition states, within the Receive E3 Framer Framing Acquisition/Maintenance State Machine are discussed below.

The FAS Pattern Search State

When the Receive E3 Framer block is first powered up, it will be operating in the FAS Pattern Search state. While the Receive E3 Framer is operating in this state, it will be performing a bit-by-bit search for the FAS (Framing Alignment Signal) pattern of, 1111010000. Figure 125, which presents an illustration of the E3, ITU-T G.751 Framing Format, indicates that this framing alignment signal will occur at the beginning of each E3 frame.

FIGURE 124. THE STATE MACHINE DIAGRAM FOR THE RECEIVE E3 FRAMER E3 FRAME ACQUISITION/MAINTENANCE ALGORITHM

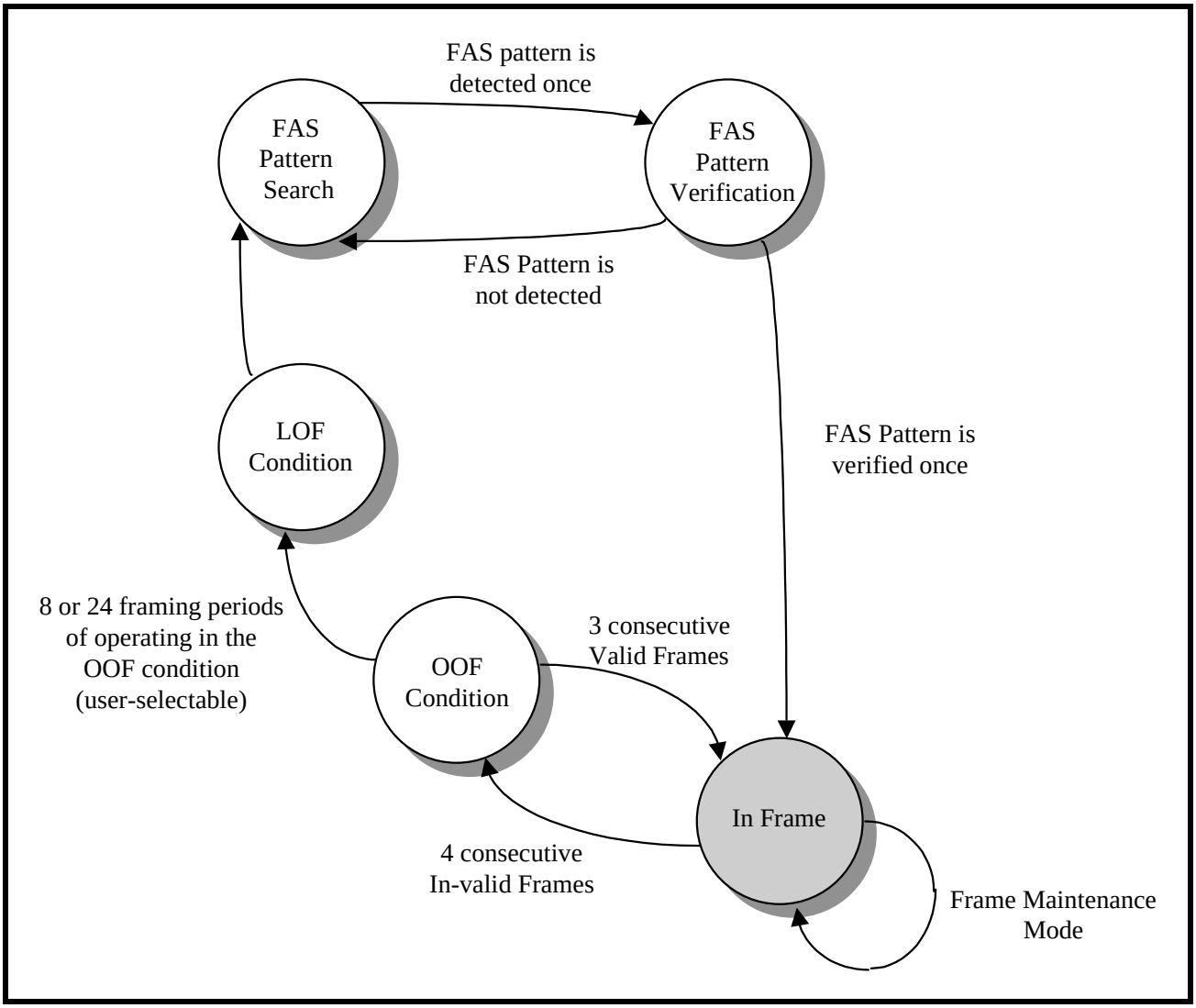
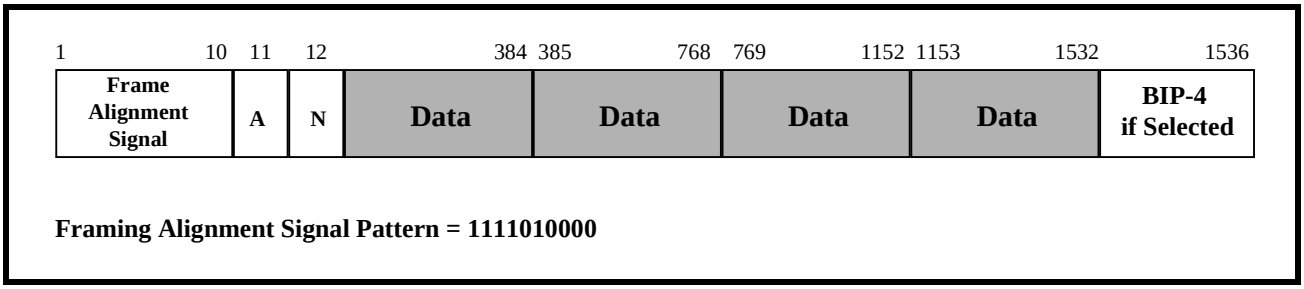


FIGURE 125. ILLUSTRATION OF THE E3, ITU-T G.751 FRAMING FORMAT



When the Receive E3 Framer block detects the FAS pattern, it will then transition over to the FAS Pattern Verification state, per Figure 125.

The FAS Pattern Verification State

Once the Receive E3 Framer block has detected a 1111010000 pattern, it must verify that this pattern is indeed the FAS pattern and not some other set of bits, within the E3 frame, mimicking the FAS Pattern. Hence, the purpose of the FAS Pattern Verification state.

When the Receive E3 Framer block enters this state, it will then quit performing its bit-by-bit search for the Frame Alignment Signaling bits. Instead, the Receive E3 Framer block will read in the 10 bits that occur 1536 bit (e.g., one E3 frame period later) after the candidate FAS pattern was first detected. If these ten bits match the assigned values for the FAS Pattern octets, then the Receive E3 Framer block will conclude that it has found the FAS pattern and will then transition to the In-Frame state. However, if these two bytes do not match the assigned values for the FAS pattern then the Receive E3 Framer block will concluded that it has been fooled by data mimicking the Frame Alignment bytes, and will transition back to the FAS Pattern Search state.

In Frame State

Once the Receive E3 Framer block enters the In-Frame state, then it will cease performing Frame Acquisition functions, and will proceed to perform Framing Maintenance functions. Therefore, the operation of the Receive E3 Framer block, while operating in the In-Frame state, can be found in Section 5.3.2.2 (The Framing Maintenance Mode).

OOF (Out of Frame) Condition State

If the Receive E3 Framer while operating in the In-Frame state detects four (4) consecutive frames, which do not have the valid Frame Alignment Signaling (FAS) patterns, then it will transition into the OOF Condition State. The Receive E3 Framer block's operation, while in the OOF condition state is a unique mix of Framing Maintenance and Framing Acquisition operation. The Receive E3 Framer block will exhibit some Framing Acquisition characteristics by attempting to locate (once again) the FAS pattern. However, the Receive E3 Framer block will also exhibit some Frame Maintenance behavior by still using the most recent frame synchronization for its overhead bits and payload bits processing.

The Receive E3 Framer block will inform the Microprocessor/Microcontroller of its transition from the In-Frame state to the OOF Condition state, by generating a Change in OOF Condition Interrupt. When this occurs, Bit 3 (OOF Interrupt Status), within the Rx E3 Interrupt Status Register - 1, will be set to "1", as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

The Receive E3 Framer block will also inform the external circuitry of its transition into the OOF Condition state, by toggling the RxOOF output pin "High".

If the Receive E3 Framer block is capable of finding the FAS pattern within a user-selectable number of E3 frame periods, then it will transition back into the In-Frame state. The Receive E3 Framer block will then inform the Microprocessor/Microcontroller of its transition back into the In-Frame state by generating the Change in OOF Condition Interrupt.

However, if the Receive E3 Framer block resides in the OOF Condition state for more than this user-selectable number of E3 frame periods, then it will automatically transition to the LOF (Loss of Frame) Condition state.

The user can select this user-selectable number of E3 frame periods that the Receive E3 Framer block will remain in the OOF Condition state by writing the appropriate value into Bit 7 (RxLOF Algo) within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	X	X	X	X

Writing a “0” into this bit-field causes the Receive E3 Framer block to reside in the OOF Condition state for at most 24 E3 frame periods. Writing a “1” into this bit-field causes the Receive E3 Framer block to reside in the OOF Condition state for at most 8 E3 frame periods.

LOF (Loss of Framing) Condition State

If the Receive E3 Framer block enters the LOF Condition state, then the following things will happen.

- The Receive E3 Framer block will discard the most recent frame synchronization and,
- The Receive E3 Framer block will make an unconditional transition to the FAS Pattern Search state.
- The Receive E3 Framer block will notify the Microprocessor/Microcontroller of its transition to the LOF Condition state, by generating the Change in LOF Condition interrupt. When this occurs, Bit 2 (LOF Interrupt Status), within the Rx E3 Interrupt Status Register - 1 will be set to “1”, as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

Finally, the Receive E3 Framer block will also inform the external circuitry of this transition to the LOF Condition state by toggling the RxLOF output pin "High”.

5.3.2.2 *The Framing Maintenance Mode*

Once the Receive E3 Framer block enters the In-Frame state, then it will notify the Microprocessor/ Microcontroller of this fact by generating both the Change in OOF Condition and Change in LOF Condition Interrupts. When this happens, bits 2 and 3 (LOF Interrupt Status and OOF Interrupt Status) will be set to “1”, as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	1	0	0

Additionally, the Receive E3 Framer block will inform the external circuitry of its transition to the In-Frame state by toggling both the RxOOF and RxLOF output pins "Low".

Finally, the Receive E3 Framer block will negate both the RxOOF and the RxLOF bit-fields within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	X	X	X

When the Receive E3 Framer block is operating in the In-Frame state, it will then begin to perform Frame Maintenance operations, where it will continue to verify that the Frame Alignment signal (FAS pattern) is present, and at its proper location. While the Receive E3 Framer block is operating in the Frame Maintenance Mode, it will declare an Out-of-Frame (OOF) Condition if it detects an invalid FAS pattern in four consecutive frames.

Since the Receive E3 Framer block requires the detection of an invalid FAS pattern in four consecutive frames, in order for it to transition to the OOF Condition state, it can tolerate some errors in the Framing Alignment bytes, and still remain in the In-Frame state. However, each time the Receive E3 Framer block detects an error in the FAS pattern, it will increment the PMON Framing Error Event Count Registers (Address = 0x52 and 0x53). The bit-format for these two registers are depicted below.

PMON Framing Bit/Byte Error Count Register - MSB (Address = 0x52)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit/Byte Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON Framing Bit/Byte Error Count Register - LSB (Address = 0x53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit/Byte Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

5.3.2.3 *Forcing a Reframe via Software Command*

The XRT72L50 Framer IC permits the user to command a reframe procedure with the Receive E3 Framer block via software command. If the user writes a “1” into Bit 0 (Reframe) within the I/O Control Register (Address = 0x01), as depicted below, then the Receive E3 Framer block will be forced into the FAS Pattern Search state, per Figure 126, and will begin its search for the FAS Pattern.

I/O CONTROL REGISTER (ADDRESS = 0X01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ $\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine Clk Invert	RxLine Clk Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	1

The Framer IC will respond to this command by doing the following.

1. Asserting both the RxOOF and RxLOF output pins.
2. Generating both the Change in OOF Status and the Change in LOF Status interrupts to the Microprocessor.
3. Asserting both the RxLOF and RxOOF bit-fields within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	0	1	1	0

5.3.2.4 *Performance Monitoring of the Frame Synchronization Section, within the Receive E3 Framer block*

The user can monitor the number of FAS pattern errors that have been detected by the Receive E3 Framer block. This is accomplished by periodically reading the PMON Framing Bit/Byte Error Event Count Registers (Address = 0x52 and 0x53). The byte format of these registers are presented below.

5.3.2.5 *The RxOOF and RxLOF output pin.*

The user can roughly determine the current framing state that the Receive E3 Framer block is operating in by reading the logic state of the RxOOF and the RxLOF output pins. Table 58 presents the relationship between the state of the RxOOF and RxLOF output pins, and the Framing State of the Receive E3 Framer block.

TABLE 58: THE RELATIONSHIP BETWEEN THE LOGIC STATE OF THE RXOOF AND RXLOF OUTPUT PINS, AND THE FRAMING STATE OF THE RECEIVE E3 FRAMER BLOCK

RXLOF	RXOOF	FRAMING STATE OF THE RECEIVE E3 FRAMER BLOCK
0	0	In Frame
0	1	OOF Condition (The Receive E3 Framer block is operating in the 3ms OOF period).
1	0	Invalid
1	1	LOF Condition

5.3.2.6 *E3 Receive Alarms*

5.3.2.7 *The Loss of Signal (LOS) Alarm*

Declaring an LOS Condition

The Receive E3 Framer block will declare a Loss of Signal (LOS) Condition, when it detects 32 consecutive incoming “0’s” via the RxPOS and RxNEG input pins or if the ExtLOS input pin (from the XRT73L00 DS3/E3/STS-1 LIU IC) is asserted.

The Framer chip allows the user to modify the LOS Declaration criteria such that an LOS condition is declared only if the RLOS input pin (from the XRT73L00 DS3/E3/STS-1 LIU IC) is asserted. In this case, the internally-generated LOS criteria of 180 consecutive “zeros” will be disabled. This can be accomplished by writing a "0" to bit 5 (Internal LOS Enable) of the Framer Operating Mode Register, as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	0	0	X	X	X	X	X

NOTE: *For more information on the RLOS input pin, please see Section 2.1.*

The Receive E3 Framer block will indicate that it is declaring an LOS condition by.

- Asserting the RxLOS output pin (e.g., toggling it "High”).
- Setting Bit 4 (RxLOS) of the Rx E3 Configuration & Status Register to “1” as depicted below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	1	0	0	0	0

- The Receive E3 Framer block will generate a Change in LOS Condition interrupt request. Upon generating this interrupt request, the Receive E3 Framer block will assert Bit 1 (LOS Interrupt Status within the Rx E3 Framer Interrupt Status Register - 1, as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	1	0

Clearing the LOS Condition

The Receive E3 Framer block will clear the LOS condition when it encounters a stream of 32 bits that does not contain a string of 4 consecutive zeros or if ExtLOS pin goes “Low”.

When the Receive E3 Framer block clears the LOS condition, then it will notify the Microprocessor and the external circuitry of this occurrence by:

- Generating the Change in LOS Condition Interrupt to the Microprocessor.
- Clearing Bit 4 (RxLOS) within the Rx E3 Configuration & Status Register, as depicted below.

NOTE: *The Receive DS3 Framer block will also generate the Change in LOS Condition interrupt, when it clears the LOS Condition.*

The Framer chip allows the user to modify the LOS Declaration criteria such that an LOS condition is declared only if the RLOS input pin (from the XRT73L00 DS3/E3/STS-1 LIU IC) is asserted. In this case, the internally-generated LOS criteria of 180 consecutive “zeros” will be disabled. This can be accomplished by writing a "0" to bit 5 (Internal LOS Enable) of the Framer Operating Mode Register, as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	0	X	X	X	X	X

NOTE: *For more information on the RLOS input pin, please see Section 2.1.*

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	0	1	1	1

- Clear the RxLOS output pin (e.g., toggle it "Low”).

5.3.2.8 *The AIS (Alarm Indication Status) Condition*

Declaring the AIS Condition

The Receive E3 Framer block will identify and declare an AIS condition, if it detects an All Ones” pattern in the incoming E3 data stream. More specifically, the Receive E3 Framer block will declare an AIS Condition if 7 or less “0’s” are detected in each of 2 consecutive E3 frames.

If the Receive E3 Framer block declares an AIS Condition, then it will do the following.

- Generate the Change in AIS Condition Interrupt to the Microprocessor. Hence, the Receive E3 Framer block will assert Bit 0 (AIS Interrupt Status) within the Rx E3 Framer Interrupt Status register - 1, as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	1

- Assert the RxAIS output pin.
- Set Bit 3 (RxAIS) within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	1	1	1	1

Clearing the AIS Condition

The Receive E3 Framer block will clear the AIS condition when it detects two consecutive E3 frames, with eight or more zeros in the incoming data stream. The Receive E3 Framer block will inform the Microprocessor that the AIS Condition has been cleared by:

- Generating the Change in AIS Condition Interrupt to the Microprocessor. Hence, the Receive E3 Framer block will assert Bit 0 (AIS Interrupt Status) within the Rx E3 Framer Interrupt Status Register - 1.
- Clearing the RxAIS output pin (e.g., toggling it "Low").
- Setting the RxAIS bit-field, within the Rx E3 Configuration & Status Register to “0”, as depicted below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	0	0	0	X

5.3.2.9 *The Far-End-Receive Failure (FERF) Condition*

Declaring the FERF Condition

The Receive E3 Framer block will declare a Far-End Receive Failure (FERF) condition if it detects a user-selectable number of consecutive incoming E3 frames, with the A bit-field set to “1”.

This User-selectable number of E3 frames is either 3 or 5, depending upon the value that has been written into Bit 4 (RxFERF Algo) within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register - 1 G.751 (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			RxFERF Algo	Reserved			RxBIP4
RO	RO	RO	R/W	RO	RO	RO	R/W
0	0	0	X	0	0	0	0

Writing a “0” into this bit-field causes the Receive E3 Framer block to declare a FERF condition, if it detects 3 consecutive incoming E3 frames, that have the A bit set to “1”.

Writing a “1” into this bit-field causes the Receive E3 Framer block to declare a FERF condition, if it detects 5 consecutive incoming E3 frames, that have the A bit set to “1”.

Whenever the Receive E3 Framer block declares a FERF condition, then it will do the following.

- Generate a Change in FERF Condition interrupt to the Microprocessor. Hence, the Receive E3 Framer block will assert Bit 3 (FERF Interrupt Status) within the Rx E3 Framer Interrupt Status register - 2, as depicted below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Status	BIP-4 Error Interrupt Status	Framing Error Interrupt Status	Not Used
RO	RO	RO	RO	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

- Set the RxFERF bit-field, within the Rx E3 Configuration/Status Register to “1”, as depicted below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	0	0	0	1

Clearing the FERF Condition

The Receive E3 Framer block will clear the FERF condition once it has received a User-Selectable number of E3 frames with the A bit-field being set to “0” (e.g., no FERF condition). This User-Selectable number of E3 frames is either 3 or 5 depending upon the value that has been written into Bit 4 (RxFERF Algo) of the Rx E3 Configuration/Status Register, as discussed above.

Whenever the Receive E3 Framer clears the FERF status, then it will do the following:

1. Generate a Change in the FERF Status Interrupt to the Microprocessor.
2. Clear the Bit 0 (RxFERF) within the Rx E3 Configuration & Status register, as depicted below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	0	1	1	0

5.3.2.10 *Error Checking of the Incoming E3 Frames*

The Receive E3 Framer block can be configured to perform error-checking on the incoming E3 frame data that it receives from the Remote Terminal Equipment. If configured accordingly, the Receive E3 Framer block will perform this error-checking by computing the BIP-4 value of an incoming E3 frame. Once the Receive E3

Framer block has obtained this value, it will compare this value with that of the BIP-4 value that it receives, within the very next E3 frame. If the locally computed BIP-4 value matches the EM byte of the corresponding E3 frame, then the Receive E3 Framer block will conclude that this particular frame has been properly received. The Receive E3 Framer block will then inform the Remote Terminal Equipment of this fact by having the Local Terminal Equipment Transmit E3 Framer block send the Remote Terminal an E3 frame, with the A bit-field, set to "0".

This procedure is illustrated in Figure 126 and Figure 127, below.

Figure 126 illustrates the Local Receive E3 Framer receiving an error-free E3 frame. In this figure, the locally computed BIP-4 value of 0xA matches that received from the Remote Terminal, within the EM byte-field. Figure 127 illustrates the subsequent action of the Local Transmit E3 Framer block, which will transmit an E3 frame, with the A bit-field set to "0", to the Remote Terminal. This signaling indicates that the Local Receive E3 Framer has received an error-free E3 frame.

FIGURE 126. ILLUSTRATION OF THE LOCAL RECEIVE E3 FRAMER BLOCK, RECEIVING AN E3 FRAME (FROM THE REMOTE TERMINAL) WITH A CORRECT BIP-4 VALUE.

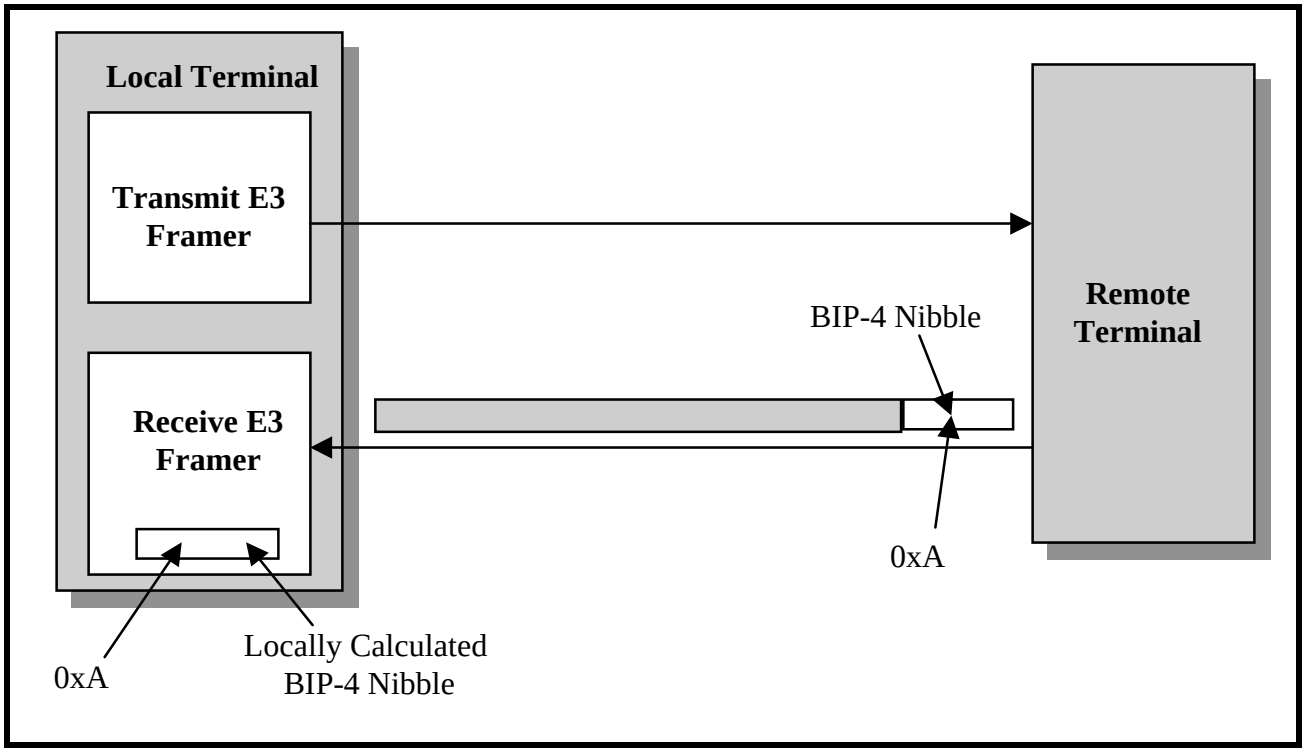
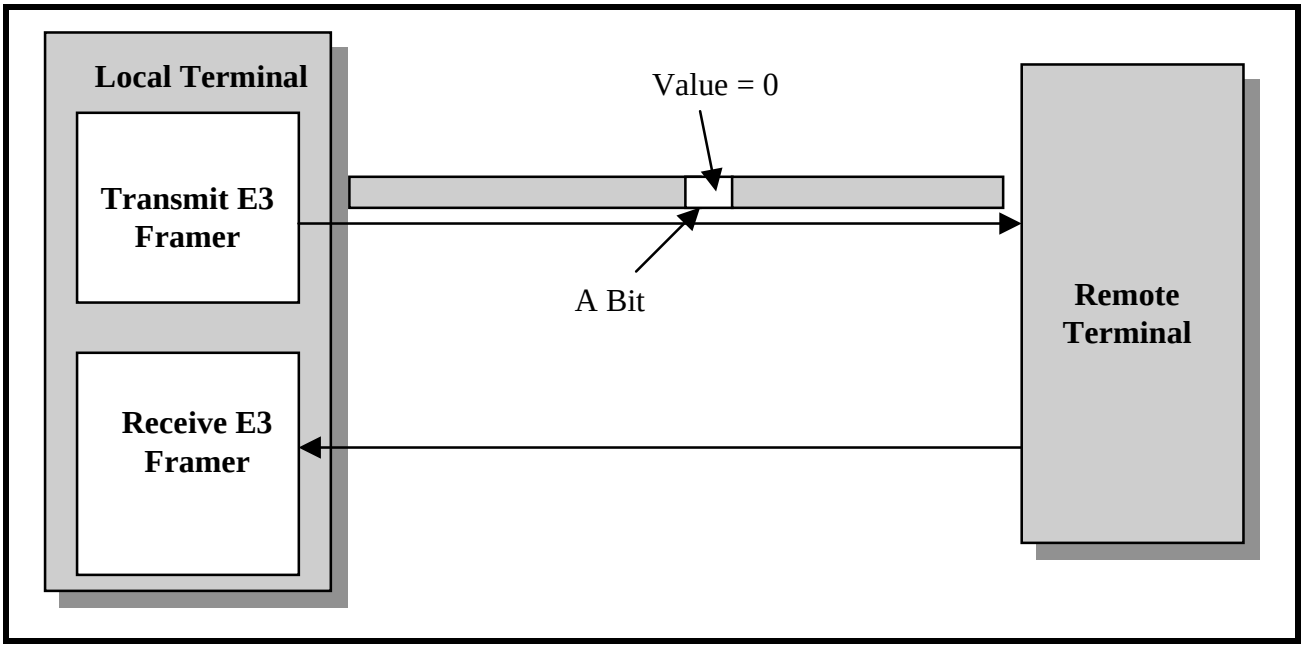


FIGURE 127. ILLUSTRATION OF THE LOCAL RECEIVE E3 FRAMER BLOCK, TRANSMITTING AN E3 FRAME (TO THE REMOTE TERMINAL) WITH THE A BIT SET TO "0"



However, if the locally computed BIP-4 value does not match the BIP-4 value of the corresponding E3 frame, then the Receive E3 Framer block will do the following.

- It will inform the Remote Terminal of this fact by having the Local Transmit E3 Framer block send the Remote Terminal an E3 frame, with the A bit-field set to "1". This phenomenon is illustrated below in Figure 128 and Figure 129.

Figure 128 illustrates the Local Receive E3 Framer receiving an errored E3 frame. In this figure, the Local Receive E3 Frame block is receiving an E3 frame with an BIP-4 containing the value, 0xA. This value does not match the locally computed BIP-4 value of, 0xB. Consequently, there is an error in the previous E3 frame.

Figure 129 illustrates the subsequent action of the Local Transmit E3 Framer block, which will transmit an E3 frame, with the A bit-field set to "1" to the Remote Terminal. This signaling indicates that the Local Receive E3 Framer block has received an errored E3 frame.

FIGURE 128. ILLUSTRATION OF THE LOCAL RECEIVE E3 FRAMER BLOCK, RECEIVING AN E3 FRAME (FROM THE REMOTE TERMINAL) WITH AN INCORRECT BIP-4 VALUE.

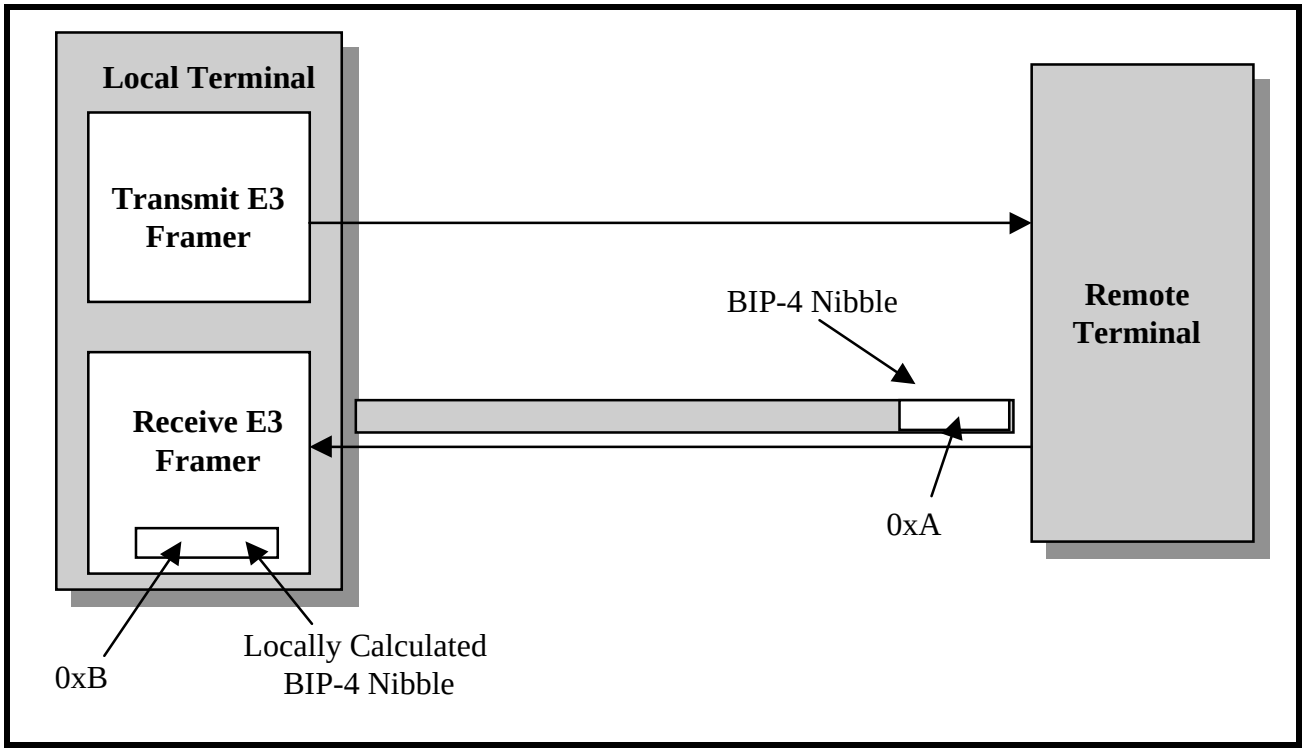
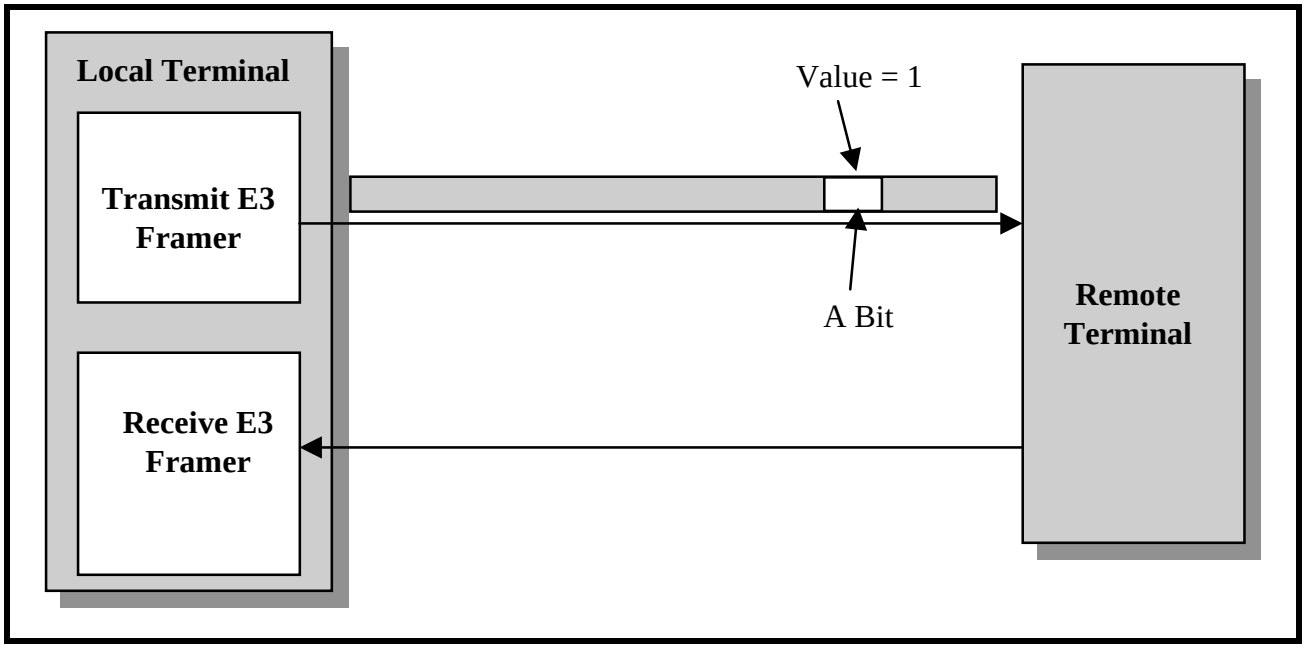


FIGURE 129. ILLUSTRATION OF THE LOCAL RECEIVE E3 FRAMER BLOCK, TRANSMITTING AN E3 FRAME (TO THE REMOTE TERMINAL) WITH THE A BIT-FIELD SET TO "1"



In additional to the FEBE bit-field signaling, the Receive E3 Framer block will generate the BIP-4 Error Interrupt to the Microprocessor. Hence, it will set bit 2 (BIP-4 Error Interrupt Status) to "1", as depicted below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Status	BIP-4 Error Interrupt Status	Framing Error Interrupt Status	Not Used
RO	RO	RO	RO	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

Finally, the Receive E3 Framer block will increment the PMON Parity Error Count registers. The byte format of these registers are presented below.

PMON Parity Error Count Register - MSB (Address = 0x54)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Parity Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON Parity Error Count Register - LSB (Address = 0x55)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Parity Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

The user can determine the number of BIP-4 Errors that have been detected by the Receive E3 Framer block, since the last read of these registers. These registers are reset-upon-read.

Configuring the XRT72L50 Framer IC to support BIP-4 Error Detection

In order to perform BIP-4 checking of each E3 frame, the user must configure the XRT72L50 Framer IC accordingly, by executing the following steps.

1. Configure the Transmit Section (of the XRT72L50 Framer IC) to insert the BIP-4 value into the outbound E3 frames. This is accomplished by writing a “1” into bit-field 7 (Tx BIP-4 Enable) within the TxE3 Configuration Register, as illustrated below.

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx BIP-4 Enable	TxASourceSel[1:0]		TxNSourceSel[1:0]		Tx AIS Enable	Tx LOS Enable	Tx FAS Source Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

2. Enable the BIP-4 Error Interrupt. This is accomplished by writing a "1" into bit-field 2 (BIP-4 Error Interrupt Enable) within the RxE3 Interrupt Enable Register, as illustrated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Enable	BIP-4 Error Interrupt Enable	Framing Error Interrupt Enable	Not Used
R/W	RO	RO	RO	R/W	R/W	R/W	RO
0	0	0	0	0	1	0	0

After doing this, the XRT72L50 Framer IC will generate an interrupt to the Microprocessor/Microcontroller anytime the Receive Section detects a BIP-4 error.

5.3.3 The Receive HDLC Controller Block

The Receive E3 HDLC Controller block can be used to receive message-oriented signaling (MOS) type data link messages from the remote terminal equipment.

The MOS types of HDLC message processing is discussed in detail below.

The Message Oriented Signaling (e.g., LAP-D) Processing via the Receive E3 HDLC Controller block

The LAPD Receiver (within the Receive E3 HDLC Controller block) allows the user to receive PMDL messages from the remote terminal equipment, via the inbound E3 frames. In this case, the inbound message bits will be carried by the N bit-field within each inbound E3 Frame. The remote LAPD Transmitter will transmit a LAPD Message to the Local Receiver via either the N bit within each E3 Frame. The LAPD Receiver will receive and store the information portion of the received LAPD frame into the Receive LAPD Message Buffer, which is located at addresses: 0xDE through 0x135 within the on-chip RAM. The LAPD Receiver has the following responsibilities.

- Framing to the incoming LAPD Messages
- Filtering out stuffed "Zeros" (Between the two flag sequence bytes, 0x7E)
- Storing the Frame Message into the Receive LAPD Message Buffer
- Perform Frame Check Sequence (FCS) Verification
- Provide status indicators for
  - End of Message (EOM)
  - Flag Sequence Byte detected
  - Abort Sequence detected
  - Message Type
  - C/R Type
  - The occurrence of FCS Errors

The LAPD receiver's actions are facilitated via the following two registers.

- Rx E3 LAPD Control Register
- Rx E3 LAPD Status Register

Operation of the LAPD Receiver

The LAPD Receiver, once enabled, will begin searching for the boundaries of the incoming LAPD message. The LAPD Message Frame boundaries are delineated via the Flag Sequence octets (0x7E), as depicted in Figure 130.

FIGURE 130. LAPD MESSAGE FRAME FORMAT

Flag Sequence (8 bits)		
SAPI (6-bits)	C/R	EA
TEI (7 bits)		EA
Control (8-bits)		
76 or 82 Bytes of Information (Payload)		
FCS - MSB		
FCS - LSB		
Flag Sequence (8-bits)		

Where: Flag Sequence = 0x7E

SAPI + CR + EA = 0x3C or 0x3E

TEI + EA = 0x01

Control = 0x03

The 16 bit FCS is calculated using CRC-16, x16 + x12 + x5 + 1

The first byte of the information field indicates the type and size of the message being transferred. The value of this information or payload field and the corresponding message type/size follow:

CL Path Identification = 0x38 (76 bytes)

IDLE Signal Identification = 0x34 (76 bytes)

Test Signal Identification = 0x32 (76 bytes)

ITU-T Path Identification = 0x3F (82 bytes)

Enabling and Configuring the LAPD Receiver

Before the LAPD Receiver can begin to receive and process incoming LAPD Message frames, the user must do two things.

1. Enabling the LAPD Receiver

The LAPD Receiver must be enabled before it can begin receiving and processing any LAPD Message frames. The LAPD Receiver can be enabled by writing a “1” to Bit 2 (RxLAPD Enable) of the Rx E3 LAPD Control Register, as indicated below.

RxE3 LAPD Control Register (Address = 0x18

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	1	0	0

Once the LAPD Receiver has been enabled, it will begin searching for the Flag Sequence octet (0x7E), in the N bit-fields within each incoming E3 frame. When the LAPD Receiver finds the flag sequence byte, it will assert the Flag Present bit (Bit 0) within the Rx E3 LAPD Status Register, as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	1

The receipt of the Flag Sequence octet can mean one of two things.

1. This Flag Sequence byte may be marking the beginning or end of an incoming LAPD Message frame.
2. The Received Flag Sequence octet could be just one of many Flag Sequence octets that are transmitted via the E3 Transport Medium, during idle periods between the transmission of LAPD Message frames.

The LAPD Receiver will negate the Flag Present bit as soon as it has received an octet that is something other than the Flag Sequence octet. Once this happens, the LAPD Receiver should be receiving either octet # 2 of the incoming LAPD Message, or an ABORT Sequence (e.g., a string of seven or more consecutive "1's"). If this next set of data is an ABORT Sequence, then the LAPD Receiver will assert the RxABORT bit-field (Bit 6) within the Rx E3 LAPD Status Register, as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	1	0	0	0	0	0	0

However, if this next octet is Octet #2 of an incoming LAPD Message frame, then the LAPD Receiver is beginning to receive a LAPD Message frame.

As the LAPD Receiver receives this LAPD Message frame, it is reading in the LAPD Message frame octets, from N bit-fields within each incoming E3 frame. Secondly, it is reassembling these bits into a LAPD Message frame.

Once the LAPD Receiver has received the complete LAPD Message frame, then it will proceed to perform the following five (5) steps.

1. PMDL Message Extraction

The LAPD Receiver will extract out the PMDL Message, from the newly received LAPD Message frame. The LAPD Receiver will then write this PMDL Message into the Receive LAPD Message buffer.

NOTE: *As the LAPD Receiver is extracting the PMDL Message, from the newly received LAPD Message frame, the LAPD Receiver will also check the PMDL data for the occurrence of stuff bits (e.g., "0's" that were inserted into the PMDL Message by the Remote LAPD Transmitter, in order to prevent this data from mimicking the Flag Sequence byte or an ABORT Sequence), and remove them prior to writing the PMDL Message into the Receive LAPD Message Buffer. Specifically, the LAPD Receiver will search through the PMDL Message data and will remove any "0" that immediately follows a string of 5 consecutive "1's".*

NOTE: *For more information on how the LAPD Transmitter inserted these stuff bits, please see* Section 5.2.3.1.

2. FCS (Frame Check Sequence) Word Verification

The LAPD Receiver will compute the CRC-16 value of the header octets and the PMDL Message octets, within this LAPD Message frame and will compare it with the value of the two octets, residing in the FCS word-field of this LAPD Message frame. If the FCS value of the newly received LAPD Message frame matches the locally-computed CRC-16 value, then the LAPD Receiver will conclude that it has received this LAPD Message frame in an error-free manner.

However, if the FCS value does not match the locally-computed CRC-16 value, then the LAPD Receiver will conclude that this LAPD Message frame is erred.

The LAPD Receiver will indicate the results of this FCS Verification process by setting Bit 2 (RxFCS Error) within the Rx E3 LAPD Status Register, to the appropriate value as tabulated below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	1	0	0

If the LAPD Receiver detects an error in the FCS value, then it will set the RxFCS Error bit-field to “1”. Conversely, if the LAPD Receiver does not detect an error in the FCS value, then it will clear the RxFCS Error bit-field to “0”.

NOTE: *The LAPD Receiver will extract and write the PMDL Message into the Receive LAPD Message buffer independent of the results of FCS Verification. Hence, the user is urged to validate each PMDL Message that is read in from the Receive LAPD Message buffer, by first checking the state of this bit-field.*

3. Check and Report the State of the C/R Bit-field

After receiving the LAPD Message frame, the LAPD Receiver will check the state of the C/R bit-field, within octet # 2 of the LAPD Message frame header and will reflect this value in Bit 3 (Rx CR Type) within the Rx E3 LAPD Status Register, as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	1	0	0	0

When this bit-field is “0”, it means that this LAPD Message frame is originating from a customer installation. When this bit-field is “1”, it means that this LAPD Message frame is originating from a network terminal.

4. Identify the Type of LAPD Message Frame/PMDL Message

Next, the LAPD Receiver will check the value of the first octet within the PMDL information payload field, of the LAPD Message frame. When operating the LAPD Transmitter, the user is required to write in a byte of a specific value at address ox8A within the Transmit LAPD Message buffer. The value of this byte corresponds to the type of LAPD Message frame/PMDL Message that is to be transmitted to the Remote LAPD Receiver. This Message-Type Identification octet is transported to the Remote LAPD Receiver, along with the rest of the LAPD frame. From this Message Type Identification octet, the LAPD Receiver will know the type of size of the newly received PMDL Message. The LAPD Receiver will then reflect this information in Bits 4 and 5 (RxLAPDType[1:0]) within the Rx E3 LAPD Status Register, as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Table 59 presents the relationship between the contents of RxLAPDType[1:0] and the type of message received by the LAPD Receiver.

TABLE 59: THE RELATIONSHIP BETWEEN THE CONTENTS OF RXLAPDTYPE[1:0] BIT-FIELDS AND THE PMDL MESSAGE TYPE/SIZE

RXLAPDTYPE[1:0]	PMDL MESSAGE TYPE	PMDL MESSAGE SIZE
00	CL Path Identification	76 Bytes
01	Idle Signal Identification	76 Bytes
10	Test Signal Identification	76 Bytes
11	ITU-T Path Identification	82 Bytes

NOTE: *Prior to reading in the PMDL Message from the Receive LAPD Message buffer, the user is urged to read the state of the RxLAPDType[1:0] bit-fields in order to determine the size of this message.*

5. Inform the Local Microprocessor/External Circuitry of the receipt of the new LAPD Message frame.

Finally, after the LAPD Receiver has received and processed the newly received LAPD Message frame (per steps 1 through 4, as described above), it will inform the local Microprocessor that a LAPD Message frame has been received and is ready for user-system handling. The LAPD Receiver will inform the Microprocessor/ Microcontroller and the external circuitry by:

- Generating a LAPD Message Frame Received interrupt to the Microprocessor. The purpose of this interrupt is to let the Microprocessor know that the Receive LAPD Message buffer contains a new PMDL Message that needs to be read and processed. When the LAPD Receiver generates this interrupt, it will set bit 0 (RxLAPD Interrupt Status) within the Rx E3 LAPD Control Register to “1” as depicted below.

RxE3 LAPD Control Register (Address = 0x18

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	0	1

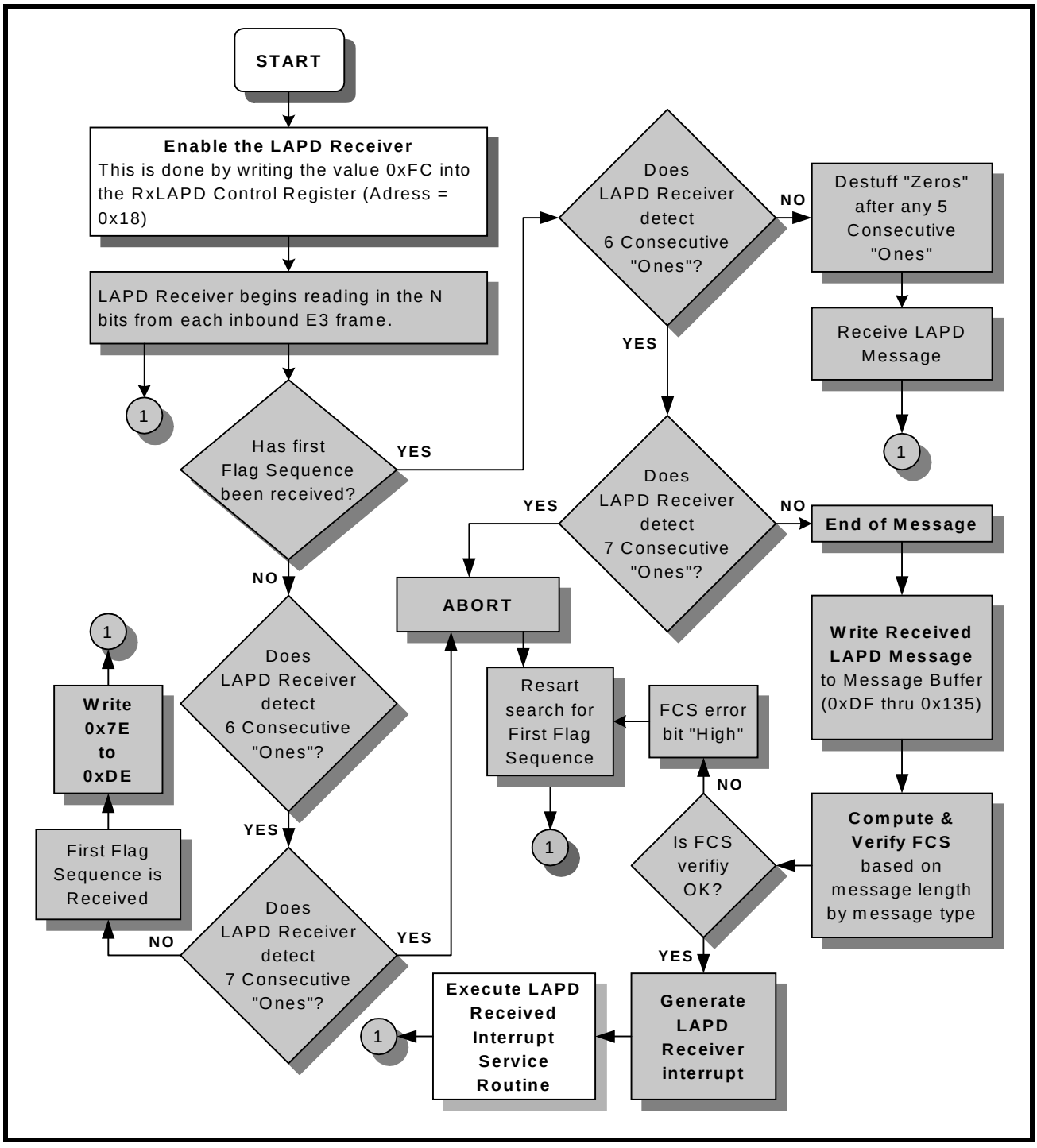
- Setting Bit 1 (End of Message) within the Rx E3 LAPD Status Register, to “1” as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	1	0

In summary, Figure 131 presents a flow chart depicting how the LAPD Receiver functions.

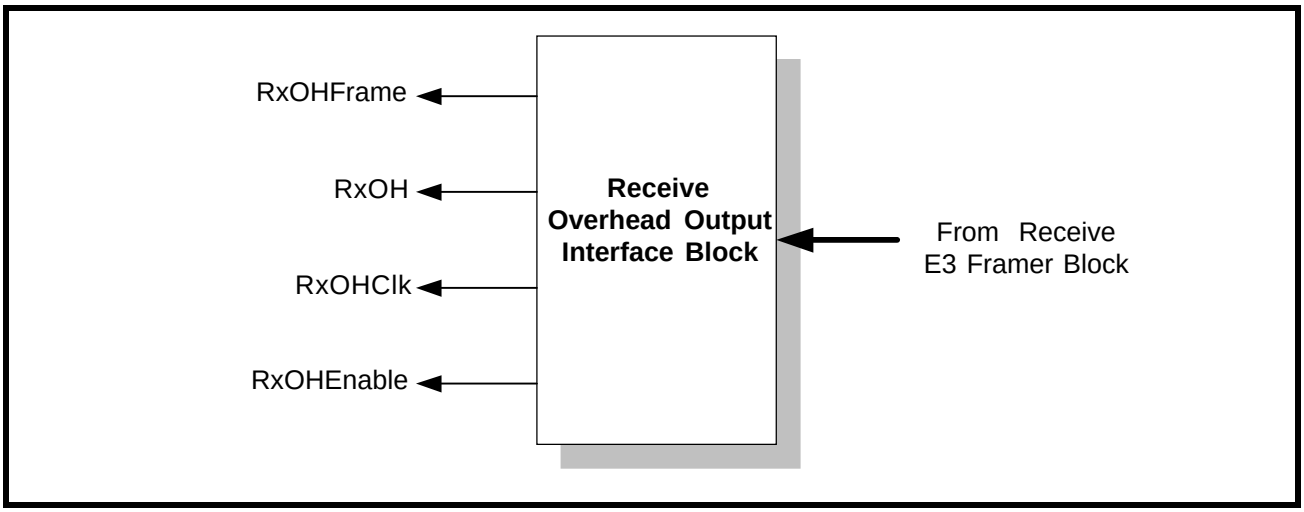
FIGURE 131. FLOW CHART DEPICTING THE FUNCTIONALITY OF THE LAPD RECEIVER



5.3.4 The Receive Overhead Data Output Interface

Figure 132 presents a simple illustration of the Receive Overhead Data Output Interface block within the XRT72L50.

FIGURE 132. THE RECEIVE OVERHEAD OUTPUT INTERFACE BLOCK



The E3, ITU-T G.751 frame consists of 1536 bits. Of these bytes, 1524 bits are payload bits and the remaining 12 bits are overhead bits. The XRT72L50 has been designed to handle and process both the payload type and overhead type bits for each E3 frame.

Within the Receive Section of the XRT72L50, the Receive Payload Data Output Interface block has been designed to handle the payload bits. Likewise, the Receive Overhead Data Output Interface block has been designed to handle and process the overhead bits.

The Receive Overhead Data Output Interface block unconditionally outputs the contents of all overhead bits. The XRT72L50 does not offer the user a means to shut off this transmission of data. However, the Receive Overhead Output Interface block does provide the user with the appropriate output signals for external Data Link Layer equipment to sample and process these overhead bits, via the following two methods.

- Method 1- Using the RxOHClk clock signal.
- Method 2 - Using the RxClk and RxOHEnable output signals.

Each of these methods are described below.

5.3.4.1 *Method 1 - Using the RxOHClk Clock signal*

The Receive Overhead Data Output Interface block consists of four (4) signals. Of these four signals, the following three signals are to be used when sampling the E3 overhead bits via Method 1.

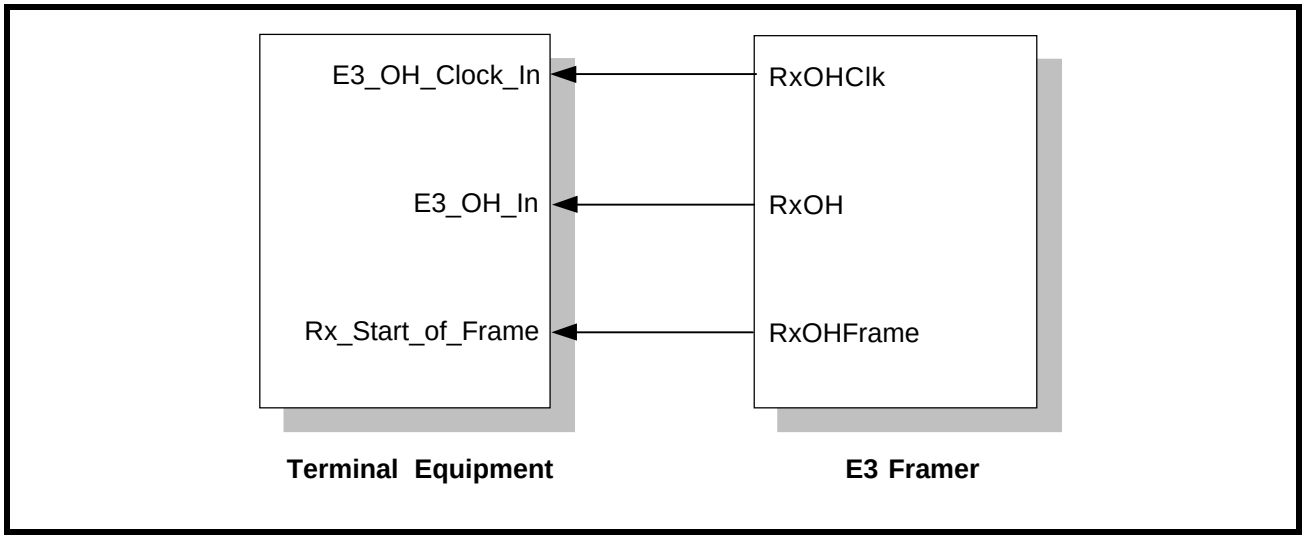
- RxOH
- RxOHClk
- RxOHFrame

Each of these signals are listed and described below in Table 60.

Interfacing the Receive Overhead Data Output Interface block to the Terminal Equipment (Method 1)

Figure 133 illustrates how one should interface the Receive Overhead Data Output Interface block to the Terminal Equipment when using Method 1 to sample and process the overhead bits from the inbound E3 data stream.

FIGURE 133. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE (METHOD 1)



Method 1 Operation of the Terminal Equipment

If the Terminal Equipment intends to sample any overhead data from the inbound E3 data stream (via the Receive Overhead Data Output Interface block) then it is expected to do the following:

1. Sample the state of the RxOHFrame signal (e.g., the Rx_Start_of_Frame input signal) on the rising edge of the RxOHClk (e.g., the E3_OH_Clock_In) signal.
2. Keep track of the number of rising clock edges that have occurred in the RxOHClk (e.g., the E3_OH_Clock_In) signal, since the last time the RxOHFrame signal was sampled "High". By doing this, the Terminal Equipment will be able to keep track of which overhead byte is being output via the RxOH output pin. Based upon this information, the Terminal Equipment will be able to derive some meaning from these overhead bits.

TABLE 60: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (FOR METHOD 1)

SIGNAL NAME	TYPE	DESCRIPTION
RxOH	Output	**Receive Overhead Data Output pin:** The XRT72L50 will output the overhead bits, within the incoming E3 frames, via this pin. The Receive Overhead Data Output Interface block will output a given overhead bit, upon the falling edge of RxOHClk. Hence, the external data link equipment should sample the data, at this pin, upon the rising edge of RxOHClk. ***NOTE:*** *The XRT72L50 will always output the E3 Overhead bits via this output pin. There are no external input pins or register bit settings available that will disable this output pin.*
RxOHClk	Output	**Receive Overhead Data Output Interface Clock Signal:** The XRT72L50 will output the Overhead bits (within the incoming E3 frames), via the RxOH output pin, upon the falling edge of this clock signal. As a consequence, the user's data link equipment should use the rising edge of this clock signal to sample the data on both the RxOH and RxOHFrame output pins. ***NOTE:*** *This clock signal is always active.*
RxOHFrame	Output	**Receive Overhead Data Output Interface - Start of Frame Indicator:** The XRT72L50 will drive this output pin "High" (for one period of the RxOHClk signal) whenever the first overhead bit within a given E3 frame is being driven onto the RxOH output pin.

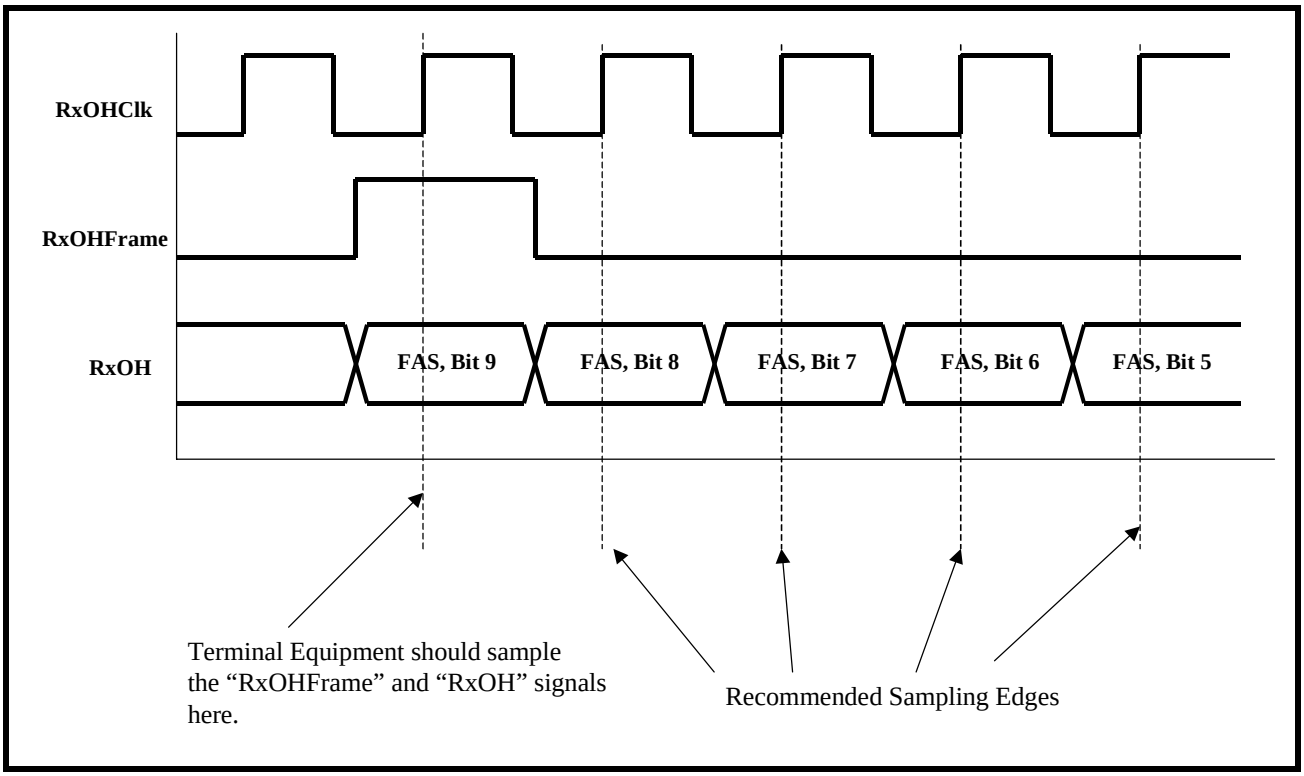
Table 61 relates the number of rising clock edges (in the RxOHClk signal, since the RxOHFrame signal was last sampled "High") to the E3 Overhead bit that is being output via the RxOH output pin.

TABLE 61: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN RXOHCLK, (SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE E3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

NUMBER OF RISING CLOCK EDGES IN RXOHCLK	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
0 (Clock edge is coincident with RxOHFrame being detected "High")	FAS Pattern - Bit 9
1	FAS Pattern - Bit 8
2	FAS Pattern - Bit 7
3	FAS Pattern - Bit 6
4	FAS Pattern - Bit 5
5	FAS Pattern - Bit 4
6	FAS Pattern - Bit 3
7	FAS Pattern - Bit 2
8	FAS Pattern - Bit 1
9	FAS Pattern - Bit 0
10	A Bit
11	N Bit

Figure 134 presents the typical behavior of the Receive Overhead Data Output Interface block, when Method 1 is being used to sample the incoming E3 overhead bits.

FIGURE 134. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE OVERHEAD OUTPUT INTERFACE (FOR METHOD 1).



Method 2 - Using RxOutClk and the RxOHEnable signals

Method 1 requires that the Terminal Equipment be able to handle an additional clock signal, RxOHClk. However, there may be a situation in which the Terminal Equipment circuitry does not have the means to deal with this extra clock signal, in order to use the Receive Overhead Data Output Interface. Method 2 involves the use of the following signals.

- RxOH
- RxOutClk
- RxOHEnable
- RxOHFrame

Each of these signals are listed and described below in Table 62.

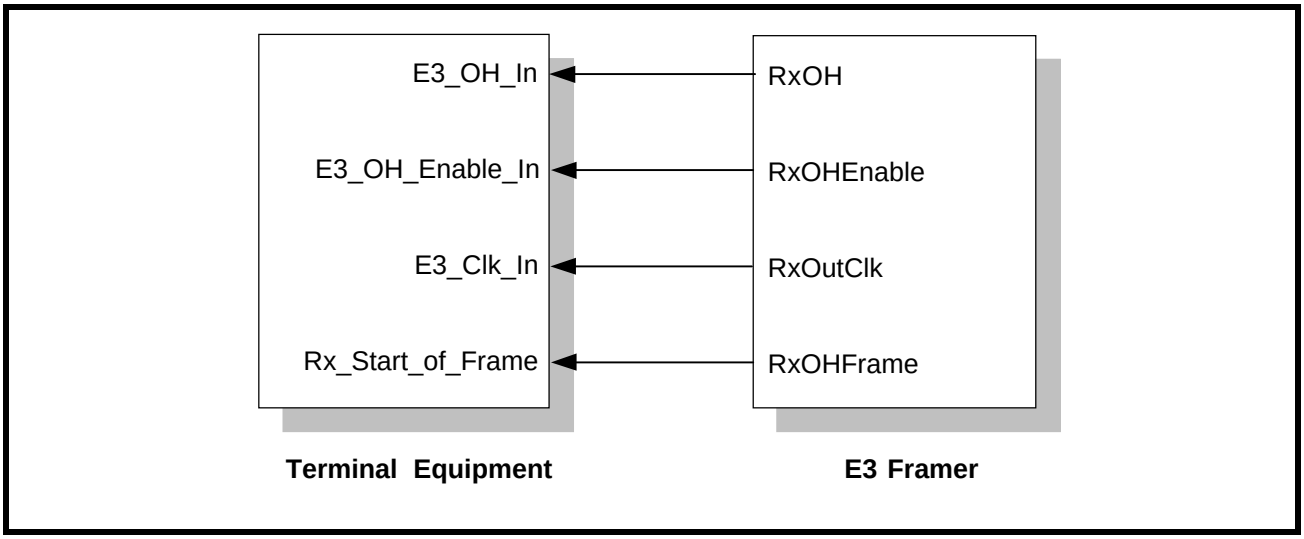
TABLE 62: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (METHOD 2)

SIGNAL NAME	TYPE	DESCRIPTION
RxOH	Output	**Receive Overhead Data Output pin:** The XRT72L50 will output the overhead bits, within the incoming E3 frames, via this pin. The Receive Overhead Output Interface will pulse the RxOHEnable output pin (for one RxOutClk period) at approximately the middle of the RxOH bit period. The user is advised to design the Terminal Equipment to latch the contents of the RxOH output pin, whenever the RxOHEnable output pin is sampled "High" on the falling edge of RxOutClk.
RxOHEnable	Output	**Receive Overhead Data Output Enable - Output pin:** The XRT72L50 will assert this output signal for one RxOutClk period when it is safe for the Terminal Equipment to sample the data on the RxOH output pin.
RxOHFrame	Output	**Receive Overhead Data Output Interface - Start of Frame Indicator:** The XRT72L50 will drive this output pin "High" (for one period of the RxOH signal), whenever the first overhead bit, within a given E3 frame is being driven onto the RxOH output pin.
RxOutClk	Output	**Receive Section Output Clock Signal:** This clock signal is derived from the RxLineClk signal (from the LIU) for loop-timing applications, and the TxInClk signal (from a local oscillator) for local-timing applications. For E3 applications, this clock signal will operate at 34.368MHz. The user is advised to design the Terminal Equipment to latch the contents of the RxOH pin, anytime the RxOHEnable output signal is sampled "High" on the falling edge of this clock signal.

Interfacing the Receive Overhead Data Output Interface block to the Terminal Equipment (Method 2)

Figure 135 illustrates how one should interface the Receive Overhead Data Output Interface block to the Terminal Equipment, when using Method 2 to sample and process the overhead bits from the inbound E3 data stream.

FIGURE 135. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE (METHOD 2)



Method 2 Operation of the Terminal Equipment

If the Terminal Equipment intends to sample any overhead data from the inbound E3 data stream (via the Receive Overhead Data Output Interface), then it is expected to do the following.

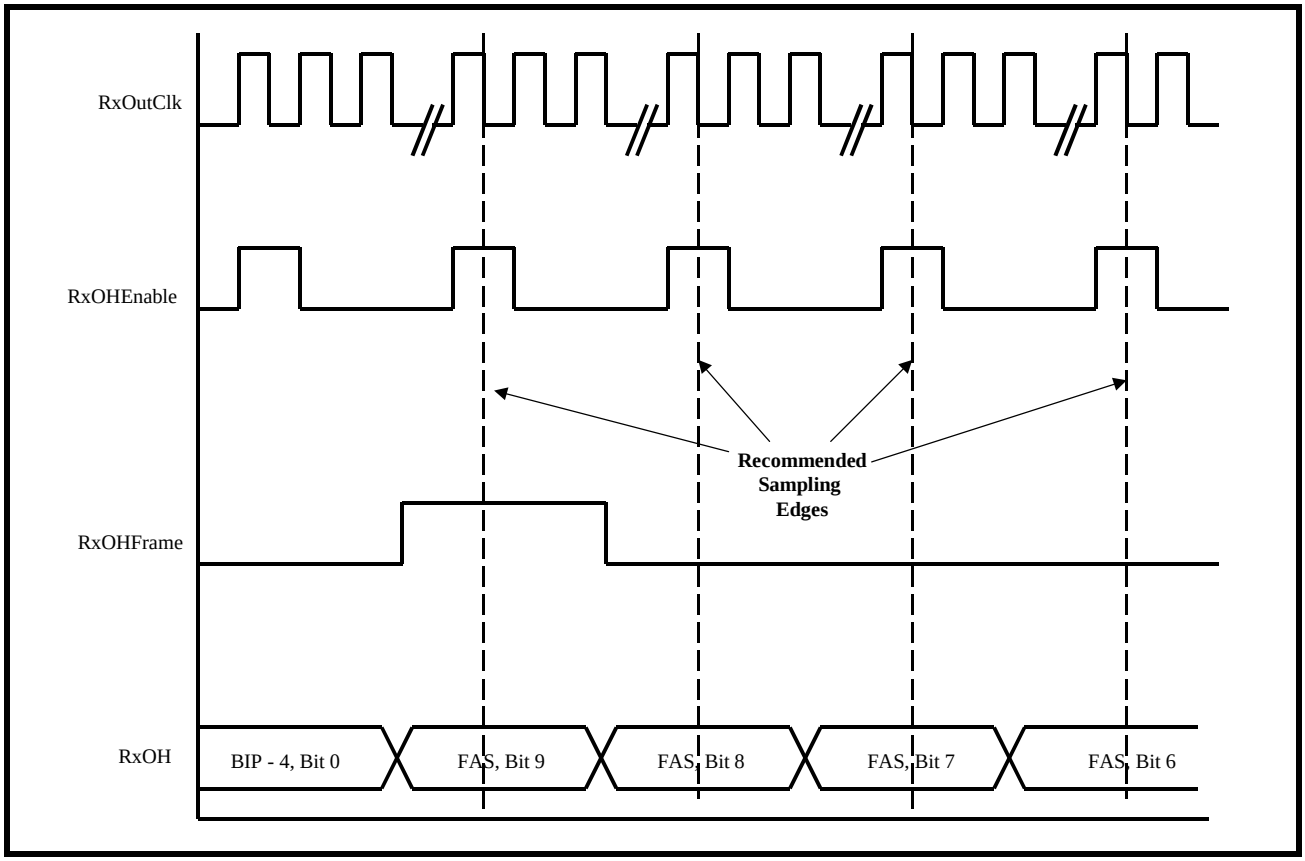
1. Sample the state of the RxOHFrame signal (e.g., the Rx_Start_of_Frame input) on the falling edge of the RxOutClk clock signal, whenever the RxOHEnable output signal is also sampled "High".
2. Keep track of the number of times that the RxOHEnable signal has been sampled "High" since the last time the RxOHFrame was also sampled "High". By doing this, the Terminal Equipment will be able to keep track of which overhead bit is being output via the RxOH output pin. Based upon this information, the Terminal Equipment will be able to derive some meaning from these overhead bits.
3. Table 63 relates the number of RxOHEnable output pulses (that have occurred since both the RxOHFrame and the RxOHEnable pins were both sampled "High") to the E3 overhead bit that is being output via the RxOH output pin.

TABLE 63: THE RELATIONSHIP BETWEEN THE NUMBER OF RXOHENABLE OUTPUT PULSES (SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE E3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

NUMBER OF RXOHENABLE OUTPUT PULSES	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
0 (Clock edge is coincident with RxOHFrame being detected "High")	FAS Pattern - Bit 9
1	FAS Pattern - Bit 8
2	FAS Pattern - Bit 7
3	FAS Pattern - Bit 6
4	FAS Pattern - Bit 5
5	FAS Pattern - Bit 4
6	FAS Pattern - Bit 3
7	FAS Pattern - Bit 2
8	FAS Pattern - Bit 1
9	FAS Pattern - Bit 0
10	A Bit
11	N Bit

Figure 136 presents the typical behavior of the Receive Overhead Data Output Interface block, when Method 2 is being used to sample the incoming E3 overhead bits.

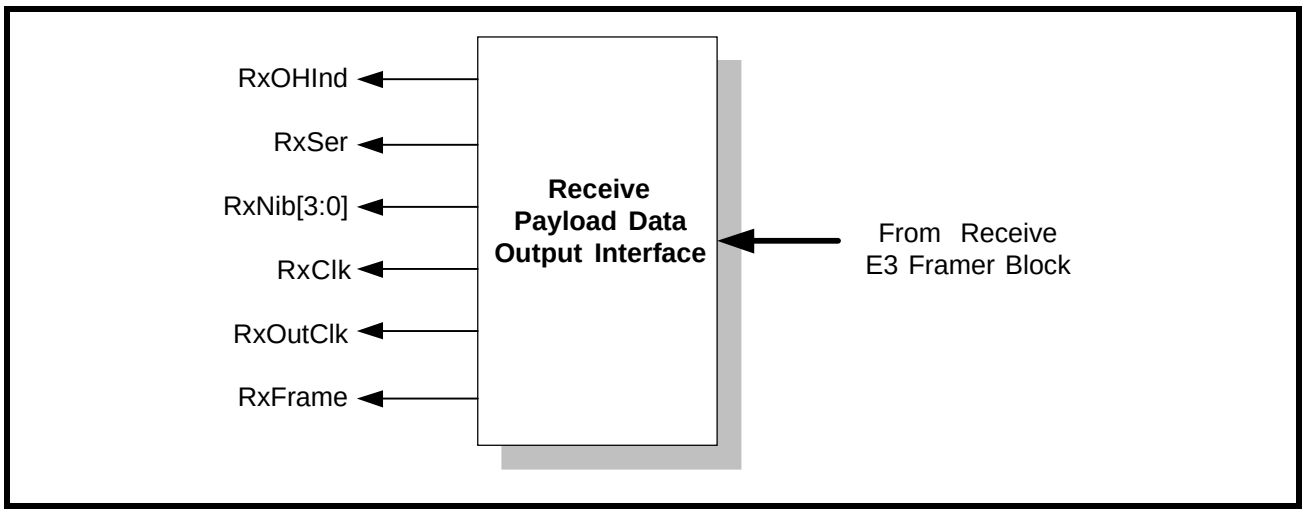
FIGURE 136. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (FOR METHOD 2).



5.3.5 The Receive Payload Data Output Interface

Figure 137 presents a simple illustration of the Receive Payload Data Output Interface block.

FIGURE 137. THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK



Each of the output pins of the Receive Payload Data Output Interface block are listed in Table 64 and described below. The exact role that each of these output pins assume, for a variety of operating scenarios are described throughout this section.

TABLE 64: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

SIGNAL NAME	TYPE	DESCRIPTION
RxSer	Output	**Receive Serial Payload Data Output pin:** If the user opts to operate the XRT72L50 in the serial mode, then the chip will output the payload data, of the incoming E3 frames, via this pin. The XRT72L50 will output this data upon the rising edge of RxClk. The user is advised to design the Terminal Equipment such that it will sample this data on the falling edge of RxClk. This signal is only active if the NibIntf input pin is pulled "Low".
RxNib[3:0]	Output	**Receive Nibble-Parallel Payload Data Output pins:** If the user opts to operate the XRT72L50 in the nibble-parallel mode, then the chip will output the payload data, of the incoming E3 frames, via these pins. The XRT72L50 will output data via these pins, upon the falling edge of the RxClk output pin. The user is advised to design the Terminal Equipment such that it will sample this data upon the rising edge of RxClk. ***NOTE:*** *These pins are only active if the NibIntf input pin is pulled "High".*
RxClk	Output	**Receive Payload Data Output Clock pin:** The exact behavior of this signal depends upon whether the XRT72L50 is operating in the Serial or in the Nibble-Parallel-Mode. **Serial Mode Operation** In the serial mode, this signal is a 34.368MHz clock output signal. The Receive Payload Data Output Interface will update the data via the RxSer output pin, upon the rising edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxSer pin, upon the falling edge of this clock signal. **Nibble-Parallel Mode Operation** In this Nibble-Parallel Mode, the XRT72L50 will derive this clock signal, from the RxLineClk signal. The XRT72L50 will pulse this clock 1060 times for each inbound E3 frame. The Receive Payload Data Output Interface will update the data, on the RxNib[3:0] output pins upon the falling edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxNib[3:0] output pins, upon the rising edge of this clock signal
RxOHInd	Output	**Receive Overhead Bit Indicator Output:** This output pin will pulse "High" whenever the Receive Payload Data Output Interface outputs an overhead bit via the RxSer output pin. The purpose of this output pin is to alert the Terminal Equipment that the current bit, (which is now residing on the RxSer output pin), is an overhead bit and should not be processed by the Terminal Equipment. The XRT72L50 will update this signal, upon the rising edge of RxOHInd. The user is advised to design (or configure) the Terminal Equipment to sample this signal (along with the data on the RxSer output pin) on the falling edge of the RxClk signal.
RxFrame	Output	**Receive Start of Frame Output Indicator:** The exact behavior of this pin, depends upon whether the XRT72L50 has been configured to operate in the Serial Mode or the Nibble-Parallel Mode. **Serial Mode Operation:** The Receive Section of the XRT72L50 will pulse this output pin "High" (for one bit period) when the Receive Payload Data Output Interface block is driving the very first bit (or Nibble) of a given E3 frame, onto the RxSer output pin. **Nibble-Parallel Mode Operation:** The Receive Section of the XRT72L50 will pulse this output pin "High" for one nibble period, when the Receive Payload Data Output Interface is driving the very first nibble of a given E3 frame, onto the RxNib[3:0] output pins.

Operation of the Receive Payload Data Output Interface block

The Receive Payload Data Output Interface permits the user to read out the payload data of inbound E3 frames, via either of the following modes.

- Serial Mode
- Nibble-Parallel Mode

Each of these modes are described in detail, below.

5.3.5.1 *Serial Mode Operation Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will behave as follows.

Payload Data Output

The XRT72L50 will output the payload data, of the incoming E3 frames via the RxSer output pin, upon the rising edge of RxClk.

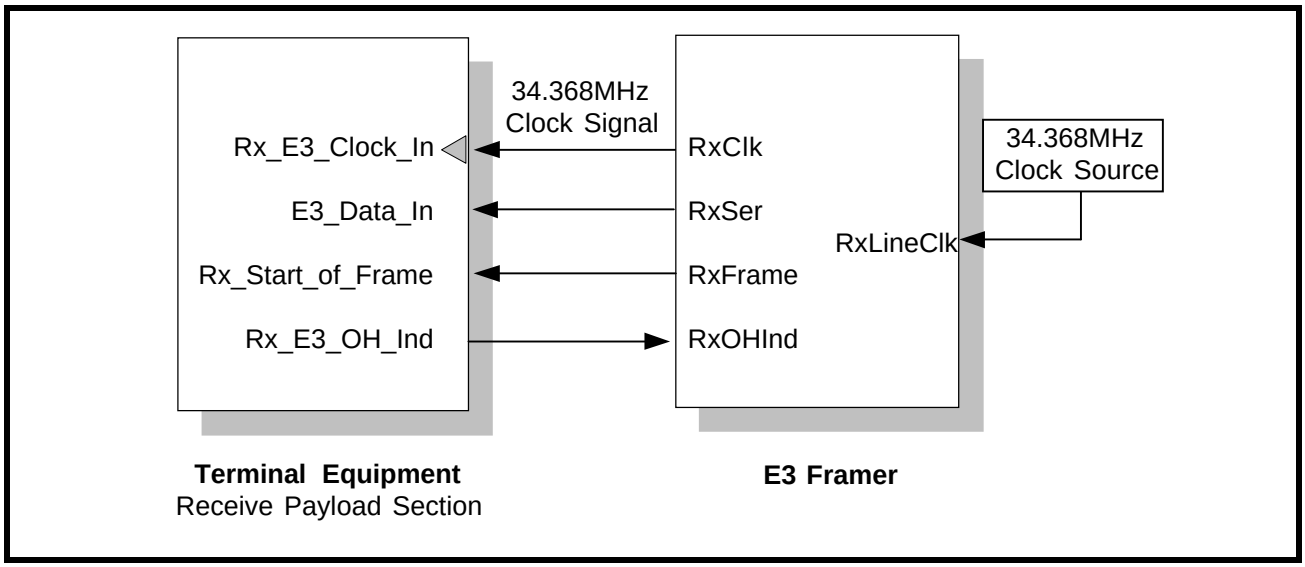
Delineation of inbound E3 Frames

The XRT72L50 will pulse the RxFrame output pin "High" for one bit-period coincident with it driving the first bit within a given E3 frame, via the RxSer output pin.

Interfacing the XRT72L50 to the Receive Terminal Equipment

Figure 138 presents a simple illustration as how the user should interface the XRT72L50 to that terminal equipment which processes Receive Direction payload data.

FIGURE 138. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE RECEIVE PAYLOAD DATA INPUT INTERFACE BLOCK (SERIAL MODE OPERATION)



Required Operation of the Terminal Equipment

The XRT72L50 will update the data on the RxSer output pin, upon the rising edge of RxClk. Hence, the Terminal Equipment should sample the data on the RxSer output pin (or the E3_Data_In pin at the Terminal Equipment) upon the rising edge of RxClk. As the Terminal Equipment samples RxSer with each rising edge of RxClk it should also be sampling the following signals.

- RxFrame
- RxOHInd

The Need for sampling RxFrame

The XRT72L50 will pulse the RxFrame output pin "High" coincident with it driving the very first bit of a given E3 frame onto the RxSer output pin. If knowledge of the E3 Frame Boundaries is important for the operation of the Terminal Equipment, then this is a very important signal for it to sample.

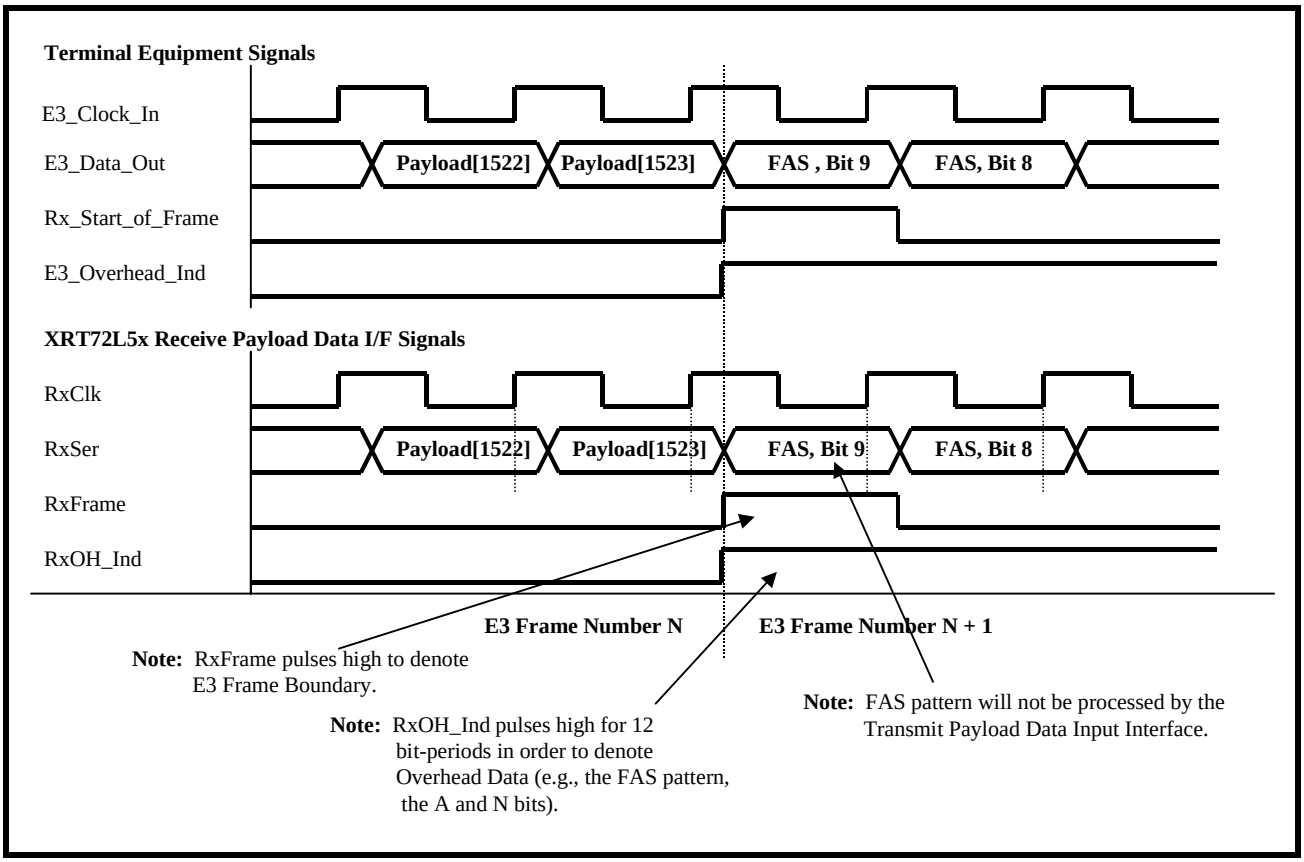
The Need for sampling RxOHInd

The XRT72L50 will indicate that it is currently driving an overhead bit onto the RxSer output pin, by pulsing the RxOHInd output pin "High". If the Terminal Equipment samples this signal "High", then it should know that the bit, that it is currently sampling via the RxSer pin is an overhead bit and should not be processed.

The Behavior of the Signals between the Receive Payload Data Output Interface block and the Terminal Equipment

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Serial Mode Operation is illustrated in Figure 139.

FIGURE 139. AN ILLUSTRATION OF THE BEHAVIOR OF THE SIGNALS BETWEEN THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK OF THE XRT72L50 AND THE TERMINAL EQUIPMENT



5.3.5.2 *Nibble-Parallel Mode Operation Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in the Nibble-Parallel Mode, then the XRT72L50 will behave as follows.

Payload Data Output

The XRT72L50 will output the payload data of the incoming E3 frames, via the RxNib[3:0] output pins, upon the rising edge of RxClk.

NOTES:

1. *In this case, RxClk will function as the Nibble Clock signal between the XRT72L50 the Terminal Equipment. The XRT72L50 will pulse the RxClk output signal "High" 1060 times, for each inbound E3 frame.*

2. Unlike Serial Mode operation, the duty cycle of RxClk, in Nibble-Parallel Mode operation is approximately 25%.

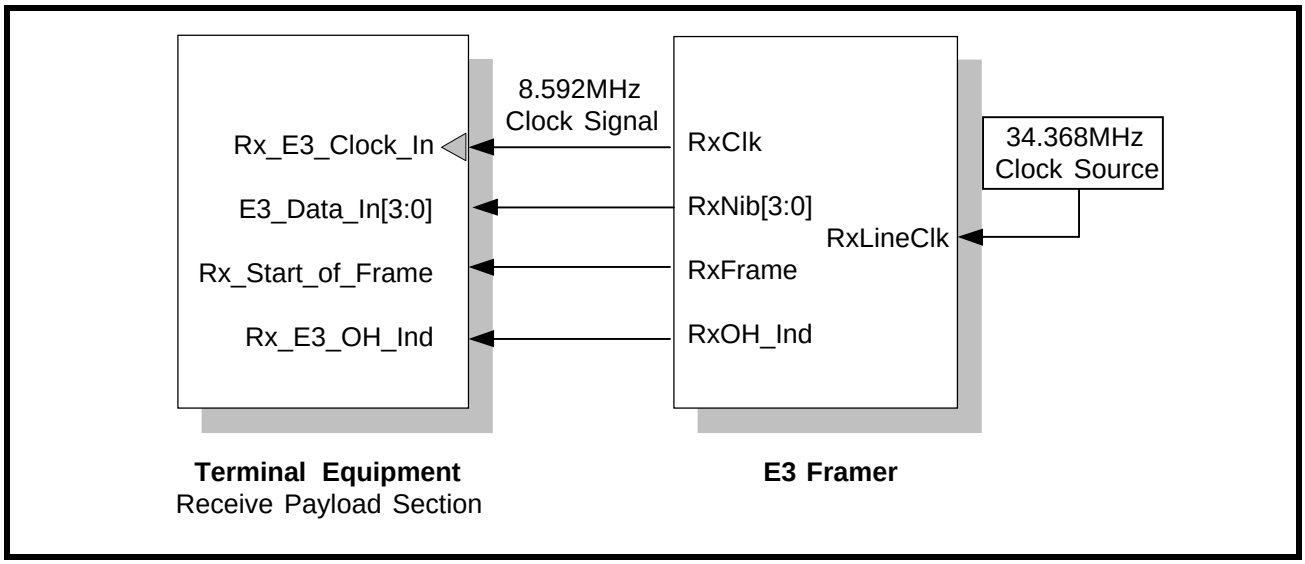
Delineation of Inbound E3 Frames

The XRT72L50 will pulse the RxFrame output pin "High" for one nibble-period coincident with it driving the very first nibble, within a given inbound E3 frame, via the RxNib[3:0] output pins.

Interfacing the XRT72L50 the Terminal Equipment.

Figure 140 presents a simple illustration as how the user should interface the XRT72L50 to that terminal equipment which processes Receive Direction payload data.

FIGURE 140. THE XRT72L50 DS3/E3 FRAMER IC BEING INTERFACED TO THE RECEIVE SECTION OF THE TERMINAL EQUIPMENT (NIBBLE-PARALLEL MODE OPERATION)



Required Operation of the Terminal Equipment

The XRT72L50 will update the data on the RxNib[3:0] line, upon the rising edge of RxClk. Hence, the Terminal Equipment should sample the data on the RxNib[3:0] output pins (or the E3_Data_In[3:0] input pins at the Terminal Equipment) upon the rising edge of RxClk. As the Terminal Equipment samples RxSer with each rising edge of RxClk it should also be sampling the RxFrame signal.

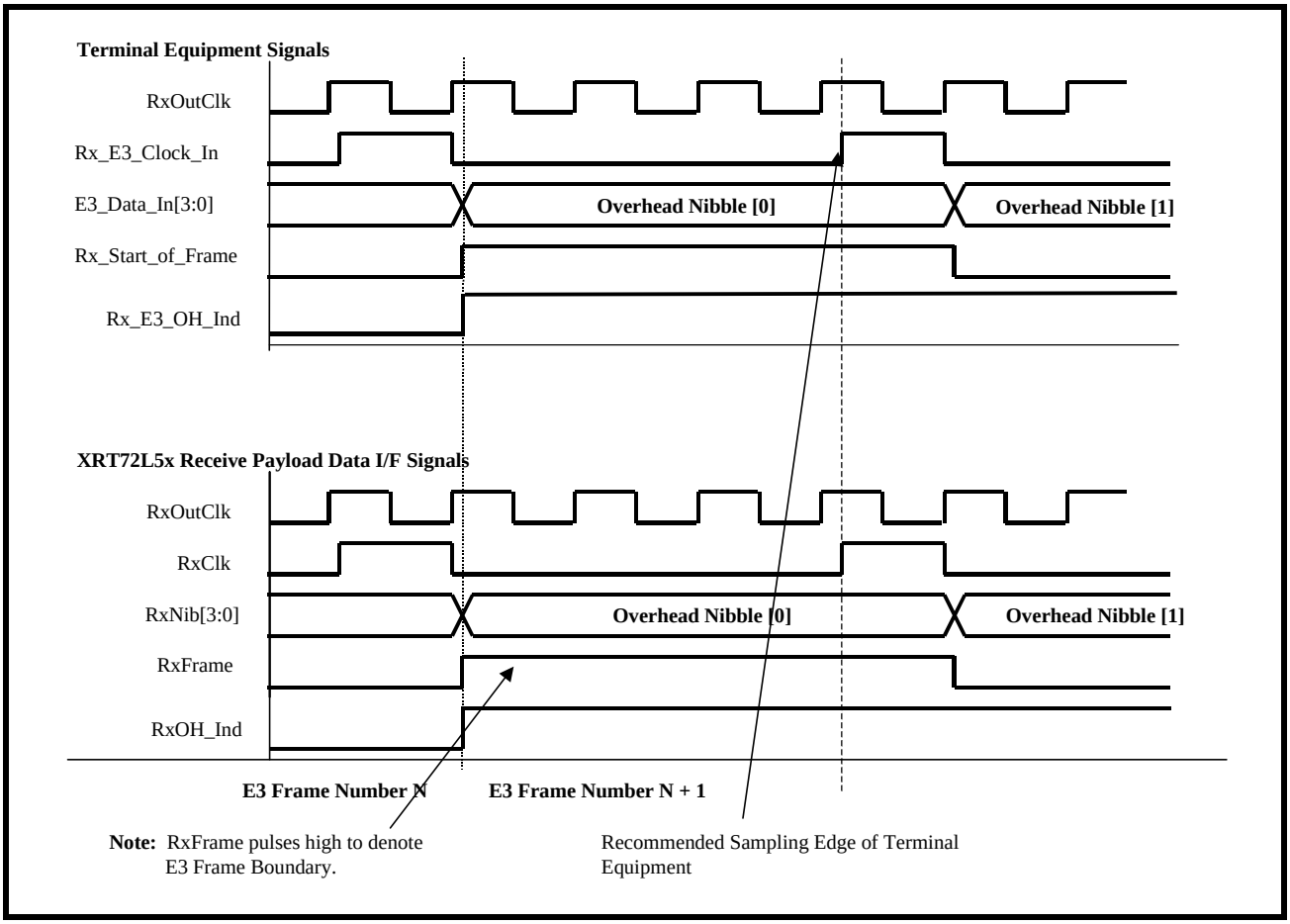
The Need for Sampling RxFrame

The XRT72L50 will pulse the RxFrame output pin "High" coincident with it driving the very first nibble of a given E3 frame, onto the RxNib[3:0] output pins. If knowledge of the E3 Frame Boundaries is important for the operation of the Terminal Equipment, then this is a very important signal for it to sample.

The Behavior of the Signals between the Receive Payload Data Output Interface block and the Terminal Equipment

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Nibble-Mode operation is illustrated in Figure 141.

FIGURE 141. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK (FOR NIBBLE-PARALLEL MODE OPERATION).



5.3.6 Receive Section Interrupt Processing

The Receive Section of the XRT72L50 can generate an interrupt to the Microcontroller/Microprocessor for the following reasons.

- Change in Receive LOS Condition
- Change in Receive OOF Condition
- Change in Receive LOF Condition
- Change in Receive AIS Condition
- Change in Receive FERF Condition
- Change of Framing Alignment
- Detection of FEBE (Far-End Block Error) Event
- Detection of BIP-4 Error
- Detection of Framing Error
- Reception of a new LAPD Message

5.3.6.1 *Enabling Receive Section Interrupts*

The Interrupt Structure within the XRT72L50 contains two hierarchical levels.

- Block Level

- Source Level

The Block Level

The Enable state of the Block level for the Receive Section Interrupts dictates whether or not interrupts (if enabled at the source level), are actually enabled.

The user can enable or disable these Receive Section interrupts, at the Block Level by writing the appropriate data into Bit 7 (Rx DS3/E3 Interrupt Enable) within the Block Interrupt Enable register (Address = 0x04), as illustrated below.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One-Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
X	0	0	0	0	0	0	0

Setting this bit-field to “1” enables the Receive Section at the Block Level) for interrupt generation. Conversely, setting this bit-field to “0” disables the Receive Section for interrupt generation.

5.3.6.2 *Enabling/Disabling and Servicing Interrupts*

As mentioned previously, the Receive Section of the XRT72L50 Framer IC contains numerous interrupts. The Enabling/Disabling and Servicing of each of these interrupts is described below.

5.3.6.2.1 The Change in Receive LOS Condition Interrupt

If the Change in Receive LOS Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an LOS (Loss of Signal) Condition, and
2. When the XRT72L50 Framer IC clears the LOS condition.

Conditions causing the XRT72L50 Framer IC to declare an LOS Condition.

- If the XRT73L00 LIU IC declares an LOS condition, and drives the RLOS input pin (of the XRT72L50 Framer IC) "High".
- If the XRT72L50 Framer IC detects 32 consecutive “0’s”, via the RxPOS and RxNEG input pins and IntLOS is enabled, (0x00, bit 5).

Conditions causing the XRT72L50 Framer IC to clear the LOS Condition.

- If the XRT73L00 LIU IC clears the LOS condition and drives the RLOS input pin (of the XRT72L50 Framer IC) "Low".
- If the XRT72L50 Framer IC detects a string of 32 consecutive bits (via the RxPOS and RxNEG input pins) that does NOT contain a string of 4 consecutive “0’s” and IntLOS is enabled.

Enabling and Disabling the Change in Receive LOS Condition Interrupt

The user can enable or disable the Change in Receive LOS Condition Interrupt, by writing the appropriate value into Bit 1 (LOS Interrupt Enable), within the RxE3 Interrupt Enable Register - 1, as indicated below.

RxE3 Interrupt Enable Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	X	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive LOS Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "Low".
- It will set Bit 1 (LOS Interrupt Status), within the Rx E3 Interrupt Status Register - 1 to “1”, as indicated below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	1	0

Whenever the user’s system encounters the Change in Receive LOS Condition Interrupt, then it should do the following.

1. It should determine the current state of the LOS condition. Recall, that this interrupt can be generated, whenever the XRT72L50 Framer IC declares or clears the LOS defect. Hence, the user can determine the current state of the LOS defect by reading the state of Bit 4 (RxLOS) within the Rx E3 Configuration and Status Register - 2, as illustrated below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	0	1	1	1

If the LOS state is TRUE

1. It should transmit a FERF (Far-End-Receive Failure) indicator to the Remote Terminal Equipment. Please see Section 5.2.4.2.1.3.

If the LOS state is FALSE

1. It should cease transmitting the FERF indication to the Remote Terminal Equipment.

NOTE: The device cannot be configured to automatically send/clear FERF on LOS, LOOf, OOF or AIS in E3 G.751 mode. The user must implemt it in the ISR.

Please see Section 5.2.4.2.1.3 on how to control the state of the A bit, which is transmitted on each outbound E3 frame.

5.3.6.2.2 The Change in Receive OOF Condition Interrupt

If the Change in Receive OOF Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an OOF (Out of Frame) Condition, and
2. When the XRT72L50 Framer IC clears the OOF condition.

Conditions causing the XRT72L50 Framer IC to declare an OOF Condition.

- If the Receive E3 Framer block (within the XRT72L50 Framer IC) detects Framing bit errors, within four consecutive incoming E3 frames.

Conditions causing the XRT72L50 Framer IC to clear the OOF Condition.

- If the Receive E3 Framer block (within the XRT72L50 Framer IC) transitions from the FAS Pattern Verification state to the In-Frame state (see Figure 124).
- If the Receive E3 Framer block transitions from the OOF Condition state to the In-Frame state (see Figure 124).

Enabling and Disabling the Change in Receive OOF Condition Interrupt

The user can enable or disable the Change in Receive OOF Condition Interrupt, by writing the appropriate value into Bit 3 (OOF Interrupt Enable), within the RxE3 Interrupt Enable Register - 1, as indicated below.

RxE3 Interrupt Enable Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	X	0	X	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive OOF Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "Low".
- It will set Bit 3 (OOF Interrupt Status), within the Rx E3 Interrupt Status Register - 1 to “1”, as indicated below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

Whenever the user’s system encounters the Change in Receive OOF Condition Interrupt, then it should do the following.

1. It should determine the current state of the OOF condition. Recall, that this interrupt can be generated, whenever the XRT72L50 Framer IC declares or clears the OOF defect. Hence, the user can determine the current state of the OOF defect by reading the state of Bit 5 (RxOOF) within the Rx E3 Configuration and Status Register - 2, as illustrated below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	X	X	X	X

If the OOF state is TRUE

1. It should transmit a FERF (Far-End-Receive Failure) indicator to the Remote Terminal Equipment. Please see Section 5.2.4.2.1.3.

If the OOF state is FALSE

1. It should cease transmitting the FERF indication to the Remote Terminal Equipment.

NOTE: *The device cannot be configured to automatically send/clear FERF on LOS, LOOf, OOF or AIS in E3 G.751 mode. The user must implemt it in the ISR.*

Please see Section 5.2.4.2.1.3 on how to control the state of the A bit, which is transmitted via each outbound E3 frame.

5.3.6.2.3 The Change in Receive LOF Condition Interrupt

If the Change in Receive LOF Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an LOF (Out of Frame) Condition, and
2. When the XRT72L50 Framer IC clears the LOF condition.

Conditions causing the XRT72L50 Framer IC to declare an LOF Condition.

- If the Receive E3 Framer block (within the XRT72L50 Framer IC) detects Framing Bit errors, within four consecutive incoming E3 frames, and is not capable of transition back into the In-Frame state within a 1ms or 3ms period.

Conditions causing the XRT72L50 Framer IC to clear the LOF Condition.

- If the Receive E3 Framer block transitions from the OOF Condition state to the LOF Condition state (see Figure 124).
- If the Receive E3 Framer block transitions back into the In-Frame state.

Enabling and Disabling the Change in Receive LOF Condition Interrupt

The user can enable or disable the Change in Receive LOF Condition Interrupt, by writing the appropriate value into Bit 2 (LOF Interrupt Enable), within the RxE3 Interrupt Enable Register - 1, as indicated below.

RxE3 Interrupt Enable Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	X	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive LOF Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "Low".
- It will set Bit 6 (LOF Interrupt Status), within the Rx E3 Interrupt Status Register - 1 to “1”, as indicated below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	0	1	1	1

5.3.6.2.4 The Change in Receive AIS Condition Interrupt

If the Change in Receive AIS Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an AIS (Loss of Signal) Condition, and
2. When the XRT72L50 Framer IC clears the AIS condition.

Conditions causing the XRT72L50 Framer IC to declare an AIS Condition.

- If the XRT72L50 Framer IC detects 7 or less “0” within 2 consecutive E3 frames.

Conditions causing the XRT72L50 Framer IC to clear the AIS Condition.

- If the XRT72L50 Framer IC detects 2 consecutive E3 frames that each contain 8 or more “0’s”.

Enabling and Disabling the Change in Receive AIS Condition Interrupt

The user can enable or disable the Change in Receive LOS Condition Interrupt, by writing the appropriate value into Bit 0 (AIS Interrupt Enable), within the RxE3 Interrupt Enable Register - 1, as indicated below.

RxE3 Interrupt Enable Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	X	X

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive AIS Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "Low".

- It will set Bit 0 (AIS Interrupt Status), within the Rx E3 Interrupt Status Register - 1 to "1", as indicated below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	1

Whenever the user's system encounters the Change in Receive AIS Condition Interrupt, then it should do the following.

1. It should determine the current state of the AIS condition. Recall, that this interrupt can be generated, whenever the XRT72L50 Framer IC declares or clears the AIS defect. Hence, the user can determine the current state of the AIS defect by reading the state of Bit 3 (RxAIS) within the Rx E3 Configuration and Status Register - 2, as illustrated below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	0	1	1	1

If the AIS Condition is TRUE

1. It should begin transmitting the FERF indication to the Remote Terminal Equipment. Please see Section 5.2.4.2.1.3.

If the AIS Condition is FALSE

2. It should cease transmitting the FERF indication to the Remote Terminal Equipment.

NOTE: *The device cannot be configured to automatically send/clear FERF on LOS, LOOf, OOF or AIS in E3 G.751 mode. The user must implemt it in the ISR.*

Please see Section 5.2.4.2.1.3 for instructions on how to control the state of the A bit-field, within each outbound E3 frame.

5.3.6.2.5 The Change of Framing Alignment Interrupt

If the Change of Framing Alignment Interrupt is enabled then the XRT72L50 Framer IC will generate an interrupt any time the Receive E3 Framer block detects an abrupt change of framing alignment.

NOTE: *This interrupt is typically accompanied with the Change in Receive OOF Condition interrupt as well.*

Conditions causing the XRT72L50 Framer IC to generate this interrupt.

If the XRT72L50 Framer detects receives at least four consecutive E3 frames, within its Framing Alignment bytes in Error, then the XRT72L50 Framer IC will declare an OOF condition. However, while the XRT72L50 Framer IC is operating in the OOF condition, it will still rely on the old framing alignment for E3 payload data extraction, etc.

However, if the Receive E3 Framer had to change alignment, in order to re-acquire frame synchronization, then this interrupt will occur.

Enabling and Disabling the Change of Framing Alignment Interrupt

The user can enable or disable the Change of Framing Alignment Interrupt by writing the appropriate value into Bit 4 (COFA Interrupt Enable), within the Rx E3 Interrupt Enable Register - 1.

RxE3 Interrupt ENABLE Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	X	0	0	0	0

Writing a “1” into this bit-field enables the Change of Framing Alignment Interrupt. Conversely, writing a “0” into this bit-field disables the Change of Framing Alignment Interrupt.

Servicing the Change of Framing Alignment Interrupt

Whenever the XRT72L50 Framer IC generates this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$) by driving it "Low".
- It will set Bit 4 (COFA Interrupt Status), within the Rx E3 Interrupt Status Register -1, to “1”, as indicated below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	1	0	0	0	0

5.3.6.2.6 The Change in Receive FERF Condition Interrupt

If the Change in Receive FERF Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares a FERF (Far-End Receive Failure) Condition, and
2. When the XRT72L50 Framer IC clears the FERF condition.

Conditions causing the XRT72L50 Framer IC to declare an FERF Condition.

- If the XRT72L50 Framer IC begins receiving E3 frames which have the A bit set to “1”).

Conditions causing the XRT72L50 Framer IC to clear the AIS Condition.

- If the XRT72L50 Framer IC begins receiving E3 frames that do NOT have the A bit set to “1”.

Enabling and Disabling the Change in Receive AIS Condition Interrupt

The user can enable or disable the Change in Receive FERF Condition Interrupt, by writing the appropriate value into Bit 3 (FERF Interrupt Enable), within the RxE3 Interrupt Enable Register - 2, as indicated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Enable	BIP-4 Error Interrupt Enable	Framing Error Interrupt Enable	Not Used
R/W	RO	RO	RO	R/W	R/W	R/W	RO
0	0	0	0	X	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive FERF Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "Low".
- It will set Bit 3 (FERF Interrupt Status), within the Rx E3 Interrupt Status Register - 2 to “1”, as indicated below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Status	BIP-4 Error Interrupt Status	Framing Error Interrupt Status	Not Used
RO	RO	RO	RO	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

Whenever the user’s system encounters the Change in Receive FERF Condition Interrupt, then it should do the following.

1. It should determine the current state of the FERF condition. Recall, that this interrupt can be generated, whenever the XRT72L50 Framer IC declares or clears the FERF defect. Hence, the user can determine the current state of the FERF defect by reading the state of Bit 0 (RxFERF) within the Rx E3 Configuration and Status Register - 2, as illustrated below.

RxE3 Configuration & Status Register - 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Not Used		RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	0	0	1	1	1

5.3.6.2.7 The Detection of BIP-4 Error Interrupt

If the Detection of BIP-4 Error Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt, anytime the Receive E3 Framer block has detected an error in the BIP-4 Nibble, within an incoming E3 frame.

NOTE: This interrupt is only active if the XRT72L50 Framer IC has been configured to process the BIP-4 nibble within each incoming and outbound E3 frame.

Enabling and Disabling the Detection of FEBE Event Interrupt

The user can enable or disable the Detection of BIP-4 Error' interrupt by writing the appropriate value into Bit 2 (BIP-4 Interrupt Enable) within the Rx E3 Interrupt Enable Register - 2, as indicated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Enable	BIP-4 Error Interrupt Enable	Framing Error Interrupt Enable	Not Used
R/W	RO	RO	RO	R/W	R/W	R/W	RO
0	0	0	0	0	X	0	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the Detection of the BIP-4 Error Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "High".
- It will set the Bit 2 (BIP-4 Interrupt Status), within the RxE3 Interrupt Status Register - 2 as indicated below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Status	BIP-4 Error Interrupt Status	Framing Error Interrupt Status	Not Used
RO	RO	RO	RO	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

Whenever the Terminal Equipment encounters the Detection of BIP-4 Error Interrupt, it should do the following.

- It should read the contents of the PMON Parity Error Event Count Registers (located at Addresses 0x54 and 0x55) in order to determine the number of BIP-4 Errors that have been received by the XRT72L50 Framer IC.

5.3.6.2.8 The Detection of Framing Error Interrupt

If the Detection of Framing Error Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt, anytime the Receive E3 Framer block has received an E3 frame with an incorrect FAS pattern value.

Enabling and Disabling the Detection of Framing Error Interrupt

The user can enable or disable the Detection of Framing Error' interrupt by writing the appropriate value into Bit 1 (Framing Error Interrupt Enable) within the Rx E3 Interrupt Enable Register - 2, as indicated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Enable	BIP-4 Error Interrupt Enable	Framing Error Interrupt Enable	Not Used
R/W	RO	RO	RO	R/W	R/W	R/W	RO
0	0	0	0	0	0	X	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the Detection of Framing Error Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "High".
- It will set the Bit 1 (Framing Error Interrupt Status), within the RxE3 Interrupt Status Register - 2 as indicated below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FERF Interrupt Status	BIP-4 Error Interrupt Status	Framing Error Interrupt Status	Not Used
RO	RO	RO	RO	RUR	RUR	RUR	RUR
0	0	0	0	0	0	1	0

Whenever the Terminal Equipment encounters the Detection of Framing Error Interrupt, it should do the following.

- It should read the contents of the PMON Framing Bit/Byte Error Count Registers (located at Addresses 0x52 and 0x53) in order to determine the number of Framing errors that have been received by the XRT72L50 Framer IC.

5.3.6.2.9 The Receipt of New LAPD Message Interrupt

If the Receive LAPD Message Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt anytime the Receive HDLC Controller block has received a new LAPD Message frame from the Remote Terminal Equipment, and has stored the contents of this message into the Receive LAPD Message buffer.

Enabling/Disabling the Receive LAPD Message Interrupt

The user can enable or disable the Receive LAPD Message Interrupt by writing the appropriate data into Bit 1 (RxLAPD Interrupt Enable) within the Rx E3 LAPD Control Register, as indicated below.

RxE3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Enable
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	X	0

Writing a “1” into this bit-field enables the Receive LAPD Message Interrupt. Conversely, writing a “0” into this bit-field disables the Receive LAPD Message Interrupt.

Servicing the Receive LAPD Message Interrupt

Whenever the XRT72L50 Framer IC generates this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$), by driving it "Low".
- It will set Bit 0 (RxLAPD Interrupt Status), within the Rx E3 LAPD Control register to “1”, as indicated below.

RxE3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	0	1

- It will write the contents of the newly Received LAPD Message into the Receive LAPD Message buffer (located at 0xDE through 0x135).

Whenever the Terminal Equipment encounters the Receive LAPD Message Interrupt, then it should read out the contents of the Receive LAPD Message buffer, and respond accordingly.

6.0 E3/ITU-T G.832 OPERATION OF THE XRT72L50

The XRT72L50 can be configured to operate in the E3/ITU-T G.832 Mode by writing a “0” into bit-field 6 and a “1” into bit-field 2, within the Framer Operating Mode register, as illustrated below.

Framer Operating Mode Register (Address = 0x00)

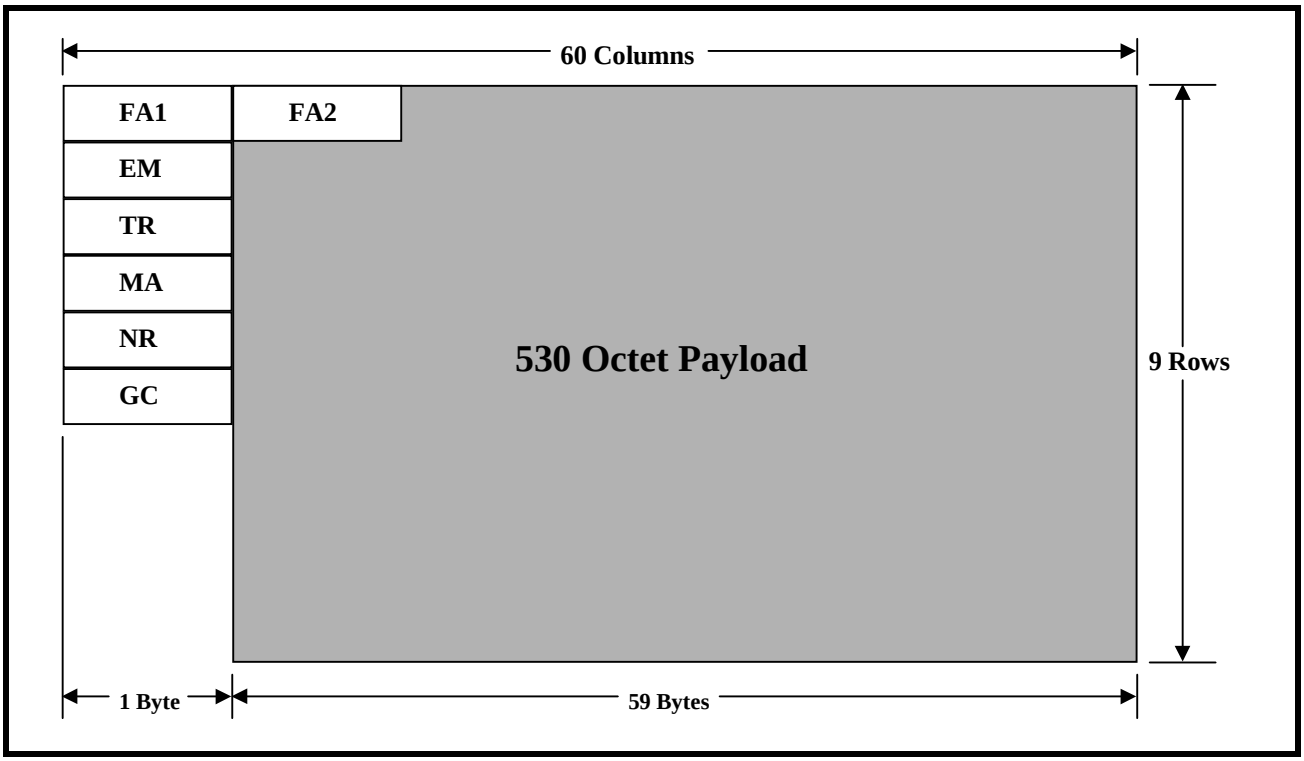
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	0	x	0	x	1	x	x

6.1 *Description of the E3, ITU-T G.832 Frames and Associated Overhead Bytes*

The E3, ITU-T G.832 Frame contains 537 bytes, of which 7 bytes are overhead and the remaining 530 bytes are payload bytes.

These 537 octets are arranged in 9 rows of 60 columns each, except for the last three rows which contain only 59 columns. The frame repetition rate for this type of E3 frame is 8000 times per second, thereby resulting in the standard E3 bit rate of 34.368 Mbps. Figure 142 presents an illustration of the E3, ITU-T G.832 Frame Format.

FIGURE 142. ILLUSTRATION OF THE E3, ITU-T G.832 FRAMING FORMAT.



6.1.1 Definition of the Overhead Bytes

The seven (7) overhead bytes are shown in Figure 142, as FA1, FA2, EM, TR, MA, NR and GC. Each of these Overhead Bytes are further defined below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	1	x	0	x	x	x	x

6.1.1.1 *Frame Alignment (FA1 and FA2) Bytes*

FA1 and FA2 are known as the frame alignment bytes. The Receive E3 Framer, while trying to acquire or maintain framing synchronization with its incoming E3 frames, will attempt to locate these two bytes. FA1 is assigned the value, 0xF6, and FA2 is assigned the value, 0x28.

6.1.1.2 *Error Monitor (EM) Byte*

The EM byte contains the results of BIP-8 (Bit-Interleaved Parity) calculations over an entire E3 frame. The Bit Interleaved Parity (BIP-8) byte field supports error detection, during the transmission of E3 frames, between the Local Terminal Equipment and the Remote Terminal Equipment.

The Transmit E3 Framer will compute the BIP-8 value over the 537 octet structure, within each E3 frame. The resulting BIP-8 value is then inserted into the EM byte-field within the very next E3 frame. BIP-8 is an eight bit code in which the nth bit of the BIP-8 code reflects the even-parity bit calculated with the nth bit of each of the 537 octets within the E3 frame. Thus, the BIP-8 value presents the results for 8 separate even-bit parity calculations.

The Receive E3 Framer will compute its own version of the EM bytes for each E3 frame that it receives. Afterwards, it will compare the value of its locally computed EM byte with the EM byte that it receives in the very next E3 frame. If the two EM byte values are equal, then the Receive E3 Framer will conclude that this E3 frame was received in an error-free manner. Further, the Receive E3 Framer block will inform the Remote Terminal Equipment of this fact by having the Local Terminal Equipment set the FEBE (Far-End-Block Error) bit, within the MA Byte of an Outbound E3 frame (to the Remote Terminal Equipment) to “0”. Please see Section 6.1.1.4 for a discussion of the MA Byte.

However, if the Receive E3 Framer block detects an error in the incoming EM byte, then it will conclude that the corresponding E3 frame is errored. Further, the Receive E3 Framer block will inform the Remote Terminal (e.g., the source of this erred E3 frame) of this fact by having the Local Terminal Equipment (e.g., the Transmit E3 Framer block) set the FEBE bit, within an Outbound E3 frame (destined to the Remote Terminal) to “1”.

NOTE: *A detailed discussion on the practical use of the EM byte is presented in* Section 6.3.2.7*.*

6.1.1.3 *The Trail-Trace Buffer (TTB) Byte*

This byte-field is used to repetitively transmit a Trail-access point identifier so that a trail receiving terminal can verify its continued connection to the intended transmitter. The trail access point identifier uses the 16-byte numbering format as tabulated in Table 65.

TABLE 65: DEFINITION OF THE TRAIL TRACE BUFFER BYTES, WITHIN THE E3, ITU-T G.832 FRAMING FORMAT

BYTE NUMBER	TRAIL TRACE BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1 (Frame Start Marker)	1	C6	C5	C4	C3	C2	C1	C0
2	X	X	X	X	X	X	X	X
*	X	X	X	X	X	X	X	X
*	X	X	X	X	X	X	X	X
16	X	X	X	X	X	X	X	X

The first byte of this 16-byte string is a frame start marker and is typically of the form [1, C6, C5, C4, C3, C2, C1, C0]. The "1" in the MSB (most significant bit) of this first byte is used to identify this byte as the frame start marker (e.g., the first byte of the 16-byte Trail Trace Buffer Sequence). The bits: C6 through C0 are the results of a CRC-7 calculation over the previous 16-byte frame. The subsequent 15 bytes are used for the transport of 15 ASCII characters required for the E.164 numbering format.

The MSB (bit 7) of these bytes is always "0".

6.1.1.4 *Maintenance and Adaptation (MA) Byte*

The MA byte is responsible for carrying the FERF (Far-End Receive Failure) and the FEBE (Far-End Block Error) status indicators from one terminal to another. The MA byte-field also carries the Payload Type, the Payload Dependent and the Timing Marker indicators. The byte format for the MA byte is presented below.

The Maintenance and Adaptation (ma) byte format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FERF	FEBE	Payload Type			Payload Dependent		Timing Marker

Bit 7 - FERF (Far-End Receive Failure)

If the Receive E3 Framer block (at a Local Terminal) is experiencing problems receiving E3 frame data from a Remote Terminal (e.g., an LOS, OOF or AIS condition), then it will inform the Remote Terminal Equipment of this fact by commanding the Local Transmit E3 Framer block to set the FERF bit-field (within the MA byte) of an Outbound E3 frame, to "1". The Local Transmit E3 Framer block will continue to set the FERF bit-field (within the subsequent Outbound E3 frames) to "1" until the Receive E3 Framer block no longer experiences problems in receiving the E3 frame data. If the Remote Terminal Equipment receives a certain number of consecutive E3 frames, with the FERF bit-field set to "1", then the Remote Terminal Equipment will interpret this signaling as an indication of a Far-End Receive Failure (e.g., a problem with the Local Terminal Equipment).

Conversely, if the Receive E3 Framer block (at a Local Terminal Equipment) is not experiencing any problems receiving E3 frame data from a Remote Terminal Equipment, then it will also inform the Remote Terminal Equipment of this fact by commanding the Local Transmit E3 Framer block to set the FERF bit-field (within the MA byte-field) of an Outbound E3 frame (which is destined for the Remote Terminal) to "0". The Remote Terminal Equipment will interpret this form of signaling as an indication of a normal operation.

NOTE: *A detailed discussion into the practical use of the FERF bit-field is presented in* Section 6.2.4.2.1.

Bit 6 - FEBE (Far-End Block Error)

If a Local Receive E3 Framer block detects an error in the EM byte, within an incoming E3 frame that it has received from the Remote Terminal Equipment, then it will inform the Remote Terminal Equipment of this error by commanding the Local Transmit E3 Framer block to set the FEBE bit-field (within the MA byte-field) of an Outbound E3 frame (which is destined for the Remote Terminal Equipment) to "1". The Remote Terminal

Equipment will interpret this signaling as an indication that the E3 frames that it is transmitting back out to the Local Receive E3 Framer block are erred.

Conversely, if the Local Receive E3 Framer block does not detect any errors in the EM byte, within the incoming E3 frame, then it will also inform the Remote Terminal Equipment of this fact by commanding the Local Transmit E3 Framer block to set the FEBE bit-field of an Outbound E3 frame (which is destined for the Remote Terminal Equipment) to "0".

NOTE: *A detailed discussion into the practical use of the FEBE bit-field is presented in* Section 6.2.4.2.1.

Bits 5 - 3 Payload Type

These bit-fields indicate to the Remote Terminal Equipment, what kind of data is being transported in the 530 bytes of E3 frame payload data. Some of the defined payload type values are tabulated in Table 66.

TABLE 66: A LISTING OF THE VARIOUS PAYLOAD TYPE VALUES AND THEIR CORRESPONDING MEANING

PAYLOAD TYPE VALUE	MEANING
000	Unequipped
001	Equipped
010	ATM Cells
011	SDH TU-12s

Bits 2 - 1 Payload Dependent

To be provided later.

Bit 0 - Timing Marker

This bit-field is set to "0" to indicate that the timing source is traceable to a Primary Reference Clock. Otherwise, this bit-field is set to "1".

6.1.1.5 *The Network Operator (NR) Byte*

The NR byte or the GC byte can be configured to transport LAP-D Message frame octets from the LAPD Transmitter to the LAPD Receiver (of the Remote Terminal Equipment) at a data rate of 64kbps (1 byte per E3 frame).

If the user opts not to use the NR byte to transport these LAPD Message frames, then the Transmit E3 Framer block will read in the contents of the TxNR Byte Register (Address = 0x37), and insert this value into the NR byte-field of each Outbound E3 frame. The Receive E3 Framer block will read in the contents of the NR byte-field within each incoming E3 frame and will write it into the RxNR Byte register. Consequently, the user can determine the value of the NR byte, within the most recently received E3 frame by reading the Rx NR Byte Register (Address = 0x1A).

6.1.1.6 *The General Purpose Communications Channel (GC) Byte*

The NR byte or the GC byte can be configured to transport LAPD Message frames from the LAPD Transmitter to the LAPD Receiver (of the Remote Terminal Equipment) at a data rate of 64kbps (1 byte per E3 frame).

If the user opts not to use the GC byte to transport these LAPD Message frames, then the Transmit E3 Framer block will read in the contents of the Tx GC Byte Register (Address = 0x35), and insert this value into the GC byte-field of each Outbound E3 frame.

The Receive E3 Framer block will read in the contents of the GC byte-field, within each incoming E3 frame, and will write it into the RxGC Byte register. Consequently, the user can determine the value of the GC byte, within the most recently received E3 frame, by reading the Rx GC Byte register (Address = 0x1B).

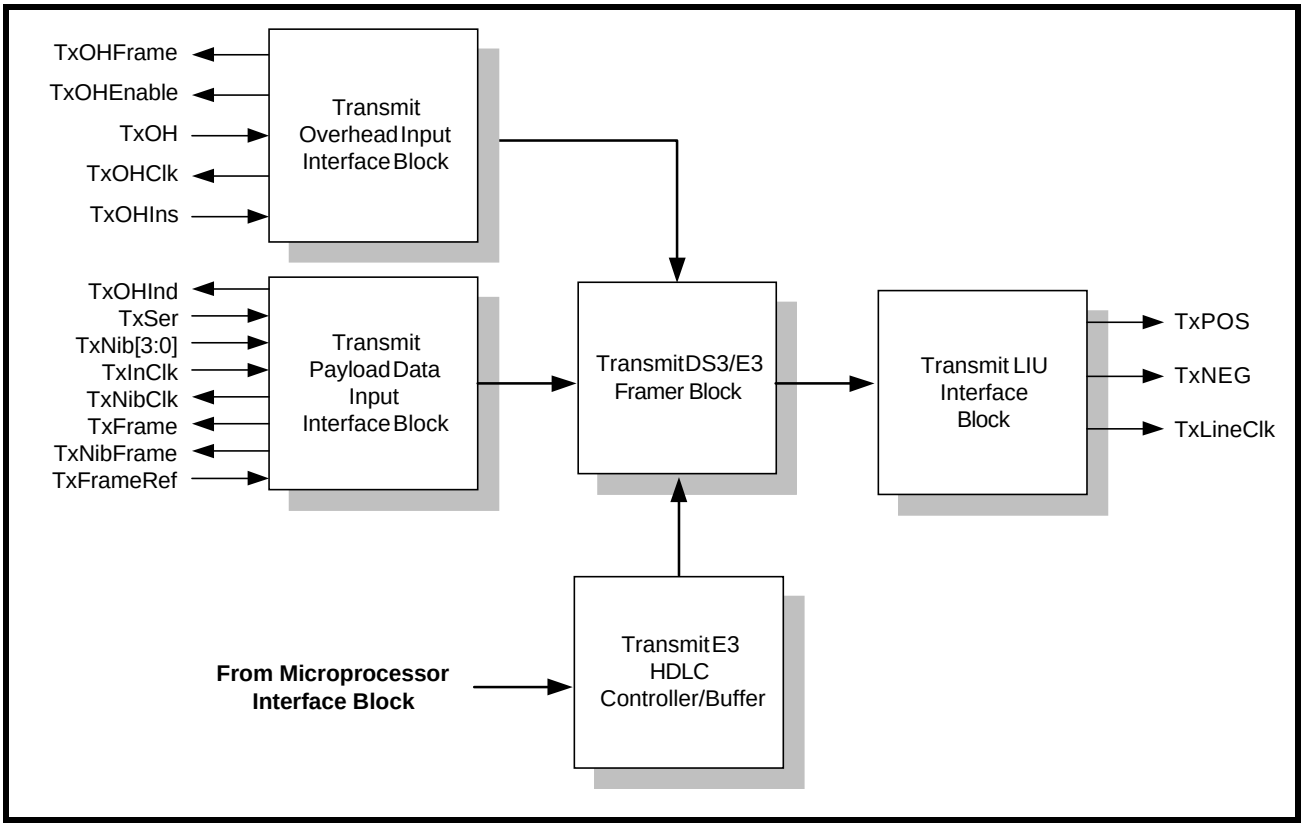
6.2 *The Transmit Section of the XRT72L50 (E3 Mode Operation)*

When the XRT72L50 has been configured to operate in the E3, ITU-T G.832 Mode, the Transmit Section of the XRT72L50 consists of the following functional blocks.

- Transmit Payload Data Input Interface block
- Transmit Overhead Data Input Interface block
- Transmit E3 Framer block
- Transmit HDLC Controller block
- Transmit LIU Interface block

Figure 143 presents a simple illustration of the Transmit Section of the XRT72L50 Framer IC.

FIGURE 143. THE TRANSMIT SECTION CONFIGURED TO OPERATE IN THE E3 MODE

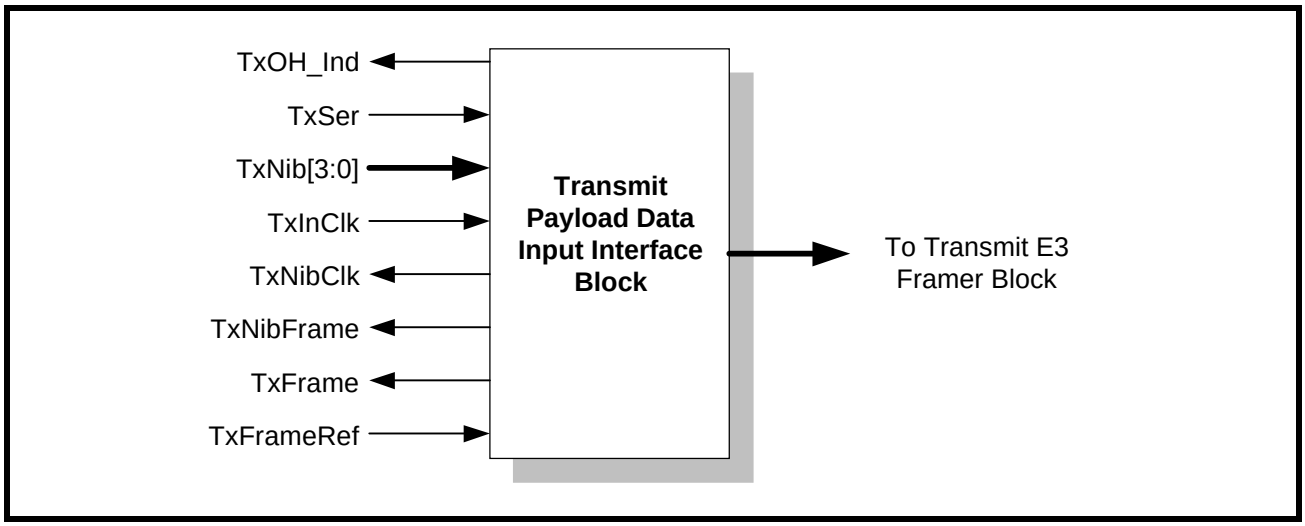


Each of these functional blocks will be discussed in detail in this document.

6.2.1 The Transmit Payload Data Input Interface Block

Figure 144 presents a simple illustration of the Transmit Payload Data Input Interface block.

FIGURE 144. THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK



Each of the input and output pins of the Transmit Payload Data Input Interface are listed in Table 67 and described below. The exact role that each of these inputs and output pins assume, for a variety of operating scenarios are described throughout this section.

TABLE 67: LISTING AND DESCRIPTION OF THE PINS ASSOCIATED WITH THE TRANSMIT PAYLOAD DATA INPUT INTERFACE

SIGNAL NAME	TYPE	DESCRIPTION
TxSer	Input	**Transmit Serial Payload Data Input Pin:** If the user opts to operate the XRT72L50 in the serial mode, then the Terminal Equipment is expected to apply the payload data (that is to be transported via the Outbound E3 data stream) to this input pin. The XRT72L50 will sample the data that is at this input pin upon the rising edge either the RxOutClk or the TxInClk signal (whichever is appropriate). ***NOTE:*** *This signal is only active if the NibIntf input pin is pulled "Low".*
TxNib[3:0]	Input	**Transmit Nibble-Parallel Payload Data Input pins:** If the user opts to operate the XRT72L50 in the Nibble-Parallel mode, then the Terminal Equipment is expected to apply the payload data (that is to be transported via the Outbound E3 data stream) to these input pins. The XRT72L50 will sample the data that is at these input pins upon the rising edge of the TxNibClk signal. ***NOTE:*** *These pins are only active if the NibIntf input pin is pulled "High".*
TxInClk	Input	**Transmit Section Timing Reference Clock Input pin:** The Transmit Section of the XRT72L50 can be configured to use this clock signal as the Timing Reference. If the user has made this configuration selection, then the XRT72L50 will use this clock signal to sample the data on the TxSer input pin. ***NOTE:*** *If this configuration is selected, then a 34.368 MHz clock signal must be applied to this input pin.*

TABLE 67: LISTING AND DESCRIPTION OF THE PINS ASSOCIATED WITH THE TRANSMIT PAYLOAD DATA INPUT INTERFACE

SIGNAL NAME	TYPE	DESCRIPTION
TxNibClk	Output	**Transmit Nibble Mode Output** If the user opts to operate the XRT72L50 in the Nibble-Parallel mode, then the XRT72L50 will derive this clock signal from the selected Timing Reference for the Transmit Section of the chip (e.g., either the TxInClk or the RxLineClk signals). The XRT72L50 will use this signal to sample the data on the TxNib[3:0] input pins.
TxOHInd	Output	**Transmit Overhead Bit Indicator Output:** This output pin will pulse "High" one-bit period prior to the time that the Transmit Section of the XRT72L50 will be processing an Overhead bit. The purpose of this output pin is to warn the Terminal Equipment that, during the very next bit-period, the XRT72L50 is going to be processing an Overhead bit and will be ignoring any data that is applied to the TxSer input pin.
TxFrame	Output	**Transmit End of Frame Output Indicator:** The Transmit Section of the XRT72L50 will pulse this output pin "High" (for one bit-period), when the Transmit Payload Data Input Interface is processing the last bit of a given E3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new E3 frame to the XRT72L50 (e.g., to permit the XRT72L50 to maintain Transmit E3 framing alignment control over the Terminal Equipment).
TxFrameRef	Input	**Transmit Frame Reference Input:** The XRT72L50 permits the user to configure the Transmit Section to use this input pin as a frame reference. If the user makes this configuration selection, then the Transmit Section will initiate its transmission of a new E3 frame, upon the rising edge of this signal. The purpose of this input pin is to permit the Terminal Equipment to maintain Transmit E3 Framing alignment control over the XRT72L50.
TxNibFrame	Output	**Transmit Frame Boundary Indicator - Nibble/Parallel Interface:** This output pin pulses "High" when the last nibble of a given DS3 or E3 frame is expected at the TxNib[3:0] input pins. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame to the XRT72L50.

Operation of the Transmit Payload Data Input Interface

The Transmit Terminal Input Interface is extremely flexible, in that it permits the user to make the following configuration options.

- The Serial or the Nibble-Parallel Interface Mode
- The Loop-Timing or the TxInClk (Local Timing) Mode

Further, if the XRT72L50 has been configured to operate in the TxInClk mode, then the user has two additional options.

- The XRT72L50 is the Frame Master (e.g., it dictates when the Terminal Equipment will initiate the transmission of data within a new E3 frame).
- The XRT72L50 is the Frame Slave (e.g., the Terminal Equipment will dictate when the XRT72L50 initiates the transmission of a new E3 frame).

Given these three set of options, the Transmit Terminal Input Interface can be configured to operate in one of the six (6) following modes.

- Mode 1 - Serial/Loop-Timed Mode
- Mode 2 - Serial/Local-Timed/Frame Slave Mode
- Mode 3 - Serial/Local-Timed/Frame Master Mode
- Mode 4 - Nibble/Loop-Timed Mode
- Mode 5 - Nibble/Local-Timed/Frame Slave Mode
- Mode 6 - Nibble/Local-Timed/Frame Master Mode

Each of these modes are described, in detail, below.

6.2.1.1 *Mode 1 - The Serial/Loop-Timing Mode*

The Behavior of the XRT72L50

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will behave as follows.

A. Loop-Timing (Uses the RxLineClk signal as the Timing Reference)

Since the XRT72L50 is configured to operate in the loop-timed mode, the Transmit Section (of the XRT72L50) will use the RxLineClk input clock signal (e.g., the Recovered Clock signal, from the LIU) as its timing source. When the XRT72L50 is operating in this mode it will do the following.

1. It will ignore any signal at the TxInClk input pin.
2. The XRT72L50 will output a 34.368MHz clock signal via the RxOutClk output pin. This clock signal functions as the Transmit Payload Data Input Interface block clock signal.
3. The XRT72L50 will use the rising edge of the RxOutClk signal to latch in the data residing on the TxSer input pin.

B. Serial Mode

The XRT72L50 will accept the E3 payload data from the Terminal Equipment, in a serial-manner, via the TxSer input pin The Transmit Payload Data Input Interface will latch this data into its circuitry, on the rising edge of the RxOutClk output clock signal.

C. Delineation of Outbound E3 frames

The XRT72L50 will pulse the TxFrame output pin "High" for one bit-period, coincident with the XRT72L50 processing the last bit of a given E3 frame.

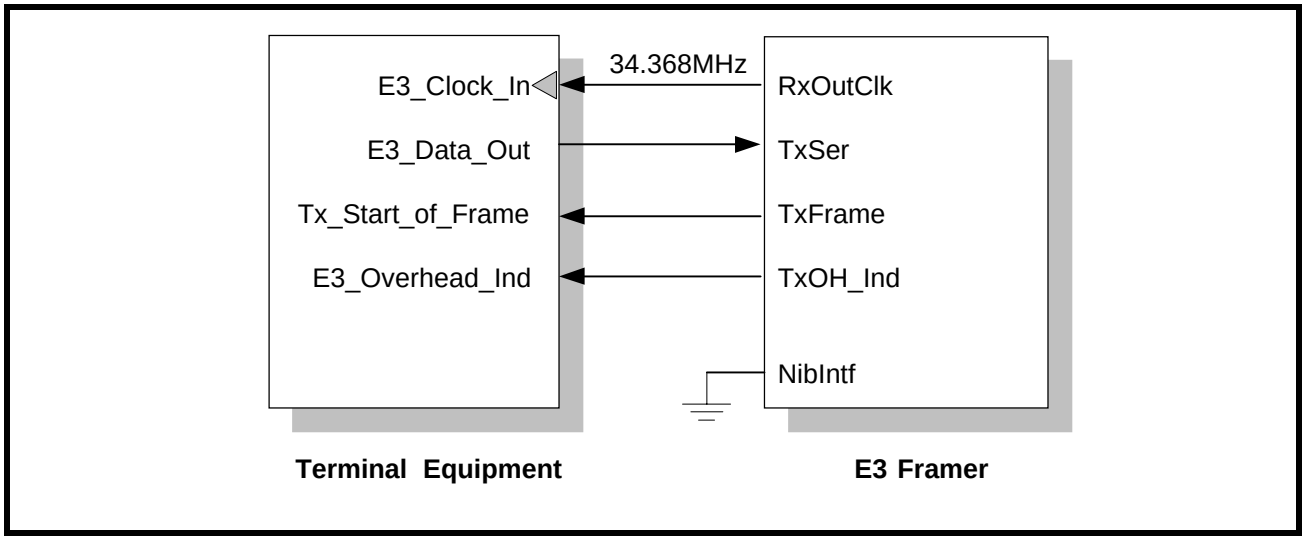
D. Sampling of Payload Data, from the Terminal Equipment

In Mode 1, the XRT72L50 will sample the data at the TxSer input, on the rising edge of RxOutClk.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 1 Operation

Figure 145 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 1 operation.

FIGURE 145. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 1(SERIAL/LOOP-TIMED) OPERATION



Mode 1 Operation of the Terminal Equipment

When the XRT72L50 is operating in this mode it will function as the source of the 34.368MHz clock signal. This clock signal will be used as the Terminal Equipment Interface clock by both the XRT72L50 IC and the Terminal Equipment.

The Terminal Equipment will serially output the payload data of the Outbound E3 data stream via its E3_Data_Out pin. The Terminal Equipment will update the data on the E3_Data_Out pin upon the rising edge of the 34.368 MHz clock signal, at its E3_Clock_In input pin (as depicted in Figure 145 and Figure 146).

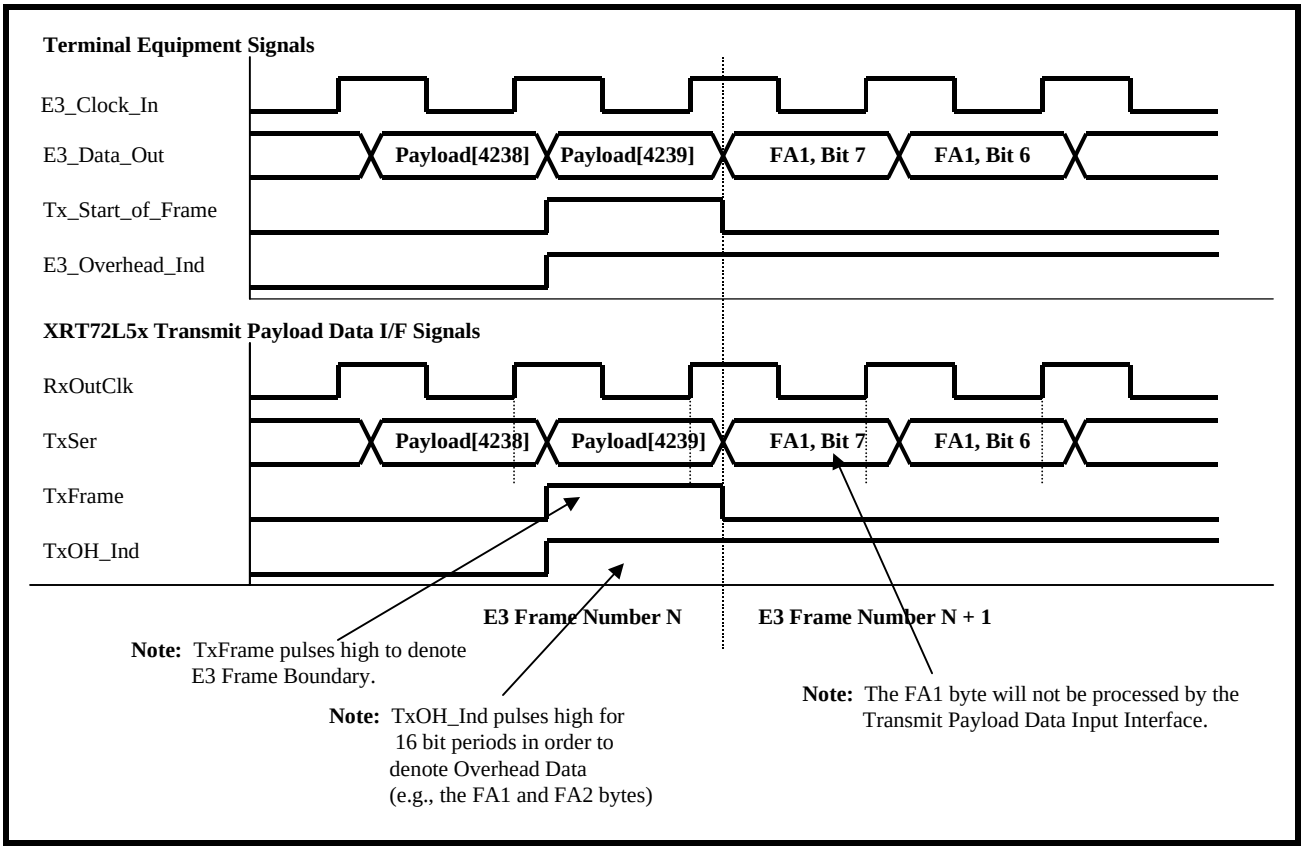
The XRT72L50 will latch the Outbound E3 data stream (from the Terminal Equipment) on the rising edge of the RxOutClk signal.

The XRT72L50 will indicate that it is processing the last bit, within a given Outbound E3 frame, by pulsing its TxFrame output pin "High" for one bit-period. When the Terminal Equipment detects this pulse at its Tx_Start_of_Frame input, it is expected to begin transmission of the very next Outbound E3 frame to the XRT72L50 via the E3_Data_Out (or TxSer pin).

Finally, the XRT72L50 will indicate that it is about to process an overhead bit by pulsing the TxOH_Ind output pin "High" one bit period prior to its processing of an OH (Overhead) bit. In Figure 145, the TxOH_Ind output pin is connected to the E3_Overhead_Ind input pin, of the Terminal Equipment. Whenever the E3_Overhead_Ind pin is pulsed "High" the Terminal Equipment is expected to not transmit a E3 payload bit upon the very next clock edge. Instead, the Terminal Equipment is expected to delay its transmission of the very next payload bit, by one clock cycle.

The behavior of the signals, between the XRT72L50 and the Terminal Equipment, for E3 Mode 1 operation is illustrated in Figure 146.

FIGURE 146. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK OF THE XRT72L50 AND THE TERMINAL EQUIPMENT (FOR MODE 1 OPERATION)



How to configure the XRT72L50 into the Serial/Loop-Timed/Non-Overhead Interface Mode

1. Set the NibIntf input pin "Low".
2. Set the TimRefSel[1:0] bit fields (within the Framer Operating Mode Register) to "00" as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	1	0	0

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 145.

6.2.1.2 *Mode 2 - The Serial/Local-Timed/Frame-Slave Mode Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will function as follows.

A. Local Timing - Uses the TxInClk signal as the Timing Reference

In this mode, the Transmit Section of the XRT72L50 will use the TxInClk signal as its timing reference.

B. Serial Mode

The XRT72L50 will receive the E3 payload data, in a serial manner, via the TxSer input pin. The Transmit Payload Data Input Interface (within the XRT72L50) will latch this data into its circuitry, on the rising edge of the TxInClk input clock signal.

C. Delineation of Outbound E3 frames (Frame Slave Mode)

The Transmit Section of the XRT72L50 will use the TxInClk input as its timing reference, and will use the TxFrameRef input signal as its framing reference. In other words, the Transmit Section of the XRT72L50 will initiate frame generation upon the rising edge of the TxFrameRef input signal).

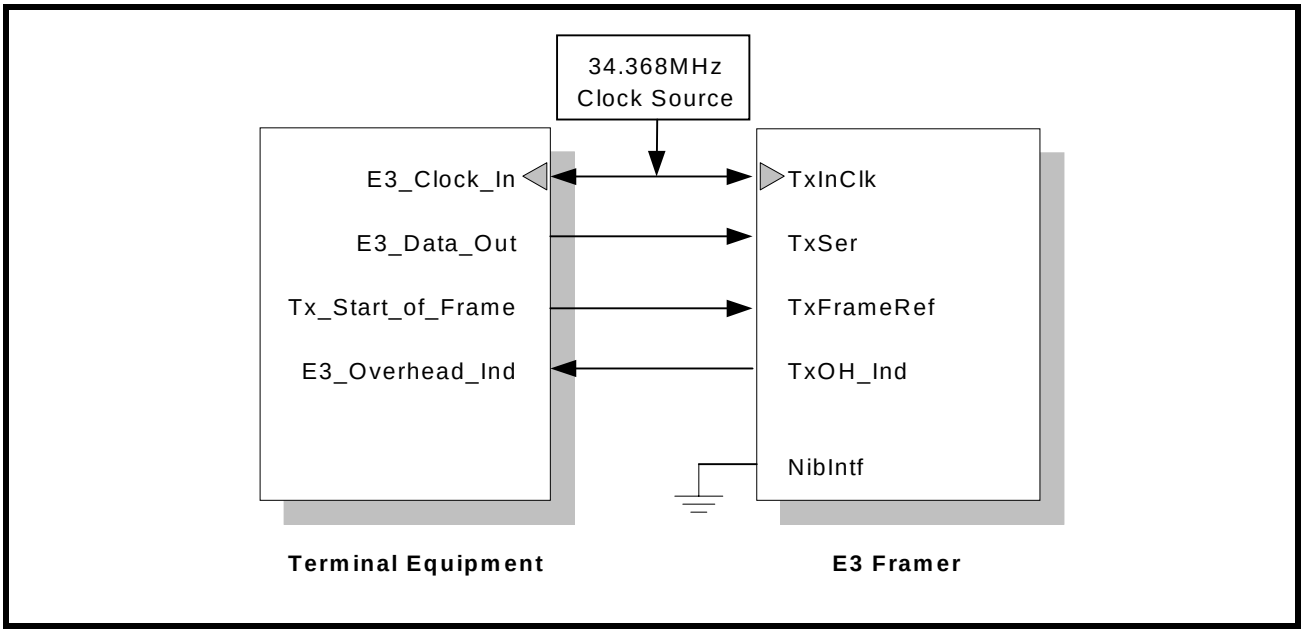
D. Sampling of payload data, from the Terminal Equipment

In Mode 2, the XRT72L50 will sample the data, at the TxSer input pin, on the rising edge of TxInClk.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 2 Operation

Figure 147 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 2 operation.

FIGURE 147. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 2 (SERIAL/LOCAL-TIMED/FRAME-SLAVE) OPERATION



Mode 2 Operation of the Terminal Equipment

As shown in Figure 147, both the Terminal Equipment and the XRT72L50 will be driven by an external 34.368MHz clock signal. The Terminal Equipment will receive the 34.368MHz clock signal via its E3_Clock_In input pin, and the XRT72L50 Framer IC will receive the 34.368MHz clock signal via the TxInClk input pin.

The Terminal Equipment will serially output the payload data of the Outbound E3 data stream, via the E3_Data_Out output pin, upon the rising edge of the signal at the E3_Clock_In input pin. (Note: The E3_Data_Out output pin of the Terminal Equipment is electrically connected to the TxSer input pin). The XRT72L50 Framer IC will latch the data, residing on the TxSer input line, on the rising edge of the TxInClk signal.

In this case, the Terminal Equipment has the responsibility of providing the framing reference signal by pulsing its Tx_Start_of_Frame output signal (and in turn, the TxFrameRef input pin of the XRT72L50), "High" for one-bit period, coincident with the first bit of a new E3 frame. Once the XRT72L50 detects the rising edge of the input at its TxFrameRef input pin, it will begin generation of a new E3 frame.

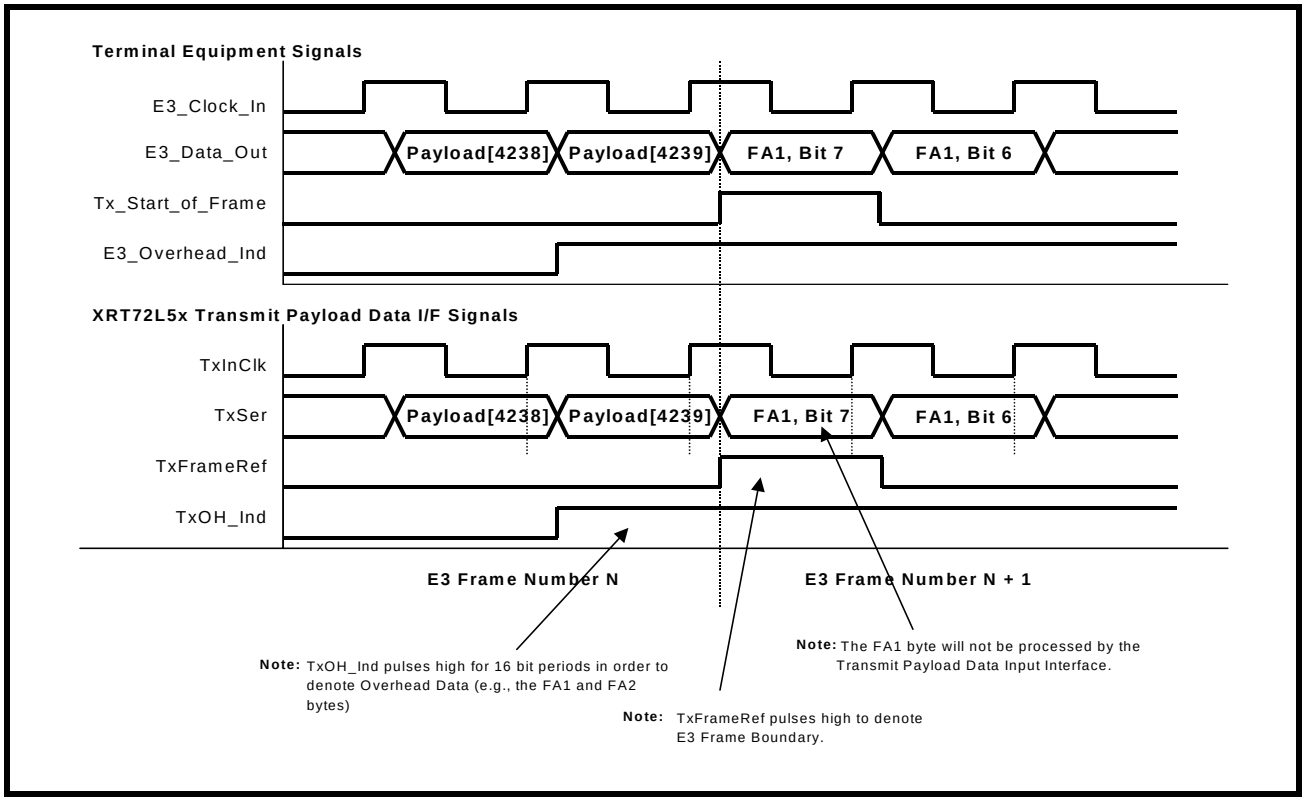
NOTES:

1. *In this case, the Terminal Equipment is controlling the start of Frame Generation, and is therefore referred to as the Frame Master. Conversely, since the XRT72L50 does not control the generationi of a new E3 frame, but is rather driven by the Terminal Equipment, the XRT72L50 is referred to as the Frame Slave.*
2. *If the user opts to configure the XRT72L50 to operate in Mode 2, it is imperative that the Tx_Start_of_Frame (or TxFrameRef) signal is synchronized to the TxInClk input clock signal.*

Finally, the XRT72L50 will pulse its TxOH_Ind output pin, one bit-period prior to it processing a given overhead bit, within the Outbound E3 frame. Since the TxOH_Ind output pin (of the XRT72L50) is electrically connected to the E3_Overhead_Ind, whenever the XRT72L50 pulses the TxOH_Ind output pin "High", it will also be driving the E3_Overhead_Ind input pin (of the Terminal Equipment) "High". Whenever the Terminal Equipment detects this pin toggling "High", it should delay transmission of the very next E3 frame payload bit by one clock cycle.

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Mode 2 Operation is illustrated in Figure 148.

FIGURE 148. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (MODE 2 OPERATION)



How to configure the XRT72L50 to operate in this mode.

1. Set the NibIntf input pin "Low".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "01" as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	1	0	1

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 147.

6.2.1.3 *Mode 3 - The Serial/Local-Timed/Frame-Master ModeBehavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will function as follows.

A. Local Timed - Uses the TxInClk signal as the Timing Reference

In this mode, the Transmit Section of the XRT72L50 will use the TxInClk signal as its timing reference.

B. Serial Mode

The XRT72L50 will receive the E3 payload data, in a serial manner, via the TxSer input pin. The Transmit Payload Data Input Interface (within the XRT72L50) will latch this data into its circuitry, on the rising edge of the TxInClk input clock signal.

C. Delineation of Outbound E3 frames (Frame Master Mode)

The Transmit Section of the XRT72L50 will use the TxInClk signal as its timing reference, and will initiate E3 frame generation, asynchronously with respect to any externally applied signal. The XRT72L50 will pulse its TxFrame output pin "High" whenever it is processing the very last bit-field within a given E3 frame.

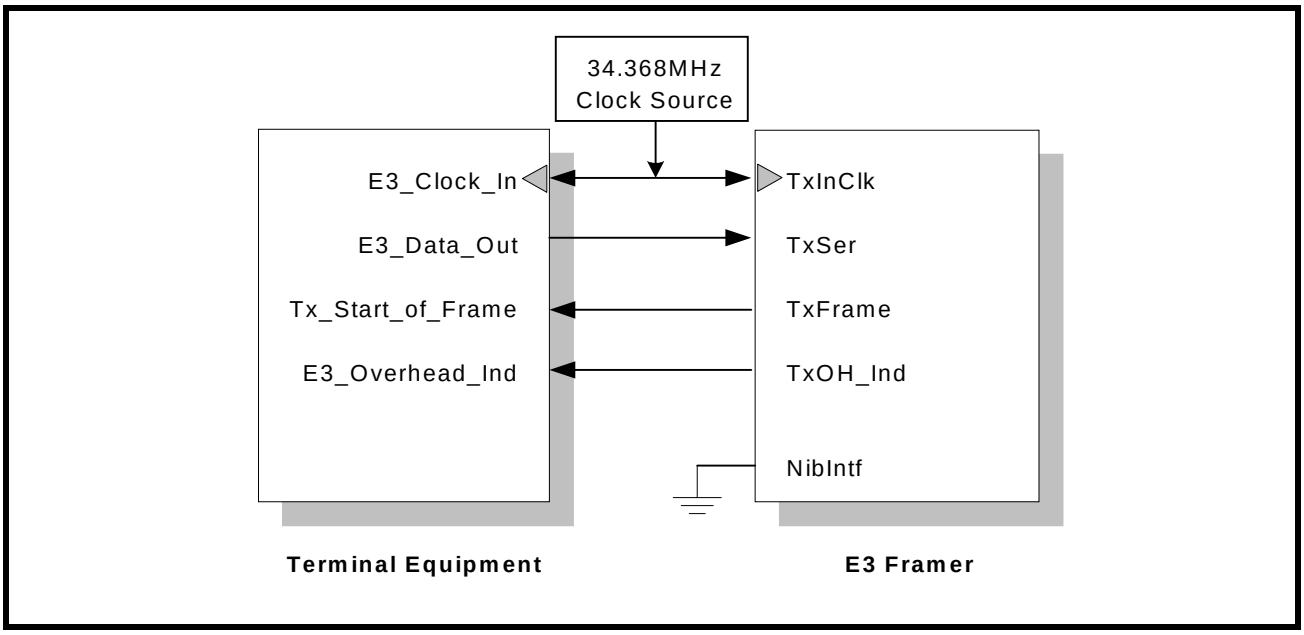
D. Sampling of payload data, from the Terminal Equipment

In Mode 3, the XRT72L50 will sample the data, at the TxSer input pin, on the rising edge of TxInClk.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 3 Operation

Figure 149 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 3 operation.

FIGURE 149. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 3 (SERIAL/LOCAL-TIMED/FRAME-MASTER) OPERATION



Mode 3 Operation of the Terminal Equipment

In Figure 149, both the Terminal Equipment and the XRT72L50 are driven by an external 34.368 MHz clock signal. This clock signal is connected to the E3_Clock_In input of the Terminal Equipment and the TxInClk input pin of the XRT72L50.

The Terminal Equipment will serially output the payload data on its E3_Data_Out output pin, upon the rising edge of the signal at the E3_Clock_In input pin. Similarly, the XRT72L50 will latch the data, residing on the TxSer input pin, on the rising edge of TxInClk.

The XRT72L50 will pulse the TxFrame output pin "High" for one bit-period, coincident while it is processing the last bit-field within a given Outbound E3 frame. The Terminal Equipment is expected to monitor the TxFrame signal (from the XRT72L50) and to place the first bit, within the very next Outbound E3 frame on the TxSer input pin.

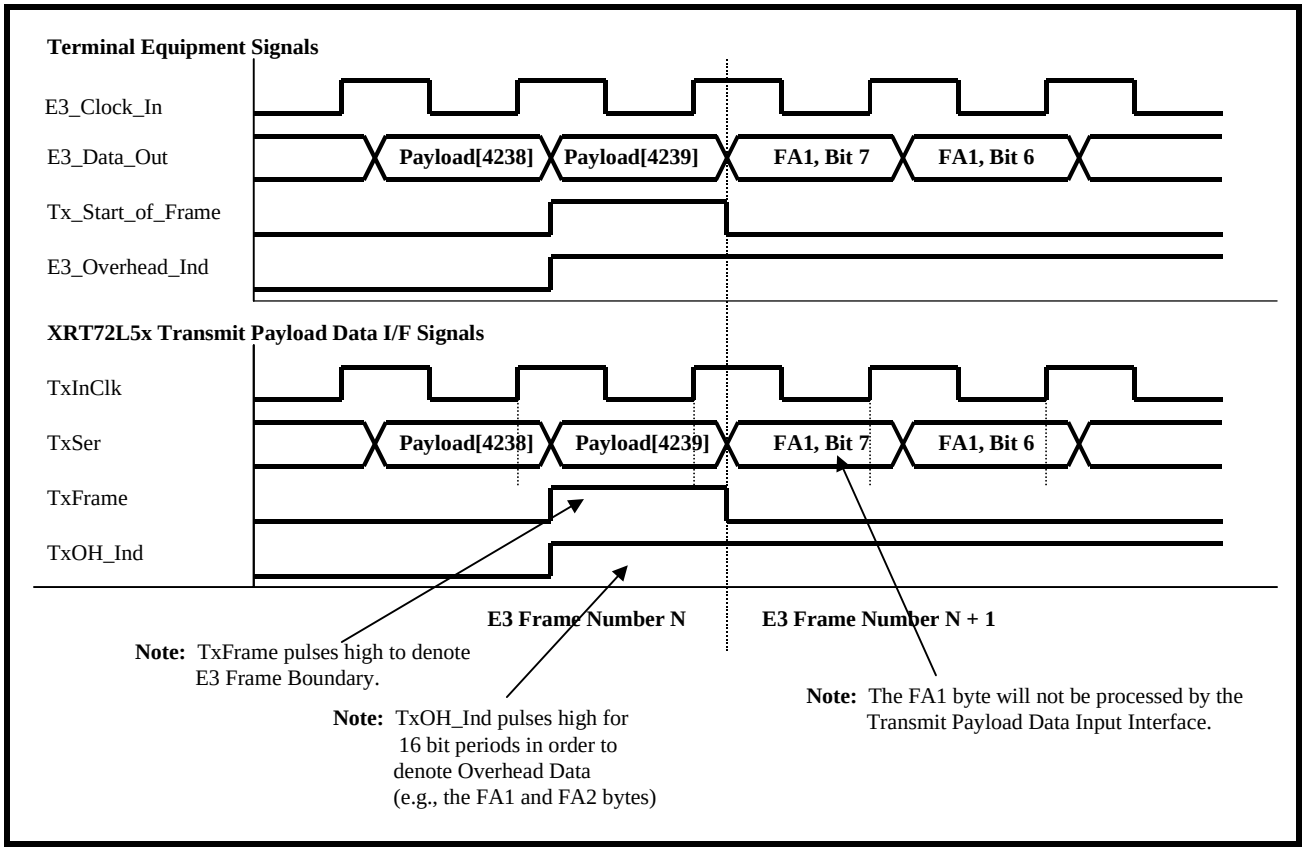
NOTE: *In this case, the XRT72L50 dictates exactly when the very next E3 frame will be generated. The Terminal Equipment is expected to respond appropriately by providing the XRT72L50 with the first bit of the new E3 frame, upon demand. Hence, in this mode, the XRT72L50 is referred to as the Frame Master and the Terminal Equipment is referred to as the Frame Slave.*

Finally, the XRT72L50 will pulse its TxOH_Ind output pin, one bit-period prior to it processing a given overhead bit, within the Outbound E3 frame. Since the TxOH_Ind output pin of the XRT72L50 is electrically connected to the E3_Overhead_Ind whenever the XRT72L50 pulses the TxOH_Ind output pin "High", it will also be driving the E3_Overhead_Ind input pin (of the Terminal Equipment) "High". Whenever the Terminal Equipment

detects this pin toggling "High", it should delay transmission of the very next E3 frame payload bit by one clock cycle.

The behavior of the signal between the XRT72L50 and the Terminal Equipment for E3 Mode 3 Operation is illustrated in Figure 150.

FIGURE 150. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (E3 MODE 3 OPERATION)



How to configure the XRT72L50 to operate in this mode.

1. Set the NibIntf input pin "Low".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "1X".

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	1	1	X

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 150.

6.2.1.4 *Mode 4 - The Nibble-Parallel/Loop-Timed Mode Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will behave as follows.

A. Looped Timing (Uses the RxLineClk as the Timing Reference)

In this mode, the Transmit Section of the XRT72L50 will use the RxLineClk signal as its timing reference. When the XRT72L50 is operating in the Nibble-Mode, it will internally divide the RxLineClk signal, by a factor of four (4) and will output this signal via the TxNibClk output pin.

B. Nibble-Parallel Mode

The XRT72L50 will accept the E3 payload data, from the Terminal Equipment in a nibble-parallel manner, via the TxNib[3:0] input pins. The Transmit Terminal Equipment Input Interface block will latch this data into its circuitry, on the rising edge of the TxNibClk output signal.

C. Delineation of the Outbound E3 frames

The XRT72L50 will pulse the TxNibFrame output pin "High" for one bit-period, coincident with the XRT72L50 processing the last nibble of a given E3 frame.

D. Sampling of payload data, from the Terminal Equipment

In Mode 4, the XRT72L50 will sample the data, at the TxNib[3:0] input pins, on the third rising edge of the RxOutClk clock signal, following a pulse in the TxNibClk signal (see Figure 152).

NOTE: *The TxNibClk signal, from the XRT72L50, operates nominally at 8.592 MHz (e.g., 34.368 MHz divided by 4).*

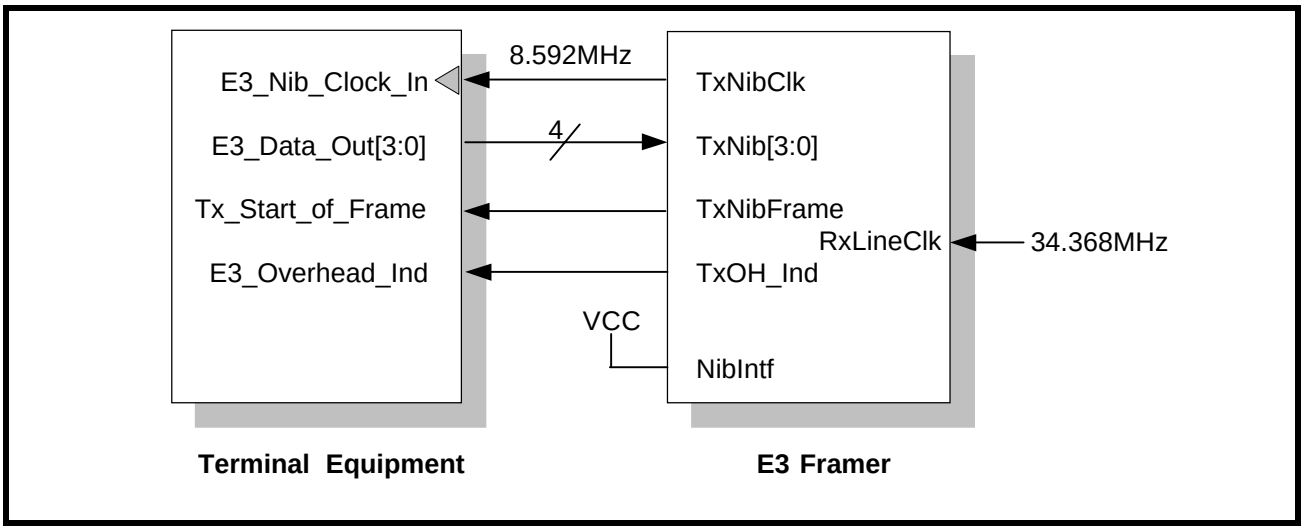
The E3 Frame consists of 537 bytes or 1074 nibbles. Therefore, the XRT72L50 will supply 1074 TxNibClk pulses between the rising edges of two consecutive TxNibFrame pulses. The E3 Frame repetition rate is 8.0kHz. Hence, 1074 TxNibClk pulses for each E3 frame period amounts to TxNibClk running at approximately 8.592 MHz.

Nominally, the Transmit Section within the XRT72L50 will generate a TxNibClk pulse for every 4 RxOutClk (or TxInClk) periods.

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 4 Operation

Figure 151 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 4 Operation.

FIGURE 151. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 4 (NIBBLE-PARALLEL/LOOP-TIMED) OPERATION



Mode 4 Operation of the Terminal Equipment

When the XRT72L50 is operating in this mode, it will function as the source of the 8.592MHz (e.g., the 34.368MHz clock signal divided by 4) clock signal that will be used as the Terminal Equipment Interface clock by both the XRT72L50 and the Terminal Equipment.

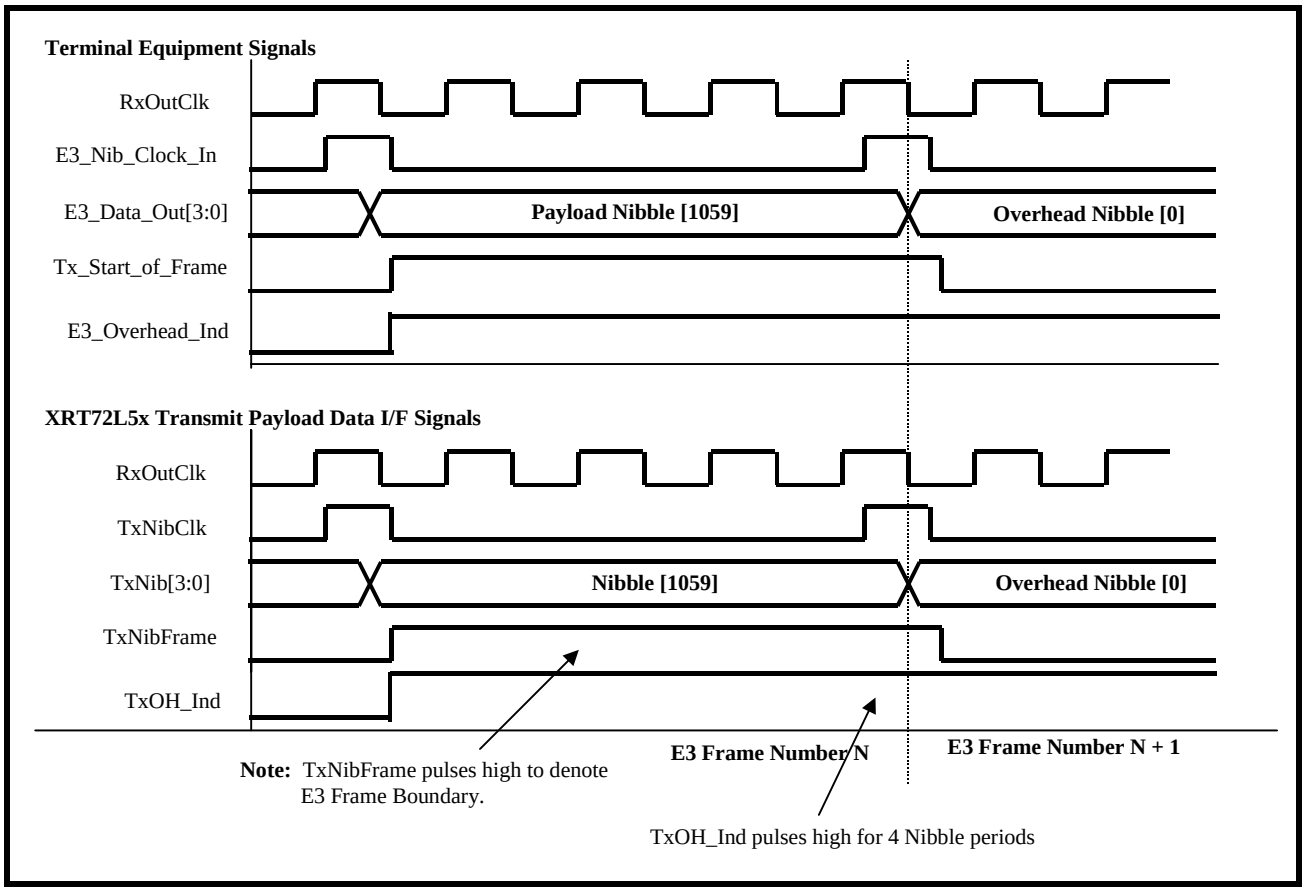
The Terminal Equipment will output the payload data of the Outbound E3 data stream via its E3_Data_Out[3:0] pins on the rising edge of the 8.592MHz clock signal at the E3_Nib_Clock_In input pin.

The XRT72L50 will latch the Outbound E3 data stream (from the Terminal Equipment) on the rising edge of the TxNibClk output clock signal. The XRT72L50 will indicate that it is processing the last nibble, within a given E3 frame, by pulsing its TxNibFrame output pin "High" for one TxNibClk clock period. When the Terminal Equipment detects a pulse at its Tx_Start_of_Frame input pin, it is expected to transmit the first nibble, of the very next Outbound E3 frame to the XRT72L50 via the E3_Data_Out[3:0] (or TxNib[3:0] pins).

Finally, for the Nibble-Parallel Mode operation, the XRT72L50 will pulse the TxOHInd output pin "High" for a total of 14 nibble periods (e.g., for the 7 overhead bytes, within each of the E3, ITU-T G.832 frames). At the beginning of an E3 frame, the XRT72L50 will pulse the TxOHInd output pin "High" for 4 nibble periods. These four nibbles represent the FA1 and FA2 bytes within each E3 frame. Throughout the remainder of the E3 framing period, the XRT72L50 will pulse the TxOHInd output pin 5 times. The width (or duration) of each of these pulses will be two nibbles. Clearly, each of these 5 pulses corresponds to the five remaining overhead bytes, within the E3, ITU-T G.832 framing structure.

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Mode 4 Operation is illustrated in Figure 152.

FIGURE 152. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (MODE 4 OPERATION)



How to configure the XRT72L50 into Mode 4

1. Set the NibIntf input pin "High".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "00" as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	1	0	0

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 151.

6.2.1.5 *Mode 5 - The Nibble-Parallel/Local-Time/Frame-Slave Interface Mode Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will function as follows:

A. Local Timing - Uses the TxInClk signal as the Timing Reference

In this mode, the Transmit Section of the XRT72L50 will use the TxInClk signal at its timing reference. Further, the chip will internally divide the TxInClk clock signal by a factor of 4 and will output this divided clock signal via the TxNibClk output pin. The Transmit Terminal Equipment Input Interface block (within the XRT72L50) will use the rising edge of the TxNibClk signal, to latch the data, residing on the TxNib[3:0] into its circuitry.

B. Nibble-Parallel Mode

The XRT72L50 will accept the E3 payload data, from the Terminal Equipment, in a parallel manner, via the TxNib[3:0] input pins. The Transmit Terminal Equipment Input Interface will latch this data into its circuitry, on the rising edge of the TxNibClk output signal.

C. Delineation of Outbound E3 Frames

The Transmit Section will use the TxInClk input signal as its timing reference and will use the TxFrameRef input signal as its Framing Reference (e.g., the Transmit Section of the XRT72L50 initiates frame generation upon the rising edge of the TxFrameRef signal).

D. Sampling of payload data, from the Terminal Equipment

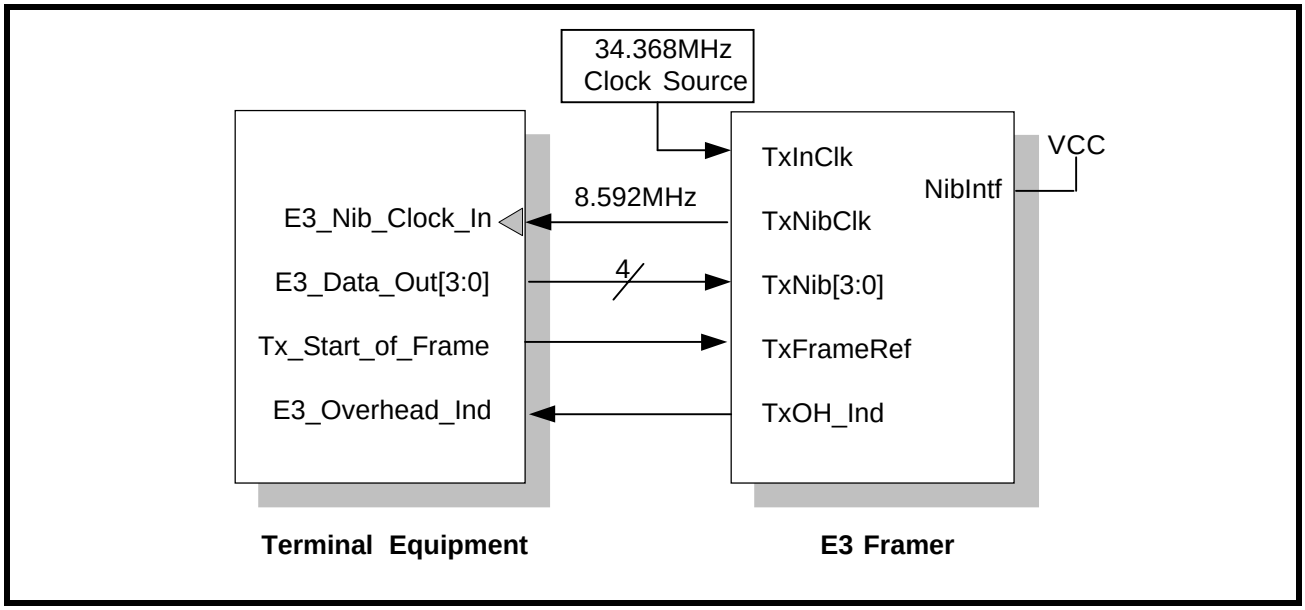
In Mode 5, the XRT72L50 will sample the data, at the TxNib[3:0] input pins, on the third rising edge of the TxInClk clock signal, following a pulse in the TxNibClk signal (see Figure 154).

NOTE: *The TxNibClk signal, from the XRT72L50 operates nominally at 8.592 MHz (e.g., 34.368 MHz divided by 4).*

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 5 Operation

Figure 153 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 5 Operation.

FIGURE 153. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 5 (NIBBLE-PARALLEL/LOCAL-TIMED/FRAME-SLAVE) OPERATION



Mode 5 Operation of the Terminal Equipment

In Figure 153 both the Terminal Equipment and the XRT72L50 will be driven by an external 8.592MHz clock signal. The Terminal Equipment will receive the 8.592MHz clock signal via the E3_Nib_Clock_In input pin. The XRT72L50 will output the 8.592MHz clock signal via the TxNibClk output pin.

The Terminal Equipment will serially output the data on the E3_Data_Out[3:0] pins, upon the rising edge of the signal at the E3_Clock_In input pin.

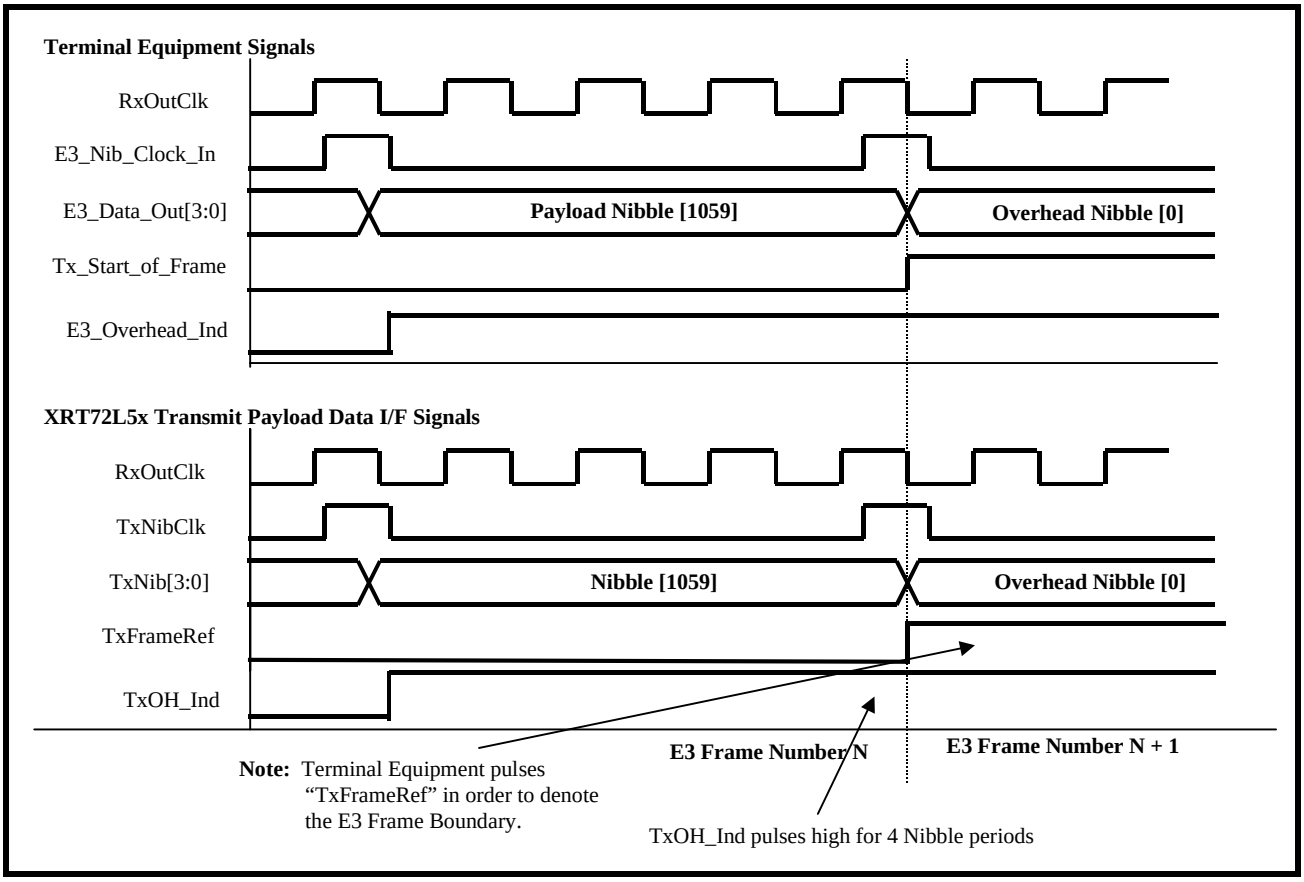
NOTE: *The E3_Data_Out[3:0] output pins of the Terminal Equipment is electrically connected to the TxNib[3:0] input pins.* The XRT72L50 will latch the data, residing on the TxNib[3:0] input pins, on the rising edge of the TxNibClk signal.

In this case, the Terminal Equipment has the responsibility of providing the framing reference signal by pulsing the Tx_Start_of_Frame output pin (and in turn, the TxFrameRef input pin of the XRT72L50) "High" for one bit-period, coincident with the first bit of a new E3 frame. Once the XRT72L50 detects the rising edge of the input at its TxFrameRef input pin, it will begin generation of a new E3 frame.

Finally, the XRT72L50 will always internally generate the Overhead bits, when it is operating in both the E3 and Nibble-parallel modes. The XRT72L50 will pull the TxOHInd input pin "Low".

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Mode 5 Operation is illustrated in Figure 154.

FIGURE 154. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (E3 MODE 5 OPERATION)



How to configure the XRT72L50 into Mode 5

1. Set the NibIntf input pin "High".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "01" as illustrated below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	1	0	1

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 153.

6.2.1.6 *Mode 6 - The Nibble-Parallel/Local-Timed/Frame-Master Interface Mode Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will function as follows:

A. Local Timing - Uses the TxInClk signal as the Timing Reference

In this mode, the Transmit Section of the XRT72L50 will use the TxInClk signal at its timing reference. Further, the chip will internally divide the TxInClk clock signal by a factor of 4 and will output this divided clock signal via

the TxNibClk output pin. The Transmit Terminal Equipment Input Interface block (within the XRT72L50) will use the rising edge of the TxNibClk signal, to latch the data, residing on the TxNib[3:0] into its circuitry.

B. Nibble-Parallel Mode

The XRT72L50 will accept the E3 payload data, from the Terminal Equipment, in a parallel manner, via the TxNib[3:0] input pins. The Transmit Terminal Equipment Input Interface will latch this data into its circuitry, on the rising edge of the TxNibClk output signal.

C. Delineation of Outbound E3 Frames

The Transmit Section will use the TxInClk input signal as its timing reference and will initiate the generation of E3 frames, asynchronous with respect to any external signal. The XRT72L50 will pulse the TxFrame output pin "High" whenever it is processing the last bit, within a given Outbound E3 frame.

D. Sampling of payload data, from the Terminal Equipment

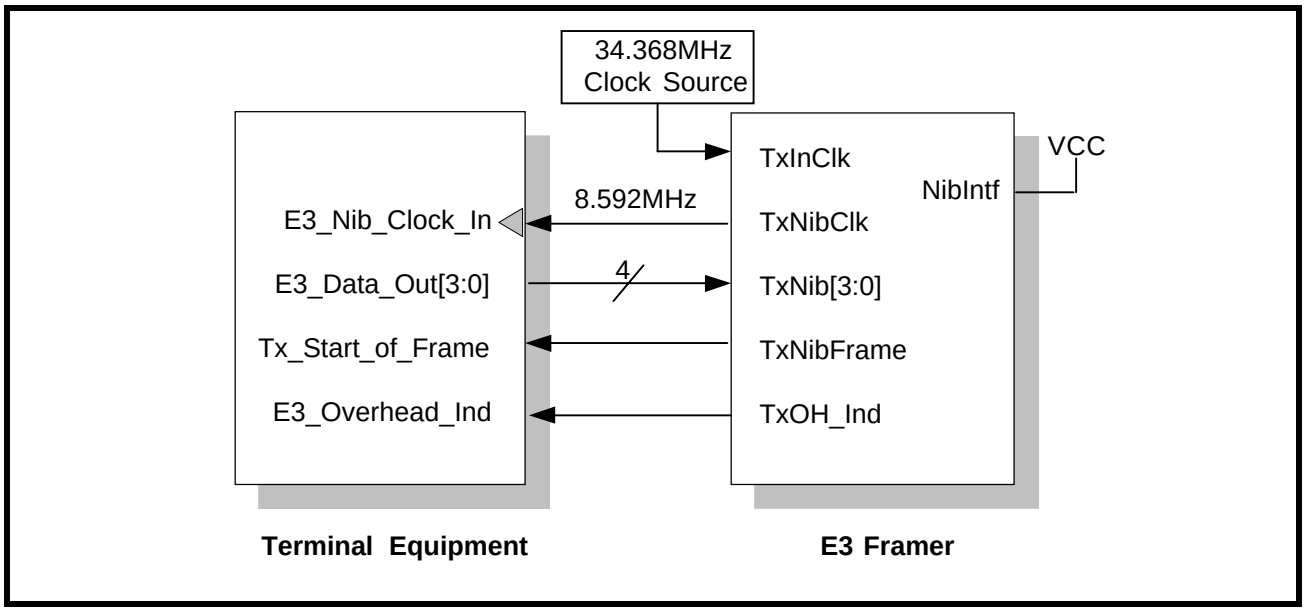
In Mode 6, the XRT72L50 will sample the data, at the TxNib[3:0] input pins, on the third rising edge of the TxInClk clock signal, following a pulse in the TxNibClk signal (see Figure 156).

NOTE: *The TxNibClk signal, from the XRT72L50 operates nominally at 8.592 MHz (e.g., 34.368 MHz divided by 4).*

Interfacing the Transmit Payload Data Input Interface block of the XRT72L50 to the Terminal Equipment for Mode 6 Operation

Figure 155 presents an illustration of the Transmit Payload Data Input Interface block (within the XRT72L50) being interfaced to the Terminal Equipment, for Mode 6 Operation.

FIGURE 155. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK FOR MODE 6 (NIBBLE-PARALLEL/LOCAL-TIMED/FRAME-MASTER) OPERATION



Mode 6 Operation of the Terminal Equipment

In Figure 155 both the Terminal Equipment and the XRT72L50 will be driven by an external 8.592MHz clock signal. The Teriminal Equipment will receive the 8.592MHz clock signal via the E3_Nib_Clock_In input pin. The XRT72L50 will output the 8.592MHz clock signal via the TxNibClk output pin.

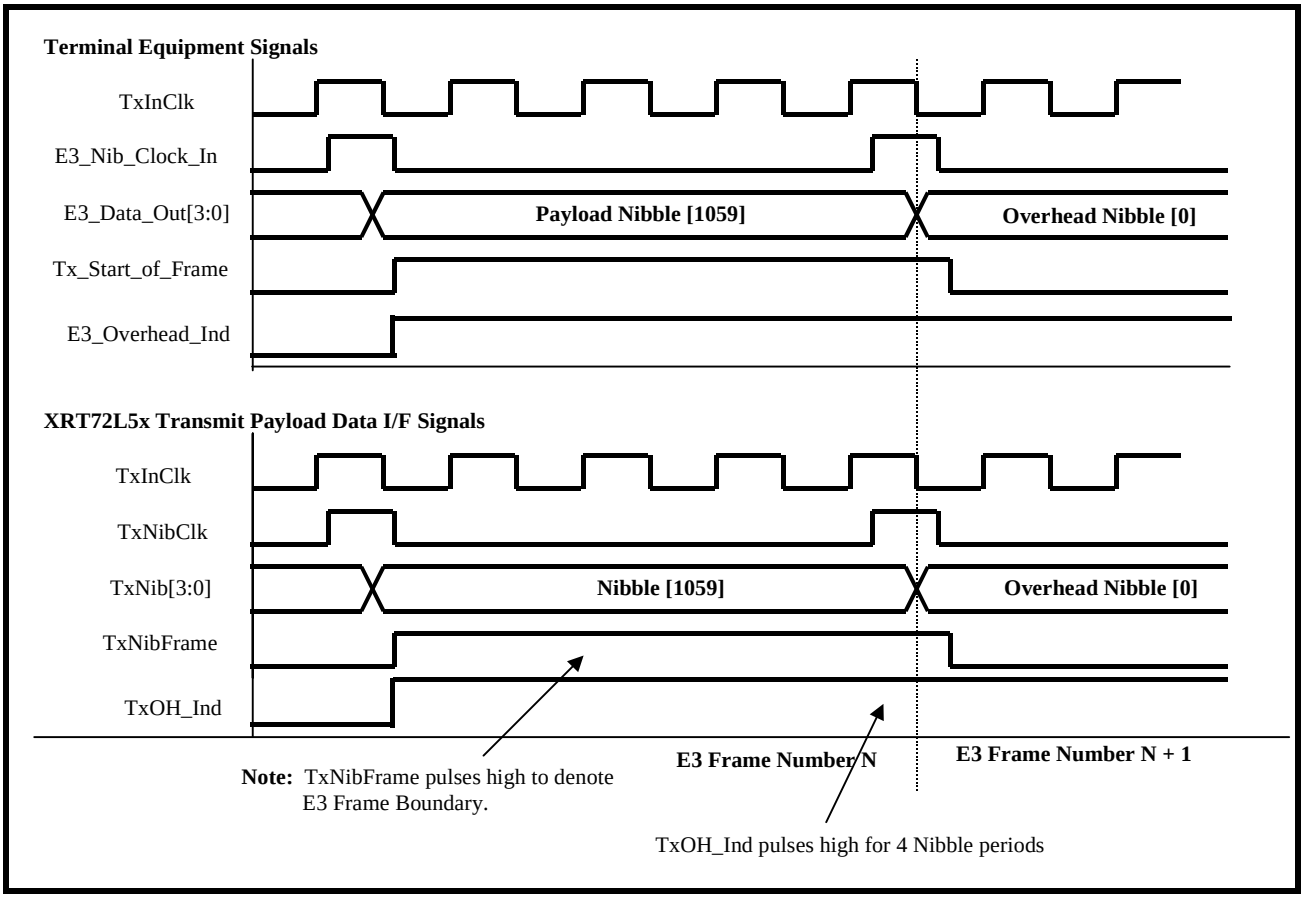
The Terminal Equipment will serially output the data on the E3_Data_Out[3:0] pins upon the rising edge of the signal at the E3_Clock_In input pin. The XRT72L50 will latch the data, residing on the TxNib[3:0] input pins, on the rising edge of the TxNibClk signal.

In this case the XRT72L50 has the responsibility of providing the framing reference signal by pulsing the TxFrame output pin (and in turn the Tx_Start_of_Frame input pin of the Terminal Equipment) "High" for one bit-period, coincident with the last bit within a given E3 frame.

Finally, the XRT72L50 will always internally generate the Overhead bits, when it is operating in both the E3 and Nibble-parallel modes. The XRT72L50 will pull the TxOHInd input pin "Low".

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Mode 6 Operation is illustrated in Figure 156.

FIGURE 156. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (E3 MODE 6 OPERATION)



How to configure the XRT72L50 into Mode 6

1. Set the NibIntfinput pin "High".
2. Set the TimRefSel[1:0] bit-fields (within the Framer Operating Mode Register) to "1X" as illustrated below.

Framer Operating Mode Register (Address = 0x00)

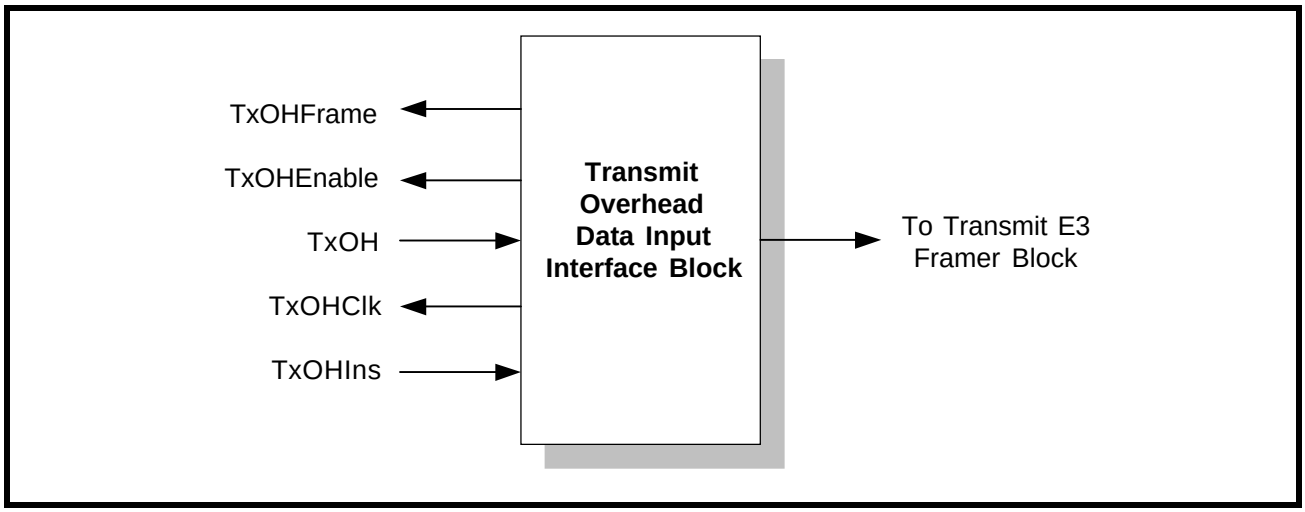
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	1	1	x

3. Interface the XRT72L50, to the Terminal Equipment, as illustrated in Figure 155.

6.2.2 The Transmit Overhead Data Input Interface

Figure 157 presents a simple illustration of the Transmit Overhead Data Input Interface block within the XRT72L50.

FIGURE 157. THE TRANSMIT OVERHEAD DATA INPUT INTERFACE BLOCK



The E3, ITU-T G.832 Frame consists of 537 bytes. Of these bytes, 530 bytes are payload bytes and the remaining 7 are overhead bytes. The XRT72L50 has been designed to handle and process both the payload type and overhead type bits for each E3 frame. Within the Transmit Section within the XRT72L50, the Transmit Payload Data Input Interface has been designed to handle the payload data. Likewise, the Transmit Overhead Input Interface has been designed to handle and process the overhead bits.

The Transmit Section of the XRT72L50 generates or processes the various overhead bits within the E3 frame, in the following manner.

The Frame Alignment Overhead Bytes (e.g., the FA1 and FA2 bytes)

The "FA1" and "FA2" bytes are always internally generated by the Transmit Section of the XRT72L50. Hence, the user cannot insert his/her value for the "FA1" and "FA2" bytes into the Outbound E3 data stream, via the Transmit Overhead Data Input Interface.

The Error Monitoring (EM) Overhead Byte

The EM byte is always internally generated by the Transmit Section of the XRT72L50. Hence, the user cannot insert his/her value for the EM byte into the Outbound E3 data stream, via the Transmit Overhead Data Input Interface.

The Alarm and signaling related Overhead bytes

Bytes that are used to transport the alarm conditions can be either internally generated by the Transmit Section within the XRT72L50, or can be externally generated and inserted into the Outbound E3 data stream, via the Transmit Overhead Data Input Interface. The E3 frame overhead bits that fall into this category are:

- The "MA" byte
- The "TR" byte

The Data Link Related Overhead Bits

The E3 frame structure also contains bits which can be used to transport User Data Link information and Path Maintenance Data Link information. The UDL (User Data Link) bits are only accessible via the Transmit Overhead Data Input Interface. The Path Maintenance Data Link (PMDL) bits can either be sourced from the Transmit LAPD Controller/Buffer or via the Transmit Overhead Data Input Interface.

Table 68 lists the Overhead Bits within the E3 frame. Additionally, this table also indicates whether or not these overhead bits can be sourced by the Transmit Overhead Data Input Interface or not.

TABLE 68: A LISTING OF THE OVERHEAD BITS WITHIN THE E3 FRAME, AND THEIR POTENTIAL SOURCES, WITHIN THE XRT72L50 IC

OVERHEAD BIT	INTERNALLY GENERATED	ACCESSIBLE VIA THE TRANSMIT OVERHEAD DATA INPUT INTERFACE	BUFFER/REGISTER ACCESSIBLE
FA1 - Bit 7	Yes	No	Yes
FA1 - Bit 6	Yes	No	Yes
FA1 - Bit 5	Yes	No	Yes
FA1 - Bit 4	Yes	No	Yes
FA1 - Bit 3	Yes	No	Yes
FA1 - Bit 2	Yes	No	Yes
FA1 - Bit 1	Yes	No	Yes
FA1 - Bit 0	Yes	No	Yes
FA2 - Bit 7	Yes	No	Yes
FA2 - Bit 6	Yes	No	Yes
FA2 - Bit 5	Yes	No	Yes
FA2 - Bit 4	Yes	No	Yes
FA2 - Bit 3	Yes	No	Yes
FA2 - Bit 2	Yes	No	Yes
FA2 - Bit 1	Yes	No	Yes
FA2 - Bit 0	Yes	No	Yes
EM - Bit 7	Yes	No	Yes
EM - Bit 6	Yes	No	Yes
EM - Bit 5	Yes	No	Yes
EM - Bit 4	Yes	No	Yes
EM - Bit 3	Yes	No	Yes
EM - Bit 2	Yes	No	Yes
EM - Bit 1	Yes	No	Yes
EM - Bit 0	Yes	No	Yes
TR - Bit 7	No	Yes	Yes
TR - Bit 6	No	Yes	Yes
TR - Bit 5	No	Yes	Yes
TR - Bit 4	No	Yes	Yes
TR - Bit 3	No	Yes	Yes
TR - Bit 2	No	Yes	Yes
TR - Bit 1	No	Yes	Yes

TABLE 68: A LISTING OF THE OVERHEAD BITS WITHIN THE E3 FRAME, AND THEIR POTENTIAL SOURCES, WITHIN THE XRT72L50 IC

OVERHEAD BIT	INTERNALLY GENERATED	ACCESSIBLE VIA THE TRANSMIT OVERHEAD DATA INPUT INTERFACE	BUFFER/REGISTER ACCESSIBLE
TR - Bit 0	No	Yes	Yes
MA - Bit 7	Yes	Yes	Yes
MA - Bit 6	Yes	Yes	Yes
MA - Bit 5	Yes	Yes	Yes
MA - Bit 4	Yes	Yes	Yes
MA - Bit 3	Yes	Yes	Yes
MA - Bit 2	Yes	Yes	Yes
MA - Bit 1	Yes	Yes	Yes
MA - Bit 0	Yes	Yes	Yes
NR - Bit 7	No	Yes	Yes
NR - Bit 6	No	Yes	Yes
NR - Bit 5	No	Yes	Yes
NR - Bit 4	No	Yes	Yes
NR - Bit 3	No	Yes	Yes
NR - Bit 2	No	Yes	Yes
NR - Bit 1	No	Yes	Yes
NR - Bit 0	No	Yes	Yes
GC - Bit 7	No	Yes	Yes
GC - Bit 6	No	Yes	Yes
GC - Bit 5	No	Yes	Yes
GC - Bit 4	No	Yes	Yes
GC - Bit 3	No	Yes	Yes
GC - Bit 2	No	Yes	Yes
GC - Bit 1	No	Yes	Yes
GC - Bit 0	No	Yes	Yes

NOTES:

1. *The XRT72L50 contains mask register bits that permit the user to alter the state of the internally generated value for these bits.*
2. *The Transmit LAPD Controller/Buffer can be configured to be the source of the NR or GC bytes, within the Outbound E3 data stream.*

In all, the Transmit Overhead Data Input Interface permits the user to insert overhead data into the Outbound E3 frames via the following two different methods.

- Method 1 - Using the TxOHClk clock signal
- Method 2 - Using the TxInClk and the TxOHEnable signals.

6.2.2.1 *Method 1 - Using the TxOHClk Clock Signal*

The Transmit Overhead Data Input Interface consists of the five signals. Of these five (5) signals, the following four (4) signals are to be used when implementing Method 1.

- TxOH
- TxOHClk
- TxOHFrame
- TxOHIns

Each of these signals are listed and described in Table 69.

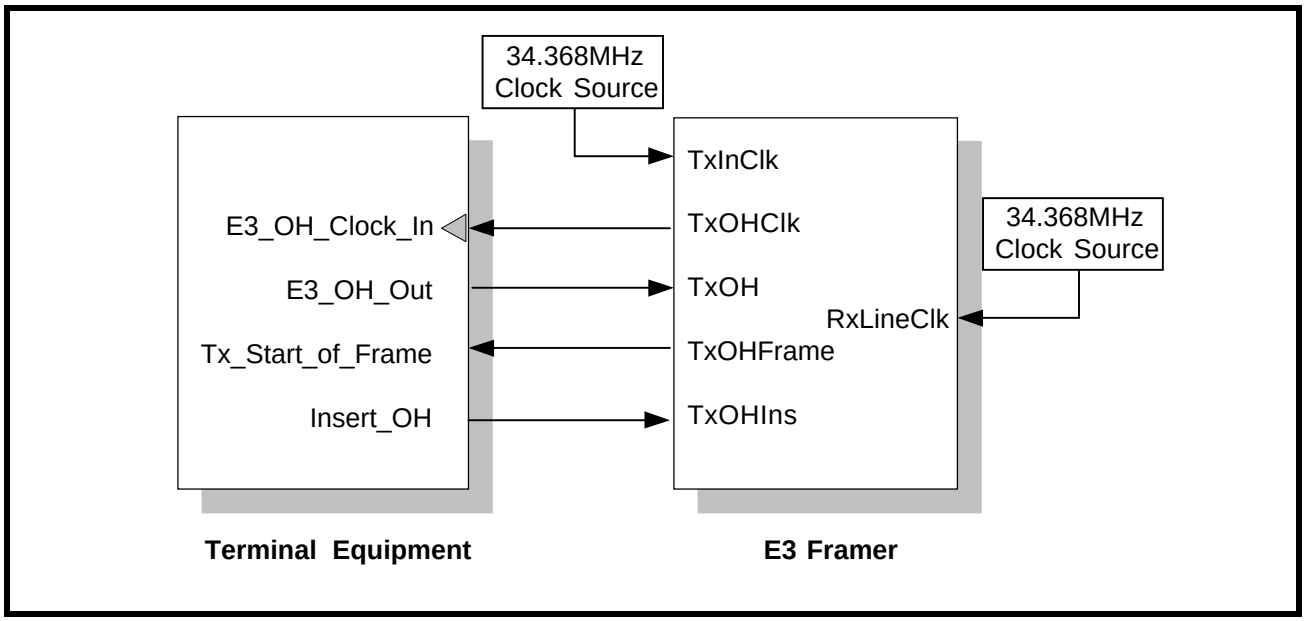
TABLE 69: DESCRIPTION OF METHOD 1 TRANSMIT OVERHEAD INPUT INTERFACE SIGNALS

NAME	TYPE	DESCRIPTION
TxOHIns	Input	**Transmit Overhead Data Insert Enable input pin.** Asserting this input signal (e.g., setting it "High") enables the Transmit Overhead Data Input Interface to accept overhead data from the Terminal Equipment. In other words, while this input pin is "High", the Transmit Overhead Data Input Interface will sample the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. Conversely, setting this pin "Low" configures the Transmit Overhead Data Input Interface to NOT sample (e.g., ignore) the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. ***NOTE:*** *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the Transmit Overhead Data Input Interface (e.g., if the Terminal Equipment asserts the TxOHIns signal, at a time when one of these non-insertable overhead bits are being processed), that particular insertion effort will be ignored.*
TxOH	Input	**Transmit Overhead Data Input pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the overhead bit position within the very next Outbound E3 frame. If the TxOHIns pin is pulled "High", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the TxOHClk output pin. Conversely, if the TxOHIns pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.
TxOHClk	Output	**Transmit Overhead Input Interface Clock Output signal:** This output signal serves two purposes: 1. The Transmit Overhead Data Input Interface will provide a rising clock edge on this signal, one bit-period prior to the instant that the Transmit Overhead Data Input Interface is processing an overhead bit. 2. The Transmit Overhead Data Input Interface will sample the data at the TxOH input, on the falling edge of this clock signal (provided that the TxOHIns input pin is "High"). ***NOTE:*** *The Transmit Overhead Data Input Interface will supply a clock edge for all overhead bits within the E3 frame (via the TxOHClk output signal). This includes those overhead bits that the Transmit Overhead Data Input Interface will not accept from the Terminal Equipment.*
TxOHFrame	Output	**Transmit Overhead Input Interface Frame Boundary Indicator Output:** This output signal pulses "High" when the XRT72L50 is processing the last bit within a given E3 frame. The purpose of this output signal is to alert the Terminal Equipment that the Transmit Overhead Data Input Interface block is about to begin processing the overhead bits for a new E3 frame.

Interfacing the Transmit Overhead Data Input Interface to the Terminal Equipment.

Figure 158 illustrates how one should interface the Transmit Overhead Data Input Interface to the Terminal Equipment, when using Method 1.

FIGURE 158. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 1)



Method 1 Operation of the Terminal Equipment

If the Terminal Equipment intends to insert any overhead data into the Outbound E3 data stream, (via the Transmit Overhead Data Input Interface), then it is expected to do the following.

1. To sample the state of the TxOHFrame signal (e.g., the Tx_Start_of_Frame input signal) on the rising edge of the TxOHClk (e.g., the E3_OH_Clock_In signal).
2. To keep track of the number of rising clock edges that have occurred, via the TxOHClk (e.g., the E3_OH_Clock_In signal) since the last time the TxOHFrame signal was sampled "High". By doing this the Terminal Equipment will be able to keep track of which overhead bit is being processed by the Transmit Overhead Data Input Interface block at any given time. When the Terminal Equipment knows which overhead bit is being processed, at a given TxOHClk period, it will know when to insert a desired overhead bit value into the Outbound E3 data stream. From this, the Terminal Equipment will know when it should assert the TxOHIns input pin and place the appropriate value on the TxOH input pin (of the XRT72L50).

Table 70 relates the number of rising clock edges (in the TxOHClk signal, since TxOHFrame was sampled "High") to the E3 Overhead Bit, that is being processed.

TABLE 70: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN TXOHCLK, (SINCE "TXOHFRAME" WAS LAST SAMPLED "HIGH") TO THE E3 OVERHEAD BIT, THAT IS BEING PROCESSED

NUMBER OF RISING CLOCK EDGES IN TXOHCLK	THE OVERHEAD BIT EXPECTED BY THE "XRT72L50"	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
0 (Clock edge is coincident with TxOHFrame being detected "High")	FA1 Byte - Bit 7	No
1	FA1 Byte - Bit 6	No
2	FA1 Byte - Bit 5	No
3	FA1 Byte - Bit 4	No
4	FA1 Byte - Bit 3	No
5	FA1 Byte - Bit 2	No
6	FA1 Byte - Bit 1	No
7	FA1 Byte - Bit 0	No
8	FA2 Byte - Bit 7	No
9	FA2 Byte - Bit 6	No
10	FA2 Byte - Bit 5	No
11	FA2 Byte - Bit 4	No
12	FA2 Byte - Bit 3	No
13	FA2 Byte - Bit 2	No
14	FA2 Byte - Bit 1	No
15	FA2 Byte - Bit 0	No
16	EM Byte - Bit 7	No
17	EM Byte - Bit 6	No
18	EM Byte - Bit 5	No
19	EM Byte - Bit 4	No
20	EM Byte - Bit 3	No
21	EM Byte - Bit 2	No
22	EM Byte - Bit 1	No
23	EM Byte - Bit 0	No
24	TR Byte - Bit 7	Yes
25	TR Byte - Bit 6	Yes
26	TR Byte - Bit 5	Yes
27	TR Byte - Bit 4	Yes
28	TR Byte - Bit 3	Yes
29	TR Byte - Bit 2	Yes

TABLE 70: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN TXOHCLK, (SINCE "TXOHFRAME" WAS LAST SAMPLED "HIGH") TO THE E3 OVERHEAD BIT, THAT IS BEING PROCESSED

NUMBER OF RISING CLOCK EDGES IN TXOHCLK	THE OVERHEAD BIT EXPECTED BY THE "XRT72L50"	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
30	TR Byte - Bit 1	Yes
31	TR Byte - Bit 0	Yes
32	MA Byte - Bit 7	Yes (FERF Bit)
33	MA Byte - Bit 6	Yes (FEBE Bit)
34	MA Byte - Bit 5	Yes
35	MA Byte - Bit 4	Yes
36	MA Byte - Bit 3	Yes
37	MA Byte - Bit 2	Yes
38	MA Byte - Bit 1	Yes
39	MA Byte - Bit 0	Yes
40	NR Byte - Bit 7	Yes
41	NR Byte - Bit 6	Yes
42	NR Byte - Bit 5	Yes
43	NR Byte - Bit 4	Yes
44	NR Byte - Bit 3	Yes
45	NR Byte - Bit 2	Yes
46	NR Byte - Bit 1	Yes
47	NR Byte - Bit 0	Yes
48	GC Byte - Bit 7	Yes
49	GC Byte - Bit 6	Yes
50	GC Byte - Bit 5	Yes
51	GC Byte - Bit 4	Yes
52	GC Byte - Bit 3	Yes
53	GC Byte - Bit 2	Yes
54	GC Byte - Bit 1	Yes
55	GC Byte - Bit 0	Yes

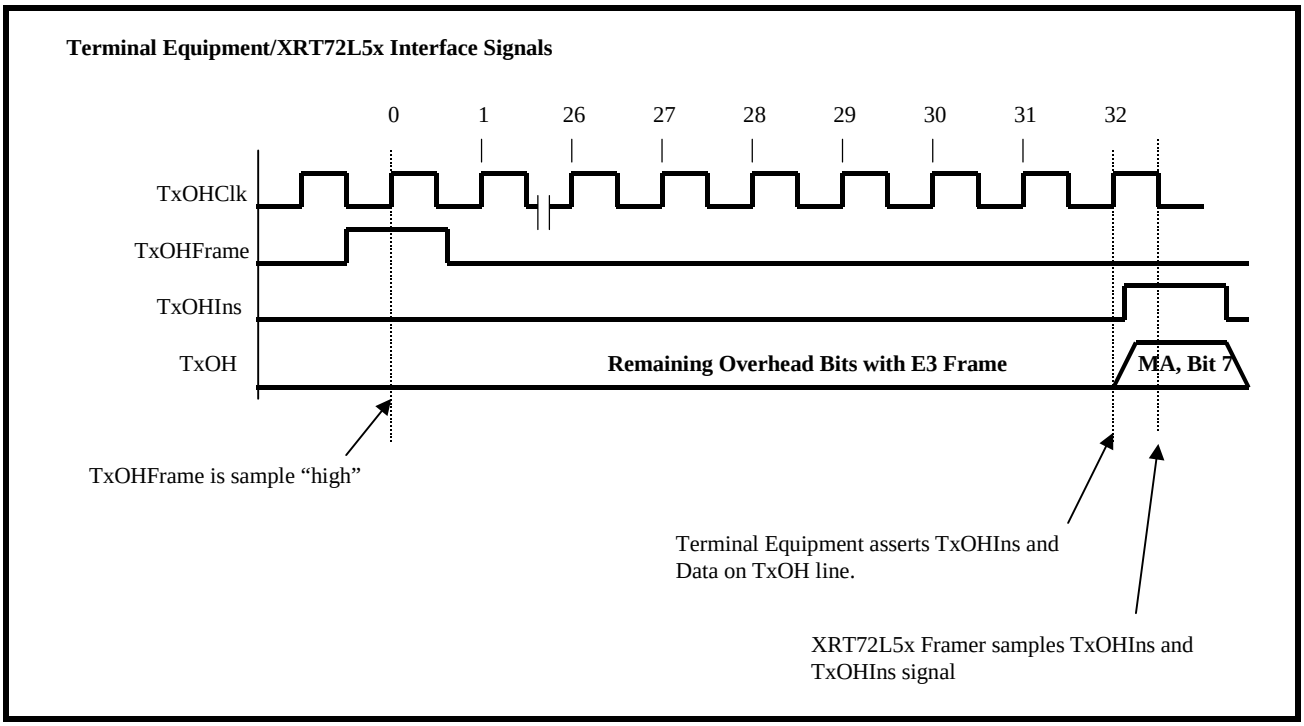
3. After the Terminal Equipment has waited the appropriate number of clock edges (from the TxOHFrame signal being sampled "High"), it should assert the TxOHIns input signal. Concurrently, the Terminal Equipment should also place the appropriate value (of the inserted overhead bit) onto the TxOH signal.
4. The Terminal Equipment should hold both the TxOHIns input pin "High" and the value of the TxOH signal, stable until the next rising edge of TxOHClk is detected.

Case Study: The Terminal Equipment intends to insert the appropriate overhead bits into the Transmit Overhead Data Input Interface (using Method 1) in order to transmit a Yellow Alarm to the remote terminal equipment.

In this example, the Terminal Equipment intends to insert the appropriate overhead bits, into the Transmit Overhead Data Input Interface, such that the XRT72L50 will transmit a Yellow Alarm to the remote terminal equipment. Recall that, for E3 Applications, a Yellow Alarm is transmitted by setting the FERF bit (within the MA Byte) to "0".

If one assumes that the connection between the Terminal Equipment and the XRT72L50 are as illustrated in Figure 158 then Figure 159 presents an illustration of the signaling that must go on between the Terminal Equipment and the XRT72L50.

FIGURE 159. ILLUSTRATION OF THE SIGNAL THAT MUST OCCUR BETWEEN THE TERMINAL EQUIPMENT AND THE XRT72L50, IN ORDER TO CONFIGURE THE XRT72L50 TO TRANSMIT A YELLOW ALARM TO THE REMOTE TERMINAL EQUIPMENT



In Figure 159 the Terminal Equipment samples the TxOHFrame signal being "High" at rising clock edge # “0". From this point, the Terminal Equipment waits until it has detected 32 rising edges in the TxOHClk signal. At this point, the Terminal Equipment knows that the XRT72L50 is just about to process the FERF bit within the MA byte (in a given Outbound E3 frame). Additionally, according to Table 70, the 32nd overhead bit to be processed is the FERF bit. In order to facilitate the transmission of the Yellow Alarm, the Terminal Equipment must set this FERF bit to "1". Hence, the Terminal Equipment starts this process by implementing the following steps concurrently.

a. Assert the TxOHIns input pin by setting it "High".

b. Set the TxOH input pin to "0".

After the Terminal Equipment has applied these signals, the XRT72L50 will sample the data on both the TxOHIns and TxOH signals upon the very next falling edge of TxOHClk (designated at 32- in Figure 159). Once the XRT72L50 has sampled this data, it will then insert a "1" into the FERF bit position, in the Outbound E3 frame.

Upon detection of the very next rising edge of the TxOHClk clock signal (designated as clock edge 1 in Figure 159), the Terminal Equipment will negate the TxOHIns signal (e.g., toggles it "Low") and will cease inserting data into the Transmit Overhead Data Input Interface.

6.2.2.2 *Method 2 - Using the TxInClk and TxOHEnable Signals*

Method 1 requires the use of an additional clock signal, TxOHClk. However, there may be a situation in which the user does not wish to add this extra clock signal to their design, in order to use the Transmit Overhead Data Input Interface. Hence, Method 2 is available. When using Method 2, either the TxInClk or RxOutClk signal is used to sample the overhead bits and signals which are input to the Transmit Overhead Data Input Interface. Method 2 involves the use of the following signals:

- TxOH
- TxInClk
- TxOHFrame
- TxOHEnable

Each of these signals are listed and described in Table 71.

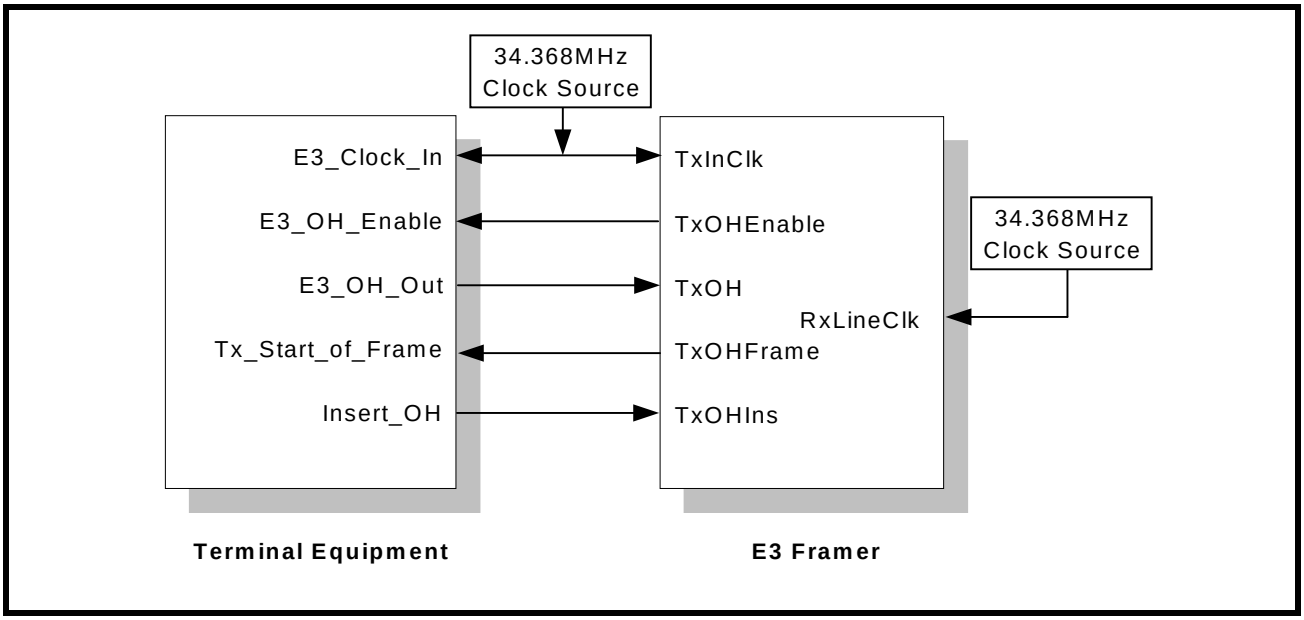
TABLE 71: DESCRIPTION OF METHOD 1 TRANSMIT OVERHEAD INPUT INTERFACE SIGNALS

NAME	TYPE	DESCRIPTION
TxOHEnable	Output	**Transmit Overhead Data Enable Output pin** The XRT72L50 will assert this signal, for one TxInClk period, just prior to the instant that the Transmit Overhead Data Input Interface is processing an overhead bit.
TxOHFrame	Output	**Transmit Overhead Input Interface Frame Boundary Indicator Output:** This output signal pulses "High" when the XRT72L50 is processing the last bit within a given E3 frame.
TxOHIns	Input	**Transmit Overhead Data Insert Enable input pin.** Asserting this input signal (e.g., setting it "High") enables the Transmit Overhead Data Input Interface to accept overhead data from the Terminal Equipment. In other words, while this input pin is "High", the Transmit Overhead Data Input Interface will sample the data at the TxOH input pin, on the falling edge of the TxInClk output signal. Conversely, setting this pin "Low" configures the Transmit Overhead Data Input Interface to NOT sample (e.g., ignore) the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. ***NOTE:*** *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the Transmit Overhead Data Input Interface (e.g., if the Terminal Equipment asserts the TxOHIns signal, at a time when one of these non-insertable overhead bits are being processed), that particular insertion effort will be ignored.*
TxOH	Input	**Transmit Overhead Data Input pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the overhead bit position within the very next Outbound E3 frame. If the TxOHIns pin is pulled "High", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the TxOHClk output pin. Conversely, if the TxOHIns pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.

Interfacing the Transmit Overhead Data Input Interface to the Terminal Equipment

Figure 160 illustrates how one should interface the Transmit Overhead Data Input Interface to the Terminal Equipment when using Method 2.

FIGURE 160. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 2)



Method 2 Operation of the Terminal Equipment

If the Terminal Equipment intends to insert any overhead data into the Outbound E3 data stream (via the Transmit Overhead Data Input Interface), then it is expected to do the following.

1. To sample the state of both the TxOHFrame and the TxOHEnable input signals, via the E3_Clock_In (e.g., either the TxInClk or the RxOutClk signal of the XRT72L50) signal. If the Terminal Equipment samples the TxOHEnable signal "High", then it knows that the XRT72L50 is about to process an overhead bit. Further, if the Terminal Equipment samples both the TxOHFrame and the TxOHEnable pins "High" (at the same time) then the Terminal Equipment knows that the XRT72L50 is about to process the first overhead bit, within a new E3 frame.
2. To keep track of the number of times that the TxOHEnable signal has been sampled "High" since the last time both the TxOHFrame and the TxOHEnable signals were sampled "High". By doing this, the Terminal Equipment will be able to keep track of which overhead bit the Transmit Overhead Data Input Interface is about ready to process. From this, the Terminal Equipment will know when it should assert the TxOHIns input pin and place the appropriate value on the TxOH input pins of the XRT72L50.

Table 72 also relates the number of TxOHEnable output pulses (that have occurred since both the TxOHFrame and TxOHEnable pins were sampled "High") to the E3 overhead bit, that is being processed.

TABLE 72: THE RELATIONSHIP BETWEEN THE NUMBER OF TXOHENABLE PULSES (SINCE THE LAST OCCURRENCE OF THE TXOHFRAME PULSE) TO THE E3 OVERHEAD BIT, THAT IS BEING PROCESSED BY THE XRT72L50

NUMBER OF TXOHENABLE PULSES	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
0 (Clock edge is coincident with TxOHFrame being detected "High")	FA1 Byte - Bit 7	No
1	FA1 Byte - Bit 6	No
2	FA1 Byte - Bit 5	No
3	FA1 Byte - Bit 4	No
4	FA1 Byte - Bit 3	No

TABLE 72: THE RELATIONSHIP BETWEEN THE NUMBER OF TXOHENABLE PULSES (SINCE THE LAST OCCURRENCE OF THE TXOHFRAME PULSE) TO THE E3 OVERHEAD BIT, THAT IS BEING PROCESSED BY THE XRT72L50

NUMBER OF TXOHENABLE PULSES	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
5	FA1 Byte - Bit 2	No
6	FA1 Byte - Bit 1	No
7	FA1 Byte - Bit 0	No
8	FA2 Byte - Bit 7	No
9	FA2 Byte - Bit 6	No
10	FA2 Byte - Bit 5	No
11	FA2 Byte - Bit 4	No
12	FA2 Byte - Bit 3	No
13	FA2 Byte - Bit 2	No
14	FA2 Byte - Bit 1	No
15	FA2 Byte - Bit 0	No
16	EM Byte - Bit 7	No
17	EM Byte - Bit 6	No
18	EM Byte - Bit 5	No
19	EM Byte - Bit 4	No
20	EM Byte - Bit 3	No
21	EM Byte - Bit 2	No
22	EM Byte - Bit 1	No
23	EM Byte - Bit 0	No
24	TR Byte - Bit 7	Yes
25	TR Byte - Bit 6	Yes
26	TR Byte - Bit 5	Yes
27	TR Byte - Bit 4	Yes
28	TR Byte - Bit 3	Yes
29	TR Byte - Bit 2	Yes
30	TR Byte - Bit 1	Yes
31	TR Byte - Bit 0	Yes
32	MA Byte - Bit 7 (FERF)	Yes
33	MA Byte - Bit 6 (FEBE)	Yes
34	MA Byte - Bit 5	Yes
35	MA Byte - Bit 4	Yes

TABLE 72: THE RELATIONSHIP BETWEEN THE NUMBER OF TXOHENABLE PULSES (SINCE THE LAST OCCURRENCE OF THE TXOHFRAME PULSE) TO THE E3 OVERHEAD BIT, THAT IS BEING PROCESSED BY THE XRT72L50

NUMBER OF TXOHENABLE PULSES	THE OVERHEAD BIT EXPECTED BY THE XRT72L50	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L50?
36	MA Byte - Bit 3	Yes
37	MA Byte - Bit 2	Yes
38	MA Byte - Bit 1	Yes
39	MA Byte - Bit 0	Yes
40	NR Byte - Bit 7	Yes
41	NR Byte - Bit 6	Yes
42	NR Byte - Bit 5	Yes
43	NR Byte - Bit 4	Yes
44	NR Byte - Bit 3	Yes
45	NR Byte - Bit 2	Yes
46	NR Byte - Bit 1	Yes
47	NR Byte - Bit 0	Yes
48	GC Byte - Bit 7	Yes
49	GC Byte - Bit 6	Yes
50	GC Byte - Bit 5	Yes
51	GC Byte - Bit 4	Yes
52	GC Byte - Bit 3	Yes
53	GC Byte - Bit 2	Yes
54	GC Byte - Bit 1	Yes
55	GC Byte - Bit 0	Yes

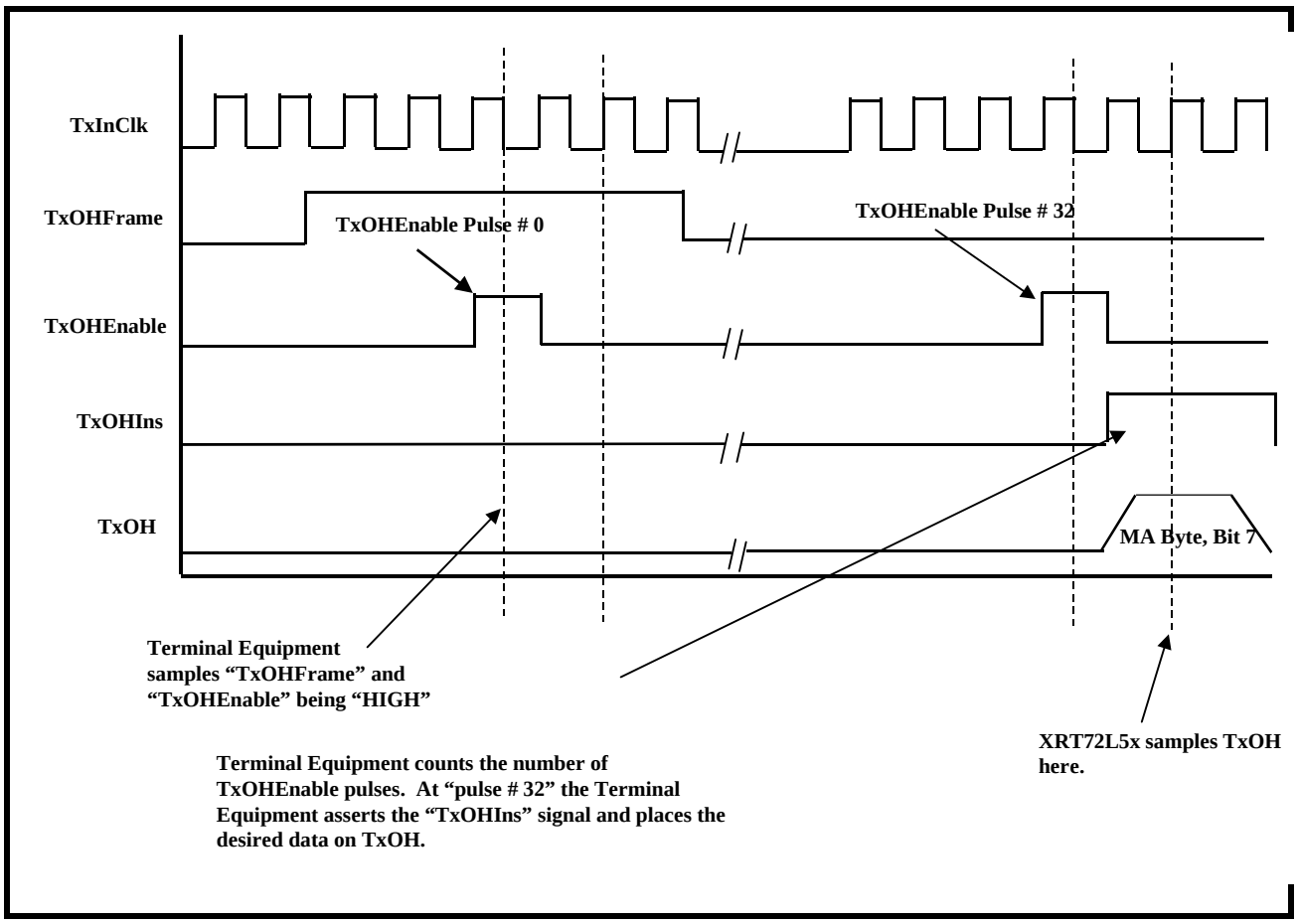
3. After the Terminal Equipment has waited through the appropriate number of pulses via the TxOHEnable pin, it should then assert the TxOHIns input signal. Concurrently, the Terminal Equipment should also place the appropriate value (of the inserted overhead bit) onto the TxOH signal.
4. The Terminal Equipment should hold both the TxOHIns input pin "High" and the value of the TxOH signal stable, until the next TxOHEnable pulse is detected.

Case Study: The Terminal Equipment intends to insert the appropriate overhead bits into the Transmit Overhead Data Input Interface (using Method 2) in order to transmit a Yellow Alarm to the remote terminal equipment.

In this case, the Terminal Equipment intends to insert the appropriate overhead bits, into the Transmit Overhead Data Input Interface such that the XRT72L50 will transmit a Yellow Alarm to the remote terminal equipment. Recall that, for E3, ITU-T G.832 applications, a Yellow Alarm is transmitted by setting the FERF bit (within the MA byte) to "1".

If one assumes that the connection between the Terminal Equipment and the XRT72L50 is as illustrated in Figure 160 then, Figure 161 presents an illustration of the signaling that must go on between the Terminal Equipment and the XRT72L50.

FIGURE 161. BEHAVIOR OF TRANSMIT OVERHEAD DATA INPUT INTERFACE SIGNALS BETWEEN THE XRT72L50 AND THE TERMINAL EQUIPMENT (FOR METHOD 2)



6.2.3 The Transmit E3 HDLC Controller

The Transmit E3 HDLC Controller block can be used to transport Message-Oriented Signaling (MOS) type messages to the remote terminal equipment as discussed in detail below.

NOTE: While executing this particular write operation, the user should write the binary value "000xx110b" into the Tx Controller block), please see Section 4.2.3.2.

6.2.3.1 *Message-Oriented Signaling (e.g., LAP-D) processing via the Transmit E3 HDLC Controller*

The LAPD Transmitter (within the Transmit E3 HDLC Controller Block) allows the user to transmit path maintenance data link (PMDL) messages to the remote terminal via the Outbound E3 Frames. In this case the message bits are either inserted into and carried by the NR or the GC bytes, within the Outbound E3 frames. The on-chip LAPD transmitter supports both the 76 byte and 82 byte length message formats, and the Framer IC allocates 88 bytes of on-chip RAM (e.g., the Transmit LAPD Message buffer) to store the message to be transmitted. The message format complies with ITU-T Q.921 (LAP-D) protocol with different addresses and is presented below in Figure 162.

FIGURE 162. LAPD MESSAGE FRAME FORMAT

Flag Sequence (8 bits)		
SAPI (6-bits)	C/R	EA
TEI (7 bits)		EA
Control (8-bits)		
76 or 82 Bytes of Information (Payload)		
FCS - MSB		
FCS - LSB		
Flag Sequence (8-bits)		

Where: Flag Sequence = 0x7E

SAPI + CR + EA = 0x3C or 0x3E

TEI + EA = 0x01

Control = 0x03

Comprise the 4 HEADER Bytes

The following sections defines each of these bit/byte-fields within the LAPD Message Frame Format.

Flag Sequence Byte

The Flag Sequence byte is of the value 0x7E, and is used to denote the boundaries of the LAPD Message Frame.

The user must write this value (0x7E) at address 0x86.

SAPI - Service Access Point Identifier

The SAPI bit-fields are assigned the value of "001111b" or 15 (decimal).

TEI - Terminal Endpoint Identifier

The TEI bit-fields are assigned the value of 0x00. The TEI field is used in N-ISDN systems to identify a terminal out of multiple possible terminal. However, since the Framer IC transmits data in a point-to-point manner, the TEI value is unimportant.

The user must write 0x3C or 0x3E at address 0x87 and 0x01 at address ox88.

Control

The Control identifies the type of frame being transmitted. There are three general types of frame formats: Information, Supervisory, and Unnumbered. The Framer assigned the Control byte the value 03h. Hence, the Framer will be transmitting and receiving Unnumbered LAPD Message frames.

The user must write 0x03 at address 0x89.

Information Payload

The Information Payload is the 76 bytes or 82 bytes of data (e.g., the PMDL Message) that the user has written into the on-chip Transmit LAPD Message buffer (which is located at addresses 0x8A through 0xDB).

It is important to note that the user must write in a specific octet value into the first byte position within the Transmit LAPD Message buffer (located at Address = 0x8A). The value of this octet depends upon the type of LAPD Message frame/PMDL Message that the user wishes to transmit. Table 73 presents a list of the various types of LAPD Message frames/PMDL Messages that are supported by the XRT72L50 Framer and the corresponding octet value that the user must write into the first octet position within the Transmit LAPD Message buffer.

TABLE 73: THE LAPD MESSAGE TYPE AND THE CORRESPONDING VALUE OF THE FIRST BYTE, WITHIN THE INFORMATION PAYLOAD

LAPD MESSAGE TYPE	VALUE OF FIRST BYTE, WITHIN INFORMATION PAYLOAD OF MESSAGE	MESSAGE SIZE
CL Path Identification	0x38	76 bytes
IDLE Signal Identification	0x34	76 bytes
Test Signal Identification	0x32	76 bytes
ITU-T Path Identification	0x3F	82 bytes

Frame Check Sequence Bytes

The 16 bit FCS (Frame Check Sequence) is calculated over the LAPD Message Header and Information Payload bytes, by using the CRC-16 polynomial, $x^{16} + x^{12} + x^5 + 1$.

NOTE: *For FCS calculation, Header also includes the starting Flag Sequence byte (0x7E).*

Operation of the LAPD Transmitter

If a message is to be transmitted via the LAPD Transmitter then, the information portion (or the body) of the message must be written into the Transmit LAPD Message Buffer, which is located at 0x8A through 0xDB in on-chip RAM via the Microprocessor Interface. Afterwards, the user must do three things:

1. Specify the length of LAPD message to be transmitted.
2. Specify which bit-field (within the E3 frame) that the LAPD Message frame is to be transported on (e.g., either the GC or the NR byte).
3. Specify whether the LAPD Transmitter should transmit this LAPD Message frame only once, or an indefinite number of times at One-Second intervals.
4. Enable the LAPD Transmitter.
5. Initiate the Transmission of the PMDL Message.

Each of these steps will be discussed in detail.

STEP 1 - Specify the type of LAPD Message frame to be Transmitted (within the Transmit LAPD Message Buffer)

The user must write in a specific octet value into the first octet position within the Transmit LAPD Buffer (e.g., at Address Location 0x8A). This octet is referred to as the LAPD Message Frame ID octet. The value of this octet must correspond to the type of LAPD Message frame that is to be transmitted. This octet will ultimately be used by the Remote Terminal Equipment in order to help it identify the type of LAPD message frame that it is receiving. Table 73 lists these octets and the corresponding LAPD Message types.

STEP 2 - Write the PMDL Message into the remaining part of the Transmit LAPD Message Buffer.

The user must now write in his/her PMDL Message into the remaining portion of the Transmit LAPD Message buffer (e.g., addresses 0x8B through 0xDB).

STEP 3 - Specifying the Length of the LAPD Message

One of two different sizes of LAPD Messages can be transmitted, by writing the appropriate data to bit 1 within the Tx E3 LAPD Configuration Register. The bit-format of this register is presented below.

Transmit E3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	X	0	X	X

The relationship between the contents of bit-field 1 and the LAPD Message size is given in Table 74.

TABLE 74: RELATIONSHIP BETWEEN TXLAPD MSG LENGTH AND THE LAPD MESSAGE SIZE

TXLAPD MESSAGE LENGTH	LAPD MESSAGE LENGTH
0	LAPD Message size is 76 bytes
1	LAPD Message size is 82 bytes

NOTE: *The Message Type selected must correspond with the contents of the first byte of the Information (Payload) portion, as presented in* Table 73.

STEP 4 - Specifying which byte-field (within the E3 frame) that the LAPD Message frame octets are to be transported on.

The Transmit E3 Framer block allows the user to transport the LAPD Message frame octets via either the NR byte or the GC byte-field, within each Outbound E3 frame. The user makes this selection by writing the appropriate value to bit-field 4 (DLinNR), within the Tx E3 Configuration Register, as depicted below.

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			TxDL in NR	Not Used	TxAIS Enable	TxLOS Enable	TxMARx
RO	RO	RO	R/W	RO	R/W	R/W	R/W
0	0	0	X	0	0	0	0

If the user writes a “0” into this bit-field, then the LAPD Transmitter will transmit the comprising octets of the Outbound LAPD Message frame via the GC byte field. Additionally, the Transmit E3 Framer block will insert the contents of the TxNR Byte Register (Address = 0x37) into the NR byte of each Outbound E3 frame.

Conversely, if the user writes a “1” into this bit-field, then the LAPD Transmitter will transmit the Outbound LAPD Message frame octets via the NR byte-field, within each Outbound E3 frame. Additionally, the Transmit E3 Framer will insert the contents of the Tx GC Byte Register (Address = 0x35) into the GC byte-field of each Outbound E3 frame.

STEP 5 - Specify whether the LAPD Transmitter should transmit the LAPD Message frame only once, or an indefinite number of times at One-Second intervals.

The Transmit E3 HDLC Control block allows the user to configure the LAPD Transmitter to transmit this LAPD Message frame only once, or an indefinite number of times at One-Second intervals. The user implements this configuration by writing the appropriate value into Bit 3 (Auto Retransmit) within the Tx E3 LAPD Configuration Register (Address = 0x33), as depicted below.

TxE3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	1	0	0	0

If the user writes a “1” into this bit-field, then the LAPD Transmitter will transmit the LAPD Message frame repeatedly at One-Second intervals until the LAPD Transmitter is disabled.

If the user writes a “0” into this bit-field, then the LAPD Transmitter will transmit the LAPD Message frame only once. Afterwards, the LAPD Transmitter will halt its transmission until the user invokes the Transmit LAPD Message frame command, once again.

STEP 6 - Enabling the LAPD Transmitter

Prior to the transmission of any data via the LAPD Transmitter, the LAPD Transmitter must be enabled by writing a "1" to bit 0 (TxLAPD Enable) of the Tx E3 LAPD Configuration Register, as depicted below.

Transmit E3 LAPD Configuration Register (Address = 0x33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	RO	RO	RO	R/W	RO	R/W	R/W
0	0	0	0	X	0	X	1

If the user writes a “1” into this bit-field, then the LAPD Transmitter will be enabled, and the LAPD Transmitter will immediately begin to transmit a continuous stream of Flag Sequence octets (0x7E), via either the GC or the NR byte-field of each Outbound E3 frame (depending upon which byte has been selected to carry the PMDL channel).

Conversely, if the user writes a “0” into this bit-field, then the LAPD Transmitter will be disabled. The Transmit E3 Framer block will insert the contents of the Tx GC Byte Register into the GC byte-field for each Outbound E3 frame. Likewise, the Transmit E3 Framer block will also insert the contents of the Tx NR Byte Register into the NR” byte-field for each Outbound E3 frame. No transmission of PMDL data will occur.

STEP 7 - Initiate the Transmission

At this point, the user should have written the PMDL message into the on-chip Transmit LAPD Message buffer and should have specified the type of LAPD Message that is to be transmitted. The user should have also specified whether the LAPD Transmitter will transport the LAPD Message frame octets via the GC-byte field or via the NR-byte field of each Outbound E3 frame. Finally the LAPD Transmitter should have been enabled. Then initiate the transmission of this message by writing a “1” to Bit 3 (Tx DL Start) within the Tx E3 LAPD Status and Interrupt Register (Address = 0x34), as depicted below.

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	1	0	0	0

A “0” to “1” transition in Bit 3 (TxDL Start) in this register, initiates the transmission of LAPD Message frames. At this point, the LAPD Transmitter will begin to search thorugh the PMDL message, which is residing within the Transmit LAPD Message buffer. It will first compute and append a 2 byte FCS value and if the LAPD Transmitter finds any string of five (5) consecutive “1’s” in the PMDL Message, then the LAPD Transmitter will insert a “0” immediately following these strings of consecutive “1’s”. This procedure is known as stuffing. The purpose of PMDL Message stuffing is to insure that the user’s PMDL Message does not contain strings of data that mimic the Flag Sequence octet (e.g., six consecutive “1’s”) or the ABORT Sequence octet (e.g., seven consecutive “1’s”). Afterwards, the LAPD Transmitter will begin to encapsulate the PMDL Message, residing in the Transmit LAPD Message buffer, into a LAPD Message frame. Finally, the LAPD Transmitter will fragment the Outbound LAPD Message frame into octets and will begin to transport these octets via the GC or the NR byte-fields (depending upon the user’s selection) of each Outbound E3 frame.

While the LAPD Transmitter is transmitting this LAPD Message frame, the TxDL Busy bit-field (Bit 2) within the Tx E3 LAPD Status and Interrupt Register, will be set to “1”. This bit-field allows the user to poll the status of the LAPD Transmitter. Once the LAPD Transmitter has completed the transmission of the LAPD Message, then this bit-field will toggle back to “0”.

The user can configure the LAPD Transmitter to interrupt the local Microprocessor/Microcontroller upon completion of transmission of the LAPD Message frame, by setting bit-field 1 (TxLAPD Interrupt Enable) within the Tx E3 LAPD Status and Interrupt register (Address = 0x34). to “1” as depicted below.

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	1	0

‘The purpose of this interrupt is to let the Microprocessor/Microcontroller know that the LAPD Transmitter is available and ready to transmit a LAPD Message frame (which contains a new PMDL Message) to the remote terminal equipment. Bit 0 (Tx LAPD Interrupt Status) within the Tx E3 LAPD Status and Interrupt Register will reflect the status for the Transmit LAPD Interrupt.

NOTE: *This bit-field will be reset upon reading this register.*

Summary of Operating the LAPD Transmitter

Once the user has invoked the TxDL Start command, the LAPD Transmitter will do the following.

- Depending on the message type, compute the 16 bit Frame Check Sum (FCS) of the LAPD Message Frame (e.g., of the LAPD Message header and information payload) and append this value to the LAPD Message, (at the end of 76 or 82 bytes).
- Append a trailer Flag Sequence octet to the end of the message LAPD following the 16 bit FCS value.

- Serialize the composite LAPD message. Between the two 0x7E flags, ZeroStuff any consecutive five “Ones” by inserting an extra “0”. This insures that any occurrence of 0x7E in the payload does not serve as a terminating flag sequence.
- Insert the Zero Stuffed LAPD message into the GC or NR byte-fields within the Outbound E3 Frame.
- Complete the transmission of the frame overhead, payload, FCS value, and trailer Flag Sequence octet via the Transmit DS3 Framer.

Once the LAPD Transmitter has completed its transmission of the LAPD Message frame, the Framer will generate an Interrupt to the MIcroprocessor/Microcontroller (if enabled). Afterwards, the LAPD Transmitter will either halt its transmission of LAPD Message frames or will proceed to retransmit the LAPD Message frame, repeatedly at One-Second intervals. In between these transmissions of the LAPD Message frames, the LAPD Transmitter will be sending a continuous stream of Flag Sequence bytes. The LAPD Transmitter will continue this behavior until the user has disabled the LAPD Transmitter by writing a “1” into bit 3 (No Data Link) within the Tx E3 Configuration register.

NOTE: *In order to prevent the user’s data (e.g., the PMDL Message within the LAPD Message frame) from mimicking the Flag Sequence byte or an ABORT Sequence, the LAPD Transmitter will parse through the PMDL Message data and insert a “0” into this data, immediately following the detection of five (5) consecutive “1’s” (this stuffing occurs while the PMDL message data is being read in from the Transmit LAPD Message frame. The Remote LAPD Receive (See Section 6.3.3) will have the responsibility of checking the newly received PMDL messages for a string of five (5) consecutive “1’s” and removing the subsequent “0” from the payload portion of the incoming LAPD Message.*

Figure 163 is a flow chart that depicts the procedure (in white boxes) that the user should use in order to transmit a PMDL message via the LAPD Transmitter, when the LAPD Transmitter is configured to retransmit the LAPD Message frame, repeatedly at One-Second intervals. This figure also indicates (via the Shaded boxes) what the LAPD Transmitter circuitry will do before and during message transmission.

FIGURE 163. FLOW CHART DEPICTING HOW TO USE THE LAPD TRANSMITTER (LAPD TRANSMITTER IS CONFIGURED TO RE-TRANSMIT THE LAPD MESSAGE FRAME REPEATEDLY AT ONE-SECOND INTERVALS)

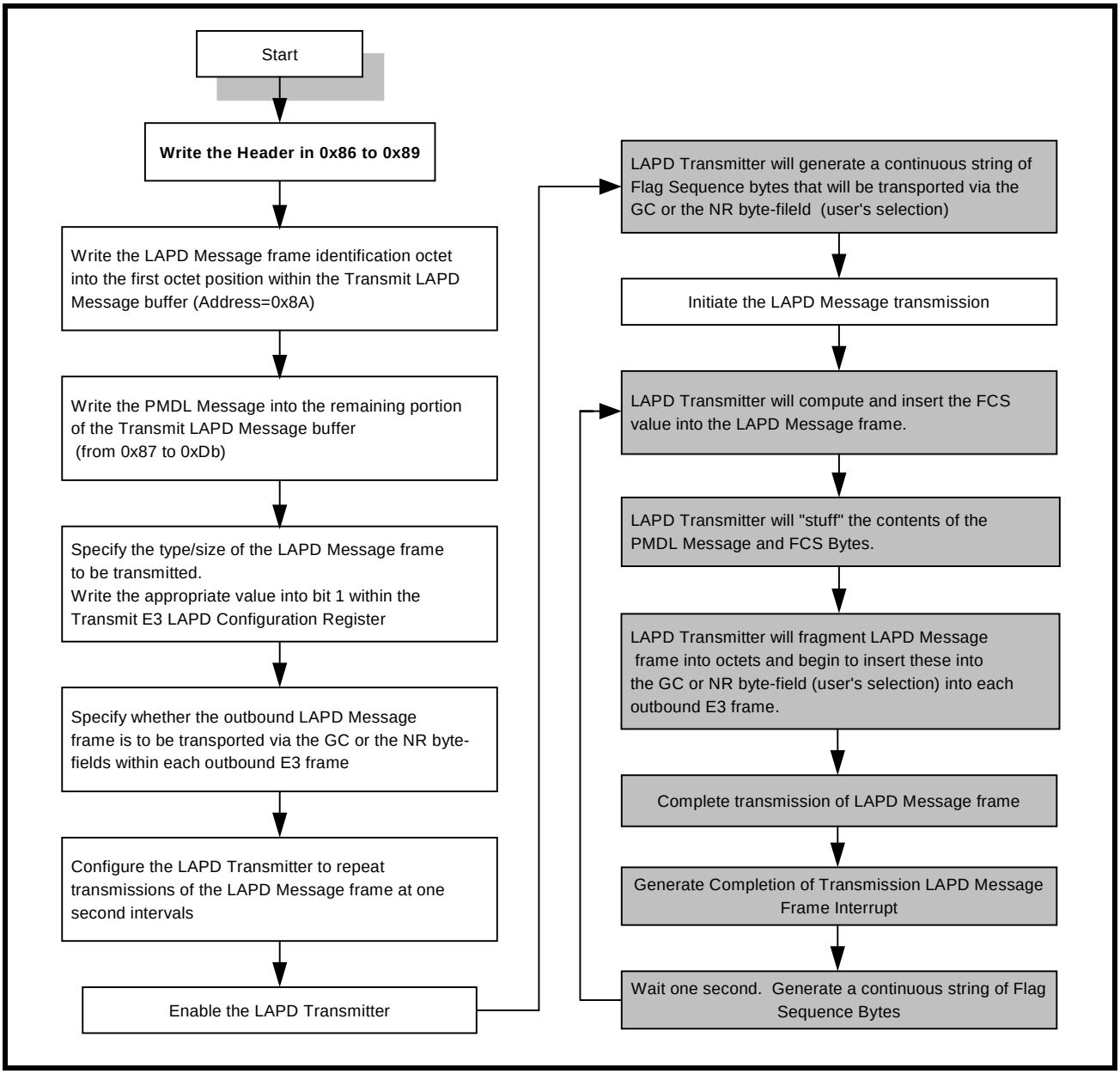
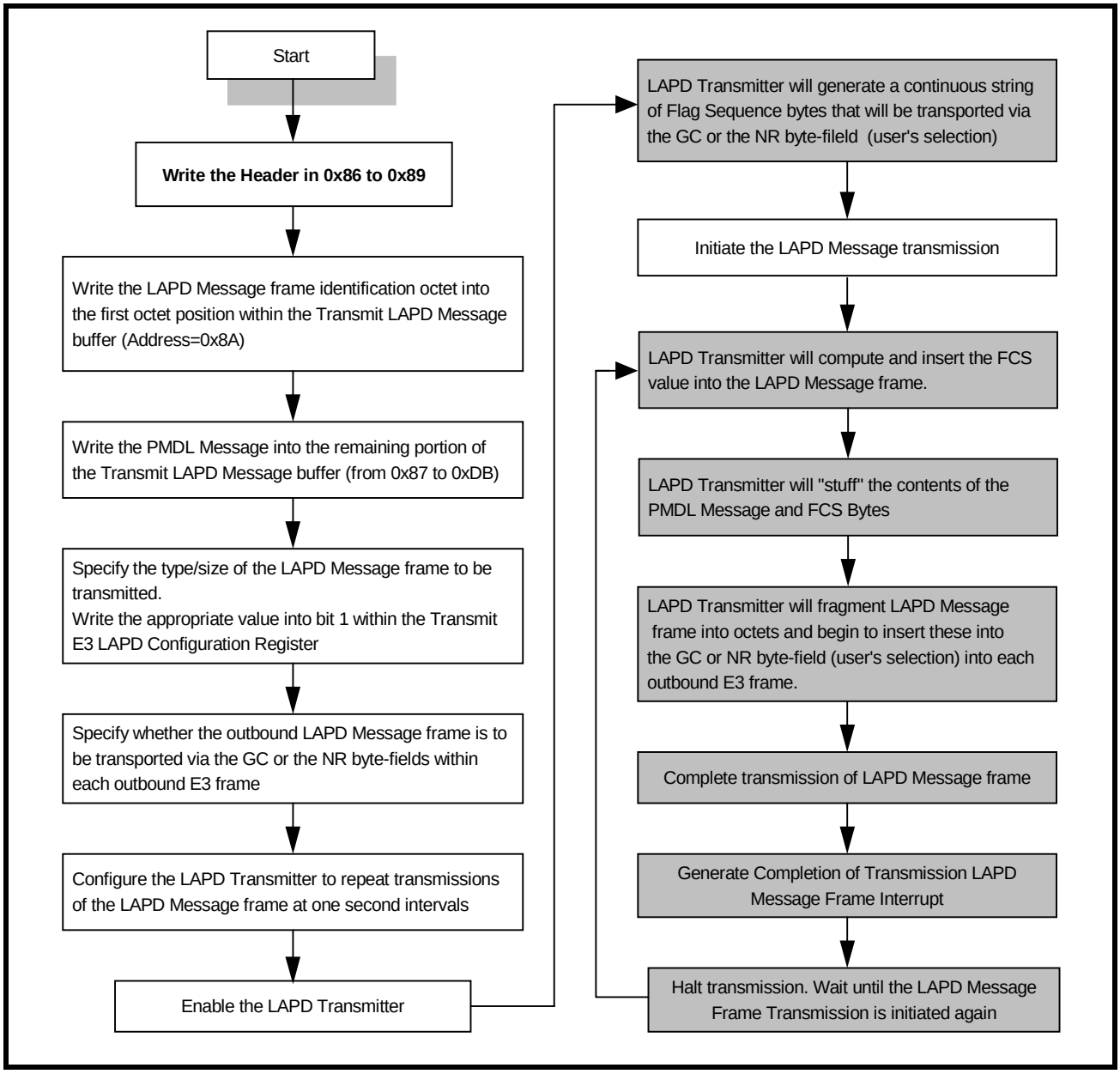


Figure 164 presents the procedure (in white boxes) which the user should use in order to transmit a PMDL Message via the LAPD Transmitter, when the LAPD Transmitter is configured to transmit a LAPD Message frame only once, and then halt transmission.

FIGURE 164. FLOW CHART DEPICTING HOW TO USE THE LAPD TRANSMITTER (LAPD TRANSMITTER IS CONFIGURED TO TRANSMIT A LAPD MESSAGE FRAME ONLY ONCE).



The Mechanics of Transmitting a New LAPD Message frame, if the LAPD Transmitter has been configured to re-transmit the LAPD Message frame, repeatedly, at One-Second intervals.

If the LAPD Transmitter has been configured to retransmit the LAPD Message frame repeatedly at One-Second intervals, then it will repeatedly transmit the stuffed PMDL Message to the Remote Terminal Equipment at one second intervals.

If another (e.g., a different) PMDL Message is to be transmitted to the Remote Terminal Equipment this new message will have to be written into the Transmit LAPD Message buffer, via the Microprocessor Interface block of the Framer IC. However, care must be taken when writing this new PMDL message. If this message is written into the Transmit LAPD Message buffer at the wrong time (with respect to these One-Second LAPD Message frame transmissions), the user's action could interfere with these transmissions, thereby causing the LAPD Transmitter to transmit a corrupted message to the Remote Terminal Equipment. In order to avoid this

problem, while writing the new message into the Transmit LAPD Message buffer, the user should do the following.

1. Configure the Framer to automatically reset activated interrupts.

The user can do this by writing a "1" into Bit 3 within the Framer Operating Mode register (Address = 0x00), as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Local Loop-back	DS3/E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	1

This action will prevent the LAPD Transmitter from generating its own One-Second interrupt (following each transmission of the LAPD Message frame).

2. Enable the One-Second Interrupt

This can be done by writing a "1" into Bit 0 (One-Second Interrupt Enable) within the Block Interrupt Enable Register, as depicted below.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One-Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	0	1

3. Write the new message into the Transmit LAPD Message buffer immediately after the occurrence of the One-Second Interrupt

By synchronizing the writes to the Transmit LAPD Message buffer to occur immediately after the occurrence of the One-Second Interrupt, the user avoids conflicting with the One-Second transmission of the LAPD Message frame, and will transmit the correct (uncorrupted) PMDL Message to the Remote LAPD Receiver.

6.2.4 The Transmit E3 Framer Block

6.2.4.1 *Brief Description of the Transmit E3 Framer*

The Transmit E3 Framer block accepts data from any of the following four sources, and uses it to form the E3 data stream.

- The Transmit Payload Data Input block
- The Transmit Overhead Data Input block
- The Transmit HDLC Controller block
- The Internal Overhead Data Generator

The manner in how the Transmit E3 Framer block handles data from each of these sources is described below.

Handling of data from the Transmit Payload Data Input Interface

For E3 applications, all data that is input to the Transmit Payload Data Input Interface will be inserted into the payload bit positions within the Outbound E3 frames.

Handling of data from the Internal Overhead Bit Generator

By default, the Transmit E3 Framer block will internally generate the overhead bytes. However, if the Terminal Equipment inserts its own values for the overhead bits or bytes (via the Transmit Overhead Data Input Interface) or, if the user enables and employs the Transmit E3 HDLC Controller block, then these internally generated overhead bytes will be overwritten.

Handling of data from the Transmit Overhead Data Input Interface

For E3 applications, the Transmit E3 Framer block automatically generates and inserts the framing alignment bytes (e.g., the FA1 and FA2 framing alignment bytes) into the Outbound E3 frames. Further, the Transmit E3 Framer block will automatically compute and insert the EM byte into the Outbound E3 frames. Hence, the Transmit E3 Framer block will not accept data from the Transmit OH Data Input Interface block for the FA1, FA2 and EM bytes.

However, the Transmit E3 Framer block will accept (and insert) data from the Transmit Overhead Data Input Interface for the following byte-fields.

- MA byte
- TR byte
- NR byte
- GC byte

If the user's local Data Link Equipment activates the Transmit Overhead Data Input Interface block and writes data into this interface for these bits or bytes, then the Transmit E3 Framer block will insert this data into the appropriate overhead bit/byte-fields, within the Outbound E3 frames.

6.2.4.2 *Detailed Functional Description of the Transmit E3 Framer Block*

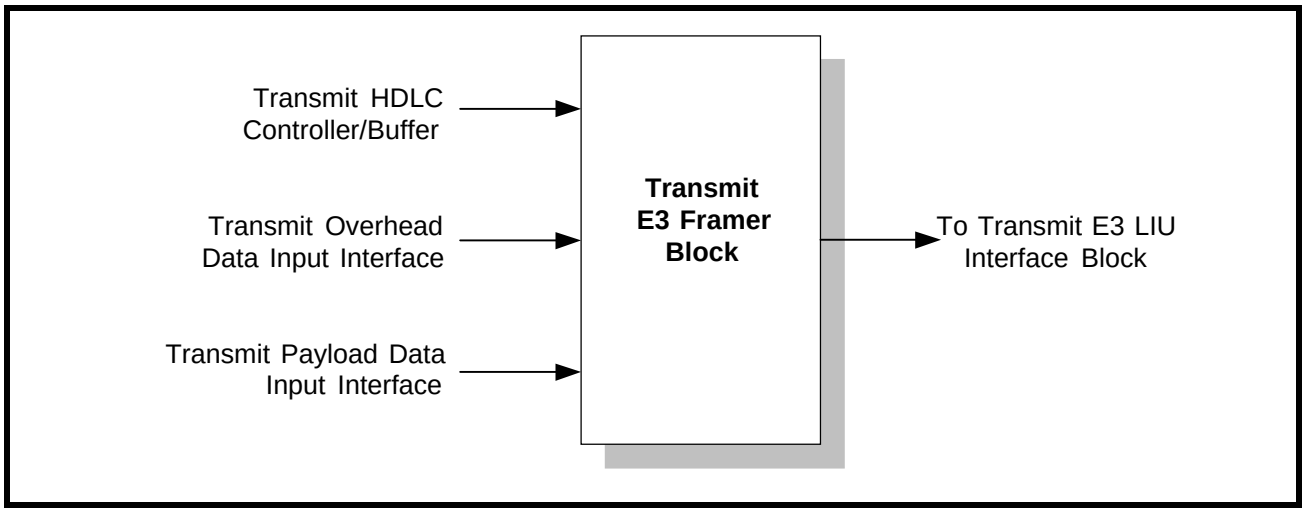
The Transmit E3 Framer receives data from the following three sources and combines them together to form a E3 data stream.

- The Transmit Payload Data Input Interface block.
- The Transmit Overhead Data Input Interface block
- The Transmit HDLC Controller block.

Afterwards, this E3 data stream will be routed to the Transmit E3 LIU Interface block, for further processing.

Figure 165 presents a simple illustration of the Transmit E3 Framer block, along with the associated paths to the other functional blocks within the chip.

FIGURE 165. THE TRANSMIT E3 FRAMER BLOCK AND THE ASSOCIATED PATHS TO OTHER FUNCTIONAL BLOCKS



In addition to taking data from multiple sources and multiplexing them, in appropriate manner, to create the Outbound E3 frames, the Transmit E3 Framer block has the following roles.

- Generating Alarm Conditions
- Generating Errored Frames (for testing purposes)
- Routing Outbound E3 frames to the Transmit E3 LIU Interface block

Each of these additional roles are discussed below.

6.2.4.2.1 Generating Alarm Conditions

The Transmit E3 Framer block permits the user to, by writing the appropriate data into the on-chip registers, to override the data that is being written into the Transmit Payload Data and Overhead Data Input Interfaces and transmit the following alarm conditions.

- Generate the Yellow Alarms (or FERF indicators)
- Manipulate the FERF-bit, within the MA byte (set them to "0")
- Generate the AIS Pattern
- Generate the LOS pattern
- Generate FERF (Yellow) Alarms, in response to detection of a Red Alarm condition (via the Receive Section of the XRT72L50).
- Generate and transmit a desired value for the FEBE (Far-End-Block Error) bit, within the MA byte.

The procedure and results of generating any of these alarm conditions is presented below.

The user can exercise each of these options by writing the appropriate data to the Tx E3 Configuration Register (Address = 0x30). The bit format of this register is presented below.

TxE3 Configuration Register (Address = 0x30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			TxDL in NR	Not Used	TxAIS Enable	TxLOS Enable	TxMARx
RO	RO	RO	R/W	RO	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit-field 2 through 0 permit the user to transmit various alarm conditions to the remote terminal equipment. The role/function of each of these three bit-fields within the register, are discussed below.

6.2.4.2.1.1 *Tx AIS Enable - Bit 2*

This read/write bit field permits the user to force the transmission of an AIS (Alarm Indication Signal) pattern to the remote terminal equipment via software control. If the user opts to transmit an AIS pattern, then the Transmit Section of the Framer IC will begin to transmit an unframed all ones pattern to the remote terminal equipment. Table 75 presents the relationship between the contents of this bit-field, and the resulting Framer action.

TABLE 75: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 2 (TX AIS ENABLE) WITHIN THE TX E3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT E3 FRAMER BLOCK'S ACTION

BIT 2	TRANSMIT E3 FRAMER'S ACTION
0	**Normal Operation:** The Transmit Section of the XRT72L50 Framer IC will transmit E3 traffic based upon data that it accepts via the Transmit Payload Data Input Interface block, the Transmit Overhead Data Input Interface block, the Transmit HDLC Controller block and internally generated overhead bytes.
1	**Transmit AIS Pattern:** The Transmit E3 Framer block will overwrite the E3 traffic, within an Unframed All Ones pattern.

NOTE: *This bit is ignored whenever the TxLOS bit-field is set.*

6.2.4.2.1.2 *Transmit LOS Enable - Bit 1*

This read/write bit field allows the user to transmit an LOS (Loss of Signal) pattern to the remote terminal, upon software control. Table 76 relates the contents of this bit field to the Transmit E3 Framer block's action.

TABLE 76: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 1 (TX LOS) WITHIN THE TX E3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT E3 FRAMER BLOCK'S ACTION

BIT 1	TRANSMIT E3 FRAMER'S ACTION
0	**Normal Operation:** The Overhead bits are either internally generated, or they are inserted via the Transmit Overhead Data Input Interface or the Transmit HDLC Controller blocks. The Payload bits are received from the Transmit Payload Data Input Interface.
1	**Transmit LOS Pattern:** When this command is invoked the Transmit E3 Framer will do the following. • Set all of the overhead bytes to "0" (including the FA1 and FA2 bytes) Overwrite the E3 payload bits with an "all zeros" pattern.

NOTE: *When this bit is set, it overrides all of the other bits in this register.*

6.2.4.2.1.3 *Transmitting FEBE (Far-End Block Error) and FERF (Far-End Receive Failures) indicators via Software control*

The "TxE3 Configuration" register (Address = 0x30) contains a register bit (Bit 0 - TxMARx) that permits the user to control the state of the FEBE and FERF bit-fields, in the outbound E3 data stream.

The bit-format of the "TxE3 Configuration" register is presented below.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			TxDL in NR	Not Used	TxAIS Enable	TxLOS Enable	TxMARx
RO	RO	RO	R/W	RO	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This read/write bit-field permits the user to configure the XRT72L50 to do one of the following.

A. Set the "FEBE" and "FERF" bit-fields (within the MA byte of "outbound" E3 frames) to the appropriate state based upon conditions detected by the "Receive DS3/E3 Framer" block.

B. To (via software-control) set the states of the "FEBE" and "FERF" bit-fields (within the MA byte of "outbound" E3 frames).

Setting this bit-field to "1" configures the Transmit DS3/E3 Framer block to automatically set the FEBE and FERF bit-fields (within the outbound E3 data stream) to states based upon conditions detected by the Receive DS3/E3 Framer block.

NOTE: *In this mode, the Transmit DS3/E3 Framer block will set and clear the FERF and FEBE bit-fields in response to the following conditions.*

A. FERF bit-field

If the Receive DS3/E3 Framer block (in the same channel) is currently experiencing an LOS, AIS or LOF condition, then the Transmit DS3/E3 Framer block will automatically set the FERF bit-field (in the outbound E3 frame) to "1". Conversely, if the Receive DS3/E3 Framer block is not experiencing any of these conditions, then the Transmit DS3/E3 Framer block will set the FERF bit-field (in the outbound E3 frame) to "0".

B. FEBE bit-field

If the Receive DS3/E3 Framer block detects a BIP-8 error in the incoming E3 frame, then the Transmit DS3/E3 Framer block will automatically set the FEBE bit-field (in the outbound E3 frame) to "1". Conversely, if the Receive DS3/E3 Framer block does not detect a BIP-8 error in the incoming E3 frame, then the Transmit DS3/E3 Framer block will set the FEBE bit-field (in the outbound E3 frame) to "0".

Setting this bit-field to "0" configures the Transmit DS3/E3 Framer block to set the FEBE and FERF bit-fields (within the outbound E3 data stream) to the values residing within the FEBE and FERF bit-fields within the TxE3 MA Byte Register (Address = 0x36), as illustrated below.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FERF	FEBE	PLDType			Payload Dependent		Timing Marker
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	0	1	0	0	0	0

6.2.4.2.2 Configuring the Transmit Trail Trace Buffer Message

The XRT72L50 Framer IC contains 16 bytes worth of Transmit Trail Trace Buffer registers and 16 bytes worth of Receive Trail Trace Buffer registers. The role of the Receive Trail Trace Buffer registers are described in Section 6.1.1.3.

The XRT72L50 Framer IC contains 16 Transmit Trail Trace Buffer registers (e.g., Tx TTB-0 through TxTTB-15). The purpose of these registers are to provide a 16-byte Trail Access Point Identifier to the Remote Terminal Equipment. The Remote Terminal Equipment will use this information in order to verify that it is still receiving data from its intended transmitter. The specific use of these registers follows.

For Trail Trace Buffer Message purposes, the Transmit E3 Framer block will group 16 consecutive E3 frames, into a Trail Trace Buffer super-frame. When the Transmit E3 Framer block is generating the first E3 frame, within a Trail Trace Buffer super-frame, it will read in the contents of the Tx TTB-0 Register (Address = 0x38) and insert this value into the TR byte-field of this very first Outbound E3 frame. When the Transmit E3 Framer is generating the very next E3 frame (e.g., the second E3 frame, within the Trail Trace Buffer super-frame), it will read in the contents of the Tx TTB-1 register (Address = 0x39) and insert this value into the TR byte-field of this Outbound E3 frame. As the Transmit E3 Framer block is creating each subsequent E3 frame, within this Trail Trace Buffer super frame, it will continue to increment to the very next Transmit Trail Trace Buffer register. The Transmit E3 Framer block will then read in the contents of this particular Transmit Trail Trace Buffer register (Tx TTB-n) and insert this value into the TR byte-field of the very next Outbound E3 frame. After the Transmit E3 Framer block has created the 16th E3 frame, within a given Trail Trace Buffer super-frame (e.g., it has read in the contents of Tx TTB-15 register and has inserted this value into the TR byte of the 16th E3 frame), it will begin to create a new Trail Trace Buffer super-frame, by reading the contents of the Tx TTB-0 register, and repeating the above-mentioned procedure.

The contents of the Tx TTB-0 register will typically be of the form [1, C6, C5, C4, C3, C2, C1, C0]. The “1” in the MSB (Most Significant bit) position of this byte is used to designate that this octet is the frame-start marker (e.g., is the first of the 16 TR bytes, within a Trail Trace Buffer super-frame). The remaining Trail Trace Buffer registers (TxTTB-1 through TxTTB-15) will typically contain a “0” in their MSB positions. The remaining bits

within the Tx TTB-0 register C6 through C0 are the CRC-7 bits calculated over the contents of all 16 TR bytes, within the previous Trail Trace Buffer super-frame. The contents of the remaining Trail Trace Buffer registers (e.g., Tx TTB-1 through Tx TTB-15) will typically contain the 15 ASCII characters required for the E.164 numbering format.

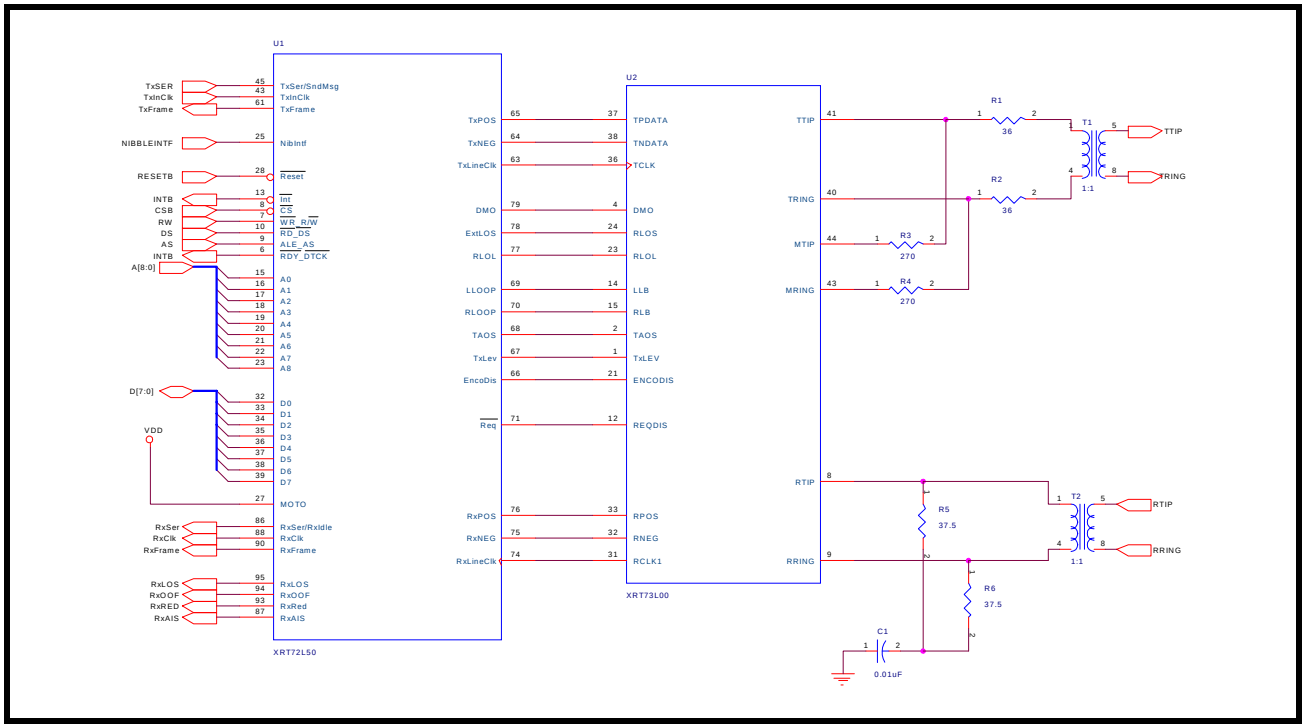
NOTES:

1. *The XRT72L50 Framer IC will not compute the CRC-7 value, to be written into the Tx TTB-0 register. The user's system must compute this value prior to writing it into the Tx TTB-0 register.*
2. *The user, when writing data into the Tx TTB registers, must take care to insure that only the Tx TTB-0 register contains an octet with a "1" in the MSB (most significant bit) position. All remaining Tx TTB registers (e.g., Tx TTB-1 through Tx TTB-15) must contain octets with a "0" in the MSB position. The reason for this cautionary note is presented in* Section 6.1.1.3*.*

6.2.5 The Transmit E3 Line Interface Block

The XRT72L50 Framer IC is a digital device that takes E3 payload and overhead bit information from some terminal equipment, processes this data and ultimately, multiplexes this information into a series of Outbound E3 frames. However, the XRT72L50 Framer IC lacks the current drive capability to be able to directly transmit this E3 data stream through some transformer-coupled coax cable with enough signal strength for it to be received by the remote receiver. Therefore, in order to get around this problem, the Framer IC requires the use of an LIU (Line Interface Unit) IC. An LIU is a device that has sufficient drive capability, along with the necessary pulse-shaping circuitry to be able to transmit a signal through the transmission medium in a manner that it can be reliably received by the far-end receiver. Figure 166 presents a circuit drawing depicting the Framer IC interfacing to an LIU (XRT73L00 DS3/E3/STS-1 Transmit LIU).

FIGURE 166. INTERFACING THE XRT72L50 FRAMER IC TO THE XRT73L00 DS3/E3/STS-1 LIU



The Transmit Section of the XRT72L50 contains a block which is known as the Transmit E3 LIU Interface block. The purpose of the Transmit E3 LIU Interface block is to take the Outbound E3 data stream, from the Transmit E3 Framer block, and to do the following:

1. Encode this data into one of the following line codes

a. Unipolar (e.g., Single-Rail)

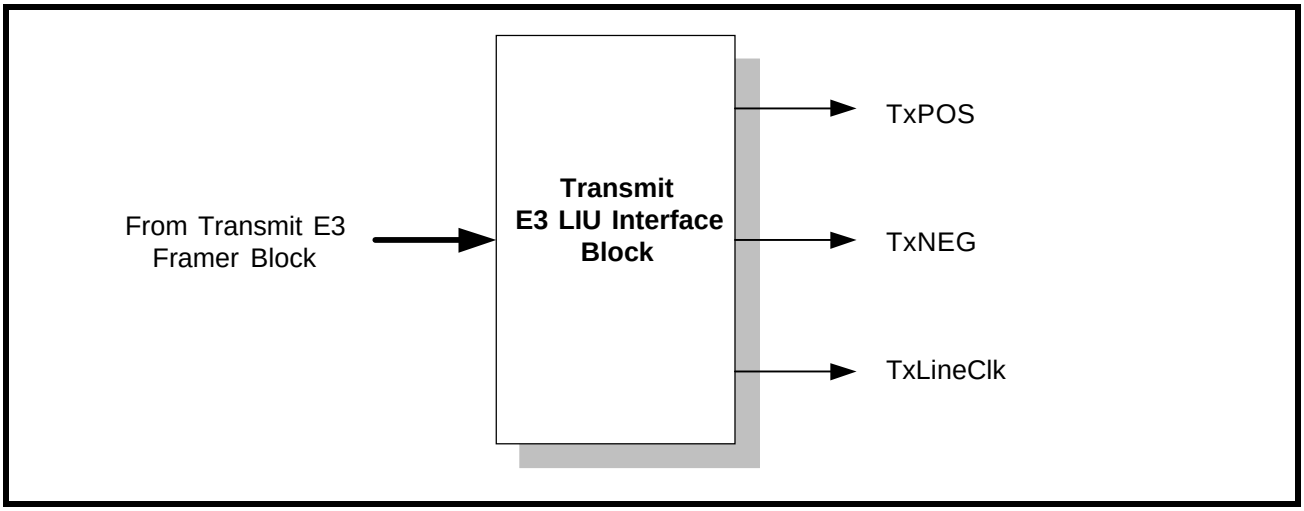
b. AMI (Alternate Mark Inversion)

c. HDB3 (High Density Bipolar - 3)

2. And to transmit this data to the LIU IC.

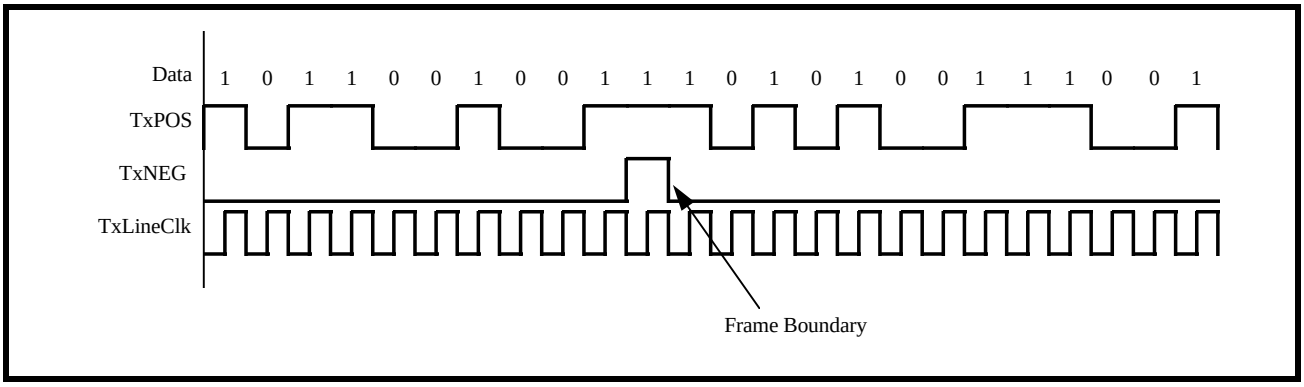
Figure 167 presents a simple illustration of the Transmit E3 LIU Interface block.

FIGURE 167. THE TRANSMIT E3 LIU INTERFACE BLOCK



The Transmit E3 LIU Interface block can transmit data to the LIU IC or other external circuitry via two different output modes: Unipolar or Bipolar. If the user selects Unipolar (or Single Rail) mode, then the contents of the E3 Frame is output, in a binary (NRZ manner) data stream via the TxPOS pin to the LIU IC. The TxNEG pin will only be used to denote the frame boundaries. TxNEG will pulse "High" for one bit period, at the start of each new E3 frame, and will remain "Low" for the remainder of the frame. Figure 168 presents an illustration of the TxPOS and TxNEG signals during data transmission while the Transmit E3 LIU Interface block is operating in the Unipolar mode. This mode is sometimes referred to as Single Rail mode because the data pulses only exist in one polarity: positive.

FIGURE 168. THE BEHAVIOR OF TXPOS AND TXNEG SIGNALS DURING DATA TRANSMISSION WHILE THE TRANSMIT E3 LIU INTERFACE IS OPERATING IN THE UNIPOLAR MODE



When the Transmit E3 LIU Interface block is operating in the Bipolar (or Dual Rail) mode, then the contents of the E3 Frame is output via both the TxPOS and TxNEG pins. If the Bipolar mode is chosen, then the E3 data can be transmitted to the LIU via one of two different line codes: Alternate Mark Inversion (AMI) or High Density Bipolar -3 (HDB3). Each one of these line codes will be discussed below. Bipolar mode is sometimes referred to as Dual Rail because the data pulses occur in two polarities: positive and negative. The role of the TxPOS, TxNEG and TxLineClk output pins, for this mode are discussed below.

TxPOS - Transmit Positive Polarity Pulse: The Transmit E3 LIU Interface block will assert this output to the LIU IC when it desires for the LIU to generate and transmit a positive polarity pulse to the remote terminal equipment.

TxNEG - Transmit Negative Polarity Pulse: The Transmit E3 LIU Interface block will assert this output to the LIU IC when it desires for the LIU to generate and transmit a negative polarity pulse to the remote terminal equipment.

TxLineClk - Transmit Line Clock: The LIU IC uses this signal from the Transmit E3 LIU Interface block to sample the state of its TxPOS and TxNEG inputs. The results of this sampling dictates the type of pulse (positive polarity, zero, or negative polarity) that it will generate and transmit to the remote Receive E3 Framer.

6.2.5.1 *Selecting the various Line Codes*

The user can select either the Unipolar Mode or Bipolar Mode by writing the appropriate value to Bit 3 of the I/O Control Register (Address = 0x01), as shown below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 77 relates the value of this bit field to the Transmit E3 LIU Interface Output Mode.

TABLE 77: THE RELATIONSHIP BETWEEN THE CONTENT OF BIT 3 (UNIPOLAR/$\overline{\text{BIPOLAR}}$) WITHIN THE UNI I/O CONTROL REGISTER AND THE TRANSMIT E3 FRAMER LINE INTERFACE OUTPUT MODE

BIT 3	TRANSMIT E3 FRAMER LIU INTERFACE OUTPUT MODE
0	**Bipolar Mode:** AMI or HDB3 Line Codes are Transmitted and Received
1	**Unipolar (Single Rail) Mode** of transmission and reception of E3 data is selected.

NOTES:

1. *The default condition is the Bipolar Mode.*
2. *This selection also effects the operation of the Receive E3 LIU Interface block*

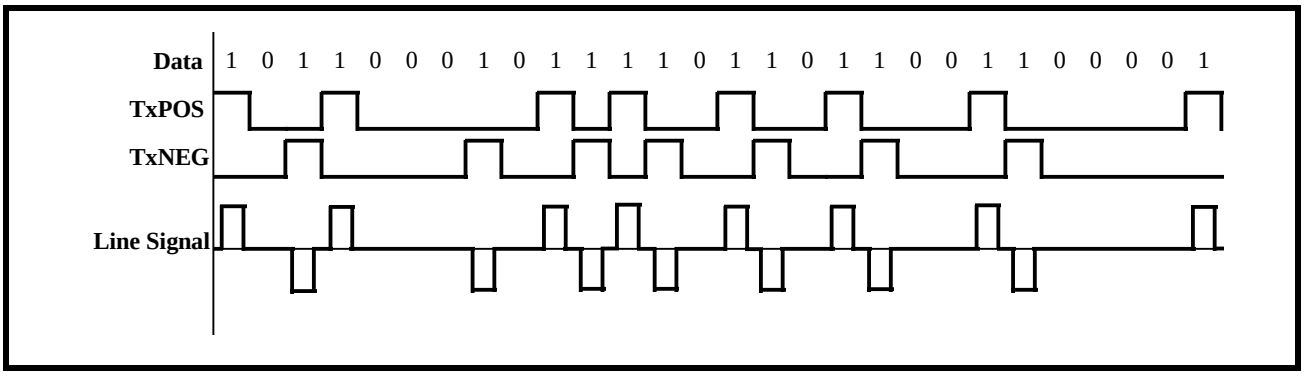
6.2.5.1.1 The Bipolar Mode Line Codes

If the Framer is selected to operate in the Bipolar Mode, then the E3 data-stream can be transmitted via the AMI (Alternate Mark Inversion) or the HDB3 Line Codes. The definition of AMI and HDB3 line codes follow.

6.2.5.1.1.1 *The AMI Line Code*

AMI or Alternate Mark Inversion, means that consecutive "one's" pulses (or marks) will be of opposite polarity with respect to each other. The line code involves the use of three different amplitude levels: +1, 0, and -1. +1 and -1 amplitude signals are used to represent one's (or mark) pulses and the "0" amplitude pulses (or the absence of a pulse) are used to represent zeros (or space) pulses. The general rule for AMI is: if a given mark pulse is of positive polarity, then the very next mark pulse will be of negative polarity and vice versa. This alternating-polarity relationship exists between two consecutive mark pulses, independent of the number of 'zeros' that may exist between these two pulses. Figure 169 presents an illustration of the AMI Line Code as would appear at the TxPOS and TxNEG pins of the Framer, as well as the output signal on the line.

FIGURE 169. ILLUSTRATION OF AMI LINE CODE



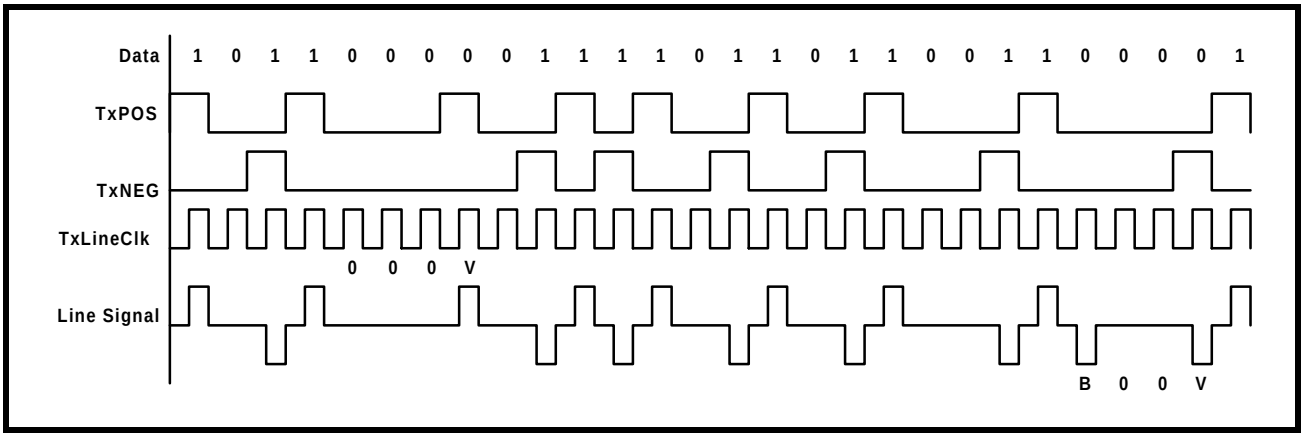
NOTE: *One of the main reasons that the AMI Line Code has been chosen for driving transformer-coupled media is that this line code introduces no dc component, thereby minimizing dc distortion in the line.*

6.2.5.1.1.2 *The HDB3 Line Code*

The Transmit E3 Framer and the associated LIU IC combine the data and timing information (originating from the TxLineClk signal) into the line signal that is transmitted to the remote receiver. The remote receiver has the task of recovering this data and timing information from the incoming E3 data stream. Many clock and data recovery schemes rely on the use of Phase Locked Loop technology. Phase-Locked-Loop (PLL) technology for clock recovery relies on transitions in the line signal, in order to maintain lock with the incoming E3 data stream. However, PLL-based clock recovery scheme, are vulnerable to the occurrence of a long stream of consecutive zeros (e.g., the absence of transitions). This scenario can cause the PLL to lose lock with the incoming E3 data, thereby causing the clock and data recovery process of the receiver to fail. Therefore, some approach is needed to insure that such a long string of consecutive zeros can never happen. One such technique is HDB3 encoding. HDB3 (or High Density Bipolar - 3) is a form of AMI line coding that implements the following rule.

In general the HDB3 line code behaves just like AMI with the exception of the case when a long string of consecutive zeros occur on the line. Any string of 4 consecutive zeros will be replaced with either a "000V" or a "B00V" where "B" refers to a Bipolar pulse (e.g., a pulse with a polarity that is compliant with the AMI coding rule). And "V" refers to a Bipolar Violation pulse (e.g., a pulse with a polarity that violates the alternating polarity scheme of AMI.) The decision between inserting an "000V" or a "B00V" is made to insure that an odd number of Bipolar (B) pulses exist between any two Bipolar Violation (V) pulses. Figure 170 presents a timing diagram that illustrates examples of HDB3 encoding.

FIGURE 170. ILLUSTRATION OF TWO EXAMPLES OF HDB3 ENCODING



The user chooses between AMI or HDB3 line coding by writing to bit 4 of the I/O Control Register (Address = 0x01), as shown below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 78 relates the content of this bit-field to the Bipolar Line Code which E3 Data will be transmitted and received at.

TABLE 78: THE RELATIONSHIP BETWEEN BIT 4 (AMI/HDB3*) WITHIN THE I/O CONTROL REGISTER AND THE BIPOLAR LINE CODE THAT IS OUTPUT BY THE TRANSMIT E3 LIU INTERFACE BLOCK

BIT 4	BIPOLAR LINE CODE
0	HDB3
1	AMI

NOTES:

1. *This bit is ignored if the Unipolar mode is selected.*
2. *This selection also effects the operation of the Receive E3 LIU Interface block*

6.2.5.2 *TxLineClk Clock Edge Selection*

The Framer also allows the user to specify whether the E3 output data (via TxPOS and/or TxNEG output pins) is to be updated on the rising or falling edges of the TxLineClk signal. This selection is made by writing to bit 2 of the I/O Control Register, as depicted below.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 79 relates the contents of this bit field to the clock edge of TxClk that E3 Data is output on the TxPOS and/or TxNEG output pins.

TABLE 79: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 2 (TXLINECLK INV) WITHIN THE I/O CONTROL REGISTER AND THE TXLINECLK CLOCK EDGE THAT TXPOS AND TXNEG ARE UPDATED ON

BIT 2	RESULT
0	**Rising Edge:** Outputs on TxPOS and/or TxNEG are updated on the rising edge of TxLineClk. See Figure 171 for timing relationship between TxLineClk, TxPOS and TxNEG signals, for this selection.
1	**Falling Edge:** Outputs on TxPOS and/or TxNEG are updated on the falling edge of TxLineClk. See Figure 172 for timing relationship between TxLineClk, TxPOS and TxNEG signals, for this selection.

NOTE: *The user will typically make the selection based upon the set-up and hold time requirements of the Transmit LIU IC.*

FIGURE 171. WAVEFORM/TIMING RELATIONSHIP BETWEEN TXLINECLK, TXPOS AND TXNEG - TXPOS AND TXNEG ARE CONFIGURED TO BE UPDATED ON THE RISING EDGE OF TXLINECLK

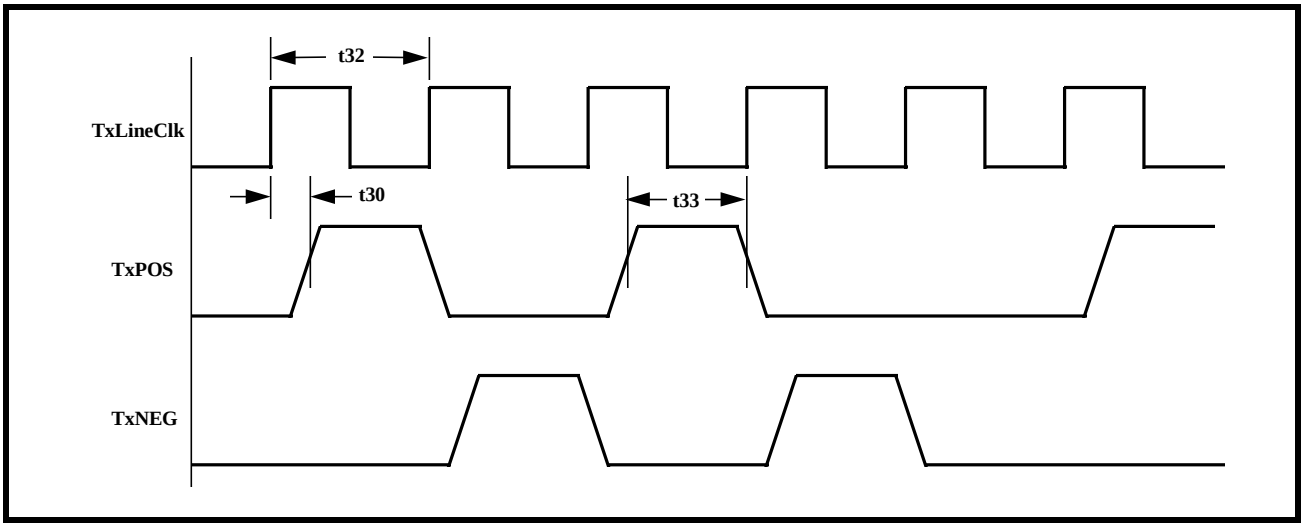
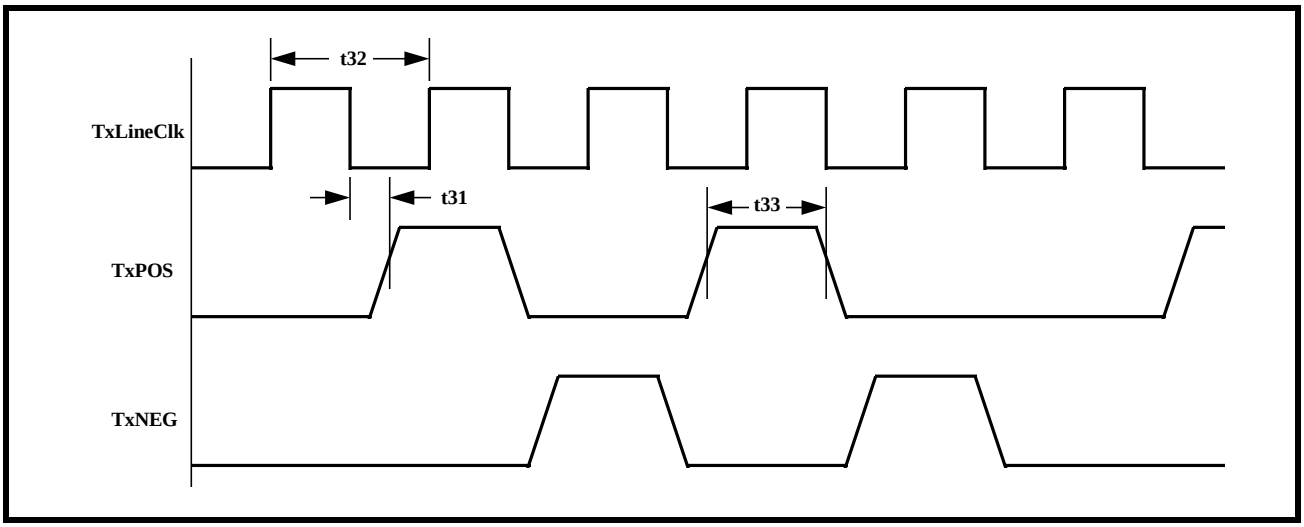


FIGURE 172. WAVEFORM/TIMING RELATIONSHIP BETWEEN TXLINECLK, TXPOS AND TXNEG - TXPOS AND TXNEG ARE CONFIGURED TO BE UPDATED ON THE FALLING EDGE OF TXLINECLK



6.2.6 Transmit Section Interrupt Processing

The Transmit Section of the XRT72L50 can generate an interrupt to the Microprocessor/Microcontroller for the following reasons.

- Completion of Transmission of LAPD Message

6.2.6.1 *Enabling Transmit Section Interrupts*

The Interrupt Structure within the XRT72L50 contains two hierarchical levels:

- Block Level
- Source Level

The Block Level

The Enable State of the Block Level for the Transmit Section Interrupts dictates whether or not interrupts (enabled) at the source level, are actually enabled.

The user can enable or disable these Transmit Section interrupts, at the Block Level by writing the appropriate data into Bit 1 (Tx DS3/E3 Interrupt Enable) within the Block Interrupt Enable register (Address = 0x04), as illustrated below.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One-Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	X	0

Setting this bit-field to “1” enables the Transmit Section (at the Block Level) for Interrupt Generation. Conversely, setting this bit-field to “0” disables the Transmit Section for interrupt generation.

What does it mean for the Transmit Section Interrupts to be enabled or disabled at the Block Level?

If the Transmit Section is disabled (for interrupt generation) at the Block Level, then ALL Transmit Section interrupts are disabled, independent of the interrupt enable/disable state of the source level interrupts.

If the Transmit Section is enabled (for interrupt generation) at the block level, then a given interrupt will be enabled if it is enabled at the source level. Conversely, if the Transmit Section is enabled (for interrupt generation) at the Block level, then a given interrupt will still be disabled, if it is disabled at the source level.

As mentioned earlier, the Transmit Section of the XRT72L50 Framer IC contains the Completion of Transmission of LAPD Message Interrupt.

The Enabling/Disabling and Servicing of this interrupt is presented below.

6.2.6.1.1 The Completion of Transmission of the LAPD Message Interrupt

If the Transmit Section interrupts have been enabled at the Block level, then the user can enable or disable the Completion of Transmission of a LAPD Message Interrupt by writing the appropriate value into Bit 1 (TxLAPD Interrupt Enable) within the Tx E3 LAPD Status & Interrupt Register (Address = 0x34), as illustrated below.

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TXDL Start	TXDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	X	0

Setting this bit-field to “1” enables the Completion of Transmission of a LAPD Message Interrupt. Conversely, setting this bit-field to “0” disables the Completion of Transmission of a LAPD Message interrupt.

6.2.6.1.2 Servicing the Completion of Transmission of a LAPD Message Interrupt

As mentioned previously, once the user commands the LAPD Transmitter to begin its transmission of a LAPD Message, it will do the following.

1. It will compute the FCS (Frame Check Sequence) value over the contents of 0x86 through 0xDB and append this 16 bit value to the back-end of the user-message.
2. It will parse through the contents of the Transmit LAPD Message Buffer (located at address locations 0x86 through 0xDB and the FCS bytes) and search for a string of five (5) consecutive “1’s”. If the LAPD Transmitter finds a string of five consecutive “1’s” (within the content of the LAPD Message Buffer, then it will insert a “0” immediately after this string. (Except at 0x86 which should contain the flag sequence 0x7E.)
3. It will append a trailing flag sequence 0x7E.

4. Finally, it will begin transmitting the contents of this LAPD Message frame via either the NR or GC bytes within each Outbound E3 frame.
5. Once the LAPD Transmitter has completed its transmission of this LAPD Message frame (to the Remote Terminal Equipment), the XRT72L50 Framer IC will generate the Completion of Transmission of a LAPD Message Interrupt to the Microcontroller/Microprocessor. Once the XRT72L50 Framer IC generates this interrupt, it will do the following.

- Assert the Interrupt Output pin ($\overline{Int}$) by toggling it "Low".
- Set Bit 0 (TxLAPD Interrupt Status) within the TxE3 LAPD Status and Interrupt Register, to “1” as illustrated below.

TxE3 LAPD Status and Interrupt Register (Address = 0x34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TXDL Start	TXDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	1

The purpose of this interrupt is to alert the Microcontroller/MIcroprocessor that the LAPD Transmitter has completed its transmission of a given LAPD (or PMDL) Message, and is now ready to transmit the next PMDL Message, to the Remote Terminal Equipment.

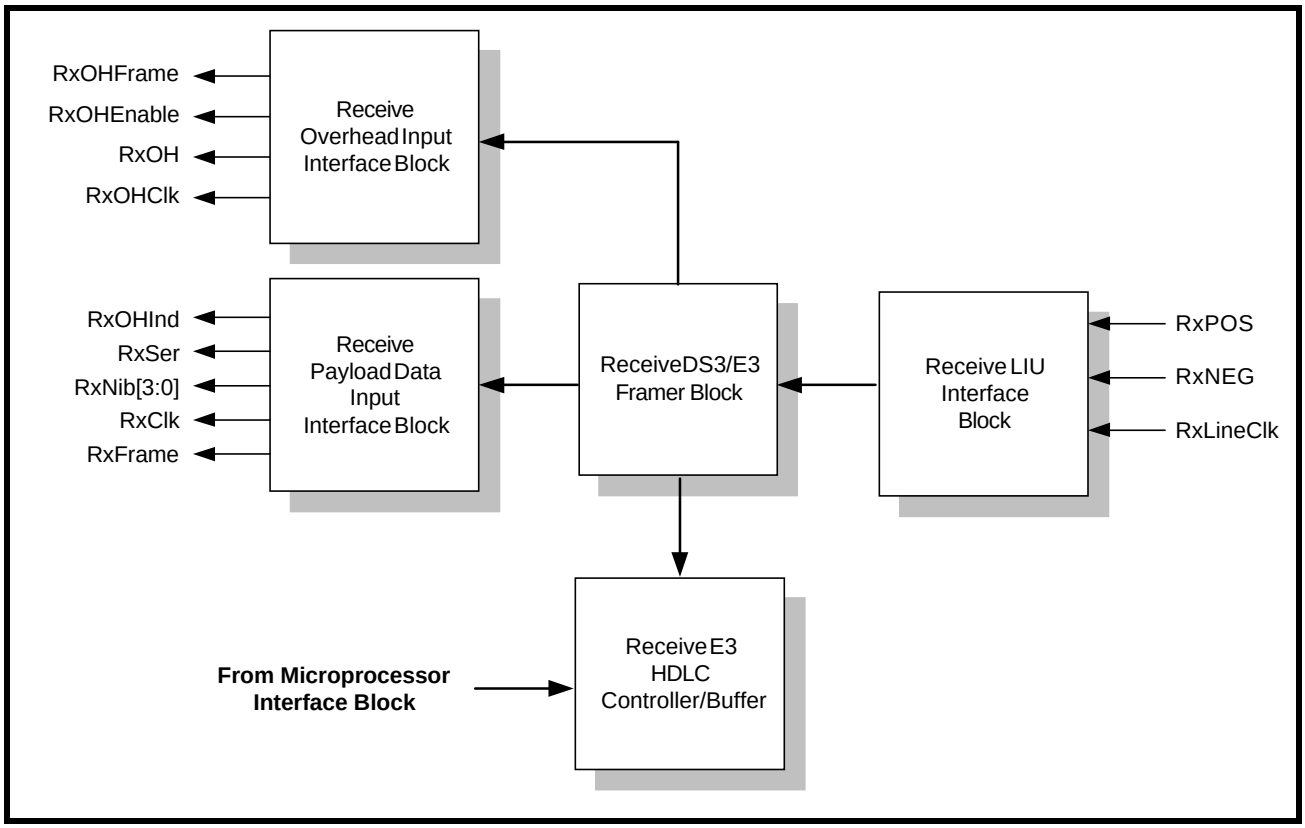
6.3 *The Receive Section of the XRT72L50 (E3 Mode Operation)*

When the XRT72L50 has been configured to operate in the E3 Mode, the Receive Section of the XRT72L50 consists of the following functional blocks.

- Receive LIU Interface block
- Receive HDLC Controller block
- Receive E3 Framer block
- Receive Overhead Data Output Interface block
- Receive Payload Data Output Interface block

Figure 173 presents a simple illustration of the Receive Section of the XRT72L50 Framer IC.

FIGURE 173. THE XRT72L50 RECEIVE SECTION CONFIGURED TO OPERATE IN THE E3 MODE



Each of these functional blocks will be discussed in detail in this document.

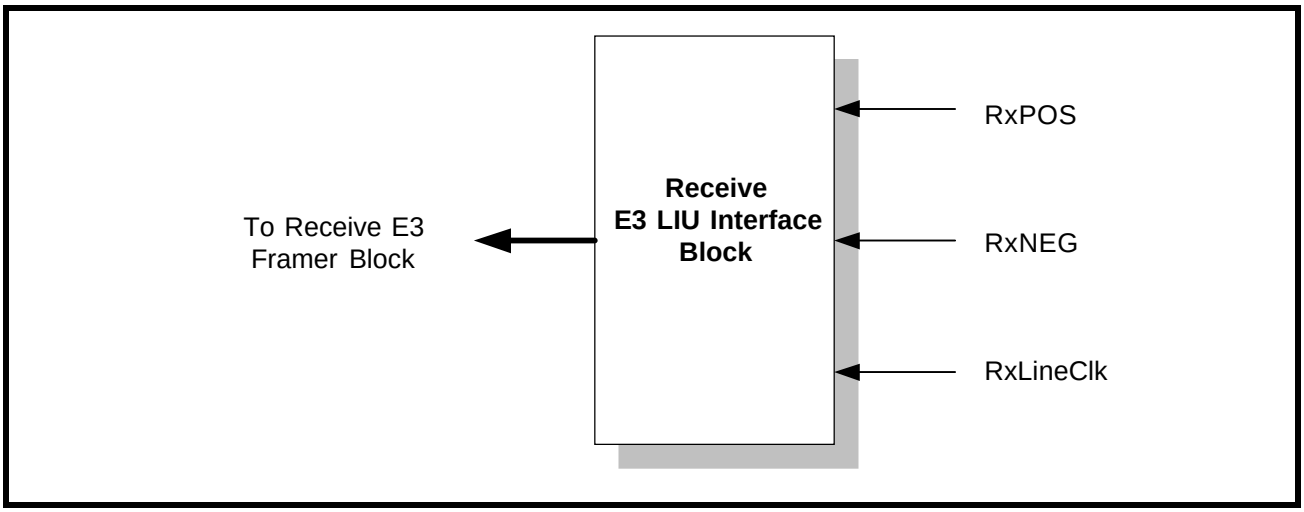
6.3.1 The Receive E3 LIU Interface Block

The purpose of the Receive E3 LIU Interface block is two-fold:

1. To receive encoded digital data from the E3 LIU IC.
2. To decode this data, convert it into a binary data stream and to route this data to the Receive E3 Framer block.

Figure 174 presents a simple illustration of the Receive E3 LIU Interface block.

FIGURE 174. THE RECEIVE E3 LIU INTERFACE BLOCK



The Receive Section of the XRT72L50 will via the Receive E3 LIU Interface Block receive timing and data information from the incoming E3 data stream. The E3 Timing information will be received via the RxLineClk input pin and the E3 data information will be received via the RxPOS and RxNEG input pins. The Receive E3 LIU Interface block is capable of receiving E3 data pulses in unipolar or bipolar format. If the Receive E3 framer is operating in the bipolar format, then it can be configured to decode either AMI or HDB3 line code data. Each of these input formats and line codes will be discussed in detail, below.

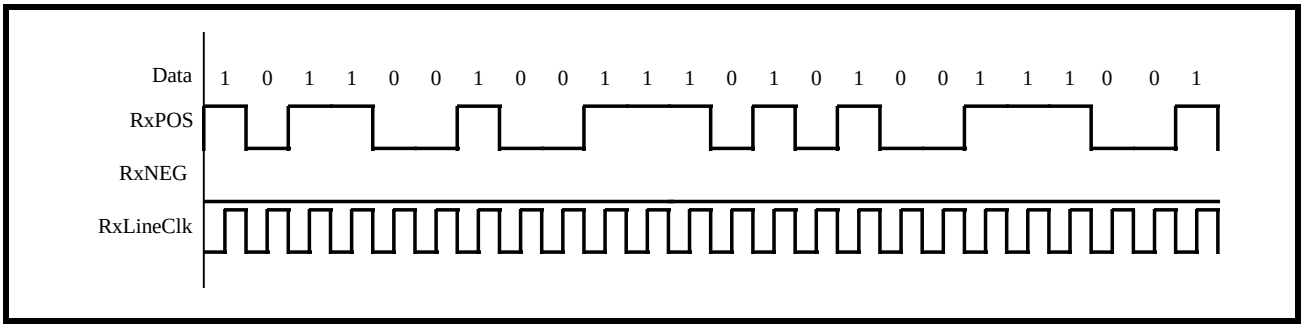
6.3.1.1 *Unipolar Decoding*

If the Receive E3 LIU Interface block is operating in the Unipolar (single-rail) mode, then it will receive the Single Rail NRZ E3 data pulses via the RxPOS input pin. The Receive E3 LIU Interface block will also receive its timing signal via the RxLineClk signal.

NOTE: *The RxLineClk signal will function as the timing source for the entire Receive Section of the XRT72L50.*

No data pulses will be applied to the RxNEG input pin. The Receive E3 LIU Interface block receives a logic "1" when a logic "1" level signal is present at the RxPOS pin, during the sampling edge of the RxLineClk signal. Likewise, a logic "0" is received when a logic "0" level signal is applied to the RxPOS pin. Figure 175 presents an illustration of the behavior of the RxPOS, RxNEG and RxLineClk input pins when the Receive E3 LIU Interface block is operating in the Unipolar mode.

FIGURE 175. BEHAVIOR OF THE RXPOS, RXNEG AND RXLINECLK SIGNALS DURING DATA RECEPTION OF UNIPOLAR DATA



The user can configure the Receive E3 LIU Interface block to operate in either the Unipolar or the Bipolar Mode by writing the appropriate data to the I/O Control Register, as depicted below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 80 relates the value of this bit-field to the Receive E3 LIU Interface Input Mode.

TABLE 80: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 3 (UNIPOLAR/BIPOLAR) WITHIN THE I/O CONTROL REGISTER

BIT 3	RECEIVE E3 LIU INTERFACE INPUT MODE
0	**Bipolar Mode (Dual Rail):** AMI or HDB3 Line Codes are Transmitted and Received.
1	**Unipolar Mode (Single Rail) Mode** of transmission and reception of E3 data is selected.

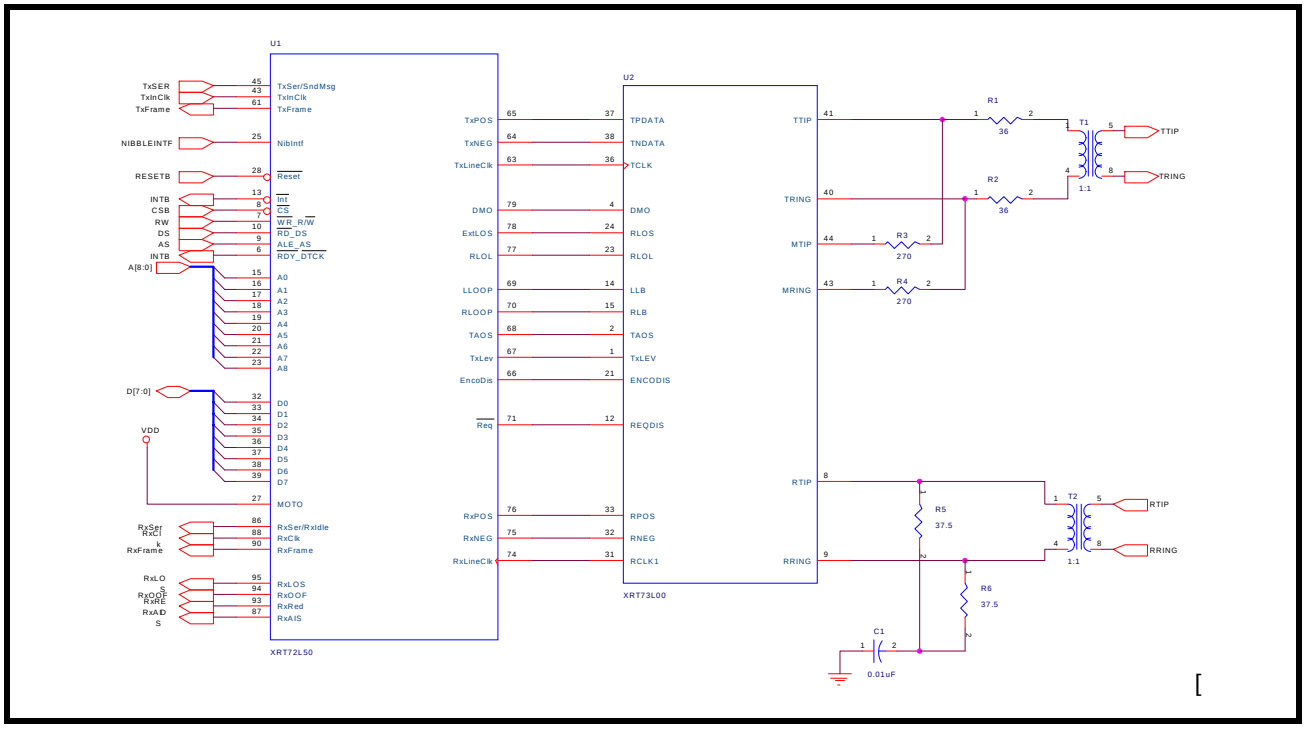
NOTES:

1. *The default condition is the Bipolar Mode.*
2. *This selection also effects the Transmit E3 Framer Line Interface Output Mode.*

6.3.1.2 *Bipolar Decoding*

If the Receive E3 LIU Interface block is operating in the Bipolar Mode, then it will receive the E3 data pulses via both the RxPOS, RxNEG, and the RxLineClk input pins. Figure 176 presents a circuit diagram illustrating how the Receive E3 LIU Interface block interfaces to the Line Interface Unit while the Framer is operating in Bipolar mode. The Receive E3 LIU Interface block can be configured to decode either the AMI or HDB3 line codes.

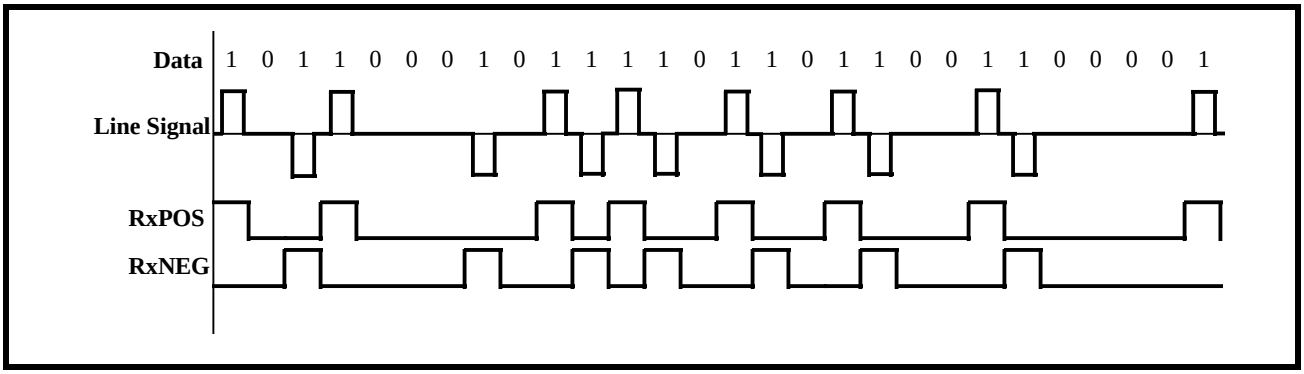
FIGURE 176. INTERFACING THE XRT72L50 FRAMER IC TO THE XRT73L00 DS3/E3/STS-1 LIU



6.3.1.2.1 AMI Decoding

AMI or Alternate Mark Inversion, means that consecutive "one's" pulses (or marks) will be of opposite polarity with respect to each other. This line code involves the use of three different amplitude levels: +1, 0, and -1. The +1 and -1 amplitude signals are used to represent one's (or mark) pulses and the "0" amplitude pulses (or the absence of a pulse) are used to represent zeros (or space) pulses. The general rule for AMI is: if a given mark pulse is of positive polarity, then the very next mark pulse will be of negative polarity and vice versa. This alternating-polarity relationship exists between two consecutive mark pulses, independent of the number of zeros that exist between these two pulses. Figure 177 presents an illustration of the AMI Line Code as would appear at the RxPOS and RxNEG pins of the Framer, as well as the output signal on the line.

FIGURE 177. ILLUSTRATION OF AMI LINE CODE



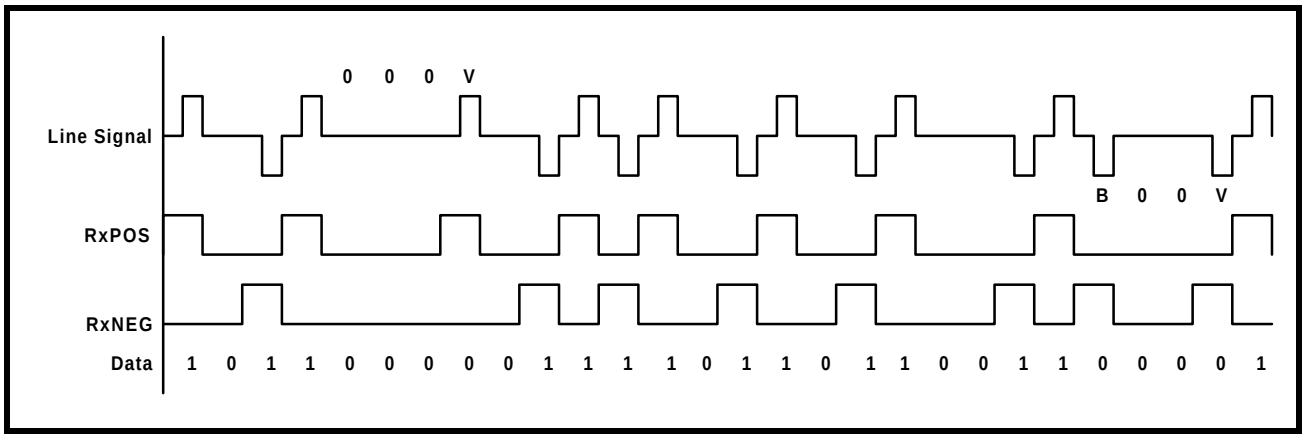
NOTE: *One of the reasons that the AMI Line Code has been chosen for driving copper medium, isolated via transformers, is that this line code has no dc component, thereby eliminating dc distortion in the line.*

6.3.1.2.2 HDB3 Decoding

The Transmit E3 LIU Interface block and the associated LIU embed and combine the data and clocking information into the line signal that is transmitted to the remote terminal equipment. The remote terminal equipment has the task of recovering this data and timing information from the incoming E3 data stream. Most clock and data recovery schemes rely on the use of Phase-Locked-Loop technology. One of the problems of using Phase-Locked-Loop (PLL) technology for clock recovery is that it relies on transitions in the line signal, in order to maintain lock with the incoming E3 data-stream. Therefore, these clock recovery scheme, are vulnerable to the occurrence of a long stream of consecutive zeros (e.g., no transitions in the line). This scenario can cause the PLL to lose lock with the incoming E3 data, thereby causing the clock and data recovery process of the receiver to fail. Therefore, some approach is needed to insure that such a long string of consecutive zeros can never happen. One such technique is HDB3 (or High Density Bipolar -3) encoding.

In general the HDB3 line code behaves just like AMI with the exception of the case when a long string of consecutive zeros occurs on the line. Any 4 consecutive zeros will be replaced with either a "000V" or a "B00V" where "B" refers to a Bipolar pulse (e.g., a pulse with a polarity that is compliant with the AMI coding rule). And "V" refers to a Bipolar Violation pulse (e.g., a pulse with a polarity that violates the alternating polarity scheme of AMI.) The decision between inserting an "000V" or a "B00V" is made to insure that an odd number of Bipolar (B) pulses exist between any two Bipolar Violation (V) pulses. The Receive E3 LIU Interface block, when operating with the HDB3 Line Code is responsible for decoding the HD-encoded data back into a unipolar (binary-format). For instance, if the Receive E3 LIU Interface block detects a "000V" or a "B00V" pattern in the incoming pattern, the Receive E3 LIU Interface block will replace it with four (4) consecutive zeros. Figure 178 presents a timing diagram that illustrates examples of HDB3 decoding.

FIGURE 178. ILLUSTRATION OF TWO EXAMPLES OF HDB3 DECODING



6.3.1.2.3 Line Code Violations

The Receive E3 LIU Interface block will also check the incoming E3 data stream for line code violations. For example, when the Receive E3 LIU Interface block detects a valid bipolar violation (e.g., in HDB3 line code), it will substitute four zeros into the binary data stream. However, if the bipolar violation is invalid, then an LCV (Line Code Violation) is flagged and the PMON LCV Event Count Register (Address = 0x50 and 0x51) will also be incremented. Additionally, the LCV-One-Second Accumulation Registers (Address = 0x6E and 0x6F) will be incremented. For example: If the incoming E3 data is HDB3 encoded, the Receive E3 LIU Interface block will also increment the LCV One-Second Accumulation Register if three (or more) consecutive zeros are received.

6.3.1.2.4 RxLineClk Clock Edge Selection

The incoming unipolar or bipolar data, applied to the RxPOS and the RxNEG input pins are clocked into the Receive E3 LIU Interface block via the RxLineClk signal. The Framer IC allows the user to specify which edge (e.g, rising or falling) of the RxLineClk signal will sample and latch the signal at the RxPOS and RxNEG input signals into the Framer IC. The user can make this selection by writing the appropriate data to bit 1 of the I/O Control Register, as depicted below.

I/O Control Register (Address = 0x01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/$\overline{\text{ZeroSup}}$	Unipolar/ $\overline{\text{Bipolar}}$	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 81 depicts the relationship between the value of this bit-field to the sampling clock edge of RxLineClk.

TABLE 81: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 1 (RXLINECLK INV) OF THE I/O CONTROL REGISTER, AND THE SAMPLING EDGE OF THE RXLINECLK SIGNAL

RXLINECLK (BIT 1)	RESULT
0	**Rising Edge:** RxPOS and RxNEG are sampled at the rising edge of RxLineClk. See Figure 179 for timing relationship between RxLineClk, RxPOS, and RxNEG.
1	**Falling Edge:** RxPOS and RxNEG are sampled at the falling edge of RxLineClk. See Figure 180 for timing relationship between RxLineClk, RxPOS, and RxNEG.

Figure 179 and Figure 180 present the Waveform and Timing Relationships between RxLineClk, RxPOS and RxNEG for each of these configurations.

FIGURE 179. WAVEFORM/TIMING RELATIONSHIP BETWEEN RXLINECLK, RXPOS AND RXNEG - WHEN RXPOS AND RXNEG ARE TO BE SAMPLED ON THE RISING EDGE OF RXLINECLK

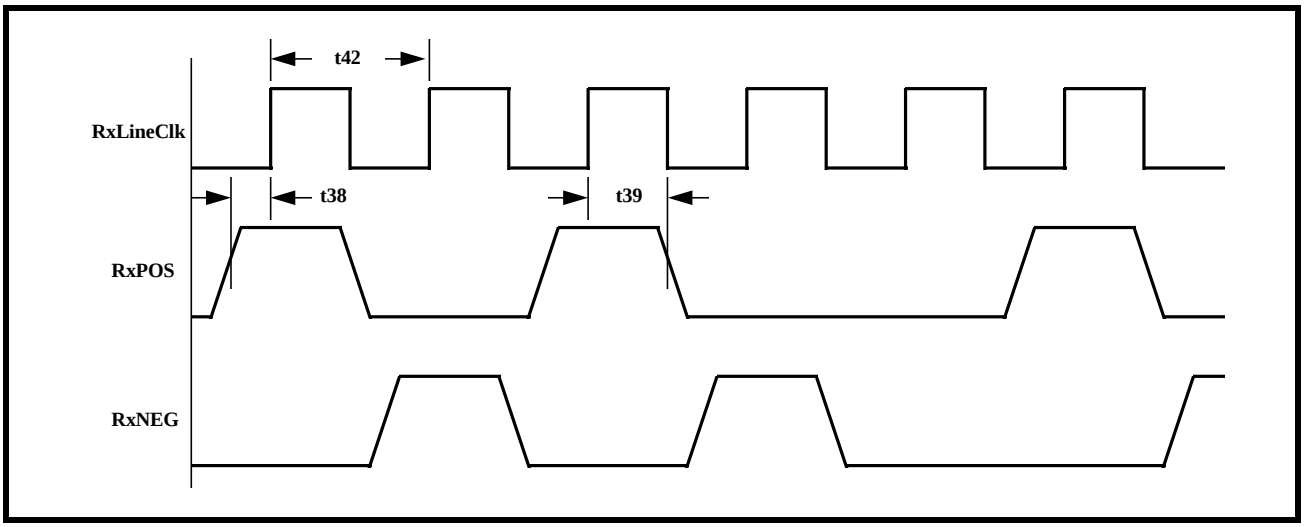
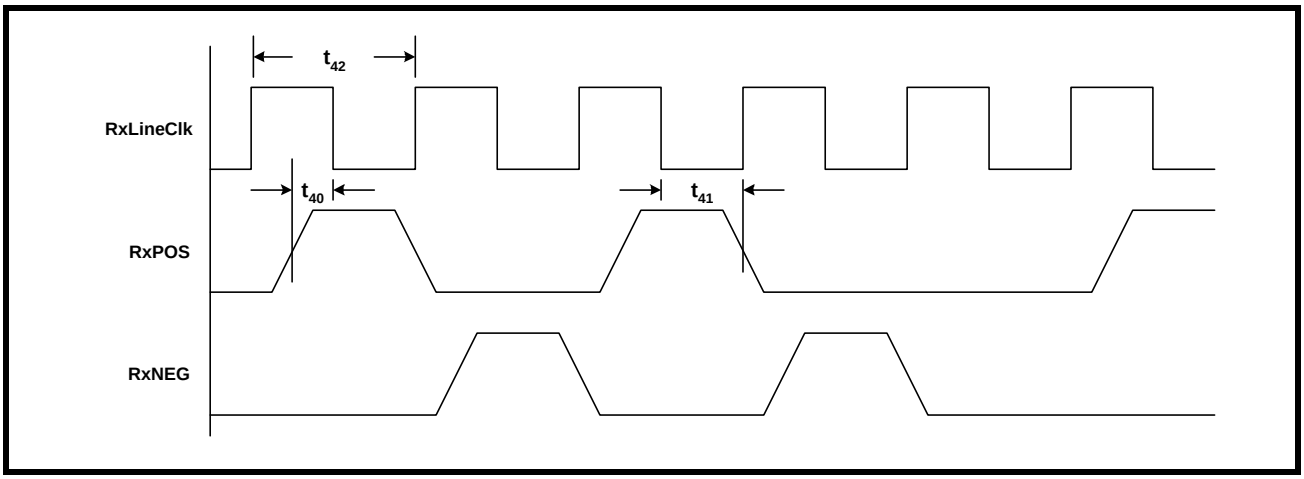


FIGURE 180. WAVEFORM/TIMING RELATIONSHIP BETWEEN RXLINECLK, RXPOS AND RXNEG - WHEN RXPOS AND RXNEG ARE TO BE SAMPLED ON THE FALLING EDGE OF RXLINECLK



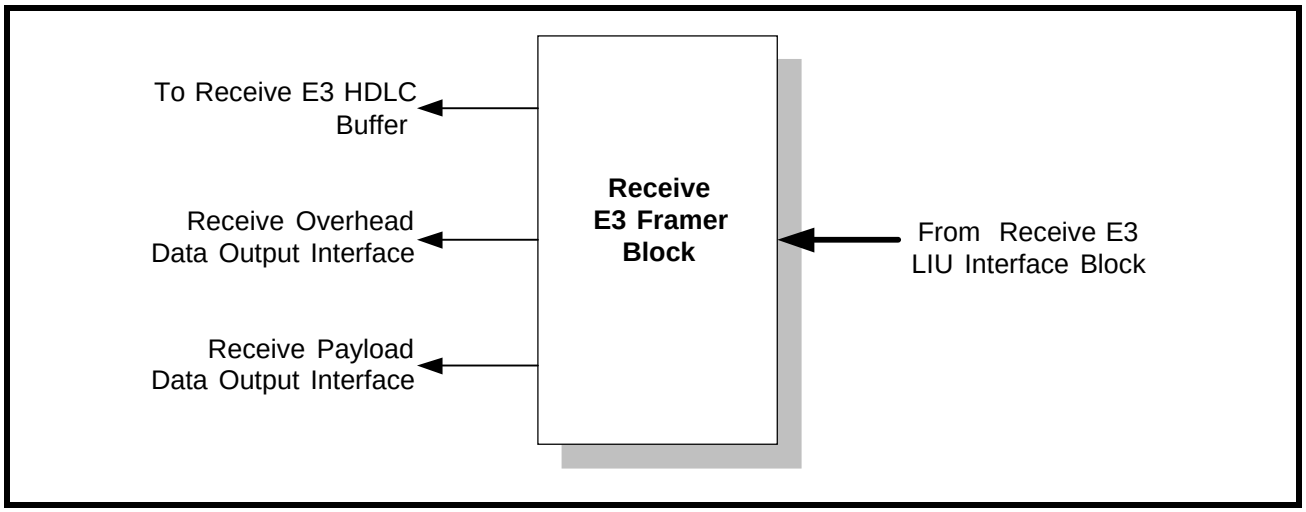
6.3.2 The Receive E3 Framer Block

The Receive E3 Framer block accepts decoded E3 data from the Receive E3 LIU Interface block, and routes data to the following destinations.

- The Receive Payload Data Output Interface Block
- The Receive Overhead Data Output Interface Block.
- The Receive E3 HDLC Controller Block

Figure 181 presents a simple illustration of the Receive E3 Framer block, along with the associated paths to the other functional blocks within the Framer chip.

FIGURE 181. THE RECEIVE E3 FRAMER BLOCK AND THE ASSOCIATED PATHS TO OTHER FUNCTIONAL BLOCKS



Once the HDB3 (or AMI) encoded data has been decoded into a binary data-stream, the Receive E3 Framer block will use portions of this data-stream in order to synchronize itself to the remote terminal equipment. At any given time, the Receive E3 Framer block will be operating in one of two modes.

- **The Frame Acquisition Mode:** In this mode, the Receive E3 Framer block is trying to acquire synchronization with the incoming E3 frame, or
- **The Frame Maintenance Mode:** In this mode, the Receive E3 Framer block is trying to maintain frame synchronization with the incoming E3 Frames.

Figure 182 presents a State Machine diagram that depicts the Receive E3 Framer block's E3/ITU-T G.832 Frame Acquisition/Maintenance Algorithm.

6.3.2.1 *The Framing Acquisition Mode*

The Receive E3 Framer block is considered to be operating in the Frame Acquisition Mode, if it is operating in any one of the following states within the E3 Frame Acquisition/Maintenance Algorithm per Figure 182.

- FA1, FA2 Octet Search State
- FA1, FA2 Octet Verification State
- OOF Condition State
- LOF Condition State

Each of these Framing Acquisition states, within the Receive E3 Framer Framing Acquisition/Maintenance State Machine are discussed below.

The FA1, FA2 Octet Search State

When the Receive E3 Framer block is first powered up, it will be operating in the FA1, FA2 Octet Search state. While the Receive E3 Framer is operating in this state, it will be performing a bit-by-bit search for the FA1 and

FA2 Framing Alignment octets. FA1 is assigned the value 0xF6, and FA2 is assigned the value of 0x28. Figure 183, which presents an illustration of the E3, ITU-T G.832 Framing Format, indicates that these two octets will occur at the beginning of each E3 frame, and that the FA2 octet will appear immediately after the FA1 octet.

FIGURE 182. THE STATE MACHINE DIAGRAM FOR THE RECEIVE E3 FRAMER E3 FRAME ACQUISITION/MAINTENANCE ALGORITHM

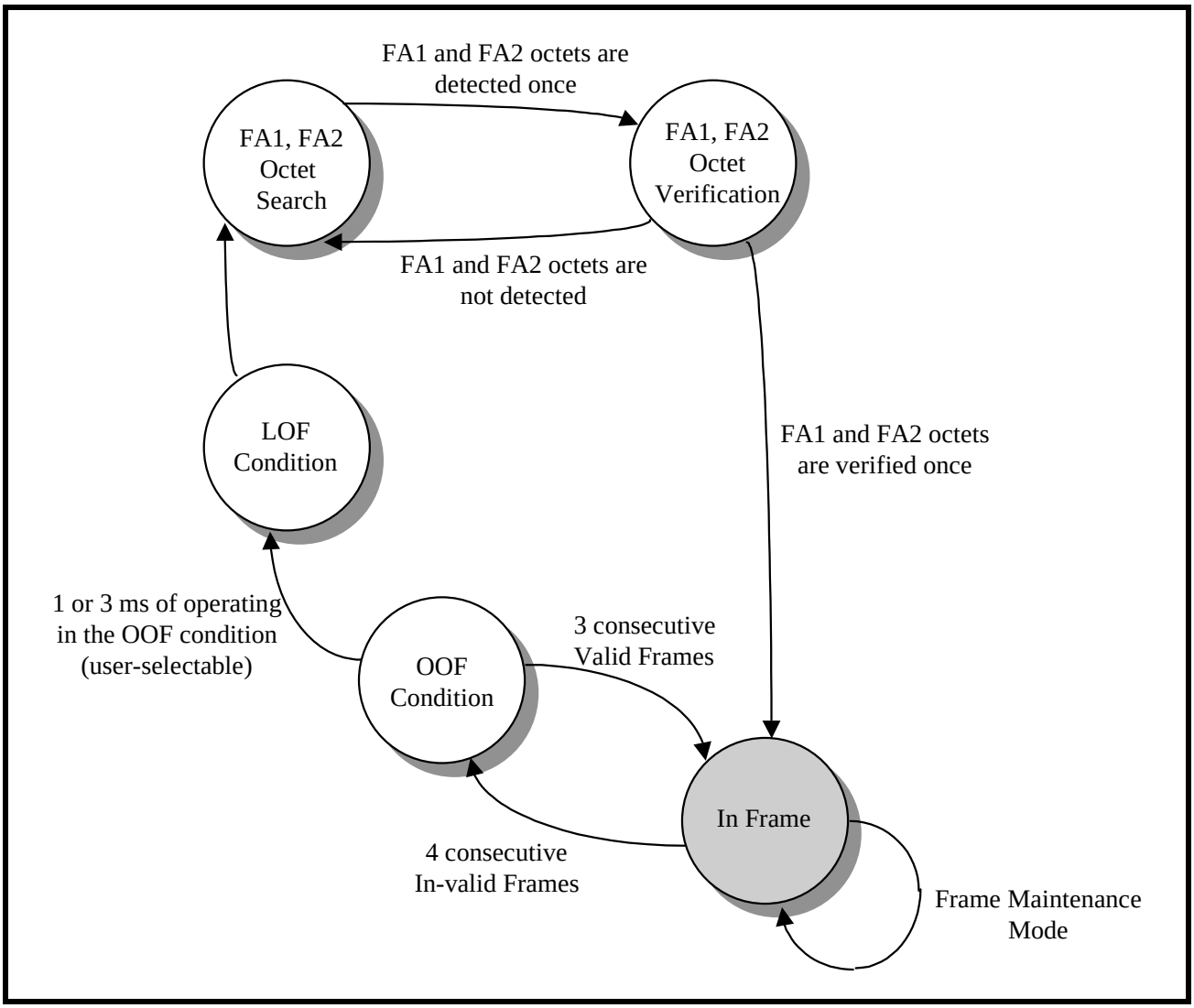
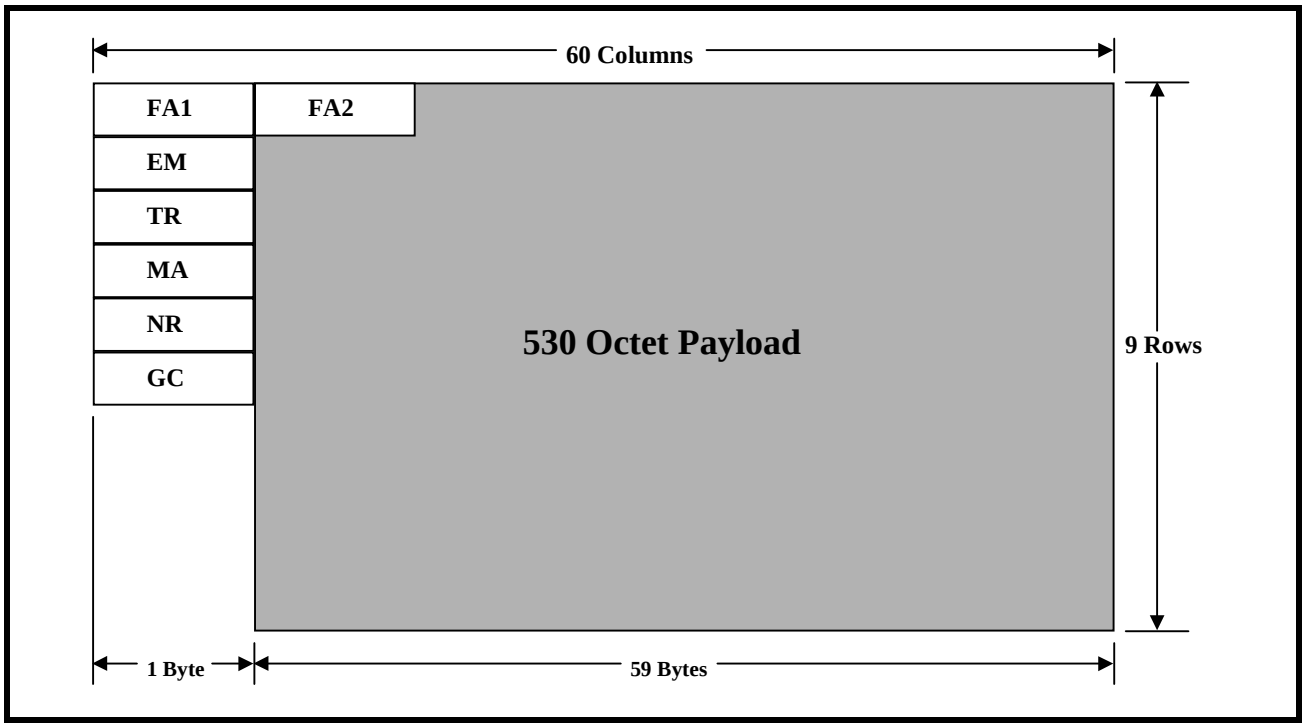


FIGURE 183. ILLUSTRATION OF THE E3, ITU-T G.832 FRAMING FORMAT



When the Receive E3 Framer block detects the FA1 octet, and determines that this octet is immediately followed by the FA2 octet, then it will transition to the FA1, FA2 Octet Verification state, per Figure 183.

The FA1, FA2 Octet Verification State

Once the Receive E3 Framer block has detected an 0xF628 pattern (e.g., the concatenation of the FA1 and FA2 octets), it must verify that this pattern is indeed the FA1 and FA2 octets and not some other set of bytes, within the E3 frame, mimicking the Frame Alignment bytes. Hence, the purpose of the FA1, FA2 Octet Verification state.

When the Receive E3 Framer block enters this state, it will then quit performing its bit-by-bit search for the Frame Alignment bytes. Instead, the Receive E3 Framer block will read in the two octets that occur 537 bytes (e.g., one E3 frame period later) after the candidate Frame Alignment patterns were first detected. If these two bytes match the assigned values for the FA1 and FA2 octets, then the Receive E3 Framer block will conclude that it has found the Frame Alignment bytes and will then transition to the In-Frame state. However, if these two bytes do not match the assigned values for the FA1 and FA2 octets then the Receive E3 Framer block will concluded that it has been fooled by data mimicking the Frame Alignment bytes, and will transition back to the FA1, FA2 Octet Search state.

In Frame State

Once the Receive E3 Framer block enters the In-Frame state, then it will cease performing Frame Acquisition functions, and will proceed to perform Framing Maintenance functions. Therefore, the operation of the Receive E3 Framer block, while operating in the In-Frame state, can be found in Section 5.3.2.2 (The Framing Maintenance Mode).

OOF (Out of Frame) Condition State

If the Receive E3 Framer while operating in the In-Frame state detects four (4) consecutive frames, which do not have the valid Frame Alignment (FA1 and FA2 octet) patterns, then it will transition into the OOF Condition State. The Receive E3 Framer block's operation, while in the OOF condition state is a unique mix of Framing Maintenance and Framing Acquisition operation. The Receive E3 Framer block will exhibit some Framing Acquisition characteristics by attempting to locate (once again) the Frame Alignment octets. However, the

Receive E3 Framer block will also exhibit some Frame Maintenance behavior by still using the most recent frame synchronization for its overhead byte and payload byte processing.

The Receive E3 Framer block will inform the Microprocessor/Microcontroller of its transition from the In-Frame state to the OOF Condition state, by generating a Change in OOF Condition Interrupt. When this occurs, Bit 3 (OOF Interrupt Status), within the Rx E3 Interrupt Status Register - 1, will be set to "1", as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

The Receive E3 Framer block will also inform the external circuitry of its transition into the OOF Condition state, by toggling the RxOOF output pin "High".

If the Receive E3 Framer block is capable of finding the Framing Alignment octets within a user-selectable number of E3 frame periods, then it will transition back into the In-Frame state. The Receive E3 Framer block will then inform the Microprocessor/Microcontroller of its transition back into the In-Frame state by generating the Change in OOF Condition Interrupt.

However, if the Receive E3 Framer block resides in the OOF Condition state for more than this user-selectable number of E3 frame periods, then it will automatically transition to the LOF (Loss of Frame) Condition state.

The user can select this user-selectable number of E3 frame periods that the Receive E3 Framer block will remain in the OOF Condition state by writing the appropriate value into Bit 7 (RxLOF Algo) within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	1	1	1	1	1

Writing a "0" into this bit-field causes the Receive E3 Framer block to reside in the OOF Condition state for at most 24 E3 frame periods (3 ms). Writing a "1" into this bit-field causes the Receive E3 Framer block to reside in the OOF Condition state for at most 8 E3 frame periods (1 ms).

LOF (Loss of Framing) Condition State

If the Receive E3 Framer block enters the LOF Condition state, then the following things will happen.

- The Receive E3 Framer block will discard the most recent frame synchronization and
- The Receive E3 Framer block will make an unconditional transition to the FA1, FA2 Octet Search state.
- The Receive E3 Framer block will notify the Microprocessor/Microcontroller of its transition to the LOF Condition state, by generating the Change in LOF Condition interrupt. When this occurs, Bit 2 (LOF Interrupt Status), within the Rx E3 Interrupt Status Register - 1 will be set to "1", as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

Finally, the Receive E3 Framer block will also inform the external circuitry of this transition to the LOF Condition state by toggling the RxLOF output pin "High".

6.3.2.2 *The Framing Maintenance Mode*

Once the Receive E3 Framer block enters the In-Frame state, then it will notify the Microprocessor/ Microcontroller of this fact by generating both the Change in OOF Condition and Change in LOF Condition Interrupts. When this happens, bits 2 and 3 (LOF Interrupt Status and OOF Interrupt Status) will be set to “1”, as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	1	0	0

Additionally, the Receive E3 Framer block will inform the external circuitry of its transition to the In-Frame state by toggling both the RxOOF and RxLOF output pins "Low”.

Finally, the Receive E3 Framer block will negate both the RxOOF and the RxLOF bit-fields within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

When the Receive E3 Framer block is operating in the In-Frame state, it will then begin to perform Frame Maintenance operations, where it will continue to verify that the Frame Alignment octets (FA1, FA2) are present, at their proper locations. While the Receive E3 Framer block is operating in the Frame Maintenance Mode, it will declare an Out-of-Frame (OOF) Condition if it detects invalid Framing Alignment bytes in four consecutive frames.

Since the Receive E3 Framer block requires the detection of invalid Frame Alignment bytes in four consecutive frames, in order for it to transition to the OOF Condition state, it can tolerate some errors in the Framing Alignment bytes, and still remain in the In-Frame state. However, each time the Receive E3 Framer block

detects an error in the Frame Alignment bytes, it will increment the PMON Framing Error Event Count Registers (Address = 0x52 and 0x53). The bit-format for these two registers are depicted below.

PMON Framing Bit/Byte Error Count Register - MSB (Address = 0x52)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit/Byte Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON Framing Bit/Byte Error Count Register - LSB (Address = 0x53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit/Byte Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

6.3.2.3 *Forcing a Reframe via Software Command*

The XRT72L50 Framer IC permits the user to command a reframe procedure with the Receive E3 Framer block via software command. If the user writes a “1” into Bit 0 (Reframe) within the I/O Control Register (Address = 0x01), as depicted below, then the Receive E3 Framer block will be forced into the FA1, FA2 Octet Search state, per Figure 182, and will begin its search for the FA1 and FA2 octets.)

I/O CONTROL REGISTER (ADDRESS = 0X01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ ZeroSup*	Unipolar/ Bipolar*	TxLine Clk Invert	RxLine Clk Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	1

The Framer IC will respond to this command by doing the following.

1. Asserting both the RxOOF and RxLOF output pins.
2. Generating both the Change in OOF Status and the Change in LOF Status interrupts to the Microprocessor.
3. Asserting both the RxLOF and RxOOF bit-fields within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	1	1	1	1	1	1	1

6.3.2.4 *Performance Monitoring of the Frame Synchronization Section, within the Receive E3 Framer block*

The user can monitor the number of framing bytes (FA1 and FA2 bytes) errors that have been detected by the Receive E3 Framer block. This is accomplished by periodically reading the PMON Framing Bit/Byte Error Event Count Registers (Address = 0x52 and 0x53). The byte format of these registers are presented in Section 6.3.2.2.

6.3.2.5 *The RxOOF and RxLOF output pin.*

The user can roughly determine the current framing state that the Receive E3 Framer block is operating in by reading the logic state of the RxOOF and the RxLOF output pins. Table 82 presents the relationship between the state of the RxOOF and RxLOF output pins, and the Framing State of the Receive E3 Framer block.

TABLE 82: THE RELATIONSHIP BETWEEN THE LOGIC STATE OF THE RXOOF AND RXLOF OUTPUT PINS, AND THE FRAMING STATE OF THE RECEIVE E3 FRAMER BLOCK

RXLOF	RXOOF	FRAMING STATE OF THE RECEIVE E3 FRAMER BLOCK
0	0	In Frame
0	1	OOF Condition (The Receive E3 Framer block is operating in the 3ms OOF period).
1	0	Invalid
1	1	LOF Condition

6.3.2.6 *E3 Receive Alarms*

6.3.2.6.1 The Loss of Signal (LOS) Alarm

Declaring an LOS Condition

The Receive E3 Framer block will declare a Loss of Signal (LOS) Condition, when it detects 32 consecutive incoming “0’s” via the RxPOS and RxNEG input pins or if the ExtLOS input pin (from the XRT73L00 DS3/E3/STS-1 LIU IC) is asserted. In this case, the internally-generated LOS criteria of 180 consecutive “zeros” will be disabled. This can be accomplished by writing a "0" to bit 5 (Internal LOS Enable) of the Framer Operating Mode Register, as depicted below.

Framer Operating Mode Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back	DS3/E3	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	1	0	X	X	X	X	X

The Receive E3 Framer block will indicate that it is declaring an LOS condition by.

- Asserting the RxLOS output pin (e.g., toggling it "High").

- Setting Bit 4 (RxLOS) of the Rx E3 Configuration & Status Register to “1” as depicted below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	0	0	1	0	0	0	0

- The Receive E3 Framer block will generate a Change in LOS Condition interrupt request. Upon generating this interrupt request, the Receive E3 Framer block will assert Bit 1 (LOS Interrupt Status within the Rx E3 Framer Interrupt Status Register - 1, as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	1	0

Clearing the LOS Condition

The Receive E3 Framer block will clear the LOS condition when it encounters a stream of 32 bits that does not contain a string of 4 consecutive zeros or if the ExtLOS pin goes low.

When the Receive E3 Framer block clears the LOS condition, then it will notify the Microprocessor and the external circuitry of this occurrence by:

- Generating the Change in LOS Condition Interrupt to the Microprocessor.
- Clearing Bit 4 (RxLOS) within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

- Clear the RxLOS output pin (e.g., toggle it "Low”).

6.3.2.6.2 The AIS (Alarm Indication Status) Condition

Declaring the AIS Condition

The Receive E3 Framer block will identify and declare an AIS condition, if it detects an “All Ones” pattern in the incoming E3 data stream. More specifically, the Receive E3 Framer block will declare an AIS Condition if 7 or less “0s” are detected in each of 2 consecutive E3 frames.

If the Receive E3 Framer block declares an AIS Condition, then it will do the following.

- Generate the Change in AIS Condition Interrupt to the Microprocessor. Hence, the Receive E3 Framer block will assert Bit 0 (AIS Interrupt Status) within the Rx E3 Framer Interrupt Status register - 1, as depicted below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	1

- Assert the RxAIS output pin.
- Set Bit 3 (Rx AIS) within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	1	0	0	0

Clearing the AIS Condition

The Receive E3 Framer block will clear the AIS condition when it detects two consecutive E3 frames, with eight or more zeros in the incoming data stream. The Receive E3 Framer block will inform the Microprocessor that the AIS Condition has been cleared by:

- Generating the Change in AIS Condition Interrupt to the Microprocessor. Hence, the Receive E3 Framer block will assert Bit 0 (AIS Interrupt Status) within the Rx E3 Framer Interrupt Status Register - 1.
- Clearing the RxAIS output pin (e.g., toggling it "Low").
- Setting the RxAIS bit-field, within the Rx E3 Configuration & Status Register to “0”, as depicted below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

6.3.2.6.3 The Far-End-Receive Failure (FERF) Condition

Declaring the FERF Condition

The Receive E3 Framer block will declare a Far-End Receive Failure (FERF) condition if it detects a user-selectable number of consecutive incoming E3 frames, with the FERF bit-field (Bit 7, within the MA Byte) set to “1”. Recall, the bit-format of the MA byte is presented below.

The Maintenance and Adaptation (ma) byte format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FERF	FEBE	Payload Type			Payload Dependent		Timing Marker

This User-selectable number of E3 frames is either 3 or 5, depending upon the value that has been written into Bit 4 (Rx FERF Algo) within the Rx E3 Configuration & Status Register, as depicted below.

RxE3 Configuration & Status Register 1 - (E3, ITU-T G.832) (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxPLDType[2:0]			RxFERF Algo	RxTMark Algo	RxPLDExp[2:0]		
RO	RO	RO	R/W	R/W	RO	RO	RO
0	0	0	0	0	0	0	0

Writing a “0” into this bit-field causes the Receive E3 Framer block to declare a FERF condition, if it detects 3 consecutive incoming E3 frames, that have the FERF bit (within the MA byte) set to “1”.

Writing a “1” into this bit-field causes the Receive E3 Framer block to declare a FERF condition, if it detects 5 consecutive incoming E3 frames, that have the FERF bit (within the MA byte) set to “1”.

Whenever the Receive E3 Framer block declares a FERF condition, then it will do the following.

- Generate a Change in FERF Condition interrupt to the MIcroprocessor. Hence, the Receive E3 Framer block will assert Bit 3 (FERF Interrupt Status) within the Rx E3 Framer Interrupt Status register - 2, as depicted below.

RxE3 Interrupt Status Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

- Set the Rx FERF bit-field, within the Rx E3 Configuration/Status Register to “1”, as depicted below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	1

Clearing the FERF Condition

The Receive E3 Framer block will clear the FERF condition once it has received a User-Selectable number of E3 frames is either 3 or 5 depending upon the value that has been written into Bit 4 (Rx FERF Algo) of the Rx E3 Configuration/Status Register, as discussed above.

Whenever the Receive E3 Framer clears the FERF status, then it will do the following:

1. Generate a Change in the FERF Status Interrupt to the Microprocessor.
2. Clear the Bit 0 (RxFERF) within the Rx E3 Configuration & Status register, as depicted below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

6.3.2.7 *Error Checking of the Incoming E3 Frames*

The Receive E3 Framer block performs error-checking on the incoming E3 frame data that it receives from the Remote Terminal Equipment. It performs this error-checking by computing the BIP-8 value of an incoming E3 frame. Once the Receive E3 Framer block has obtained this value, it will compare this value with that of the EM byte that it receives, within the very next E3 frame. If the locally computed BIP-8 value matches the EM byte of the corresponding E3 frame, then the Receive E3 Framer block will conclude that this particular frame has been properly received. The Receive E3 Framer block will then inform the Remote Terminal Equipment of this fact by having the Local Terminal Equipment Transmit E3 Framer block send the Remote Terminal an E3 frame, with the FEBE bit-field, within the MA byte, set to “0”.

This procedure is illustrated in Figure 184 and Figure 185.

Figure 184 illustrates the Local Receive E3 Framer receiving an error-free E3 frame. In this figure, the locally computed BIP-8 value of 0x5A matches that received from the Remote Terminal, within the EM byte-field. Figure 185 illustrates the subsequent action of the Local Transmit E3 Framer block, which will transmit an E3 frame to the Remote Terminal, with the FEBE bit-field set to “0” . This signaling indicates that the Local Receive E3 Framer has received an error-free E3 frame.

FIGURE 184. ILLUSTRATION OF THE LOCAL RECEIVE E3 FRAMER BLOCK, RECEIVING AN E3 FRAME (FROM THE REMOTE TERMINAL) WITH A CORRECT EM BYTE.

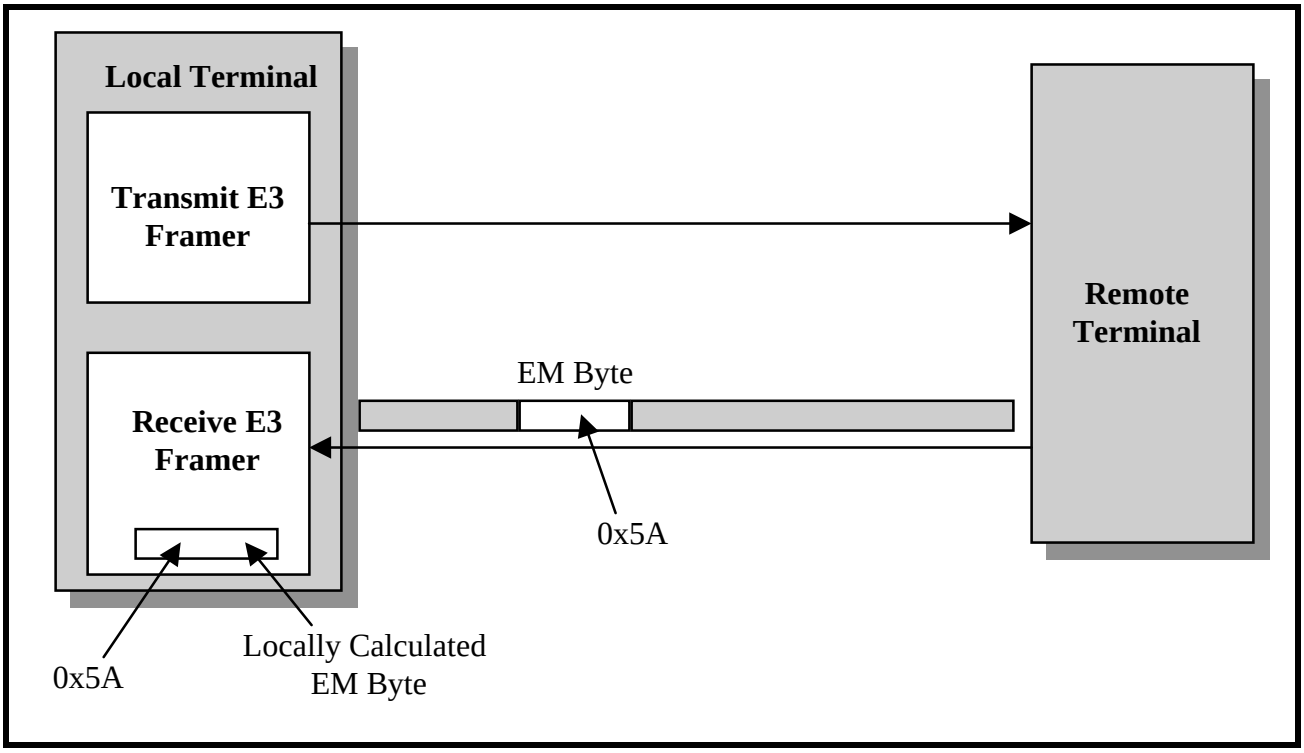
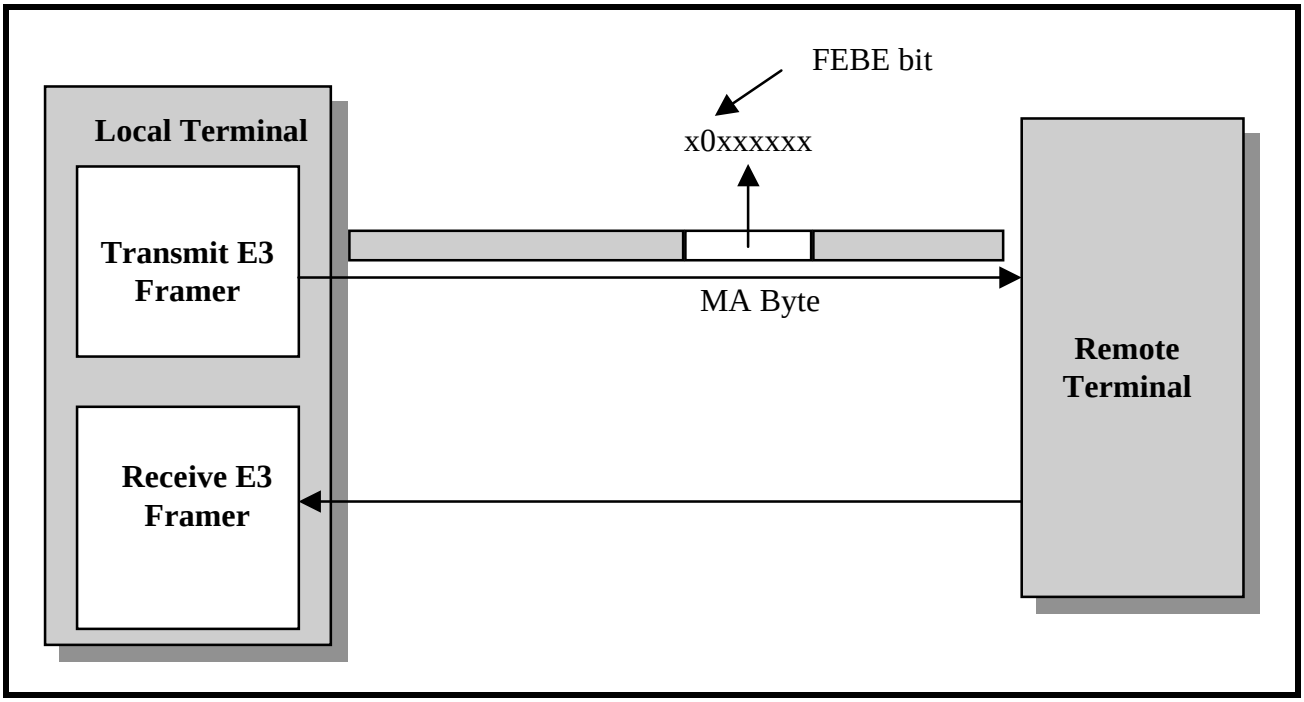


FIGURE 185. ILLUSTRATION OF THE LOCAL RECEIVE E3 FRAMER BLOCK, TRANSMITTING AN E3 FRAME (TO THE REMOTE TERMINAL) WITH THE FEBE BIT (WITHIN THE MA BYTE-FIELD) SET TO "0"



However, if the locally computed BIP-8 value does not match the EM byte of the corresponding E3 frame, then the Receive E3 Framer block will do the following.

- It will inform the Remote Terminal of this fact by having the Local Transmit E3 Framer block send the Remote Terminal an E3 frame, with the FEBE bit-field, within the MA byte, set to "1". This phenomenon is illustrated below in Figure 186 and Figure 187.

Figure 186 illustrates the Local Receive E3 Framer receiving an errored E3 frame. In this figure, the Local Receive E3 Frame block is receiving an E3 frame with an EM byte containing the value 0x5A. This value does not match the locally computed EM byte value of 0x5B. Consequently, there is an error in this E3 frame.

Figure 187 illustrates the subsequent action of the Local Transmit E3 Framer block, which will transmit an E3 frame, with the FEBE bit-field set to "1" to the Remote Terminal. This signaling indicates that the Local Receive E3 Framer block has received an errored E3 frame.

FIGURE 186. ILLUSTRATION OF THE LOCAL RECEIVE E3 FRAMER BLOCK, RECEIVING AN E3 FRAME (FROM THE REMOTE TERMINAL) WITH AN INCORRECT EM BYTE.

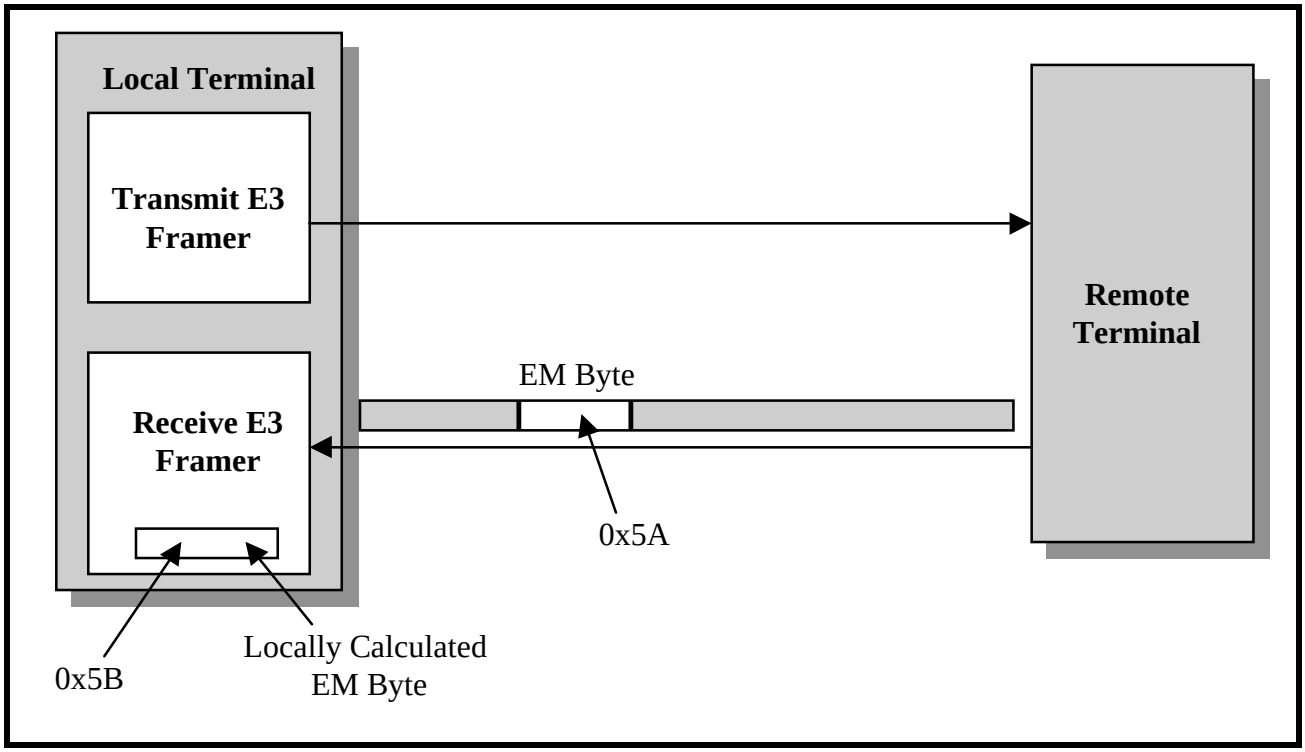
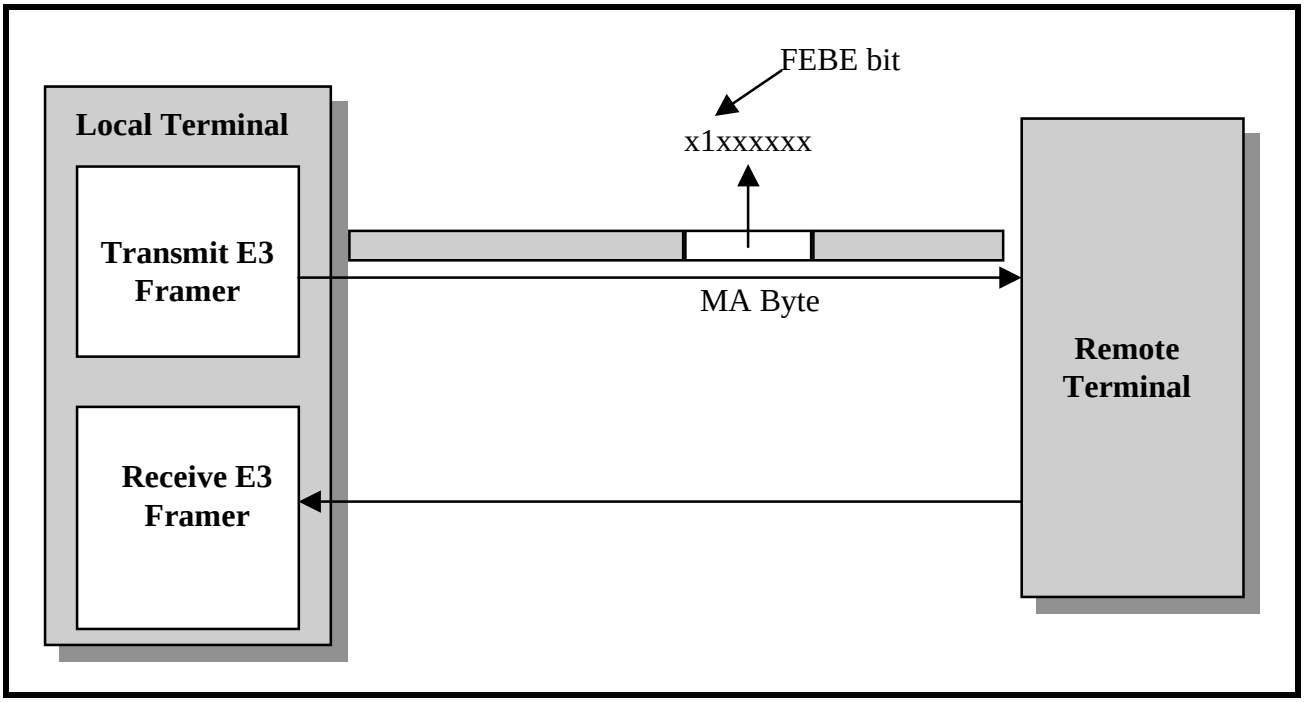


FIGURE 187. ILLUSTRATION OF THE LOCAL RECEIVE E3 FRAMER BLOCK, TRANSMITTING AN E3 FRAME (TO THE REMOTE TERMINAL) WITH THE FEBE BIT (WITHIN THE MA BYTE-FIELD) SET TO "1"



In additional to the FEBE bit-field signaling, the Receive E3 Framer block will generate the BIP-8 Error Interrupt to the Microprocessor. Hence, it will set bit 2 (BIP-8 Error Interrupt Status) to "1", as depicted below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

Finally, the Receive E3 Framer block will increment the PMON Parity Error Count registers. The byte format of these registers are presented below.

PMON Parity Error Count Register - MSB (Address = 0x54)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Parity Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON Parity Error Count Register - LSB (Address = 0x55)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Parity Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

The user can determine the number of BIP-8 Errors that have been detected by the Receive E3 Framer block, since the last read of these registers. These registers are reset-upon-read.

6.3.2.8 *Processing of the Far-End-Block Error (FEBE) Bit-fields*

Whenever the Receive E3 Framer detects an error in the incoming E3 frame, via EM byte verification, it will inform the Local Transmit E3 Framer of this fact. The Local Transmit E3 Framer will, in turn, notify the Remote Terminal (e.g., the source of the errored E3 frame) by transmitting an E3 frame, with the FEBE bit-field (within the MA byte) set to "1".

If the Receive E3 Framer receives any E3 frame, with the FEBE bit-field set to "1", then it will do the following.

- It will generate a FEBE Event interrupt to the Microprocessor/Microcontroller. Hence, the Receive E3 Framer block will set bit 4 (FEBE Interrupt Status) within the Rx E3 Framer Interrupt Status Register - 2, as depicted below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	1	0	0	0	0

- Increment the PMON Received FEBE Event Count register - MSB/LSB, which is located at 0x56 and 0x57 in the Framer Address space. The byte-format of these registers are presented below.

PMON FEBE Event Count Register - MSB (Address = 0x56)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FEBE Event Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON FEBE Event Count Register - LSB (Address = 0x57)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FEBE Event Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

The user can determine the total number of FEBE Events (e.g., E3 frames that have been received with the FEBE bit-field set to "1") that have occurred since the last read of this register. This register is reset-upon-read.

6.3.2.9 *Receiving the Trail Trace Buffer Messages*

The XRT72L50 Framer IC contains 16 bytes worth of Transmit Trail Trace Buffers, and 16 bytes worth of Receive Trail Trace Buffers, as described below. The role of the Transmit Trail Trace Buffers are described in Section 6.1.1.3 and Section 6.2.4.2.2.

The XRT72L50 DS3/E3 Framer IC contains 16 Receive Trail Trace Buffer registers (e.g., RxTTB-0 through RxTTB-15). The purpose of these registers are to receive and store the incoming Trail Access Point Identifier from the Remote Transmitting Terminal.

The Local Receiving Terminal will use this information to verify that it is still receiving data from its intended transmitter. The specific use of these registers follows.

For Trail Trace Buffer purposes, the Remote Transmit E3 Framer block will group 16 consecutive E3 frames into a Trail Trace Buffer super-frame. When the Remote Transmit E3 Framer is generating the first E3 frame, within a Trail Trace Buffer super-frame, it will insert the value [1, C6, C5, C4, C3, C2, C1, C0], into the TR byte-field of this Outbound E3 frame. The remaining 15 TR byte-fields (within this Trail Trace Buffer super-frame) will consists of ASCII characters that are required for the E.164 numbering format.

When the Local Receive E3 Framer block receives an E3 frame, containing a value in the TR byte that has a "1" in the MSB position, then it (the Receive E3 Framer block) will write this value into the RxTTB-0 Register (Address = 0x1C). Once this occurs, the Receive E3 Framer block will notify the Microprocessor of this new incoming Trail Trace Buffer message by generating the Change in Trail Trace Buffer Message interrupt. The Receive E3 Framer block will also set bit 6 (TTB Change Interrupt Status) within the Rx E3 Framer Interrupt Status Register - 2, as depicted below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	1	0	0	0	0	0	0

The contents of the TR byte-field, in the very next E3 frame will be written into the Rx TTB-1 Register (Address = 0x1D), and so on until all 16 bytes have been received.

NOTES:

1. *Anytime the Receive E3 Framer block receives an E3 frame that contains an octet in the TR byte-field, with a "1" in the MSB (Most Significant Bit) position, then the Receive E3 Framer block will (1) write the contents of the TR byte-field (in this E3 frame) into the RxTTB-0 Register,*
2. *It will generate the Change in Trail Trace Buffer Interrupt. The Receive E3 Framer will do these things independent of the number of E3 frames that have been received since the last occurrence of the Change in Trail Trace Buffer Interrupt. Hence, the user, when writing data into the Tx TTB registers, must take care to insure that only the Tx TTB-0 register contains an octet with a "1" in the MSB position. All remaining Tx TTB registers (e.g., TxTTB-1 through TxTTB-15) must contain octets with a "0" in the MSB position.*
3. *The Framer IC will not verify the CRC-7 value that is written into the Rx TTB-0" register. It is up to the user's system hardware and/or software to perform this verification.*

6.3.3 The Receive HDLC Controller Block

The Receive E3 HDLC Controller block can be used to receive message-oriented signaling (MOS) type data link messages from the remote terminal equipment.

The MOS types of HDLC message processing is discussed in detail below.

The Message Oriented Signaling (e.g., LAP-D) Processing via the Receive E3 HDLC Controller block

The LAPD Receiver (within the Receive E3 HDLC Controller block) allows the user to receive PMDL messages from the remote terminal equipment, via the Inbound E3 frames. In this case, the Inbound message bits will be carried by either the GC or the NR byte-fields within each E3 Frame. The remote LAPD Transmitter will transmit a LAPD Message to the Near-End Receiver via either one of these bytes within each E3 Frame. The LAPD Receiver will receive and store the information portion of the received LAPD frame into the Receive LAPD Message Buffer, which is located at addresses: 0xDE through 0x135 within the on-chip RAM. The LAPD Receiver has the following responsibilities.

- Framing to the incoming LAPD Messages
- Filtering out stuffed "0's" (Between the two flag sequence bytes, 0x7E)
- Storing the Frame Message into the Receive LAPD Message Buffer
- Perform Frame Check Sequence (FCS) Verification
- Provide status indicators for
  - End of Message (EOM)
  - Flag Sequence Byte detected
  - Abort Sequence detected
  - Message Type
  - C/R Type
  - The occurrence of FCS Errors

The LAPD receiver's actions are facilitated via the following two registers.

- Rx E3 LAPD Control Register
- Rx E3 LAPD Status Register

Operation of the LAPD Receiver

The LAPD Receiver, once enabled, will begin searching for the boundaries of the incoming LAPD message. The LAPD Message Frame boundaries are delineated via the Flag Sequence octets (0x7E), as depicted in Figure 188.

FIGURE 188. LAPD MESSAGE FRAME FORMAT

Flag Sequence (8 bits)		
SAPI (6-bits)	C/R	EA
TEI (7 bits)		EA
Control (8-bits)		
76 or 82 Bytes of Information (Payload)		
FCS - MSB		
FCS - LSB		
Flag Sequence (8-bits)		

Where: Flag Sequence = 0x7E
SAPI + CR + EA = 0x3C or 0x3E
TEI + EA = 0x01
Control = 0x03

The 16 bit FCS is calculated using CRC-16, x16 + x12 + x5 + 1

The first byte of the information or payload field indicates the type and size of the message being transferred. The value of this information field and the corresponding message type/size follow:

CL Path Identification = 0x38 (76 bytes)

IDLE Signal Identification = 0x34 (76 bytes)

Test Signal Identification = 0x32 (76 bytes)

ITU-T Path Identification = 0x3F (82 bytes)

Enabling and Configuring the LAPD Receiver

Before the LAPD Receiver can begin to receive and process incoming LAPD Message frames, the user must do two things.

1. The byte-field within each E3 frame which will be carrying the comprising octets of the LAPD Message frame must be specified and
2. The LAPD Receiver must be enabled.

Each of these steps are discussed in detail below.

1. Specifying which byte-field, within each E3 frame, will be carrying the LAPD Message frame.

The LAPD Receiver can receive the LAPD Message frame octets via either the GC-byte-field or the NR-byte-field, within each incoming E3 frame. The user makes this selection by writing the appropriate bit to Bit 3 (DL from NR) within the Rx E3 LAPD Control Register, as depicted below.

RxE3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				DL from NR	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	R/W	R/W	R/W	RUR
0	0	0	0	0	0	1	0

Writing a “0” into this bit-field causes the LAPD Receiver to read in the octets from the GC byte-field of each E3 frame and with these octets, reassembling the LAPD Message frame. Writing a “1” into this bit-field causes the LAPD Receiver to receive the LAPD Message frame octets from the NR byte-field of each E3 frame.

2. Enabling the LAPD Receiver

The LAPD Receiver must be enabled before it can begin receiving and processing any LAPD Message frames. The LAPD Receiver can be enabled by writing a “1” to Bit 2 (RxLAPD Enable) of the Rx E3 LAPD Control Register, as indicated below.

RxE3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				DL from NR	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	R/W	R/W	R/W	RUR
0	0	0	0	0	1	1	0

Once the LAPD Receiver has been enabled, it will begin searching for the Flag Sequence octet (0x7E), in either the GC or the NR byte-fields within each incoming E3 frame. When the LAPD Receiver finds the flag

sequence byte, it will assert the Flag Present bit (Bit 0) within the Rx E3 LAPD Status Register, as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Rx ABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	1

The receipt of the Flag Sequence octet can mean one of two things.

1. This Flag Sequence byte may be marking the beginning or end of an incoming LAPD Message frame.
2. The Received Flag Sequence octet could be just one of many Flag Sequence octets that are transmitted via the E3 Transport Medium, during idle periods between the transmission of LAPD Message frames.

The LAPD Receiver will negate the Flag Present bit as soon as it has received an octet that is something other than the Flag Sequence octet. Once this happens, the LAPD Receiver should be receiving either octet # 2 of the incoming LAPD Message, or an ABORT Sequence (e.g., a string of seven or more consecutive “1’s”). If this next set of data is an ABORT Sequence, then the LAPD Receiver will assert the RxABORT bit-field (Bit 6) within the Rx E3 LAPD Status Register, as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Rx ABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	1	0	0	0	0	0	0

However, if this next octet is Octet #2 of an incoming LAPD Message frame, then the LAPD Receiver is beginning to receive a LAPD Message frame.

As the LAPD Receiver receives this LAPD Message frame, it is reading in the LAPD Message frame octets, from either the GC or the NR byte-fields within each incoming E3 frame. Secondly, it is reassembling these octets into a LAPD Message frame.

Once the LAPD Receiver has received the complete LAPD Message frame, then it will proceed to perform the following five (5) steps.

1. PMDL Message Extraction

The LAPD Receiver will extract out the PMDL Message, from the newly received LAPD Message frame. The LAPD Receiver will then write this PMDL Message into the Receive LAPD Message buffer.

NOTE: *As the LAPD Receiver is extracting the PMDL Message, from the newly received LAPD Message frame, the LAPD Receiver will also check the PMDL data for the occurrence of stuff bits (e.g., “0s” that were inserted into the PMDL Message by the Remote LAPD Transmitter, in order to prevent this data from mimicking the Flag Sequence byte or an ABORT Sequence), and remove them prior to writing the PMDL Message into the Receive LAPD Message Buffer. Specifically, the LAPD Receiver will search through the PMDL Message data and will remove any “0” that immediately follows a string of 5 consecutive “1’s”.*

For more information on how the LAPD Transmitter inserted these stuff bits, please see Section 6.2.3.1 (step 7).

2. FCS (Frame Check Sequence) Word Verification

The LAPD Receiver will compute the CRC-16 value of the header octets and the PMDL Message octets, within this LAPD Message frame and will compare it with the value of the two octets, residing in the FCS word-field of

this LAPD Message frame. If the FCS value of the newly received LAPD Message frame matches the locally-computed CRC-16 value, then the LAPD Receiver will conclude that it has received this LAPD Message frame in an error-free manner.

However, if the FCS value does not match the locally-computed CRC-16 value, then the LAPD Receiver will conclude that this LAPD Message frame is erred.

The LAPD Receiver will indicate the results of this FCS Verification process by setting Bit 2 (RxFCS Error) within the Rx E3 LAPD Status Register, to the appropriate value as tabulated below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Rx ABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	1	0	0

If the LAPD Receiver detects an error in the FCS value, then it will set the RxFCS Error bit-field to “1”. Conversely, if the LAPD Receiver does not detect an error in the FCS value, the it will clear the RxFCS Error bit-field to “0”.

NOTE: *The LAPD Receiver will extract and write the PMDL Message into the Receive LAPD Message buffer independent of the results of FCS Verification. Hence, the user is urged to validate each PMDL Message that is read in from the Receive LAPD Message buffer, by first checking the state of this bit-field.*

3. Check and Report the State of the C/R Bit-field

After receiving the LAPD Message frame, the LAPD Receiver will check the state of the C/R bit-field, within octet # 2 of the LAPD Message frame header and will reflect this value in Bit 3 (Rx CR Type) within the Rx E3 LAPD Status Register, as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Rx ABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	1	0	0	0

When this bit-field is “0”, it means that this LAPD Message frame is originating from a customer installation. When this bit-field is “1”, it means that this LAPD Message frame is originating from a network terminal.

4. Identify the Type of LAPD Message Frame/PMDL Message

Next, the LAPD Receiver will check the value of the first octet within the PMDL Information Payload field, of the LAPD Message frame. Recall that from Section 6.2.3.1, that when operating the LAPD Transmitter, the user is required to write in a byte of a specific value at address 0x8A within the Transmit LAPD Message buffer. The value of this byte corresponds to the type of LAPD Message frame/PMDL Message that is to be transmitted to the Remote LAPD Receiver. This Message-Type Identification octet is transported to the Remote LAPD Receiver, along with the rest of the LAPD frame. From this Message Type Identification octet, the LAPD

Receiver will know the type of size of the newly received PMDL Message. The LAPD Receiver will then reflect this information in Bits 4 and 5 (RxLAPDType[1:0]) within the Rx E3 LAPD Status Register, as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Rx ABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Table 83 presents the relationship between the contents of RxLAPDType[1:0] and the type of message received by the LAPD Receiver.

TABLE 83: THE RELATIONSHIP BETWEEN THE CONTENTS OF RXLAPDTYPE[1:0] BIT-FIELDS AND THE PMDL MESSAGE TYPE/SIZE

RXLAPDTYPE[1:0]	PMDL MESSAGE TYPE	PMDL MESSAGE SIZE
00	CL Path Identification	76 Bytes
01	Idle Signal Identification	76 Bytes
10	Test Signal Identification	76 Bytes
11	ITU-T Path Identification	82 Bytes

NOTE: *Prior to reading in the PMDL Message from the Receive LAPD Message buffer, the user is urged to read the state of the RxLAPDType[1:0] bit-fields in order to determine the size of this message.*

5. Inform the Local Microprocessor/External Circuitry of the receipt of the new LAPD Message frame.

Finally, after the LAPD Receiver has received and processed the newly received LAPD Message frame (per steps 1 through 4, as described above), it will inform the local Microprocessor that a LAPD Message frame has been received and is ready for user-system handling. The LAPD Receiver will inform the Microprocessor/ Microcontroller and the external circuitry by:

- Generating a LAPD Message Frame Received interrupt to the Microprocessor. The purpose of this interrupt is to let the Microprocessor know that the Receive LAPD Message buffer contains a new PMDL Message that needs to be read and processed. When the LAPD Receiver generates this interrupt, it will set bit 0 (RxLAPD Interrupt Status) within the Rx E3 LAPD Control Register to “1” as depicted below.

RxE3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				DL from NR	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	R/W	R/W	R/W	RUR
0	0	0	0	0	0	0	1

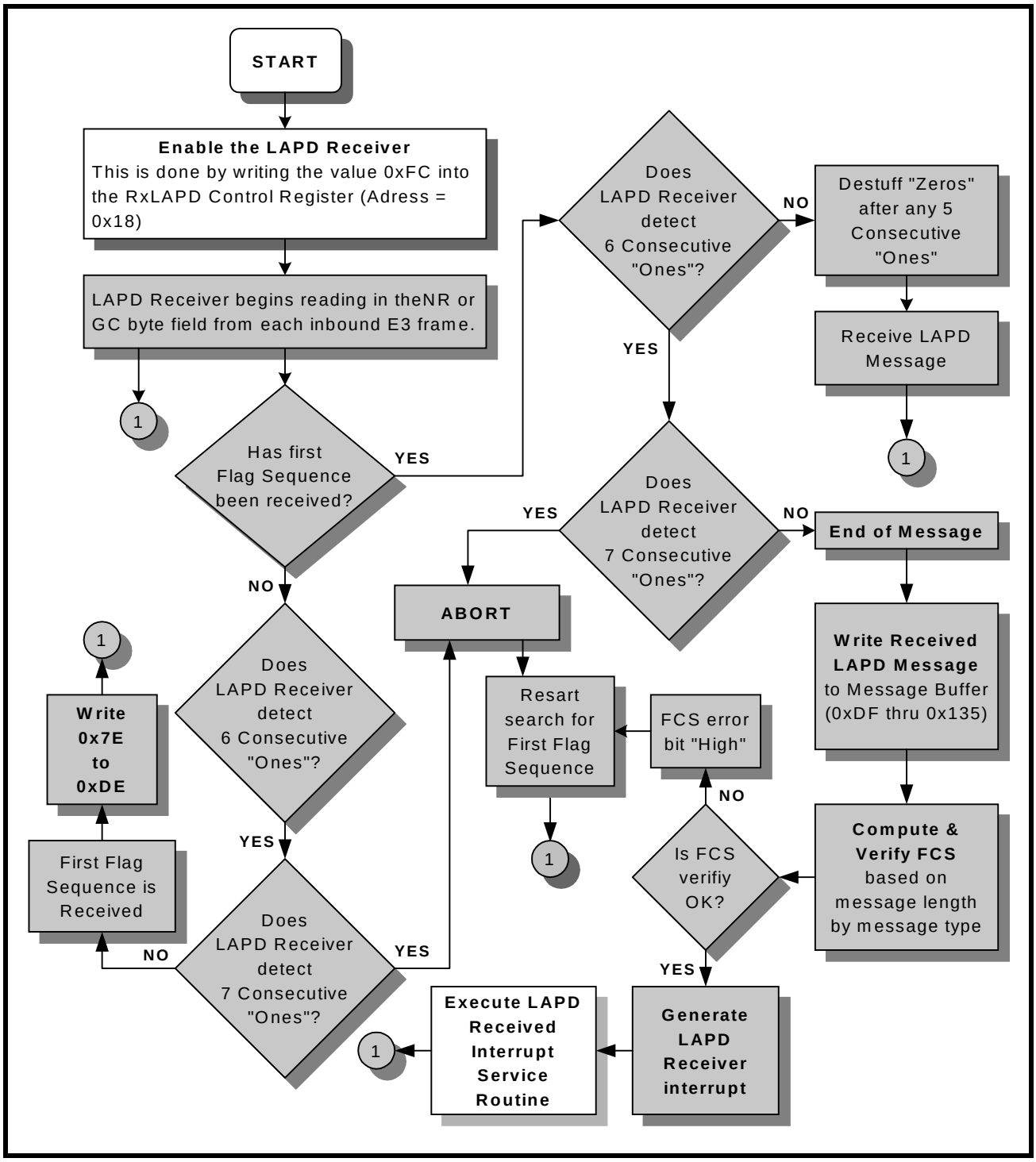
- Setting Bit 1 (End of Message) within the Rx E3 LAPD Status Register, to “1” as depicted below.

RxE3 LAPD Status Register (Address = 0x19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Rx ABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	1	0

In summary, Figure 189 presents a flow chart depicting how the LAPD Receiver functions.

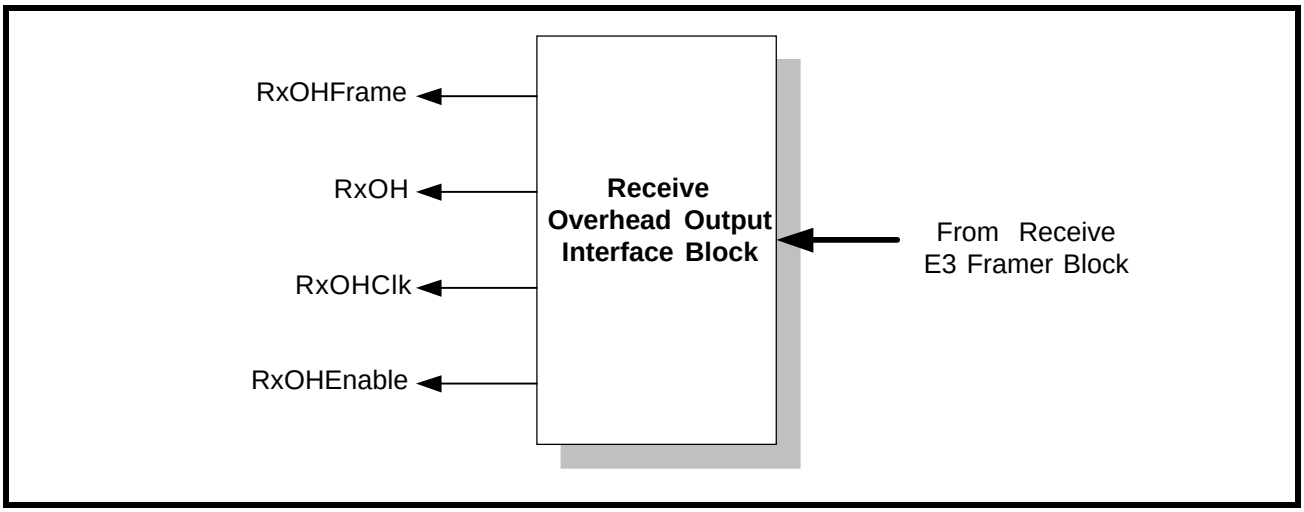
FIGURE 189. FLOW CHART DEPICTING THE FUNCTIONALITY OF THE LAPD RECEIVER



6.3.4 The Receive Overhead Data Output Interface

Figure 190 presents a simple illustration of the Receive Overhead Data Output Interface block within the XRT72L50.

FIGURE 190. THE RECEIVE OVERHEAD OUTPUT INTERFACE BLOCK



The E3, ITU-T G.832 frame consists of 537 bytes. Of these bytes, 530 bytes are payload bits and the remaining 7 bytes are overhead bytes. The XRT72L50 has been designed to handle and process both the payload type and overhead type bytes for each E3 frame.

Within the Receive Section of the XRT72L50, the Receive Payload Data Output Interface block has been designed to handle the payload bits. Likewise, the Receive Overhead Data Output Interface block has been designed to handle and process the overhead bits.

The Receive Overhead Data Output Interface block unconditionally outputs the contents of all overhead bits. The XRT72L50 does not offer the user a means to shut off this transmission of data. However, the Receive Overhead Output Interface block does provide the user with the appropriate output signals for external Data Link Layer equipment to sample and process these overhead bits, via the following two methods.

- Method 1- Using the RxOHClk clock signal.
- Method 2 - Using the RxClk and RxOHEnable output signals.

Each of these methods are described below.

6.3.4.1 *Method 1 - Using the RxOHClk Clock signal*

The Receive Overhead Data Output Interface block consists of four (4) signals. Of these four signals, the following three signals are to be used when sampling the E3 overhead bits via Method 1.

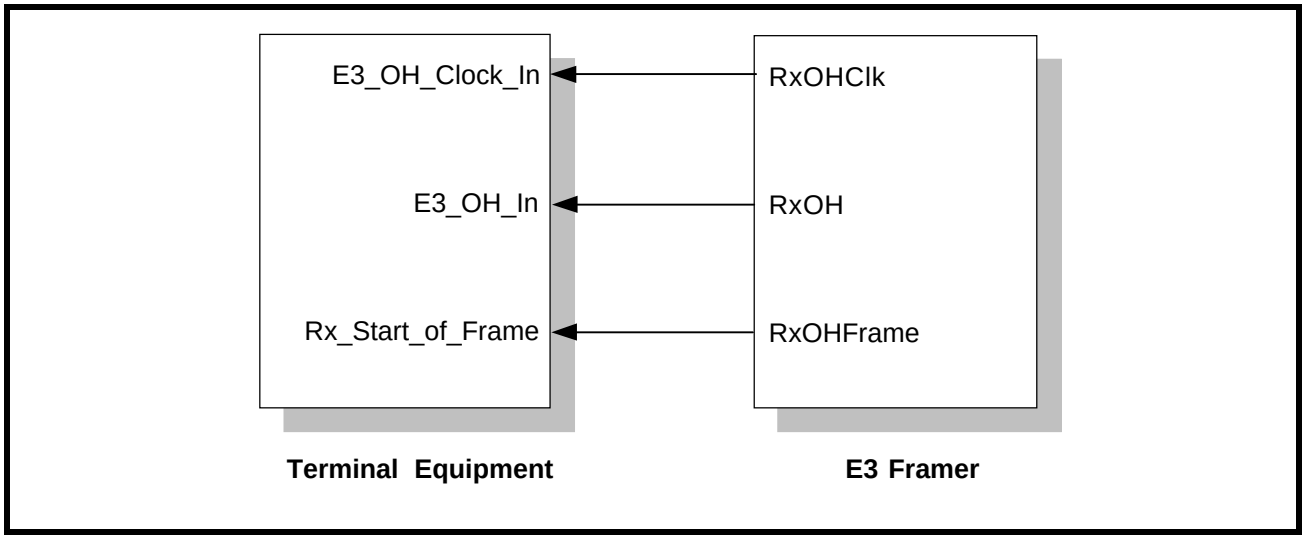
- RxOH
- RxOHClk
- RxOHFrame

Each of these signals are listed and described below in Table 84.

Interfacing the Receive Overhead Data Output Interface block to the Terminal Equipment (Method 1)

Figure 191 illustrates how one should interface the Receive Overhead Data Output Interface block to the Terminal Equipment when using Method 1, to sample and process the overhead bits from the Inbound E3 data stream.

FIGURE 191. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE (METHOD 1)



Method 1 Operation of the Terminal Equipment

If the Terminal Equipment intends to sample any overhead data from the Inbound E3 data stream (via the Receive Overhead Data Output Interface block) then it is expected to do the following:

1. Sample the state of the RxOHFrame signal (e.g., the Rx_Start_of_Frame input signal) on the rising edge of the RxOHClk (e.g., the E3_OH_Clock_In) signal.
2. Keep track of the number of rising clock edges that have occurred in the RxOHClk (e.g., the E3_OH_Clock_In) signal, since the last time the RxOHFrame signal was sampled "High". By doing this, the Terminal Equipment will be able to keep track of which overhead byte is being output via the RxOH output pin. Based upon this information, the Terminal Equipment will be able to derive some meaning from these overhead bits.

TABLE 84: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK

SIGNAL NAME	TYPE	DESCRIPTION
RxOH	Output	**Receive Overhead Data Output pin:** The XRT72L50 will output the overhead bits, within the incoming E3 frames, via this pin. The Receive Overhead Data Output Interface block will output a given overhead bit, upon the falling edge of RxOHClk. Hence, the external data link equipment should sample the data, at this pin, upon the rising edge of RxOHClk. The XRT72L50 will always output the E3 Overhead bits via this output pin. There are no external input pins or register bit settings available that will disable this output pin.
RxOHClk	Output	**Receive Overhead Data Output Interface Clock Signal:** The XRT72L50 will output the Overhead bits (within the incoming E3 frames), via the RxOH output pin, upon the falling edge of this clock signal. As a consequence, the user's data link equipment should use the rising edge of this clock signal to sample the data on both the RxOH and RxOHFrame output pins. This clock signal is always active.
RxOHFrame	Output	**Receive Overhead Data Output Interface - Start of Frame Indicator:** The XRT72L50 will drive this output pin "High" (for one period of the RxOHClk signal), whenever the first overhead bit within a given E3 frame is being driven onto the RxOH output pin.

Table 85 relates the number of rising clock edges (in the RxOHClk signal, since the RxOHFrame signal was last sampled "High") to the E3 Overhead bit that is being output via the RxOH output pin.

TABLE 85: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN RXOHCLK, (SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE E3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

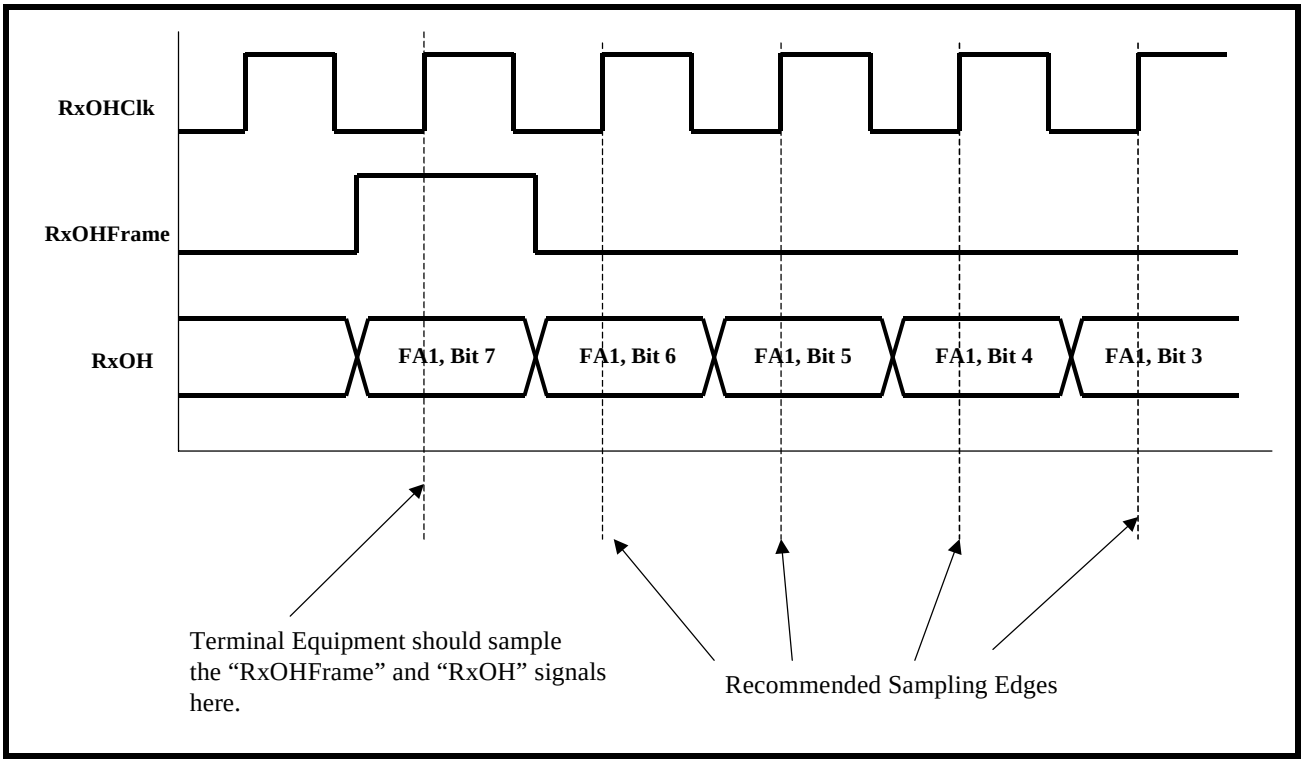
NUMBER OF RISING CLOCK EDGES IN RXOHCLK	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
0 (Clock edge is coincident with RxOHFrame being detected "High")	FA1 Byte - Bit 7
1	FA1 Byte - Bit 6
2	FA1 Byte - Bit 5
3	FA1 Byte - Bit 4
4	FA1 Byte - Bit 3
5	FA1 Byte - Bit 2
6	FA1 Byte - Bit 1
7	FA1 Byte - Bit 0
8	FA2 Byte - Bit 7
9	FA2 Byte - Bit 6
10	FA2 Byte - Bit 5
11	FA2 Byte - Bit 4
12	FA2 Byte - Bit 3
13	FA2 Byte - Bit 2
14	FA2 Byte - Bit 1
15	FA2 Byte - Bit 0
16	EM Byte - Bit 7
17	EM Byte - Bit 6
18	EM Byte - Bit 5
19	EM Byte - Bit 4
20	EM Byte - Bit 3
21	EM Byte - Bit 2
22	EM Byte - Bit 1
23	EM Byte - Bit 0
24	TR Byte - Bit 7
25	TR Byte - Bit 6
26	TR Byte - Bit 5
27	TR Byte - Bit 4

TABLE 85: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN RXOHCLK, (SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE E3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

NUMBER OF RISING CLOCK EDGES IN RXOHCLK	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
28	TR Byte - Bit 3
29	TR Byte - Bit 2
30	TR Byte - Bit 1
31	TR Byte - Bit 0
32	MA Byte - Bit 7
33	MA Byte - Bit 6
34	MA Byte - Bit 5
35	MA Byte - Bit 4
36	MA Byte - Bit 3
37	MA Byte - Bit 2
38	MA Byte - Bit 1
39	MA Byte - Bit 0
40	NR Byte - Bit 7
41	NR Byte - Bit 6
42	NR Byte - Bit 5
43	NR Byte - Bit 4
44	NR Byte - Bit 3
45	NR Byte - Bit 2
46	NR Byte - Bit 1
47	NR Byte - Bit 0
48	GC Byte - Bit 7
49	GC Byte - Bit 6
50	GC Byte - Bit 5
51	GC Byte - Bit 4
52	GC Byte - Bit 3
53	GC Byte - Bit 2
54	GC Byte - Bit 1
55	GC Byte - Bit 0

Figure 192 presents the typical behavior of the Receive Overhead Data Output Interface block, when Method 1 is being used to sample the incoming E3 overhead bits.

FIGURE 192. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE OVERHEAD OUTPUT INTERFACE (FOR METHOD 1).



6.3.4.2 *Method 2 - Using RxOutClk and the RxOHEnable signals*

Method 1 requires that the Terminal Equipment be able to handle an additional clock signal, RxOHClk. However, there may be a situation in which the Terminal Equipment circuitry does not have the means to deal with this extra clock signal, in order to use the Receive Overhead Data Output Interface. Method 2 involves the use of the following signals.

- RxOH
- RxOutClk
- RxOHEnable
- RxOHFrame

Each of these signals are listed and described in Table 86.

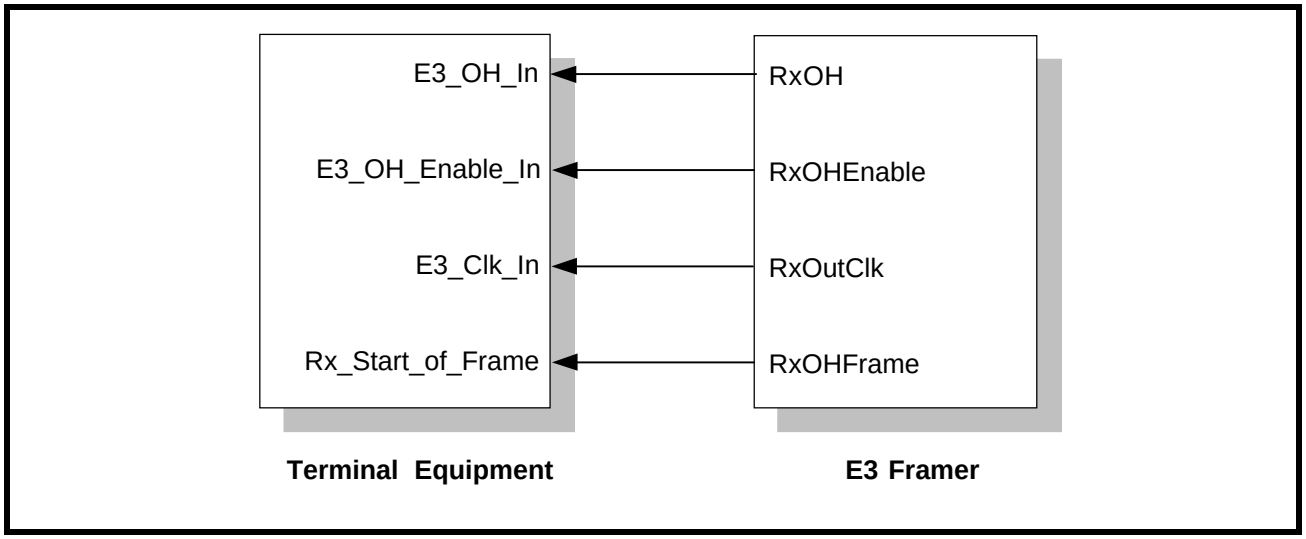
TABLE 86: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (METHOD 2)

SIGNAL NAME	TYPE	DESCRIPTION
RxOH	Output	**Receive Overhead Data Output pin:** The XRT72L50 will output the overhead bits, within the incoming E3 frames, via this pin. The Receive Overhead Output Interface will pulse the RxOHEnable output pin (for one RxOutClk period) at approximately the middle of the RxOH bit period. The user is advised to design the Terminal Equipment to latch the contents of the RxOH output pin, whenever the RxOHEnable output pin is sampled "High" on the falling edge of RxOutClk.
RxOHEnable	Output	**Receive Overhead Data Output Enable - Output pin:** The XRT72L50 will assert this output signal for one RxOutClk period when it is safe for the Terminal Equipment to sample the data on the RxOH output pin.
RxOHFrame	Output	**Receive Overhead Data Output Interface - Start of Frame Indicator:** The XRT72L50 will drive this output pin "High" (for one period of the RxOH signal), whenever the first overhead bit, within a given E3 frame is being driven onto the RxOH output pin.
RxOutClk	Output	**Receive Section Output Clock Signal:** This clock signal is derived from the RxLineClk signal (from the LIU) for loop-timing applications, and the TxInClk signal (from a local oscillator) for local-timing applications. For E3 applications, this clock signal will operate at 34.368MHz. The user is advised to design the Terminal Equipment to latch the contents of the RxOH pin, anytime the RxOHEnable output signal is sampled "High" on the falling edge of this clock signal.

Interfacing the Receive Overhead Data Output Interface block to the Terminal Equipment (Method 2)

Figure 193 illustrates how one should interface the Receive Overhead Data Output Interface block to the Terminal Equipment, when using Method 2 to sample and process the overhead bits from the Inbound E3 data stream.

FIGURE 193. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE (METHOD 2)



Method 2 Operation of the Terminal Equipment

If the Terminal Equipment intends to sample any overhead data from the Inbound E3 data stream (via the Receive Overhead Data Output Interface), then it is expected to do the following.

1. Sample the state of the RxOHFrame signal (e.g., the Rx_Start_of_Frame input) on the falling edge of the RxOutClk clock signal, whenever the RxOHEnable output signal is also sampled "High".
2. Keep track of the number of times that the RxOHEnable signal has been sampled "High" since the last time the RxOHFrame was also sampled "High". By doing this, the Terminal Equipment will be able to keep track of which overhead bit is being output via the RxOH output pin. Based upon this information, the Terminal Equipment will be able to derive some meaning from these overhead bits.
3. Table 87 relates the number of RxOHEnable output pulses (that have occurred since both the RxOHFrame and the RxOHEnable pins were both sampled "High") to the E3 overhead bit that is being output via the RxOH output pin.

TABLE 87: THE RELATIONSHIP BETWEEN THE NUMBER OF RXOHENABLE OUTPUT PULSES (SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE E3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

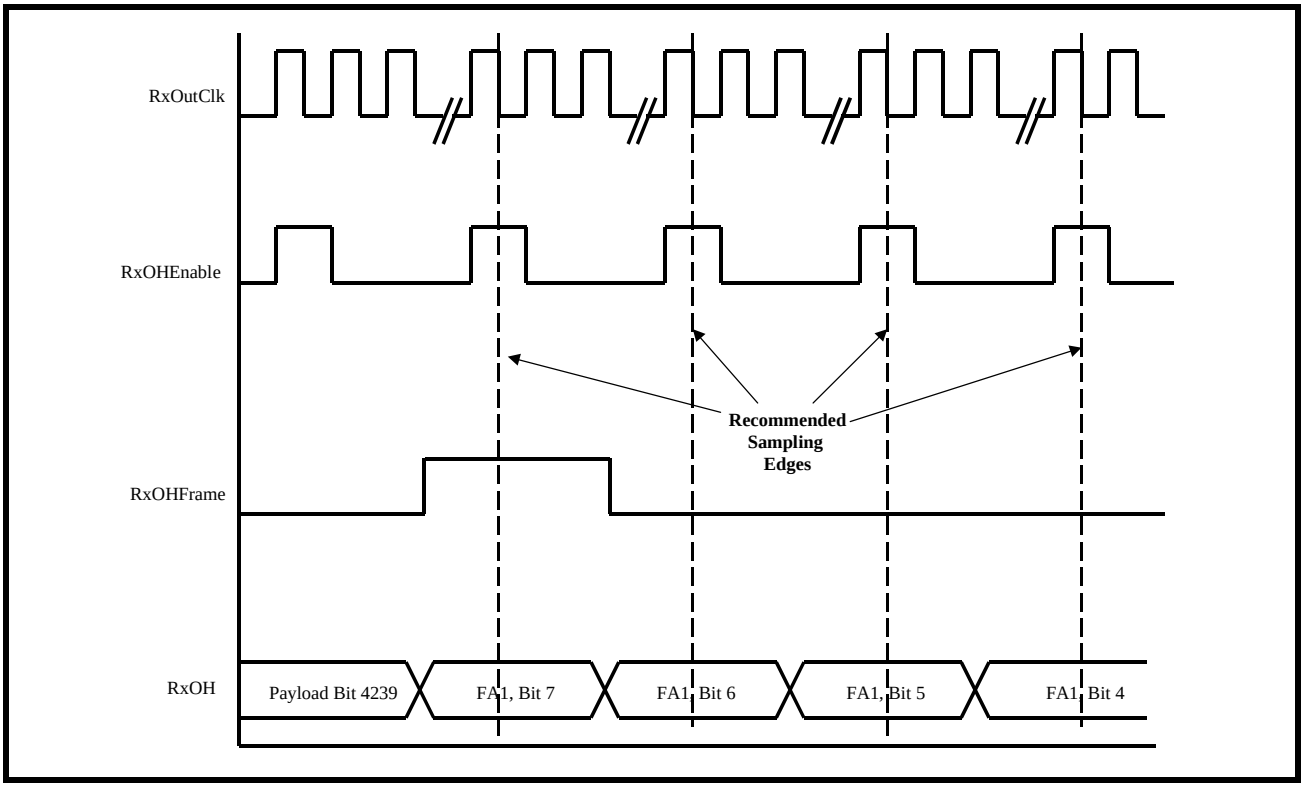
NUMBER OF RXOHENABLE OUTPUT PULSES	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
0 (Clock edge is coincident with RxOHFrame being detected "High")	FA1 Byte - Bit 7
1	FA1 Byte - Bit 6
2	FA1 Byte - Bit 5
3	FA1 Byte - Bit 4
4	FA1 Byte - Bit 3
5	FA1 Byte - Bit 2
6	FA1 Byte - Bit 1
7	FA1 Byte - Bit 0
8	FA2 Byte - Bit 7
9	FA2 Byte - Bit 6
10	FA2 Byte - Bit 5
11	FA2 Byte - Bit 4
12	FA2 Byte - Bit 3
13	FA2 Byte - Bit 2
14	FA2 Byte - Bit 1
15	FA2 Byte - Bit 0
16	EM Byte - Bit 7
17	EM Byte - Bit 6
18	EM Byte - Bit 5
19	EM Byte - Bit 4
20	EM Byte - Bit 3
21	EM Byte - Bit 2
22	EM Byte - Bit 1
23	EM Byte - Bit 0
24	TR Byte - Bit 7

TABLE 87: THE RELATIONSHIP BETWEEN THE NUMBER OF RXOHENABLE OUTPUT PULSES (SINCE RXOHFRAME WAS LAST SAMPLED "HIGH") TO THE E3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE RXOH OUTPUT PIN

NUMBER OF RXOHENABLE OUTPUT PULSES	THE OVERHEAD BIT BEING OUTPUT BY THE XRT72L50
25	TR Byte - Bit 6
26	TR Byte - Bit 5
27	TR Byte - Bit 4
28	TR Byte - Bit 3
29	TR Byte - Bit 2
30	TR Byte - Bit 1
31	TR Byte - Bit 0
32	MA Byte - Bit 7
33	MA Byte - Bit 6
34	MA Byte - Bit 5
35	MA Byte - Bit 4
36	MA Byte - Bit 3
37	MA Byte - Bit 2
38	MA Byte - Bit 1
39	MA Byte - Bit 0
40	NR Byte - Bit 7
41	NR Byte - Bit 6
42	NR Byte - Bit 5
43	NR Byte - Bit 4
44	NR Byte - Bit 3
45	NR Byte - Bit 2
46	NR Byte - Bit 1
47	NR Byte - Bit 0
48	GC Byte - Bit 7
49	GC Byte - Bit 6
50	GC Byte - Bit 5
51	GC Byte - Bit 4
52	GC Byte - Bit 3
53	GC Byte - Bit 2
54	GC Byte - Bit 1
55	GC Byte - Bit 0

Figure 194 presents the typical behavior of the Receive Overhead Data Output Interface block, when Method 2 is being used to sample the incoming E3 overhead bits.

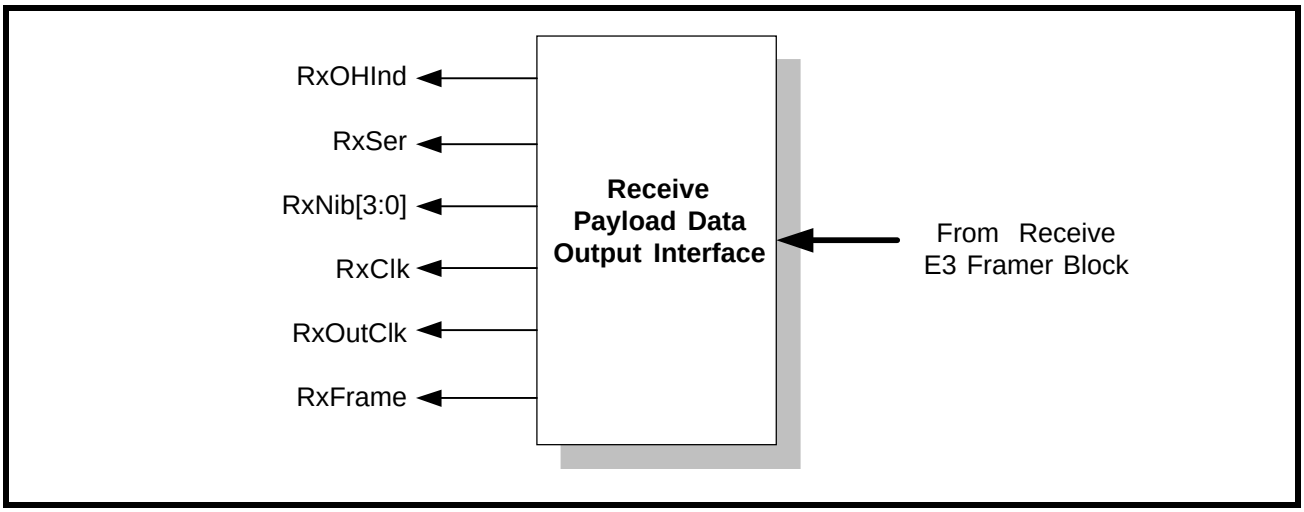
FIGURE 194. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (FOR METHOD 2).



6.3.5 The Receive Payload Data Output Interface

Figure 195 presents a simple illustration of the Receive Payload Data Output Interface block.

FIGURE 195. THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK



Each of the output pins of the Receive Payload Data Output Interface block are listed in Table 88 and described below. The exact role that each of these output pins assume, for a variety of operating scenarios are described throughout this section.

TABLE 88: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

SIGNAL NAME	TYPE	DESCRIPTION
RxSer	Output	**Receive Serial Payload Data Output pin:** If the user opts to operate the XRT72L50 in the serial mode, then the chip will output the payload data, of the incoming E3 frames, via this pin. The XRT72L50 will output this data upon the rising edge of RxClk. The user is advised to design the Terminal Equipment such that it will sample this data on the rising edge of RxClk. ***NOTE:*** *This signal is only active if the NibIntfinput pin is pulled "Low".*
RxNib[3:0]	Output	**Receive Nibble-Parallel Payload Data Output pins:** If the user opts to operate the XRT72L50 in the nibble-parallel mode, then the chip will output the payload data, of the incoming E3 frames, via these pins. The XRT72L50 will output data via these pins, upon the falling edge of the RxClk output pin. The user is advised to design the Terminal Equipment such that it will sample this data upon the rising edge of RxClk. ***NOTE:*** *These pins are only active if the NibIntfinput pin is pulled "High".*
RxClk	Output	**Receive Payload Data Output Clock pin:** The exact behavior of this signal depends upon whether the XRT72L50 is operating in the Serial or in the Nibble-Parallel-Mode. **Serial Mode Operation** In the serial mode, this signal is a 34.368MHz clock output signal. The Receive Payload Data Output Interface will update the data via the RxSer output pin, upon the rising edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxSer pin, upon the falling edge of this clock signal. **Nibble-Parallel Mode Operation** In this Nibble-Parallel Mode, the XRT72L50 will derive this clock signal, from the RxLineClk signal. The XRT72L50 will pulse this clock 1060 times for each Inbound E3 frame. The Receive Payload Data Output Interface will update the data, on the RxNib[3:0] output pins upon the falling edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxNib[3:0] output pins, upon the rising edge of this clock signal
RxOHInd	Output	**Receive Overhead Bit Indicator Output:** This output pin will pulse "High" whenever the Receive Payload Data Output Interface outputs an overhead bit via the RxSer output pin. The purpose of this output pin is to alert the Terminal Equipment that the current bit, (which is now residing on the RxSer output pin), is an overhead bit and should not be processed by the Terminal Equipment. The XRT72L50 will update this signal, upon the rising edge of RxOHInd. The user is advised to design (or configure) the Terminal Equipment to sample this signal (along with the data on the RxSer output pin) on the falling edge of the RxClk signal. ***NOTE:*** *For E3 applications, this output pin is only active if the XRT72L50 is operating in the Serial Mode. This output pin will be "Low" if the device is operating in the Nibble-Parallel Mode.*
RxFrame	Output	**Receive Start of Frame Output Indicator:** The exact behavior of this pin, depends upon whether the XRT72L50 has been configured to operate in the Serial Mode or the Nibble-Parallel Mode. **Serial Mode Operation:** The Receive Section of the XRT72L50 will pulse this output pin "High" (for one bit period) when the Receive Payload Data Output Interface block is driving the very first bit of a given E3 frame, onto the RxSer output pin. **Nibble-Parallel Mode Operation:** The Receive Section of the XRT72L50 will pulse this output pin "High" for one nibble period, when the Receive Payload Data Output Interface is driving the very first nibble of a given E3 frame, onto the RxNib[3:0] output pins.

Operation of the Receive Payload Data Output Interface block

The Receive Payload Data Output Interface permits the user to read out the payload data of Inbound E3 frames, via either of the following modes.

- Serial Mode
- Nibble-Parallel Mode

Each of these modes are described in detail, below.

6.3.5.1 *Serial Mode Operation Behavior of the XRT72L50*

If the XRT72L50 has been configured to operate in this mode, then the XRT72L50 will behave as follows.

Payload Data Output

The XRT72L50 will output the payload data, of the incoming E3 frames, upon the rising edge of RxClk.

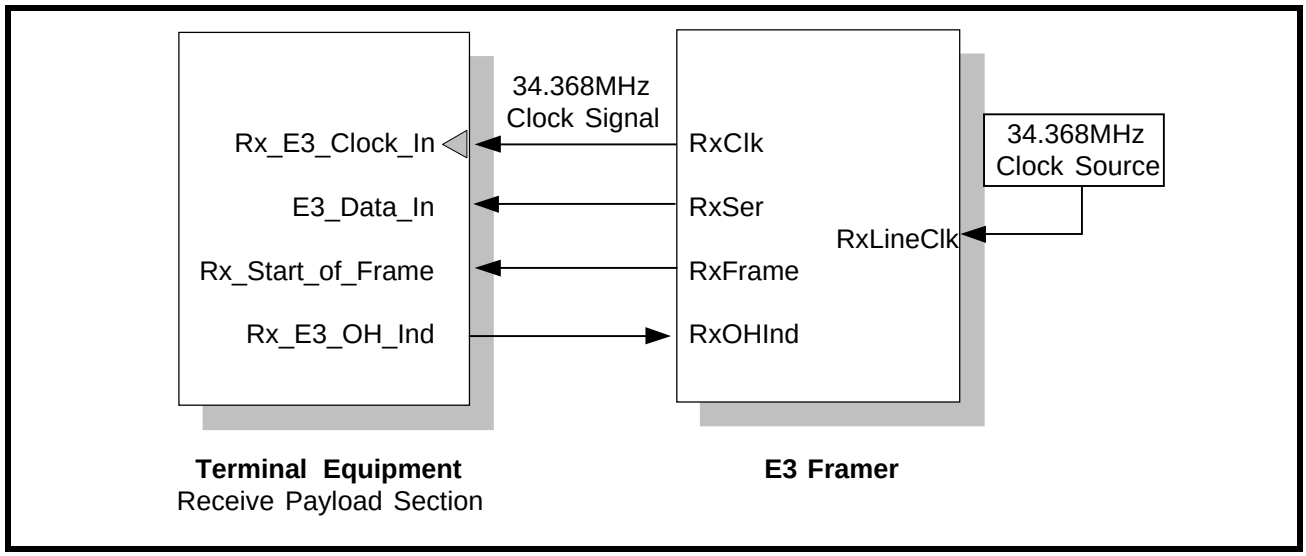
Delineation of Inbound E3 Frames

The XRT72L50 will pulse the RxFrame output pin "High" for one bit-period, coincident with it driving the first bit within a given E3 frame, via the RxSer output pin.

Interfacing the XRT72L50 to the Receive Terminal Equipment

Figure 196 presents a simple illustration as how the user should interface the XRT72L50 to that terminal equipment which processes Receive Direction payload data.

FIGURE 196. THE TERMINAL EQUIPMENT BEING INTERFACED TO THE RECEIVE PAYLOAD DATA INPUT INTERFACE BLOCK (SERIAL MODE OPERATION)



Required Operation of the Terminal Equipment

The XRT72L50 will update the data on the RxSer output pin, upon the rising edge of RxClk. Hence, the Terminal Equipment should sample the data on the RxSer output pin (or the E3_Data_In pin at the Terminal Equipment) upon the rising edge of RxClk. As the Terminal Equipment samples RxSer with each rising edge of RxClk it should also be sampling the following signals.

- RxFrame
- RxOHInd

The Need for sampling RxFrame

The XRT72L50 will pulse the RxFrame output pin "High" coincident with it driving the very first bit of a given E3 frame onto the RxSer output pin. If knowledge of the E3 Frame Boundaries is important for the operation of the Terminal Equipment, then this is a very important signal for it to sample.

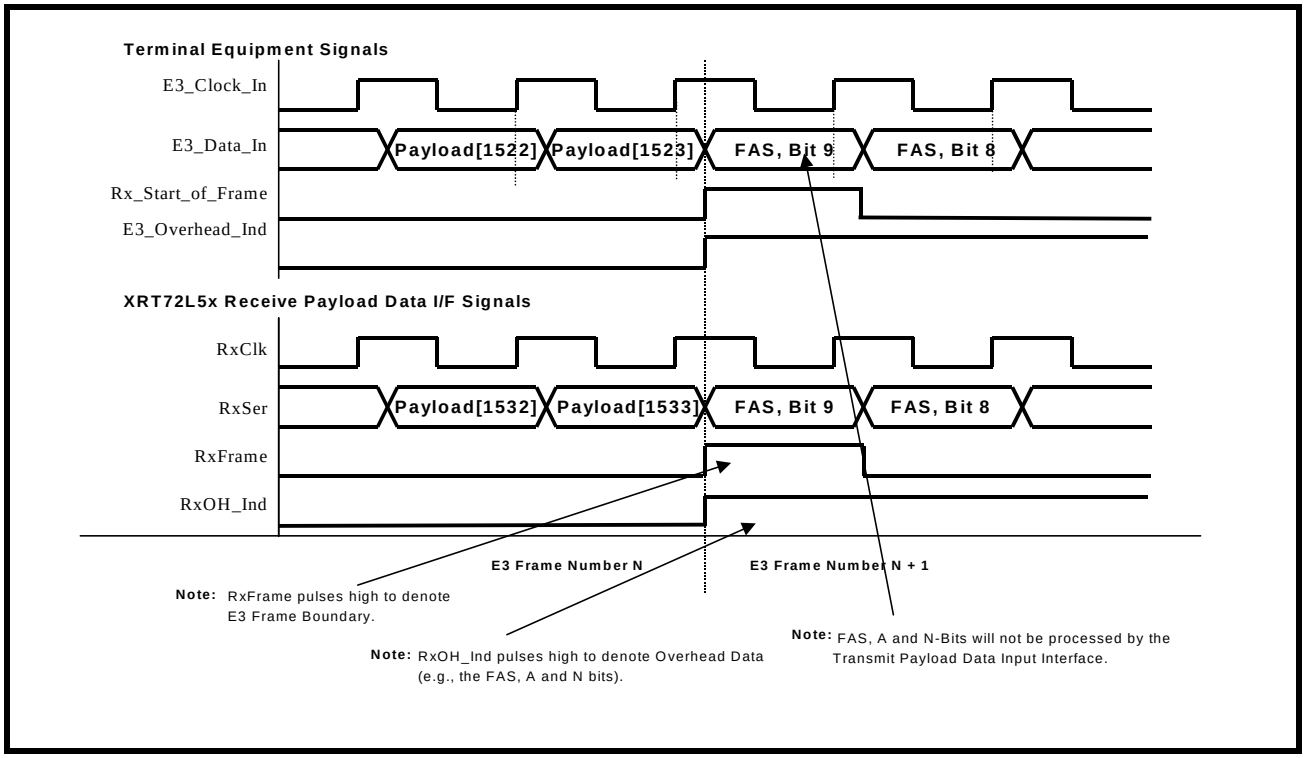
The Need for sampling RxOHInd

The XRT72L50 will indicate that it is currently driving an overhead bit onto the RxSer output pin, by pulsing the RxOHInd output pin "High". If the Terminal Equipment samples this signal "High", then it should know that the bit, that it is currently sampling via the RxSer pin is an overhead bit and should not be processed.

The Behavior of the Signals between the Receive Payload Data Output Interface block and the Terminal Equipment

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Serial Mode Operation is illustrated in Figure 197.

FIGURE 197. AN ILLUSTRATION OF THE BEHAVIOR OF THE SIGNALS BETWEEN THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK OF THE XRT72L50 AND THE TERMINAL EQUIPMENT



6.3.5.2 *Nibble-Parallel Mode OperationBehavior of the XRT72L50*

If the XRT72L50 has been configured to operate in the Nibble-Parallel Mode, then the XRT72L50 will behave as follows.

Payload Data Output

The XRT72L50 will output the payload data of the incoming E3 frames, via the RxNib[3:0] output pins, upon the rising edge of RxClk.

NOTES:

1. *In this case, RxClk will function as the Nibble Clock signal between the XRT72L50 the Terminal Equipment. The XRT72L50 will pulse the RxClk output signal "High" 1060 times, for each Inbound E3 frame.*
2. *Unlike Serial Mode operation, the duty cycle of RxClk, in Nibble-Parallel Mode operation is approximately 25%.*

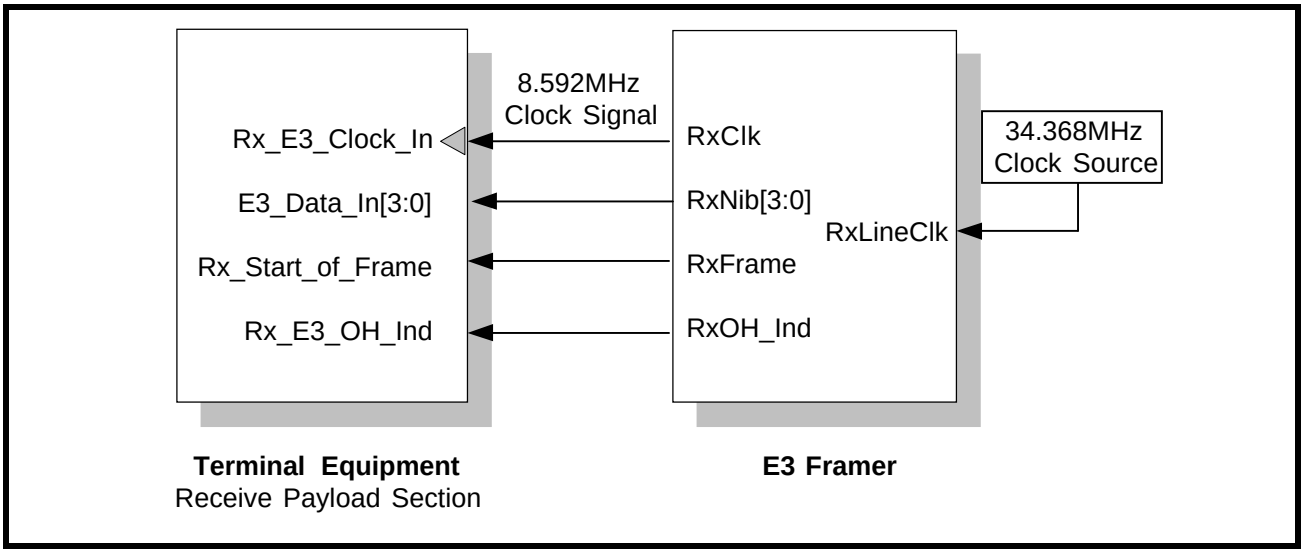
Delineation of Inbound E3 Frames

The XRT72L50 will pulse the RxFrame output pin "High" for one nibble-period coincident with it driving the very first nibble, within a given Inbound E3 frame, via the RxNib[3:0] output pins.

Interfacing the XRT72L50 the Terminal Equipment.

Figure 198 presents a simple illustration as how the user should interface the XRT72L50 to that terminal equipment which processes Receive Direction payload data.

FIGURE 198. THE XRT72L50 DS3/E3 FRAMER IC BEING INTERFACED TO THE RECEIVE SECTION OF THE TERMINAL EQUIPMENT (NIBBLE-PARALLEL MODE OPERATION)



Required Operation of the Terminal Equipment

The XRT72L50 will update the data on the RxNib[3:0] line, upon the rising edge of RxClk. Hence, the Terminal Equipment should sample the data on the RxNib[3:0] output pins (or the E3_Data_In[3:0] input pins at the Terminal Equipment) upon the rising edge of RxClk. As the Terminal Equipment samples RxSer with each rising edge of RxClk it should also be sampling the RxFrame signal.

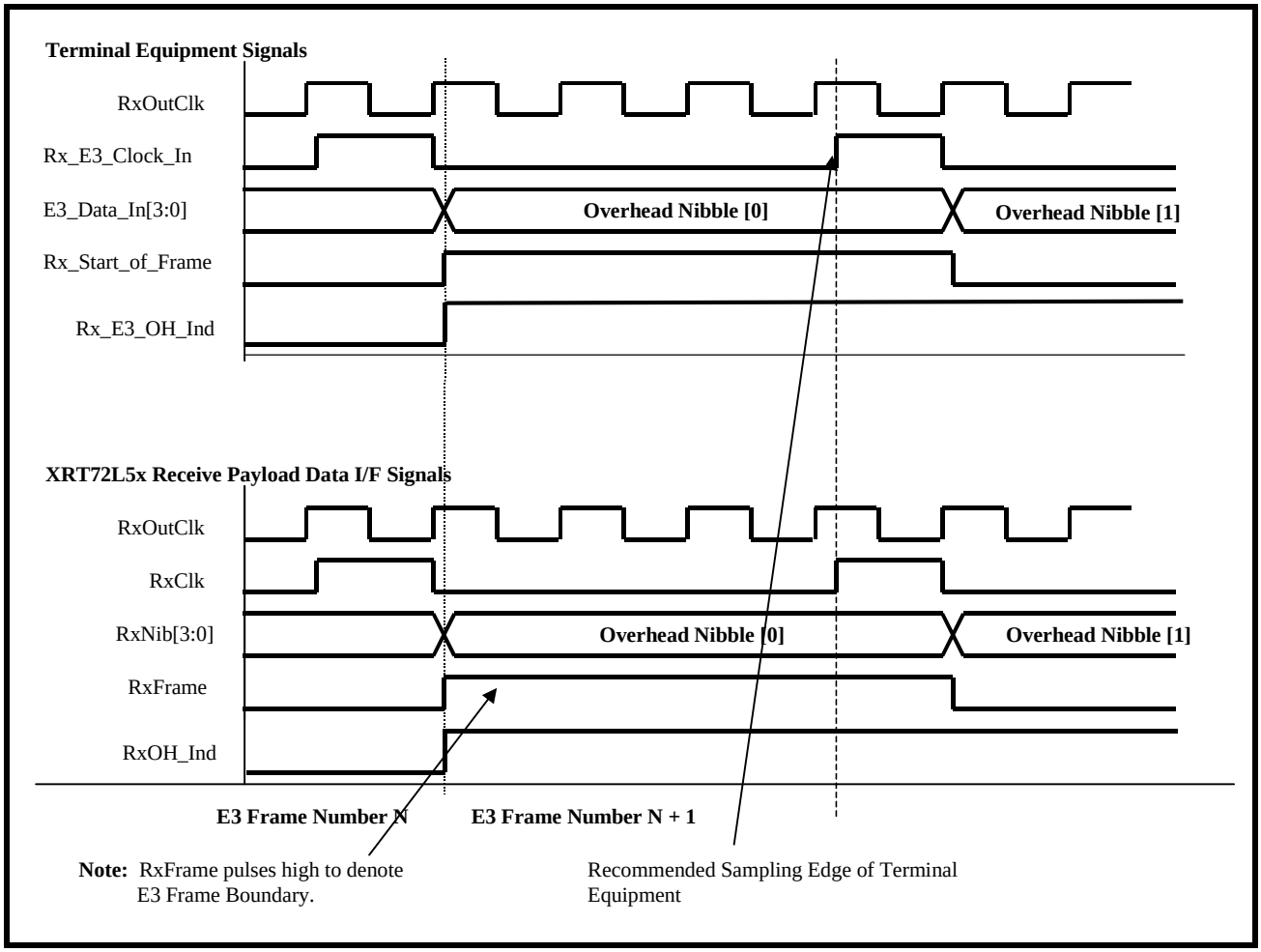
The Need for Sampling RxFrame

The XRT72L50 will pulse the RxFrame output pin "High" coincident with it driving the very first nibble of a given E3 frame, onto the RxNib[3:0] output pins. If knowledge of the E3 Frame Boundaries is important for the operation of the Terminal Equipment, then this is a very important signal for it to sample.

The Behavior of the Signals between the Receive Payload Data Output Interface block and the Terminal Equipment

The behavior of the signals between the XRT72L50 and the Terminal Equipment for E3 Nibble-Mode operation is illustrated in Figure 199.

FIGURE 199. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE BLOCK (FOR METHOD 2).



6.3.6 Receive Section Interrupt Processing

The Receive Section of the XRT72L50 can generate an interrupt to the MIcrocontroller/Microprocessor for the following reasons.

- Change in Receive LOS Condition
- Change in Receive OOF Condition
- Change in Receive LOF Condition
- Change in Receive AIS Condition
- Change in Receive FERF Condition
- Change of Framing Alignment
- Change in Receive Trail Trace Buffer Message
- Detection of FEBE (Far-End Block Error) Event
- Detection of BIP-8 Error
- Detection of Framing Byte Error
- Detection of Payload Type Mismatch
- Reception of a new LAPD Message

6.3.6.1 *Enabling Receive Section Interrupts*

The Interrupt Structure within the XRT72L50 contains two hierarchical levels.

- Block Level
- Source Level

The Block Level

The Enable state of the Block level for the Receive Section Interrupts dictates whether or not interrupts (if enabled at the source level), are actually enabled.

The user can enable or disable these Receive Section interrupts, at the Block Level by writing the appropriate data into Bit 7 (Rx DS3/E3 Interrupt Enable) within the Block Interrupt Enable register (Address = 0x04), as illustrated below.

Block Interrupt Enable Register (Address = 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used					TxDS3/E3 Interrupt Enable	One-Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
X	0	0	0	0	0	0	0

Setting this bit-field to “1” enables the Receive Section at the Block Level) for interrupt generation. Conversely, setting this bit-field to “0” disables the Receive Section for interrupt generation.

6.3.6.2 *Enabling/Disabling and Servicing Interrupts*

As mentioned earlier, the Receive Section of the XRT72L50 Framer IC contains numerous interrupts. The Enabling/Disabling and Servicing of each of these interrupts is described below.

6.3.6.2.1 The Change in Receive LOS Condition Interrupt

If the Change in Receive LOS Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an LOS (Loss of Signal) Condition, and
2. When the XRT72L50 Framer IC clears the LOS condition.

Conditions causing the XRT72L50 Framer IC to declare an LOS Condition.

- If the XRT73L00 LIU IC declares an LOS condition, and drives the RLOS input pin (of the XRT72L50 Framer IC) "High".
- If the XRT72L50 Framer IC detects 32 consecutive “0”, via the RxPOS and RxNEG input pins and Internal LOS is enabled, (Address 0x00, bit 5).

Conditions causing the XRT72L50 Framer IC to clear the LOS Condition.

- If the XRT73L00 LIU IC clears the LOS condition and drives the RLOS input pin (of the XRT72L50 Framer IC) "Low".
- If the XRT72L50 Framer IC detects a string of 32 consecutive bits (via the RxPOS and RxNEG input pins) that does NOT contain a string of 4 consecutive “0’s”and Internal LOS is enabled, (Address 0x00, bit 5).

Enabling and Disabling the Change in Receive LOS Condition Interrupt

The user can enable or disable the Change in Receive LOS Condition Interrupt, by writing the approrpriate value into Bit 1 (LOS Interrupt Enable), within the RxE3 Interrupt Enable Register - 1, as indicated below.

RxE3 Interrupt Enable Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	X	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive LOS Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "Low".
- It will set Bit 1 (LOS Interrupt Status), within the Rx E3 Interrupt Status Register - 1 to “1”, as indicated below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

Whenever the user’s system encounters the Change in Receive LOS Condition Interrupt, then it should do the following.

1. It should determine the current state of the LOS condition. Recall, that this interrupt can be generated, whenever the XRT72L50 Framer IC declares or clears the LOS defect. Hence, the user can determine the current state of the LOS defect by reading the state of Bit 4 (RxLOS) within the Rx E3 Configuration and Status Register - 2, as illustrated below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	X	X	X	X

If the LOS state is TRUE

1. It should transmit a FERF (Far-End-Receive Failure) indicator to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-LOS feature.

If the LOS state is FALSE

1. It should cease transmitting the FERF indication to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-LOS feature.

6.3.6.2.2 The Change in Receive OOF Condition Interrupt

If the Change in Receive OOF Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an OOF (Out of Frame) Condition, and
2. When the XRT72L50 Framer IC clears the OOF condition.

Conditions causing the XRT72L50 Framer IC to declare an OOF Condition.

- If the Receive E3 Framer block (within the XRT72L50 Framer IC) detects Framing Byte errors, within four consecutive incoming E3 frames.

Conditions causing the XRT72L50 Framer IC to clear the OOF Condition.

- If the Receive E3 Framer block (within the XRT72L50 Framer IC) transitions from the FA1, FA2 Octet Verification state to the In-Frame state (see Figure 182).
- If the Receive E3 Framer block transitions from the OOF Condition state to the In-Frame state (see Figure 182).

Enabling and Disabling the Change in Receive OOF Condition Interrupt

The user can enable or disable the Change in Receive OOF Condition Interrupt, by writing the appropriate value into Bit 3 (OOF Interrupt Enable), within the RxE3 Interrupt Enable Register - 1, as indicated below.

RxE3 Interrupt Enable Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	X	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive OOF Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$), by driving it "Low".
- It will set Bit 3 (OOF Interrupt Status), within the Rx E3 Interrupt Status Register - 1 to “1”, as indicated below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

Whenever the user’s system encounters the Change in Receive OOF Condition Interrupt, then it should do the following.

1. It should determine the current state of the OOF condition. Recall, that this interrupt can be generated, whenever the XRT72L50 Framer IC declares or clears the OOF defect. Hence, the user can determine the current state of the LOS defect by reading the state of Bit 5 (RxOOF) within the Rx E3 Configuration and Status Register - 2, as illustrated below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	X	X	X	X

If the OOF state is TRUE

1. It should transmit a FERF (Far-End-Receive Failure) indicator to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-OOF feature.

If the OOF state is FALSE

1. It should cease transmitting the FERF indication to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-OOF feature.

6.3.6.2.3 The Change in Receive LOF Condition Interrupt

If the Change in Receive LOF Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an LOF (Out of Frame) Condition, and
2. When the XRT72L50 Framer IC clears the LOF condition.

Conditions causing the XRT72L50 Framer IC to declare an LOF Condition.

- If the Receive E3 Framer block (within the XRT72L50 Framer IC) detects Framing Byte errors, within four consecutive incoming E3 frames and is not able to transition back into the In-Frame state within 1 or 3ms.

Conditions causing the XRT72L50 Framer IC to clear the LOF Condition.

- If the Receive E3 Framer block transitions from the OOF Condition state to the LOF Condition state (see Figure 182).
- If the Receive E3 Framer block transitions back into the In-Frame state.

Enabling and Disabling the Change in Receive LOF Condition Interrupt

The user can enable or disable the Change in Receive LOF Condition Interrupt, by writing the appropriate value into Bit 2 (LOF Interrupt Enable), within the RxE3 Interrupt Enable Register - 1, as indicated below.

RxE3 Interrupt Enable Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	X	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive LOF Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$), by driving it "Low".

- It will set Bit 6 (LOF Interrupt Status), within the Rx E3 Interrupt Status Register - 1 to “1”, as indicated below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
X	1	X	X	X	X	X	X

6.3.6.2.4 The Change of Framing Alignment (COFA) Interrupt

If the Change of Framing Alignment Interrupt is enabled then the XRT72L50 Framer IC will generate an interrupt any time the Receive E3 Framer block detects an abrupt change of framing alignment.

NOTE: *This interrupt is typically accompanied with the Change in Receive OOF Condition interrupt as well.*

Conditions causing the XRT72L50 Framer IC to generate this interrupt.

If the XRT72L50 Framer detects receives at least four consecutive E3 frames, within its Framing Alignment bytes in Error, then the XRT72L50 Framer IC will declare an OOF condition. However, while the XRT72L50 Framer IC is operating in the OOF condition, it will still rely on the old framing alignment for E3 payload data extraction, etc.

However, if the Receive E3 Framer had to change alignment, in order to re-acquire frame synchronization, then this interrupt will occur.

Enabling and Disabling the Change of Framing Alignment Interrupt

The user can enable or disable the Change of Framing Alignment Interrupt by writing the appropriate value into Bit 4 (COFA InterruptEnable).

RxE3 Interrupt ENABLE Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	X	0	0	0	0

Writing a “1” into this bit-field enables the Change of Framing Alignment Interrupt. Conversely, writing a “0” into this bit-field disables the Change of Framing Alignment Interrupt.

Servicing the Change of Framing Alignment Interrupt

Whenever the XRT72L50 Framer IC generates this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$) by driving it "Low".
- It will set Bit 4 (COFA Interrupt Status), within the Rx E3 Interrupt Status Register -1, to “1”, as indicated below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	1	0	0	0	0

6.3.6.2.5 The Change in Receive AIS Condition Interrupt

If the Change in Receive AIS Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares an AIS Condition, and
2. When the XRT72L50 Framer IC clears the AIS condition.

Conditions causing the XRT72L50 Framer IC to declare an AIS Condition.

- If the XRT72L50 Framer IC detects 7 or less “0’s” within 2 consecutive E3 frames.

Conditions causing the XRT72L50 Framer IC to clear the AIS Condition.

- If the XRT72L50 Framer IC detects 2 consecutive E3 frames that each contain 8 or more “0’s”.

Enabling and Disabling the Change in Receive AIS Condition Interrupt

The user can enable or disable the AIS Interrupt, by writing the appropriate value into Bit 0 (AIS Interrupt Enable), within the RxE3 Interrupt Enable Register - 1, as indicated below.

RxE3 Interrupt Enable Register - 1 (Address = 0x12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Enable	OOF Interrupt Enable	LOF Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable
RO	RO	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	X

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive AIS Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$), by driving it "Low".
- It will set Bit 0 (AIS Interrupt Status), within the Rx E3 Interrupt Status Register - 1 to “1”, as indicated below.

RxE3 Interrupt Status Register - 1 (Address = 0x14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			COFA Interrupt Status	OOF Interrupt Status	LOF Interrupt Status	LOS Interrupt Status	AIS Interrupt Status
RO	RO	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	1

Whenever the user’s system encounters the Change in Receive AIS Condition Interrupt, then it should do the following.

1. It should determine the current state of the AIS condition. Recall, that this interrupt can be generated, whenever the XRT72L50 Framer IC declares or clears the AIS defect. Hence, the user can determine the current state of the AIS defect by reading the state of Bit 3 (RxAIS) within the Rx E3 Configuration and Status Register - 2, as illustrated below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	X	X	X	X

If the AIS Condition is TRUE

1. It should begin transmitting the FERF indication to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-AIS feature.

If the AIS Condition is FALSE

2. It should cease transmitting the FERF indication to the Remote Terminal Equipment. The XRT72L50 Framer IC automatically supports this action via the FERF-upon-AIS feature.

6.3.6.2.6 The Change in Trail Trace Buffer Message Interrupt

If the Change in Trail Trace Buffer Message Interrupt has been enabled, then the XRT72L50 Framer IC will generate an interrupt any time the Receive E3 Framer block receives a different Trail Trace Buffer message, then it has previously read in.

Enabling and Disabling the Change in Trail Trace Buffer Message Interrupt.

The user can enable or disable the Change in Trail Trace Buffer Message interrupt by writing the appropriate value into Bit 6 (TTB Change Interrupt Enable) within the Rx E3 Interrupt Enable Register - 2, as indicated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Enable	Not Used	FEBE Interrupt Enable	FERF Interrupt Enable	BIP-8 Error Interrupt Enable	Framing Byte Error Interrupt Enable	RxPld Mis Interrupt Enable
RO	R/W	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	X	0	0	0

Writing a “1” into this bit-field enables the Change in Trail Trace Buffer Message Interrupt. Conversely, writing a “0” into this bit-field disables the Change in Trail Trace Buffer Message Interrupt.

Servicing the Change in Trail Trace Buffer Message Interrupt

Whenever the XRT72L50 Framer IC generates this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$) by driving it "Low".
- It will set Bit 6 (TTB Change Interrupt Status), within the Rx E3 Interrupt Status Register - 2, as indicated below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	1	0	0	0	0	0	0

- It will write the contents of this newly received Trail Trace Buffer Message, into the RxTTB-0 (located at 0x1C) through RxTTB-15 (located at 0x2B) registers.

Whenever the Terminal Equipment encounters the Change in Trail Trace Buffer Message Interrupt, then it should read out the contents of the 16 RxTTB registers.

6.3.6.2.7 The Change in Receive FERF Condition Interrupt

If the Change in Receive FERF Condition Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L50 Framer IC declares a FERF (Far-End Receive Failure) Condition, and
2. When the XRT72L50 Framer IC clears the FERF condition.

Conditions causing the XRT72L50 Framer IC to declare an FERF Condition.

- If the XRT72L50 Framer IC begins receiving E3 frames which have the FERF bit (within the MA byte, set to “1”).

Conditions causing the XRT72L50 Framer IC to clear the FERF Condition.

- If the XRT72L50 Framer IC begins receiving E3 frames that do NOT have the FERF bit set to “1”.

Enabling and Disabling the Change in Receive FERF Condition Interrupt

The user can enable or disable the Change in Receive FERF Condition Interrupt, by writing the appropriate value into Bit 3 (FERF Interrupt Enable), within the RxE3 Interrupt Enable Register - 2, as indicated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Enable	Not Used	FEBE Interrupt Enable	FERF Interrupt Enable	BIP-8 Error Interrupt Enable	Framing Byte Error Interrupt Enable	RxPld Mis Interrupt Enable
RO	R/W	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	X	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the Change in Receive FERF Condition Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$), by driving it "Low".
- It will set Bit 3 (FERF Interrupt Status), within the Rx E3 Interrupt Status Register - 2 to “1”, as indicated below

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

Whenever the user's system encounters the Change in Receive FERF Condition Interrupt, then it should do the following.

- It should determine the current state of the FERF condition. Recall, that this interrupt can be generated, whenever the XRT72L50 Framer IC declares or clears the FERF defect. Hence, the user can determine the current state of the LOS defect by reading the state of Bit 0 (RxFERF) within the Rx E3 Configuration and Status Register - 2, as illustrated below.

RxE3 Configuration & Status Register 2 (Address = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx LOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPld Unstab	Rx TMark	RxFERF
R/W	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	X	X	X	X

6.3.6.2.8 The Detection of FEBE (Far-End-Block Error) Event Interrupt

If the Detection of FEBE Event Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt, anytime the Receive E3 Framer block has received an E3 frame with the FEBE bit-field (within the MA byte) set to "1".

Enabling and Disabling the Detection of FEBE Event Interrupt

The user can enable or disable the Detection of FEBE Event' interrupt by writing the appropriate value into Bit 4 (FEBE Interrupt Enable) within the Rx E3 Interrupt Enable Register - 2, as indicated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Enable	Not Used	FEBE Interrupt Enable	FERF Interrupt Enable	BIP-8 Error Interrupt Enable	Framing Byte Error Interrupt Enable	RxPld Mis Interrupt Enable
RO	R/W	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	X	0	0	0	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the Detection of the FEBE Event Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$), by driving it "Low".
- It will set the Bit 4 (FEBE Interrupt Status), within the RxE3 Interrupt Status Register - 2 as indicated below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	1	0	0	0	0

Whenever the Terminal Equipment encounters the Detection of FEBE Event Interrupt, it should do the following.

- It should read the contents of the PMON FEBE Event Count Registers (located at Addresses 0x56 and 0x57) in order to determine the number of FEBE Events that have been received by the XRT72L50 Framer IC.

6.3.6.2.9 The Detection of BIP-8 Error Interrupt

If the Detection of BIP-8 Error Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt, anytime the Receive E3 Framer block has detected an error in the EM (Error Monitoring) byte, within an incoming E3 frame.

Enabling and Disabling the Detection of BIP-8 Error Interrupt

The user can enable or disable the Detection of BIP-8 Error' interrupt by writing the appropriate value into Bit 2 (BIP-8 Interrupt Enable) within the Rx E3 Interrupt Enable Register - 2, as indicated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Enable	Not Used	FEBE Interrupt Enable	FERF Interrupt Enable	BIP-8 Error Interrupt Enable	Framing Byte Error Interrupt Enable	RxPld Mis Interrupt Enable
RO	R/W	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	X	0	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the Detection of the BIP-8 Error Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "Low".
- It will set the Bit 2 (BIP-8 Interrupt Status), within the RxE3 Interrupt Status Register - 2 as indicated below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

Whenever the Terminal Equipment encounters the Detection of BIP-8 Error Interrupt, it should do the following.

- It should read the contents of the PMON Parity Error Event Count Registers (located at Addresses 0x54 and 0x55) in order to determine the number of BIP-8 Errors that have been received by the XRT72L50 Framer IC.

6.3.6.2.10 The Detection of Framing Byte Error Interrupt

If the Detection of Framing Byte Error Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt, anytime the Receive E3 Framer block has received an E3 frame with an incorrect Framing Byte (e.g., FA1 or FA2) value.

Enabling and Disabling the Detection of Framing Byte Error Interrupt

The user can enable or disable the Detection of Framing Byte Error' interrupt by writing the appropriate value into Bit 1 (Framing Byte Error Interrupt Enable) within the Rx E3 Interrupt Enable Register - 2, as indicated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Enable	Not Used	FEBE Interrupt Enable	FERF Interrupt Enable	BIP-8 Error Interrupt Enable	Framing Byte Error Interrupt Enable	RxPld Mis Interrupt Enable
RO	R/W	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	X	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the Detection of Framing Byte Error Interrupt

Whenever the XRT72L50 Framer IC detects this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{Int}$), by driving it "Low".
- It will set the Bit 1 (Framing Byte Error Interrupt Status), within the RxE3 Interrupt Status Register - 2 as indicated below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	1	0

Whenever the Terminal Equipment encounters the Detection of Framing Byte Error Interrupt, it should do the following.

- It should read the contents of the PMON Framing Bit/Byte Error Count Registers (located at Addresses 0x52 and 0x53) in order to determine the number of Framing Byte errors that have been received by the XRT72L50 Framer IC.

6.3.6.2.11 The Detection of Payload Type Mismatch Interrupt

If the Detection of Payload Type Mismatch Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt, anytime the Receive E3 Framer block receives a MA byte (within an incoming E3 frame) that contents a Payload Type value that is different from the expected Payload Type value.

Conditions causing this interrupt to be generated.

During system configuration, the user is expected to specify the Payload Type value that is expected of the Receive E3 Framer to receive (within each E3 frame), by writing this value into the RxPLDExp[2:0] bit-fields within the Rx E3 Configuration & Status Register - 1, as indicated below..

RxE3 Configuration & Status Register 1 (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxPLDType[2:0]			RxFERF Algo	RxTMark Algo	RxPLDExp[2:0]		
RO	RO	RO	RO	RO	R/W	R/W	R/W
0	0	0	0	0	0	0	0

As long as the Receive E3 Framer block receives E3 frames that contains this Payload Type value, no interrupt will be generated. However, the instant that it receives an E3 frame, that contains a different Payload Type value, then the XRT72L50 Framer IC will generate this interrupt.

RxE3 Configuration & Status Register 1 (Address = 0x10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxPLDType[2:0]			RxFERF Algo	RxTMark Algo	RxPLDExp[2:0]		
RO	RO	RO	RO	RO	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Enabling and Disabling the Detection of Payload Type Mismatch Interrupt.

The user can enable or disable the Detection of Payload Type Mismatch Interrupt by writing the appropriate data into Bit 0 (RxPld Mis Interrupt Enable), within the Rx E3 Interrupt Enable Register - 2, as indicated below.

RxE3 Interrupt Enable Register - 2 (Address = 0x13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Enable	Not Used	FEBE Interrupt Enable	FERF Interrupt Enable	BIP-8 Error Interrupt Enable	Framing Byte Error Interrupt Enable	RxPld Mis Interrupt Enable
RO	R/W	RO	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	X

Setting this bit-field to “1 enables the Detection of Payload Type Mismatch Interrupt. Conversely, setting this bit-field to “0” disables the Detection of Payload Type Mismatch Interrupt.

Servicing the Detection of Payload Type Mismatch Interrupt

Whenever the XRT72L50 Framer IC generates this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$) by driving it "Low".
- It will set Bit 0 (RxPld Mis Interrupt Status), within the Rx E3 Interrupt Enable Register -2 to “1”, as indicated below.

RxE3 Interrupt Status Register - 2 (Address = 0x15)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TTB Change Interrupt Status	Not Used	FEBE Interrupt Status	FERF Interrupt Status	BIP-8 Error Interrupt Status	Framing Byte Error Interrupt Status	RxPld Mis Interrupt Status
RO	RUR	RO	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	1

6.3.6.2.12 The Receive LAPD Message Interrupt

If the Receive LAPD Message Interrupt is enabled, then the XRT72L50 Framer IC will generate an interrupt anytime the Receive HDLC Controller block has received a new LAPD Message frame from the Remote Terminal Equipment, and has stored the contents of this message into the Receive LAPD Message buffer.

Enabling/Disabling the Receive LAPD Message Interrupt

The user can enable or disable the Receive LAPD Message Interrupt by writing the appropriate data into Bit 1 (RxLAPD Interrupt Enable) within the Rx E3 LAPD Control Register, as indicated below.

RxE3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				DL from NR	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	R/W	R/W	R/W	RUR
0	0	0	0	0	0	0	X

Writing a “1” into this bit-field enables the Receive LAPD Message Interrupt. Conversely, writing a “0” into this bit-field disables the Receive LAPD Message Interrupt.

Servicing the Receive LAPD Message Interrupt

Whenever the XRT72L50 Framer IC generates this interrupt, it will do the following.

- It will assert the Interrupt Request output pin ($\overline{\text{Int}}$), by driving it "Low".
- It will set Bit 0 (RxLAPD Interrupt Status), within the Rx E3 LAPD Control register to “1”, as indicated below.

RxE3 LAPD Control Register (Address = 0x18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				DL from NR	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	R/W	R/W	R/W	RUR
0	0	0	0	0	0	1	1

- It will write the contents of the newly Received LAPD Message into the Receive LAPD Message buffer (located at 0xDE through 0x135).

Whenever the Terminal Equipment encounters the Receive LAPD Message Interrupt, then it should read out the contents of the Receive LAPD Message buffer, and respond accordingly.

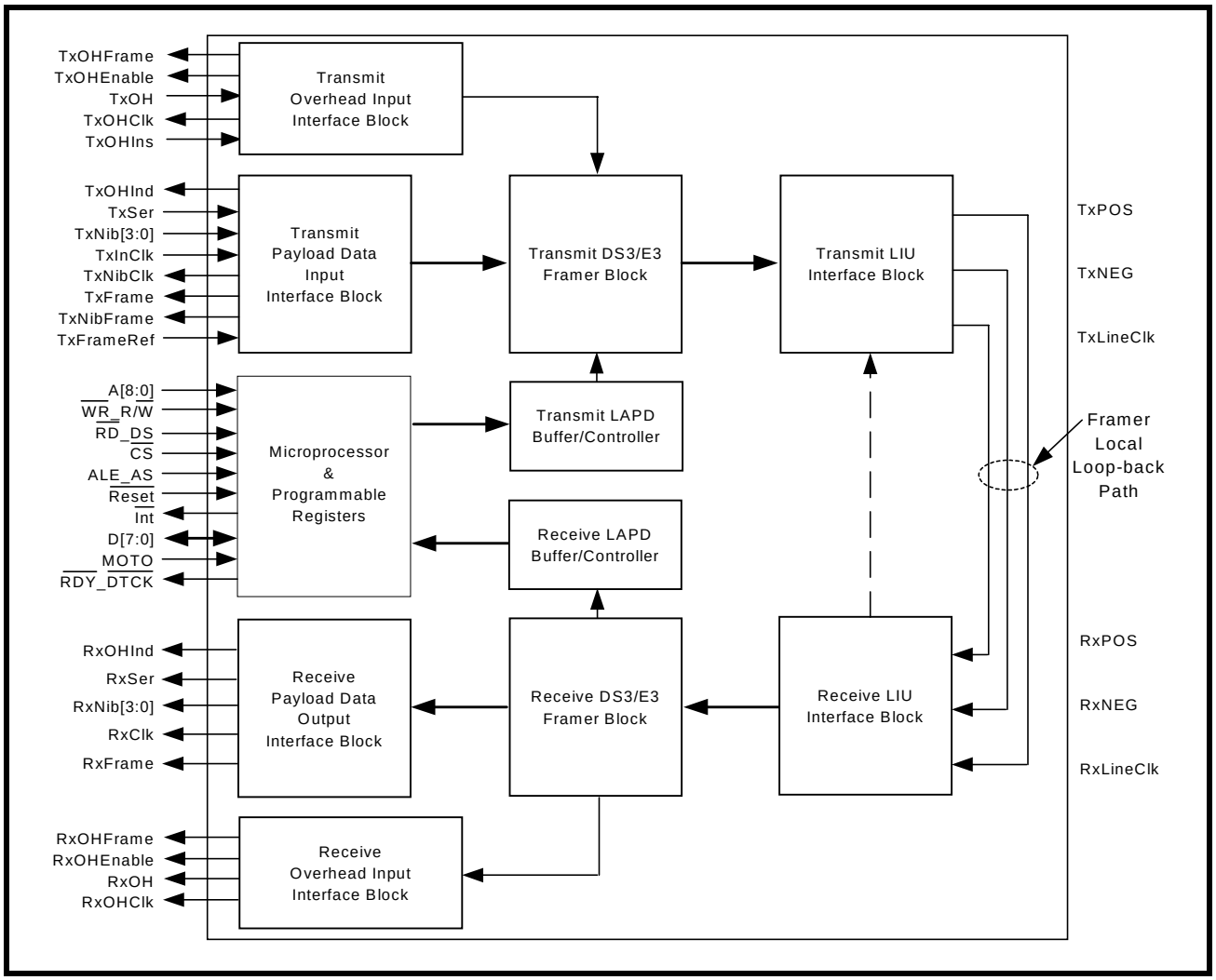
7.0 DIAGNOSTIC OPERATION OF THE XRT72L50 FRAMER IC

The XRT72L50 DS3/E3 Framer IC permits the user to command it to operate in the Framer Local Loop-back Mode. When the user does this then the data will be as follows.

1. Data enters the XRT72L50 via both the Transmit Payload Data Input Interface and the Transmit Overhead Data Input Interface blocks.
2. This data is processed through the Transmit DS3/E3 Framer block and the Transmit DS3/E3 LIU Interface block.
3. This Transmit Output data is internally looped-back into the Receive Path via the Receive LIU Interface block.
4. This data will be processed through the Receive DS3/E3 Framer block and arrive at both the Receive Payload Data Output Interface and Receive Overhead Data Output Interface blocks, where this data outputs to the terminal equipment.

The Framer Local Loop-back Path is illustrated in Figure 200.

FIGURE 200. THE FRAMER LOCAL LOOP-BACK PATH WITHIN THE XRT72L50 DS3/E3 FRAMER IC



The user can configure the XRT72L50 into the Framer Local-Loop-back Mode by writing a “1” into bit-field 7 (Local Loop-back) within the Framer Operating Mode Register, as illustrated below.

FRAMER OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Local Loop-back	DS3/$\overline{E3}$	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	X	0	X	X	X	X

When the XRT72L50 DS3/E3 Framer IC is operating in the Framer Local-Loop-back Mode, no data will be output via the TxPOS and TxNEG output pins.

The XRT72L50 cannot be configured to operate in the Framer Local Loop-back Mode if it is configured to operate in Mode 1 or Mode 4 (Loop-Timing Modes). The XRT72L50 Framer must be configured to operate in one of the Local-Timing modes.

8.0 HIGH SPEED HDLC CONTROLLER MODE OF OPERATION

The XRT72L50 can be configured to operate in the High-Speed HDLC Controller Mode. Whenever it is configured to operate in this mode then the following happens:

1. The Transmit Section of the XRT72L50 will be configured to accept outbound data from the user's Terminal Equipment via an 8-bit wide input interface labeled TxHDLCDat[7:0]. The Transmit Section then encapsulates all data that it receives via TxHDLCDat[7:0].
2. The Transmit Section of the XRT72L50 then encapsulates all data that it receives via the TxHDLCDat[7:0] interface into HDLC frames. These HDLC frames are variable-length packets transported to the remote terminal equipment via the outbound DS3 or E3 payload data bits.
3. As the Transmit Section accepts and processes data from the user's terminal equipment, it performs all the necessary "0" stuffing into the outbound HDLC frame in order to prevent the user-supplied data from mimicking either the flag sequence octet (0x7E) or the ABORT sequence.
4. The Transmit Section can also be configured to compute and append either a 16-bit or 32-bit CRC value to the end of this "0" stuffed user's data as a trailer.
5. Whenever the Transmit Section has no user data to send to the remote terminal equipment via HDLC frames, then it transmits a continuous stream of flag sequence octets (0x7E) via the DS3 or E3 payload bits.
6. The Receive Section of the XRT72L50 will be configured to receive and extract out these HDLC frames via the inbound DS3/E3 data stream. The Receive Section then outputs the contents of these received HDLC frames in a byte-wide manner via the RxHDLCDat[7:0] output pins.
7. If the Receive Section of the XRT72L50 is only receiving a stream of flag sequences (0x7E), then it will terminate this data stream and will not output any data via the RxHDLCDat[7:0] output pins.
8. As the Receive Section of the XRT72L50 receives these HDLC frames, it does the following.

- Compute and verify the 16-bit or 32-bit CRC value which has been appended to the HDLC frame, as a trailer.
- Perform the necessary "0" un-stuffing in order to restore the original content of the user-supplied data.

8.1 *Configuring the XRT72L50 to operate in the High Speed HDLC Controller Mode*

The XRT72L50 can be configured to operate in the High-Speed HDLC Controller Mode bit 6 (HDLC ON) within HDLC Control register address location 0x82, to "1", as depicted below.

NOTE: *The NibIntf pin (25), must also be set "High" for HDLC mode of operation.*

HDLC Control Register (Address = 0x82)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framer By-Pass	HDLC ON	CRC-32 Select	Reserved	HDLC Loop-Back	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	0	0	0	0	0

8.2 *Operating the High Speed HDLC Controller*

Once the user has configured the XT72L50 to operate in the High-Speed HDLC Controller Mode, then both the Transmit and Receive HDLC Controller blocks will be active.

8.2.1 Operating the Transmit HDLC Controller Block

Once the XRT72L50 has been configured to operate in the High-Speed HDLC Controller mode, then certain pins, which have multiple functions, are configured to support operation of the Transmit and Receive HDLC Controller blocks.

The Transmit HDLC Controller block within the XRT72L50 consists of the following pins

TABLE 89: DESCRIPTION OF EACH OF THE TRANSMIT HDLC CONTROLLER PIN

PIN NAME	TYPE	DESCRIPTION
Snd_Msg	I	**Send Message Command:** This input pin permits the user to command the Transmit HDLC Controller block to begin sampling and latching the data which is being applied to the TxHDLCDat[7:0] input pins. If the user pulls this input pin "High", then the Transmit HDLC Controller block samples and latches the data which is applied to the TxHDLCDat[7:0] input pins upon the rising edge of TxHDLCClk. Each byte of this sampled data will ultimately be encapsulated into an outbound HDLC Frame. If the user pulls this input pin "Low", then the Transmit HDLC Controller block will simply generate a constant stream of Flag Sequence octets (0x7E).
Snd_FCS	I	**Send Frame Check Sequence Command:** The user's terminal equipment is expected to control both this input pin and the Snd_Msg input pin during the construction and transmission of each outbound HDLC frame. This input pin permits the user to command the Transmit HDLC Controller block to compute and insert the compute FCS value into the back-end of the outbound HDLC frame as a trailer. If the user has configured the Transmit HDLC Controller to compute and insert a CRC-16 value into the outbound HDLC frame, then the terminal equipment is expected to pull this input pin "High" for two periods of TxHDLCClk. If the user has configured the Transmit HDLC Controller to compute and insert a CRC-32 value into the outbound HDLC frame, then the terminal equipment is expected to pull this input pin "High" for four periods of TxHDLCClk.

TABLE 89: DESCRIPTION OF EACH OF THE TRANSMIT HDLC CONTROLLER PIN

PIN NAME	TYPE	DESCRIPTION
TxHDLCClk	O	**Transmit HDLC Controller Clock Output signal:** This output signal functions as the demand clock for the Transmit HDLC Controller. When the user pulls the Snd_Msg input pin "High" then the Transmit HDLC Controller block begins to sample and latch the contents of the TxHDLCDat[7:0] upon the falling edge of this clock signal. The user is advised to configure their terminal equipment circuitry to output data onto the TxHDLCDat[7:0] bus upon the rising edge of this clock signal. Since the Transmit HDLC Controller block is sampling and latching 8-bits of data at a given time, it may be presumed that the frequency of the TxHDLCClk output signal is either 34.368MHz/8 or 44.736MHz/8. In general, this presumption is true. However, because the Transmit HDLC Controller is also performing “0” stuffing of the user data that it receives from the Terminal Equipment, the frequency of this signal may be slower.
TxHDLCData[7:0]	I	**Transmit HDLC Controller - Input Data Bus:** These eight input pins function as the byte-wide input interface to the Transmit HDLC Controller. If the user pulls the Snd_Msg input pin "High", then the Transmit HDLC Controller block begins to sample and latch the contents of this data bus into the Transmit HDLC Controller circuitry upon the falling edge of TxHDLCClk. All data that is sampled via this byte-wide interface will ultimately be encapsulated into an outbound HDLC Controller. LSB of the TxHDLCData[7:0] is transmitted first. If the user pulls the Snd_Msg input pin "Low", then the Transmit HDLC Controller block will ignore the data that is being applied to this data bus.

Pull the Snd_Msg input pin "High" to transmit data via the Transmit HDLC Controller block. Once the Snd_Msg pin is pulled high, then the Transmit HDLC Controller block will begin to sample the data on the TxHDLCDat[7:0] input pins upon the falling edge of the TxHDLCClk clock output signal. Each byte of data that is sampled and latched into the Transmit HDLC Controller block will be encapsulated into an outbound HDLC frame.

After the last byte of data has been latched into the Transmit HDLC Controller block, then the user must pull the Snd_FCS input pin "High" for either two or four TxHDLCClk clock periods.

If the user has configured the Transmit HDLC Controller block to append a 16-bit CRC value (from here on, referred to as CRC-16); then the user must pull and hold the Snd_FCS input pin "High" for two (2) TxHDLCClk clock periods. Conversely, if the user has configured the Transmit HDLC Controller block to append a 32 bit CRC value (from here on, referred to as CRC-32); then the user must pull and hold the Snd_FCS input pin "High" for (4) TxHDLCClk periods. Pulling the Snd_FCS input pin "High" configures the Transmit HDLC Controller to begin its insertion of either the CRC-16 or CRC-32 value into the back-end of the outbound HDLC Controller.

Figure 201ansd Figure 202indicateTxHDLC timing for the CRC16 and CRC32 modes.

An abort sequence may be transmitted by setting Snd_FCS “High” while Snd_MSG is set “Low”.

FIGURE 201. TXHDLC TIMING FOR CRC16

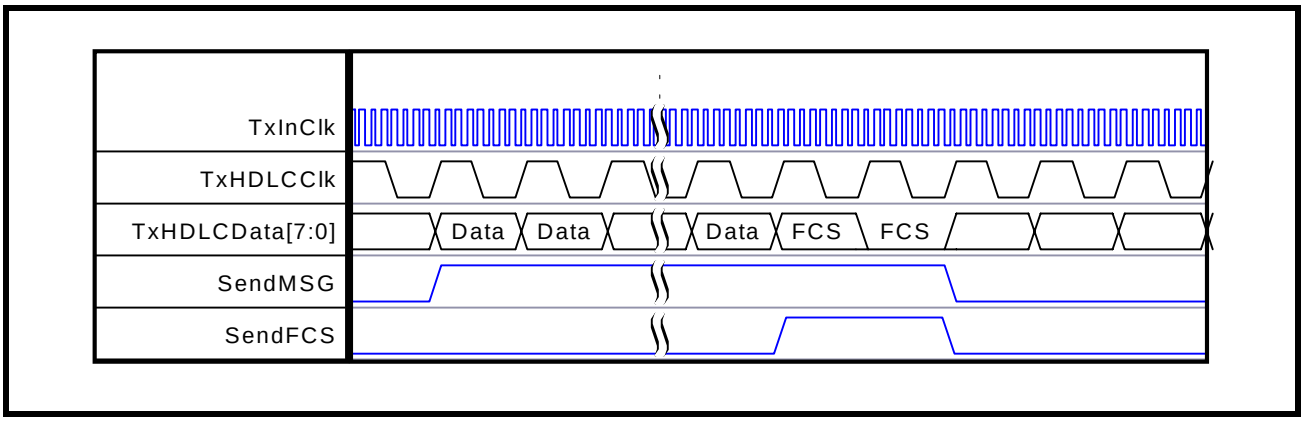
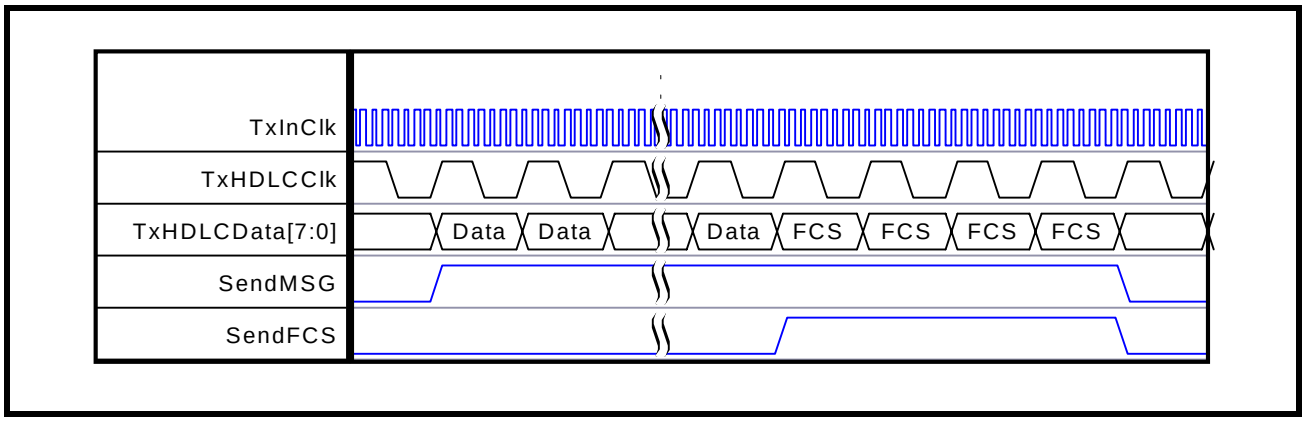


FIGURE 202. TXHDLC TIMING FOR CRC32



Selecting either CRC-16 or CRC-32

The user can configure the Transmit HDLC Controller block to append either a CRC-16 or CRC-32 value to the user-data within the outbound HDLC frame, by writing the appropriate value into Bit 5 (CRC-32 Select). Setting this bit-field "High" configures the Transmit HDLC Controller block to append a CRC-32 value to the user data, within the outbound HDLC frame. Conversely, setting this bit-field "Low" configures the Transmit HDLC Controller block to append a CRC-16 value to the user data, within the outbound HDLC frame.

An illustration of the resulting outbound HDLC Frame when CRC-32 and CRC-16 is selected is shown in Figure 203and Figure 204.

FIGURE 203. AN OUTBOUND HDLC FRAME WHEN CRC-32 IS SELECTED.

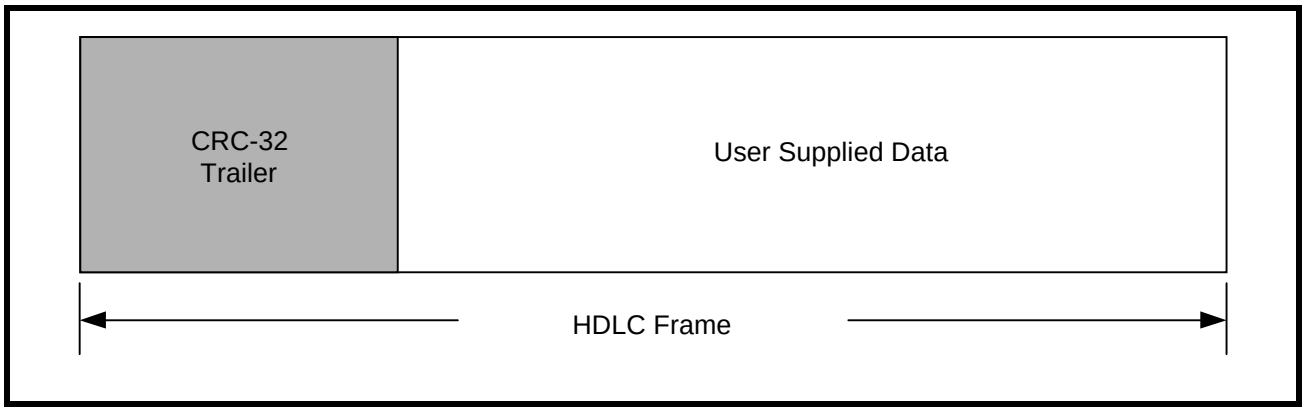
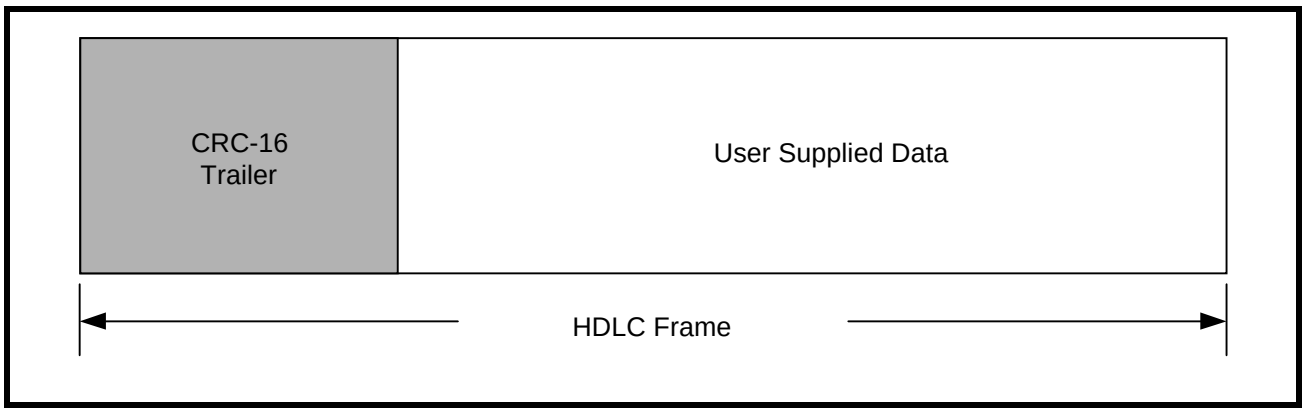


FIGURE 204. AN OUTBOUND HDLC FRAME WHEN CRC-16 IS SELECTED



Once the outbound HDLC frame has been formed, then it will be transmitted to the remote terminal equipment via payload bits of the outbound DS3 or E3 frames.

If the user's terminal equipment does not supply any more data which needs to be encapsulated into the outbound HDLC frame and transmitted to the remote terminal equipment, then the Transmit HDLC Controller block begins transmitting a constant stream of flag sequence octets (0x7E). These flag sequence octets will also be transmitted to the remote terminal equipment via the payload bits of the outbound DS3 or E3 frames.

8.2.2 Operating the Receive HDLC Controller Block

The Receive HDLC Controller block within the XRT72L50 consists of the following pins:

TABLE 90: DESCRIPTION OF EACH OF THE RECEIVE HDLC CONTROLLER PINS

PIN NAME	TYPE	DESCRIPTION
RxIdle	O	**Receive Idle (Flag Sequence) Indicator Signal** The combination of the RxIdle and Val_FCS output signals are used to convey information about data that is being received via the Receive HDLC Controller block. **If RxIdle = "High":** The Receive HDLC Controller block pulses this output pin "High" any time the flag sequence is present on the RxHDLCDat[7:0] output data bus. **If RxIdle and Val_FCS are both "High":** The Receive HDLC Controller block has received a complete HDLC frame and has determined that the FCS value within this HDLC frame is valid. **If RxIdle is "High" and Val_FCS is "Low":** The Receive HDLC Controller block has received a complete HDLC frame and has determined that the FCS value within this HDLC frame is invalid. **If RxIdle is "Low" and Val_FCS is "High":** The Receive HDLC Controller block has received an ABORT sequence.
Val_FCS	O	**Valid FCS Indicator Signal** Please see description above.
RxHDLCClk	O	**Receive HDLC Controller Clock Output signal:** The Receive HDLC Controller block outputs data via the RxHDLCDat[7:0] output pins upon the rising edge of this clock signal. The user is advised to configure the terminal equipment circuitry to sample the contents of the RxHDLCDat[7:0] output pins upon the falling edge of this clock signal.
RxHDLCData[7:0]	I	**Receive HDLC Controller - Output Data Bus:** The Receive HDLC Controller block outputs data via these output pins upon the rising edge of the RxHDLCClk clock signal. The user is advised to configure the terminal equiment circuitry to sample the contents of this data bus upon the falling edge of this clock signal.

8.2.2.1 *Receive Payload HDLC Processor*

The receiver HDLC processor is the counter part of the transmit HDLC processor for formatting the payload portion of the receive DS3/E3 data that is activated when the HDLCon bit in the HDLC Control register (0x82) is set.

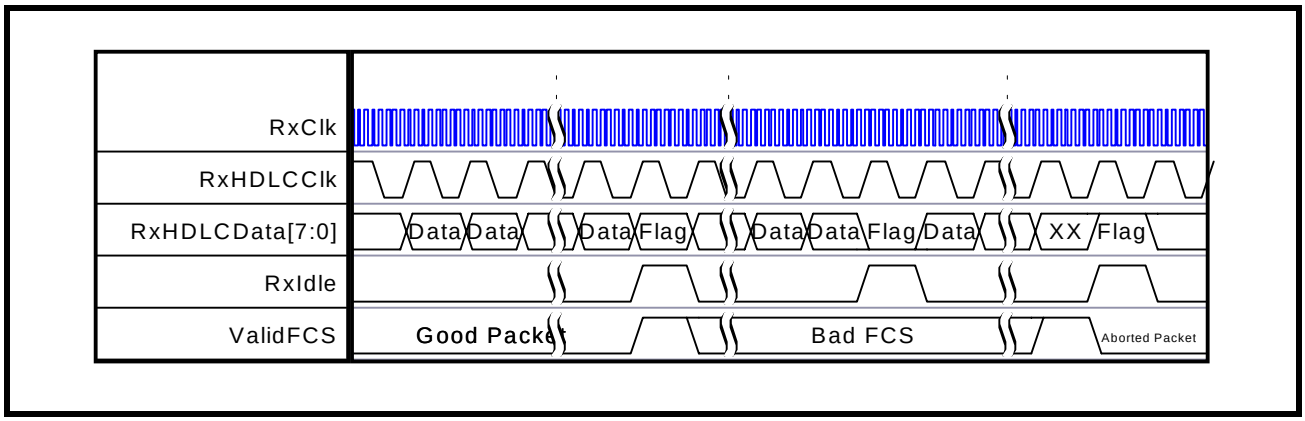
This receiver performs idle flag detection, stuffed zero removal, and FCS checking on the incoming data stream. The recovered data bytes are presented on RxHDLCData[7:0] and are valid on the rising edge of RxHDLCClk . The LSB is on RxHDLCData[0] and the MSB on RxHDLCData[7]; the LSB is the first received from the serial input. User should sample RxHDLCData on falling edge of RxHDLCClk.

If the payload stream contains idle flags, the IDLE pin will be high and the flags will be present on RxHDLCData[7:0]. If a valid FCS is received at the end of the message block, the ValidFCS pin will be active high while RxIDLE is high. At the start of the next message, both indications will go low until the end of the incoming message has been received. If a bad FCS is received, RxIDLE will go high and ValidFCS will remain low. If ValidFCS goes high and RxIDLE does not, an abort sequence was received in the data. If there is only

one flag received between incoming packets, there will be only one RxHDLCClk pulse present while RxIDLE is high. Timing for this operation is shown in Figure 205.

RxHDLCClk is generated from the receive DS3/E3 clock and is present continuously like the transmit byte clock. Nominally there will be one pulse on RxHDLCClk for every eight clock cycles on the receive DS3/E3 clock. When an inserted transparency bit must be deleted or DS3/E3 overhead bits skipped, the clock period will be stretched by one or more DS3/E3 clock cycles. RxHDLCClk is present during the reception of FCS octets and idle flags.

FIGURE 205. TIMING DIAGRAM FOR RXHDLC OPERATION

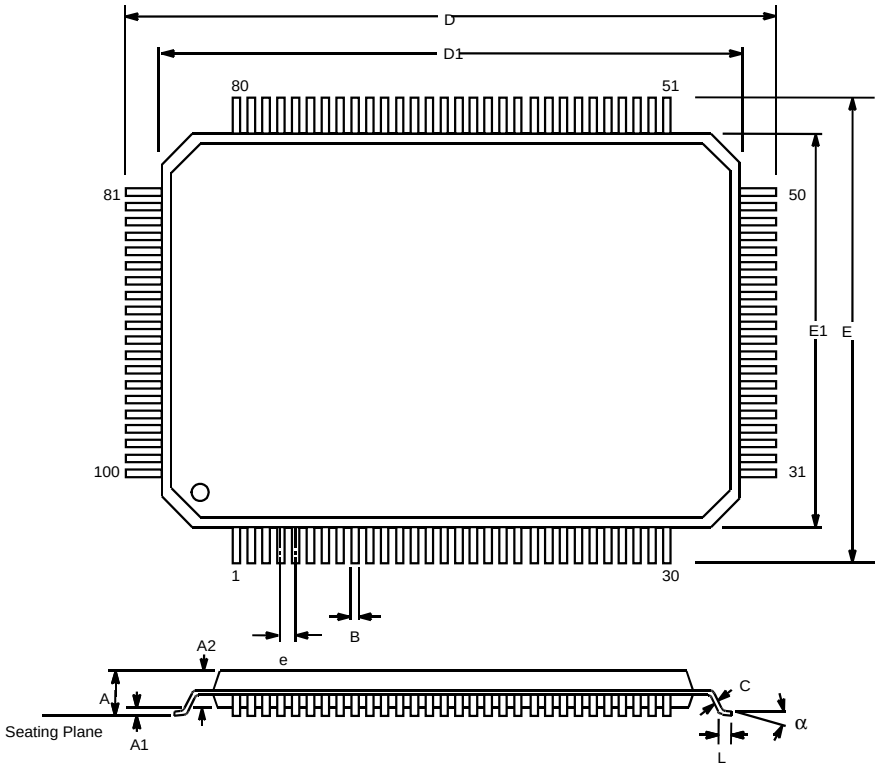


ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT72L50IQ	14x20mm, 100 Lead Plastic QFP	-40°C to +85°C

PACKAGE DIMENSIONS

100 LEAD PLASTIC QUAD FLAT PACK
(14 mm x 20 mm, QFP)
Rev. 2.00



	1.95 mm Form			
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.102	0.134	2.60	3.40
A_1	0.002	0.014	0.05	0.35
A_2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
C	0.005	0.009	0.13	0.23
D	0.931	0.951	23.65	24.15
D_1	0.783	0.791	19.90	20.10
E	0.695	0.715	17.65	18.15
E_1	0.547	0.555	13.90	14.10
e	0.0256 BSC		0.65 BSC	
L	0.026	0.037	0.65	0.95
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

REVISION HISTORY

Added sections on HDLC controller.

Rev 1.1.3 -- Made corrections to figures 37, 38, 39, 65, 75, 102, 120, 130, 161, 163, 178 and 188.

Rev 1.1.4 -- Figure 2: Pin Out diagram & Pin List were incorrect, made corrections.

Rev 1.1.5 -- Corrected many errors and typos in body of the document.

Rev 1.2.0 -- Made final additional corrections to tables, figures, timing diagrams and body text descriptions of operation. Removed preliminary designation.

Rev 1.2.1 -- Added registers (address 0x58, 0x59 and 0x4B).

NOTICE

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Single-Channel DS3/E3 Framer IC with HDLC Controller

Features

- HDLC provide higher levels of integration and better payload management
- All devices accept user data from terminal equipment
- Low power 3.3V operation
- Functions over industrial temperature range
- Pb-Free, RoHS Compliant Versions Offered

Applications

- DS3/E3 frame relay equipment
- Fiber optic terminals
- PCM test equipment
- CSU/DSU equipment
- Network interface cards

Description

Innovative silicon solutions are a hallmark of Exar's products for the communications markets. Exar offers a full line of multi-channel (1, 2, 3, 4, 6, & 8) framers for DS3/E3 network access applications including network interface units, CSU/DSU equipment, PCM test equipment, fiber optic terminals, and frame relay equipment.

These DS3/E3 access control devices meld seamlessly with Exar's industry proven physical-interface components (transceivers and jitter attenuators) offering designers maximum integration and shortened time-to-market. Whatever your design requirement, Exar is the clear choice.

Designers have a wide range of Exar framer options that expand their ability to deliver complete system solutions. Devices include the XRT72L50 (single-channel), XRT72L52 (dual-channel), XRT72L53 (triple-channel), XRT72L54 (four-channel), XRT72L56 (six-channel), and the XRT72L58 (eight-channel) products.

Each of the devices contain individual HDLC controllers for processing transmit and receive channel payloads. This provides designers with the entire link layer for a frame relay access device in a single-chip and achieve better overall payload management. All devices support full-

Specifications	
No. ofCH	1
DataRate(s)	DS3, E3
Temp.Range	Ind.
OpPwr Sup/Max Cur	3V ±5%
Pkgs	PQFP-100

Documents

Datasheets

Datasheet
Version 1.2.1
October 2003
5.42 MB

Application Notes

TAN-200, Exar APIs - OS Portability
Version 1.0.0
August 2007
88.46 KB

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duplex data flow between the terminal equipment and a transceiver. In addition, they interface with all popular microprocessors.

The family will frame data in all standard DS3 and E3 formats: DS3 C-bit parity, DS3 M13, E3 ITU-T G.751 and E3 ITU-T G.832. Also, the devices have a performance monitoring section where a large number of "Reset-upon-Read" and "Read-Only" registers will contain cumulative and "one-second" statistics reflecting the performance and health of the overall IC system.

Part Number	Pkg Code	RoHS	Min Temp. (°C)	Max Temp. (°C)	Status	Buy Now	Order Samples
XRT72L50IQ-F	PQFP100		-40	85	Active		

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