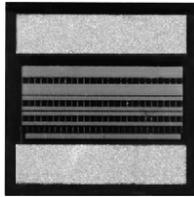
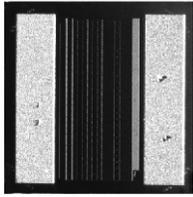


NiCr Thin Film, Top-Contact Resistor



Product may not be to scale

FEATURES

- Wire bondable
- Small single chip size: 0.050 inches square
- Resistance range: 100 Ω to 50 kΩ
- Resistor material: Nichrome
- Oxidized silicon substrate for good power dissipation
- 400 mW capability
- User trimmable

The SC3 series resistor chips on silicon offer a combination of nichrome stability, wide resistance range and higher power rating than is available on the same sized ceramic substrate.

The SC3's are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SC3s are 100 % electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

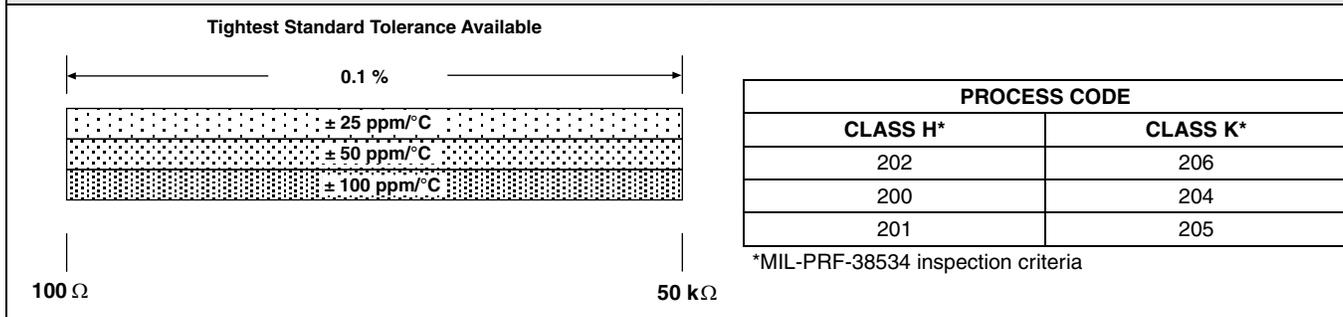
Vishay EFI SC3 chip resistors have excellent power dissipation capability and are ideally suited for prototyping.

Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

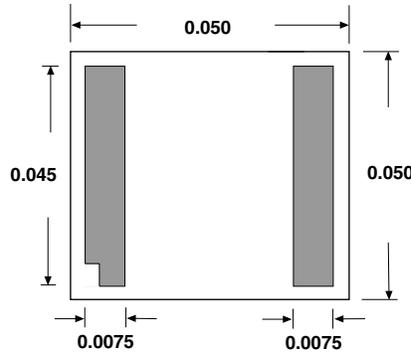
Recommended for hermetic environments where die is not exposed to moisture.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20 dB typ.
Stability, 1000 h, + 125 °C	± 0.1 % max. ΔR/R
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 % max. ΔR/R
High Temperature Exposure, + 150 °C, 100 h	± 0.25 % max. ΔR/R
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10 ¹² min.
Operating Voltage	100 V max.
DC Power Rating at + 70 °C (Derated to Zero at + 150 °C)	400 mW
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 % max. ΔR/R

DIMENSIONS in inches

SCHEMATIC


MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.050 x 0.050 ± 0.003 (1.27 x 1.27 ± 0.076 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Nichrome
Bonding Pad Size	0.0075 x 0.045 (0.190 x 1.143 mm) minimum
Number of Pads	2
Pad Material	15 kÅ minimum gold standard
Backing	None, lapped semiconductor silicon

- Options:** Gold backing for eutectic die attach
 Aluminum bonding pads, 10 kÅ minimum thickness
 User trimmable
 Consult Applications Engineer

ORDERING INFORMATION					
Example: 100 % visual, 500 Ω, ± 10 %, ± 50 ppm/°C TCR, gold pads, class H visual inspection					
W	SC3	200	5000	A	K
INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100 % visually inspected parts in matrix tray per MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4 % AQL)		See Process Code table	Use the first 4 significant digits of the resistance	B = 0.01 A = 0.1 0 = 1 1 = 10 2 = 100	B = 0.1 % D = 0.5 % F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 %



Disclaimer

All product specifications and data are subject to change without notice.

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