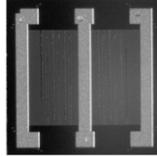
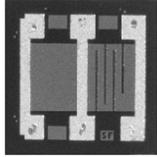


Thin Film Resistors on Silicon, User Trimmable



Product may not be to scale

The SC7 and SCB series resistor chips offer a combination of nichrome user trimmability as a single resistor or as a ratio trim while maintaining the excellent TCR tracking characteristics of two resistors on the same chip.

The SC7 and SCBs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SC7 and SCBs are 100 % electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

Vishay EFI SC7 and SCB chip resistors have excellent power dissipation capability and are ideally suited for prototyping. Typical application areas are:

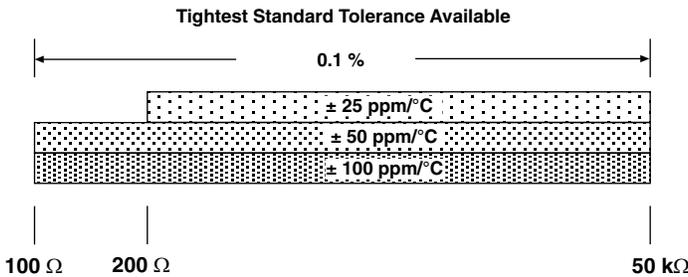
- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture

FEATURES

- Wire bondable
- Chip sizes
SC7 - 0.030 inches square
SCB - 0.050 inches square
- Resistance range R_T : 100 Ω to 20 k Ω for SC7
Resistance range R_T : 100 Ω to 50 k Ω for SCB
- Silicon substrate
- Power: 250 or 400 mW capability
- Resistor material: Nichrome
- User trimmable

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE			
SC7		SCB	
CLASS H*	CLASS K*	CLASS H*	CLASS K*
220	224	220	224
221	225	221	225
222	226	222	226

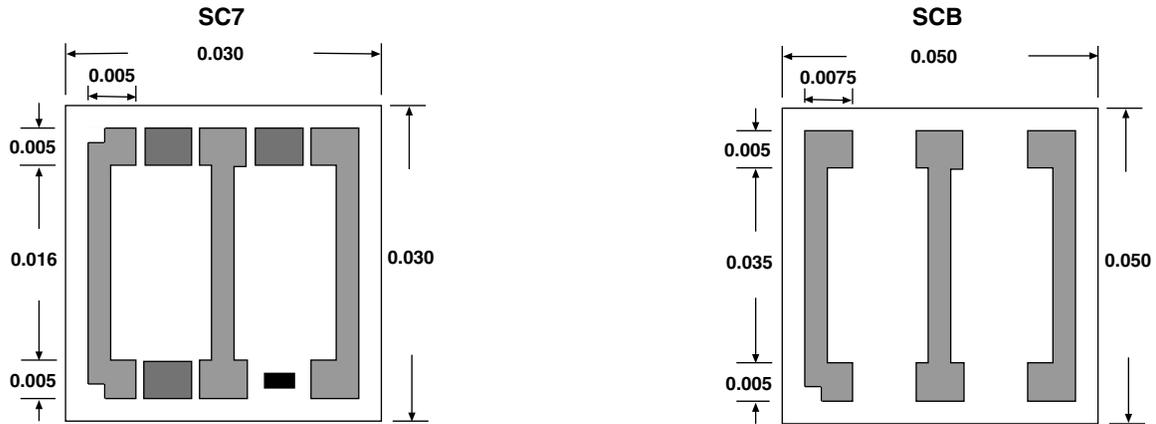
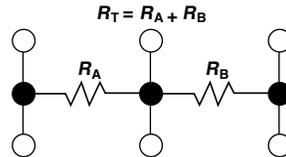
*MIL-PRF-38534 inspection criteria
 R_A user trimmable 50 % above
 R_T value specified in P/N

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308	- 20 dB typ.
Stability, 1000 h, + 125 °C at Rated Power	± 0.2 % max. $\Delta R/R$
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 % max. $\Delta R/R$
High Temperature Exposure, + 150 °C, 100 h	± 0.25 % max. $\Delta R/R$
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10^{12} min.
Operating Voltage	100 V max.
DC Power Rating at 70 °C Derated to Zero at 150 °C	250 mW max. (0.030 inches) 400 mW max. (0.050 inches)
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	+ 0.25 % max. $\Delta R/R$

Note:

- Performance characteristics are not guaranteed once user trimmed

DIMENSIONS in inches

SCHEMATIC


MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.030 x 0.030 ± 0.003 (0.76 x 0.76 ± 0.076 mm) 0.050 x 0.050 ± 0.003 (1.27 x 1.27 ± 0.076 mm)
Chip Thickness	0.010 ± 0.002 (0.25 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Nichrome
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127 mm) minimum
Number of Pads	6
Pad Material	15 kÅ minimum gold standard
Backing	None, lapped semiconductor silicon

Options: Gold back for solder die attach
Consult Application Engineer

ORDERING INFORMATION					
Example: 100 % visualled, $R_T = 500$, ± 10 %, ± 50 ppm/°C TCR, R_A user trim gold pads, class H visual inspection					
Standard user trim versions will be supplied with R_A untrimmed					
For custom R_A , R_B combinations consult Application Engineer					
W	SC7	221	5000	A	K
INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100 % visually inspected parts in matrix MIL-STD-883 X = Sample, commercial visually inspected parts loaded in matrix trays (4 % AQL)	SC7 SCB	See Process Code table	Use first 4 digits significant digits of the resistance (R_T)	B = 0.01 A = 0.1 0 = 1 1 = 10	B = 0.1 % D = 0.5 % F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 % M = 20 %



Disclaimer

All product specifications and data are subject to change without notice.

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