

# Low Skew, Low Additive Jitter 10 output LVPECL/LVDS/HCSL Fanout Buffer with one LVC MOS output

## Features

- 3 to 1 input Multiplexer: Two inputs accept any differential (LVPECL, HCSL, LVDS, SSTL, CML, LVC MOS) or a single ended signal and the third input accepts a crystal or a single ended signal
- Ten differential LVPECL/LVDS/HCSL outputs
- One LVC MOS output
- Ultra-low additive jitter: 24fs ( integration band: 12kHz to 20MHz at 625MHz clock frequency)
- Supports clock frequencies from 0 to 1.6GHz
- Supports 2.5V or 3.3V power supplies on LVPECL/LVDS/HCSL outputs
- Supports 1.5V, 1.8V, 2.5V or 3.3V on LVC MOS output
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 40ps
- Device controlled via SPI or hardware control pins

## Ordering Information

ZL40230LDG1	48 Pin QFN	Trays
ZL40230LDF1	48 pin QFN	Tape and Reel

Package size: 7 x 7 mm  
-40°C to +85°C

## Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3/4 clock distribution
- Wireless communications
- High performance microprocessor clock distribution
- Test Equipment

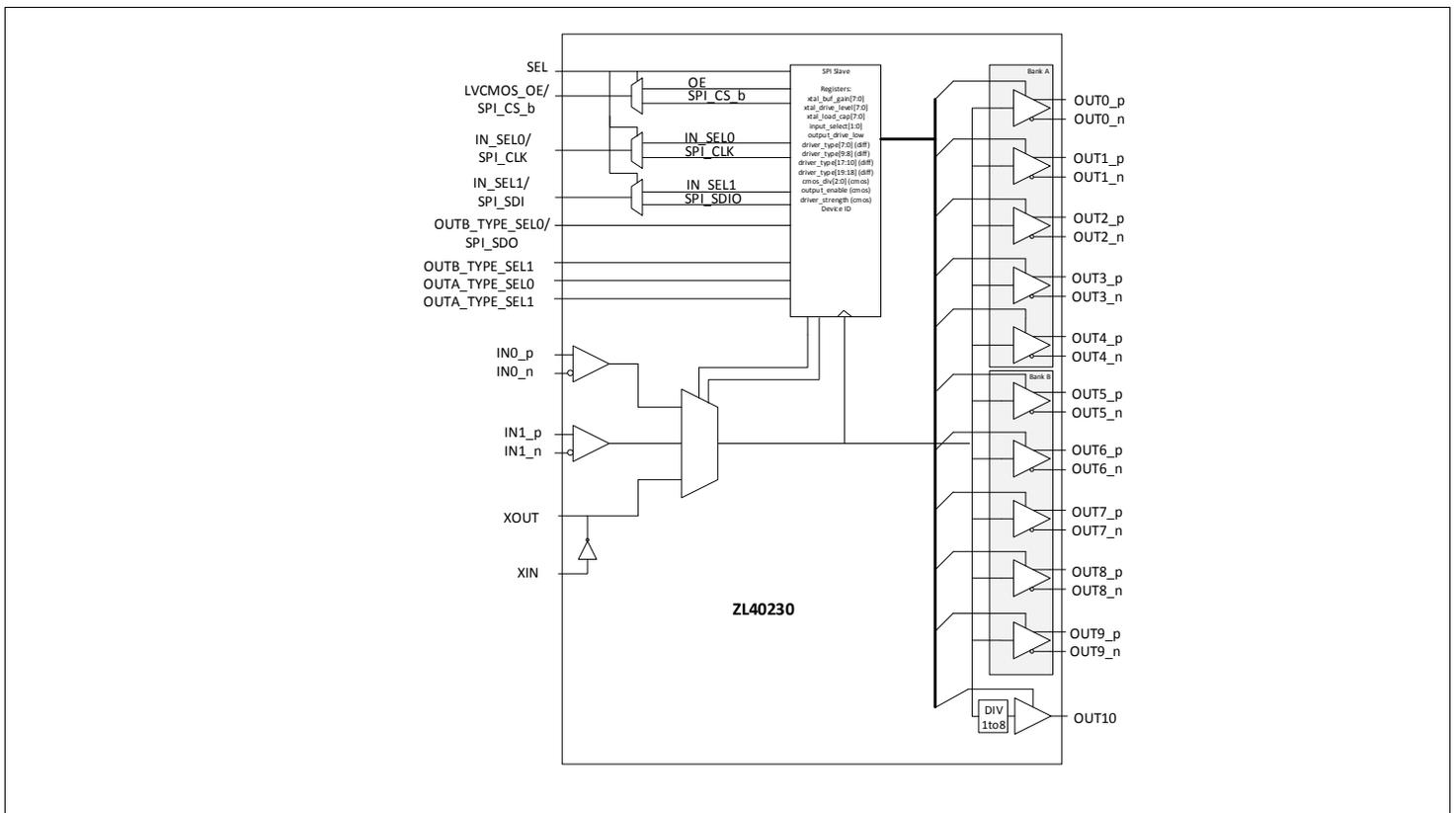


Figure 1. Functional Block Diagram

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## Pin Diagram

The device is packaged in a 7x7mm 48-pin QFN.

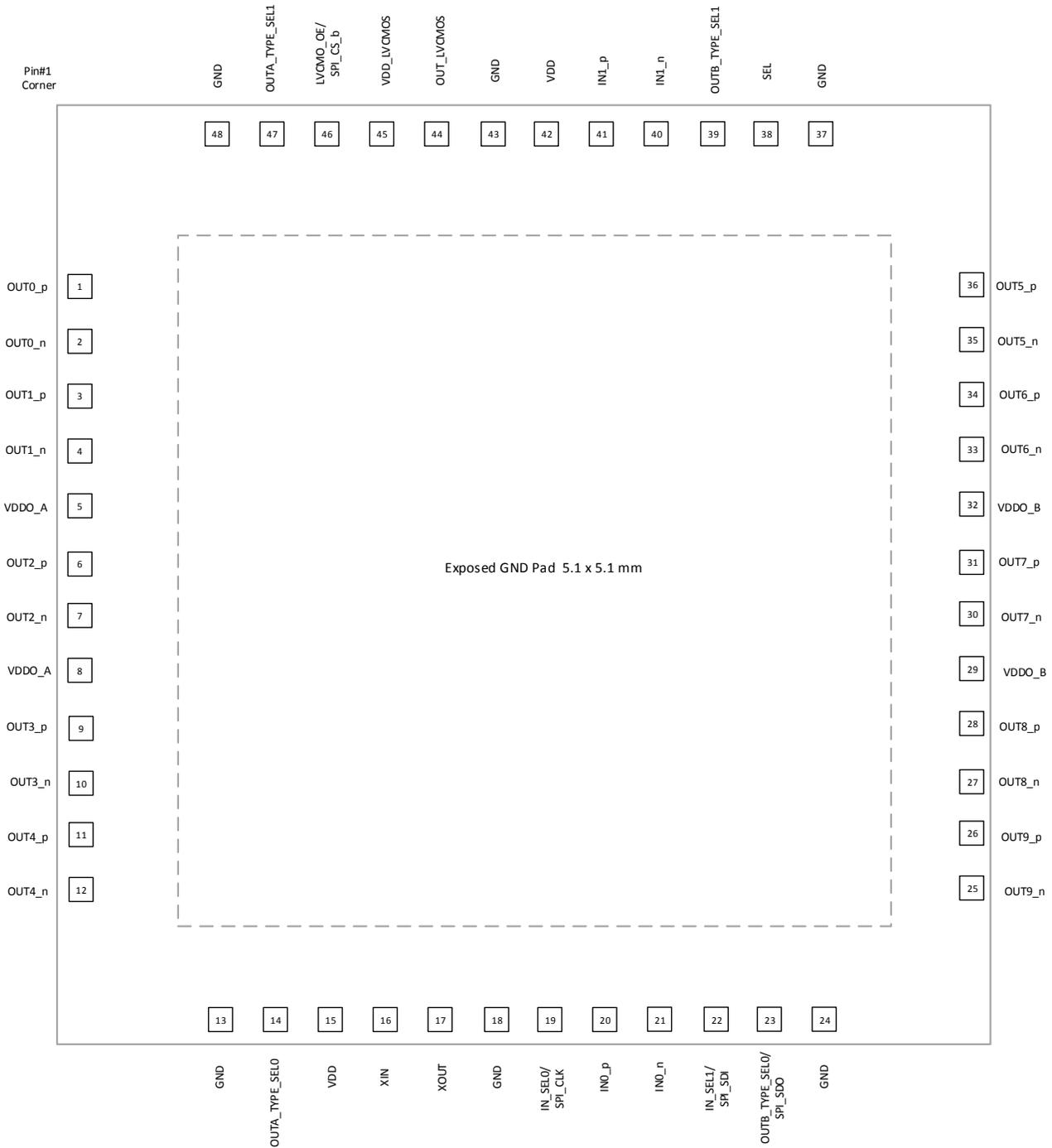


Figure 2. Pin Diagram

## Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I<sub>PU</sub> – input with 300kΩ internal pull-up resistor, I<sub>PD</sub> – input with 300kΩ internal pull-down resistor, I<sub>APU</sub> – input with 31kΩ internal pull-up resistor, I<sub>APD</sub> – input with 30kΩ internal pull-down resistor, I<sub>APU/APD</sub> – input biased to VDD/2 with 60kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC – No connect, P – power supply pin.

**Table 1 Pin Descriptions**

#	Name	I/O	Description
<b>Input Reference</b>			
20 21 41 40	IN0_p IN0_n IN1_p IN1_n	I <sub>APD</sub> I <sub>APU/APD</sub> I <sub>APD</sub> I <sub>APU/APD</sub>	<p><b>Differential/Single Ended References 0 and 1</b></p> <p>Input frequency range 0Hz to 1.6GHz.</p> <p>Non inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60kΩ internal resistors (30kΩ equivalent) to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).</p>
<b>Output Clocks</b>			
1 2 3 4 6 7 9 10 11 12 36 35 34 33 31 30 28 27 26 25	OUT0_p OUT0_n OUT1_p OUT1_n OUT2_p OUT2_n OUT3_p OUT3_n OUT4_p OUT4_n OUT5_p OUT5_n OUT6_p OUT6_n OUT7_p OUT7_n OUT8_p OUT8_n OUT9_p OUT9_n	O	<p><b>Ultra Low Additive Jitter Differential LVPECL/HCSL/LVDS Outputs 0 to 9</b></p> <p>Output frequency range 0 to 1.6GHz</p> <p>In SPI bus controlled mode (SEL pin pulled high on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output is programmable via SPI bus</p> <p>In Hardware control mode (SEL pin pulled low on the power up) type (LVPECL/HCSL/LVDS/High-Z) of each output bank is controlled via OUTA/B_TYPE_SEL0/1 pins.</p>
44	OUT_LVCMOS	O	<p><b>Ultra Low Additive Jitter LVCMOS Output 0 to 9</b></p> <p>Output frequency range 0 to 250MHz</p>
<b>Control</b>			

19	IN_SEL0/SPI_CLK	$I_{PD}$ or $I_{PU}$	<p><b>Input Select 0 or Clock for Serial Interface</b> When SEL pin is low this pin is Input Select 0 hardware control input pin and it is pulled-down with 300 k<math>\Omega</math> resistor. When SEL pin is high this pin provides clock for serial micro-port interface and it is pulled-up with 300 k<math>\Omega</math> resistor.</p> <table border="1" data-bbox="620 331 1510 562"> <thead> <tr> <th>IN_SEL1</th> <th>IN_SEL0</th> <th>OUTN</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Input 0 (IN0)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Input 1 (IN1)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Crystal Oscillator or overdrive</td> </tr> <tr> <td>1</td> <td>1</td> <td>Crystal Bypass</td> </tr> </tbody> </table>	IN_SEL1	IN_SEL0	OUTN	0	0	Input 0 (IN0)	0	1	Input 1 (IN1)	1	0	Crystal Oscillator or overdrive	1	1	Crystal Bypass
IN_SEL1	IN_SEL0	OUTN																
0	0	Input 0 (IN0)																
0	1	Input 1 (IN1)																
1	0	Crystal Oscillator or overdrive																
1	1	Crystal Bypass																
22	IN_SEL1/SPI_SDI	$I_{PD}$ or $I_{PU}$	<p><b>Input Select 1 or Serial Interface Input.</b> When SEL pin is low this pin is Input Select 1 hardware control pin and it is pulled-down with 300 k<math>\Omega</math> resistor. When SEL pin is high this pin is serial interface input stream and it is pulled-up with 300 k<math>\Omega</math> resistor. The serial data stream holds the access command, the address and the write data bits.</p>															
23	OUTB_TYPE_SELO SPI_SDO	I/O	<p><b>Output Signal for Bank B or Serial Interface Output.</b></p> <p>When SEL pin is low this pin and pin 39 select type of the output Bank B (outputs 5 to 9).</p> <table border="1" data-bbox="620 919 1510 1155"> <thead> <tr> <th>OUTB_TYPE_SEL1</th> <th>OUTB_TYPE_SELO</th> <th>Output 5 to 9</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>LVPECL</td> </tr> <tr> <td>0</td> <td>1</td> <td>LVDS</td> </tr> <tr> <td>1</td> <td>0</td> <td>HCSL</td> </tr> <tr> <td>1</td> <td>1</td> <td>High-Z (Disabled)</td> </tr> </tbody> </table> <p>When SEL pin is high this pin is Serial interface output stream. As an output the serial stream holds the read data bits.</p>	OUTB_TYPE_SEL1	OUTB_TYPE_SELO	Output 5 to 9	0	0	LVPECL	0	1	LVDS	1	0	HCSL	1	1	High-Z (Disabled)
OUTB_TYPE_SEL1	OUTB_TYPE_SELO	Output 5 to 9																
0	0	LVPECL																
0	1	LVDS																
1	0	HCSL																
1	1	High-Z (Disabled)																
39	OUTB_TYPE_SEL1	$I_{PD}$	<p><b>Output Signal for Bank B</b></p> <p>When SEL pin is low this pin and pin 23 selects type of the output Bank B (outputs 5 to 9).</p> <p>When SEL pin is high this pin is unused and it should be left unconnected or connected to GND for mechanical support.</p>															
46	LVCMOS_OE/ SPI_CS_b	$I_{PD}$ or $I_{PU}$	<p><b>LVCMOS Output Enable or Chip Select for Serial Interface.</b></p> <p>When SEL pin is low this pin is LVCMOS Output Enable hardware control input and it is pulled-down with 300 k<math>\Omega</math> resistor.</p> <p>When SEL pin is high this pin is serial interface chip select and it is pulled-up with 300 k<math>\Omega</math> resistor--this is an active low signal.</p>															

14 47	OUTA_TYPE_SELO OUTA_TYPE_SEL1	I <sub>PD</sub>	<p><b>Output Signal for Bank A:</b></p> <p>When SEL pin is low these two pins Selects Type of the output for Bank A (Outputs 0 to 4)</p> <table border="1"> <thead> <tr> <th>OUTA_TYPE_SEL1</th> <th>OUTA_TYPE_SELO</th> <th>Output 0 to 4</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>LVPECL</td> </tr> <tr> <td>0</td> <td>1</td> <td>LVDS</td> </tr> <tr> <td>1</td> <td>0</td> <td>HCSL</td> </tr> <tr> <td>1</td> <td>1</td> <td>High-Z (Disabled)</td> </tr> </tbody> </table> <p>When SEL pin is high these two pins are unused and should be left unconnected or connected to GND for mechanical support.</p>	OUTA_TYPE_SEL1	OUTA_TYPE_SELO	Output 0 to 4	0	0	LVPECL	0	1	LVDS	1	0	HCSL	1	1	High-Z (Disabled)
OUTA_TYPE_SEL1	OUTA_TYPE_SELO	Output 0 to 4																
0	0	LVPECL																
0	1	LVDS																
1	0	HCSL																
1	1	High-Z (Disabled)																
<b>Crystal Oscillator</b>																		
16	XIN	I	<b>Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode</b>															
17	XOUT	O	<b>Crystal Oscillator Output</b>															
<b>Hardware/SPI Control selection</b>																		
38	SEL	I	<p><b>Select control.</b></p> <p>When this pin is low, the device is controlled via hardware pins, IN_SEL0/1 and OE. When this pin is high, the device is controlled via SPI port.</p> <p>Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly.</p>															
<b>Power and Ground</b>																		
15 42	VDD	P	<b>Positive Supply Voltage.</b> Connect to 3.3V or 2.5V supply.															
5 8	VDDO_A	P	<b>Positive Supply Voltage for Differential Outputs Bank A</b> Connect to 3.3V or 2.5V power supply. VDDO_A does not have to be connected to the same voltage level as VDD or VDDO_B. These pins power up differential outputs OUT[0:4]_p/n.															
29 32	VDDO_B	P	<b>Positive Supply Voltage for Differential Outputs Bank B</b> Connect to 3.3V or 2.5V power supply. VDDO_B does not have to be connected to the same voltage level as VDD or VDDO_A. These pins power up differential outputs OUT[5:9]_p/n.															
45	VDD_LVCMOS	P	<b>Power Supply Voltage for LVCMOS Output</b> Connect to 3.3V, 2.5V, 1.8V or 1.5V power supply.															

13 18 24 43 37 48	GND	P	<b>Ground</b> Connect to the ground
E-Pad	GND	P	<b>Ground.</b> Connect to the ground

### Functional Description

The ZL40230 is a programmable or hardware pin controlled low additive jitter, low power 3 x 10 LVPECL/HCSL/LVDS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML ) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins. All the other components for building crystal oscillator are built in device such as load capacitance, series and shunt resistors.

The ZL40230 has ten LVPECL/HCSL/LVDS outputs which can be powered from 3.3V or 2.5V supply. Each output can be independently enabled/disabled via SPI bus. The type of each output driver can be programmed to be LVPECL, HCSL or LVDS. Hence, the device can be configured to support different signaling formats depending on the application.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

### Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40230 inputs.

Figure 3 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and Ro + Rs should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor Rs should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 8). The source resistors of Rs = 270Ω could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of  $(3.3V/2) * (1/(270\Omega + 50\Omega)) = 5.16mA$ .

For optimum performance both differential input pins (\_p and \_n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

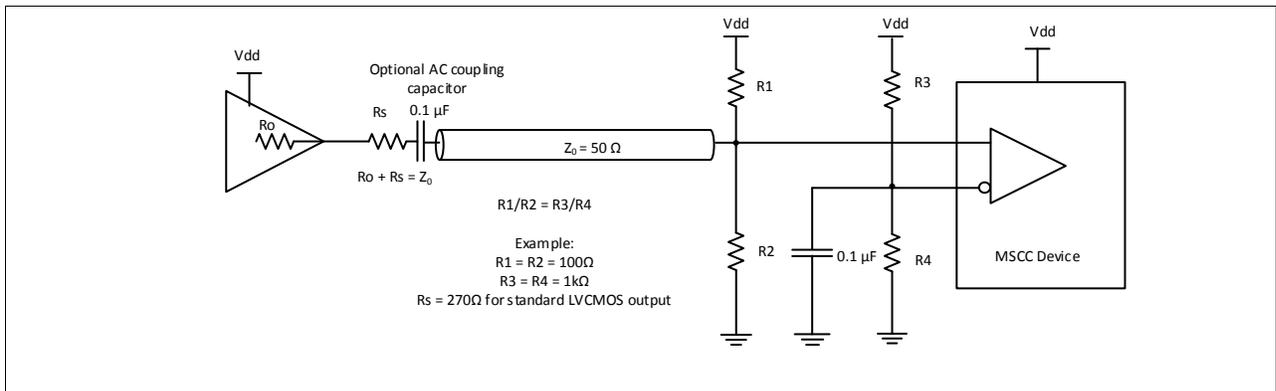


Figure 3. Input driven by a single ended output

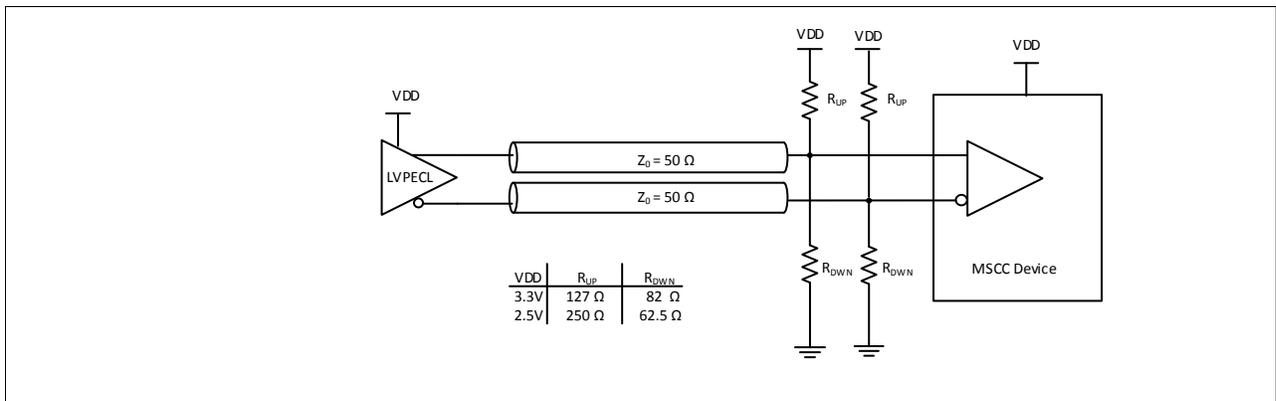
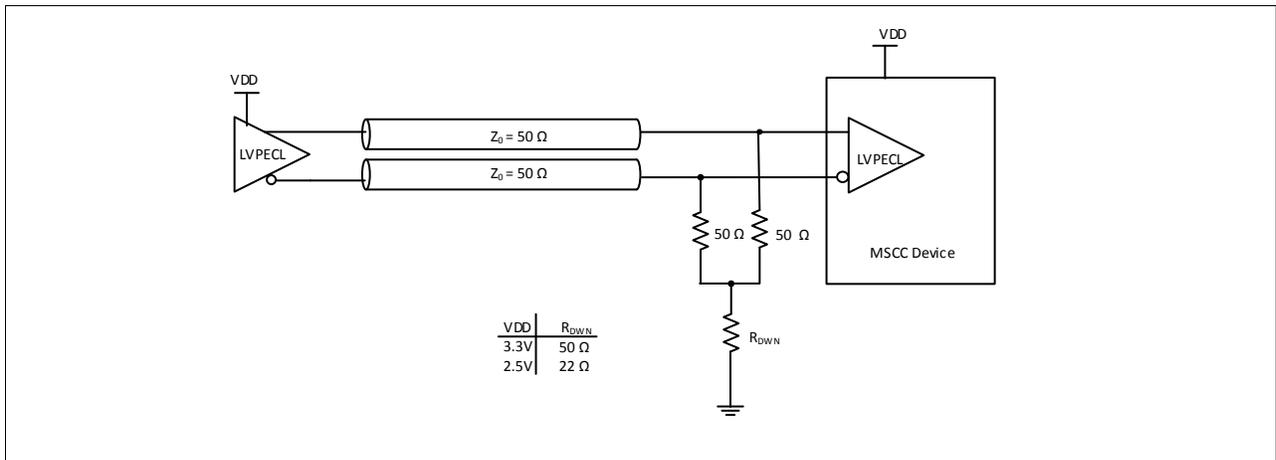
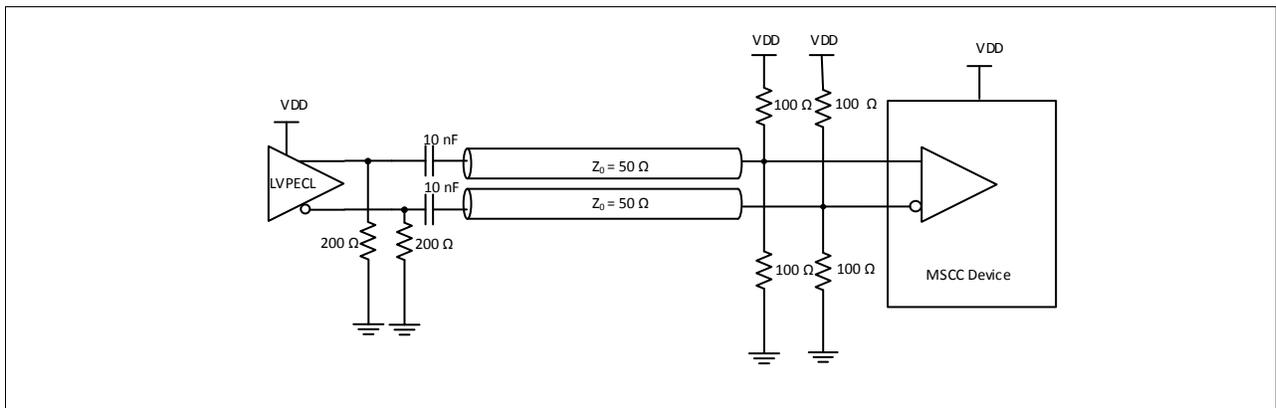


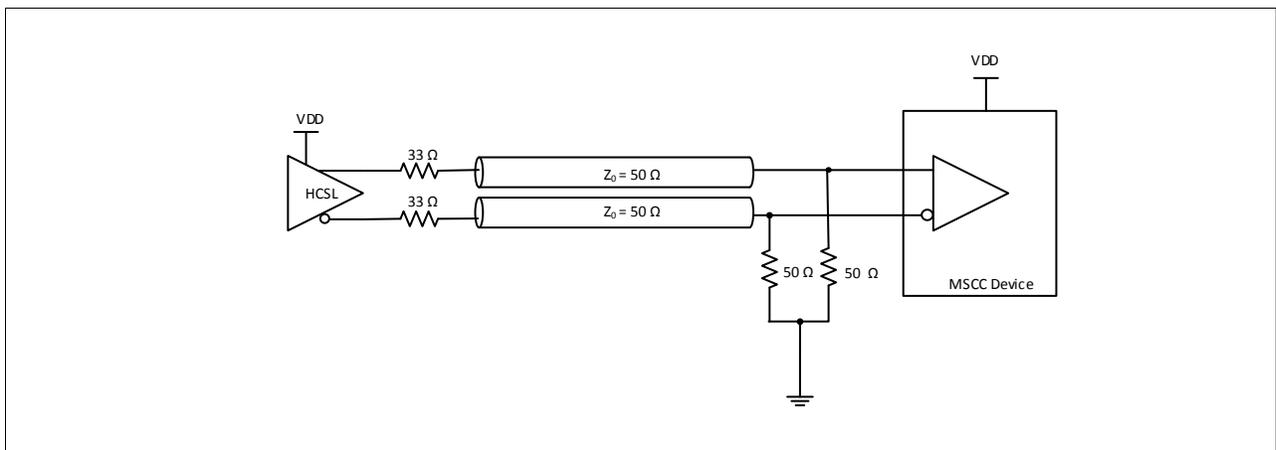
Figure 4. Input driven by DC coupled LVPECL output



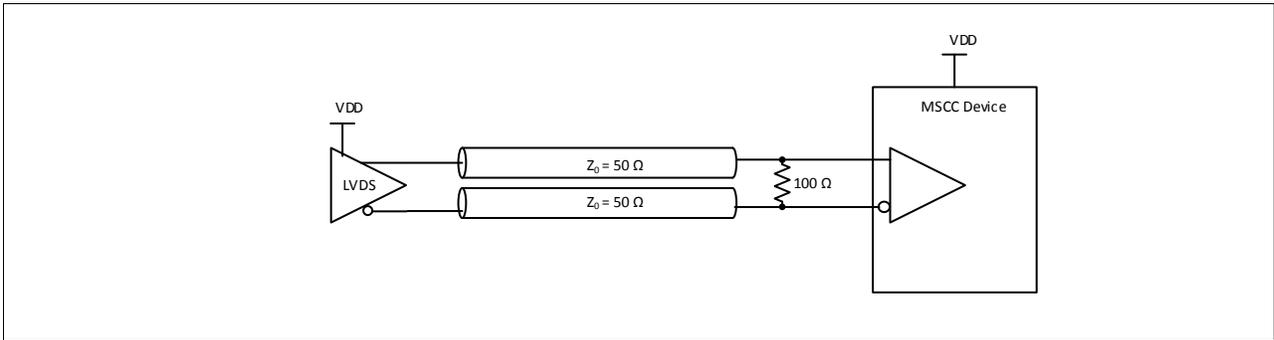
**Figure 5. Input driven by DC coupled LVPECL output (alternative termination)**



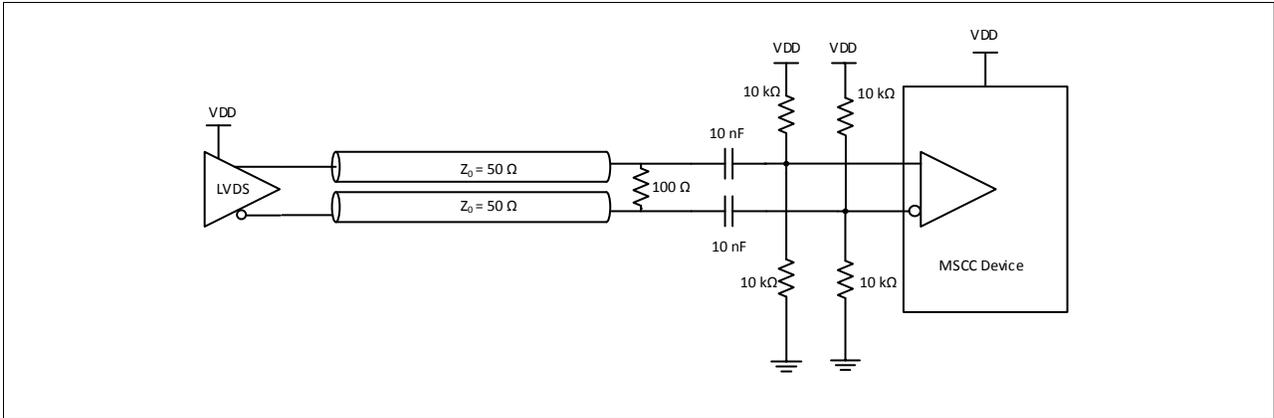
**Figure 6. Input driven by AC coupled LVPECL output**



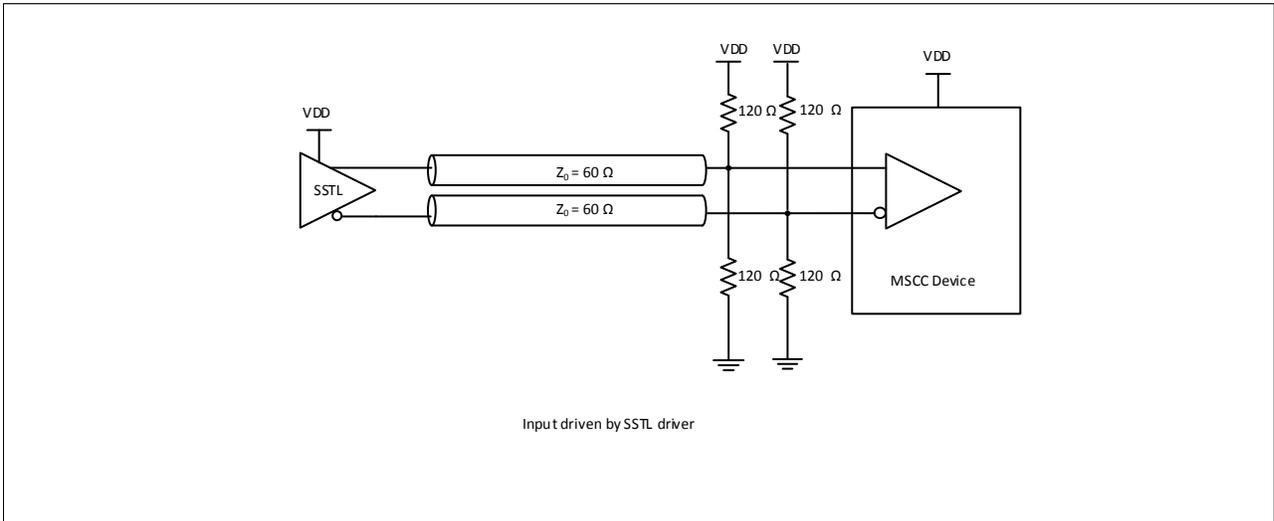
**Figure 7. Input driven by HCSL output**



**Figure 8. Input driven by LVDS output**



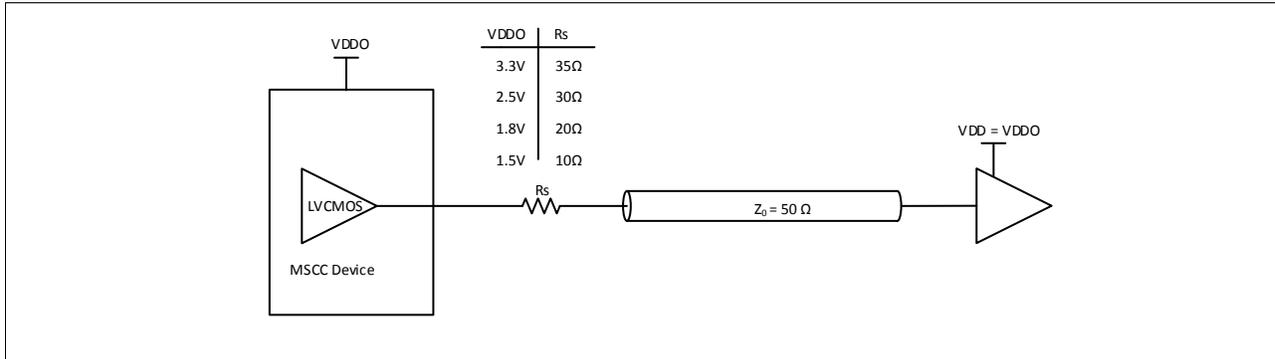
**Figure 9. Input driven by AC coupled LVDS**



**Figure 10. Input driven by an SSTL output**

### Clock Outputs

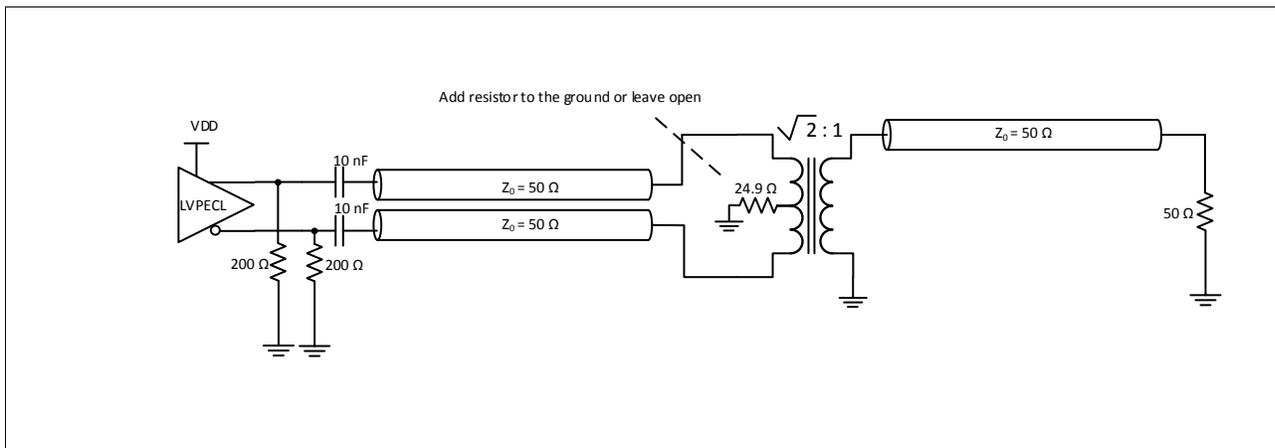
LVC MOS output OUT10 require only series termination resistor whose value is depending on LVC MOS output voltage as shown in Figure 11.



**Figure 11. Termination for LVC MOS output**

Differential outputs LVPECL, LVDS and HCSL should have same termination as corresponding outputs described in previous section.

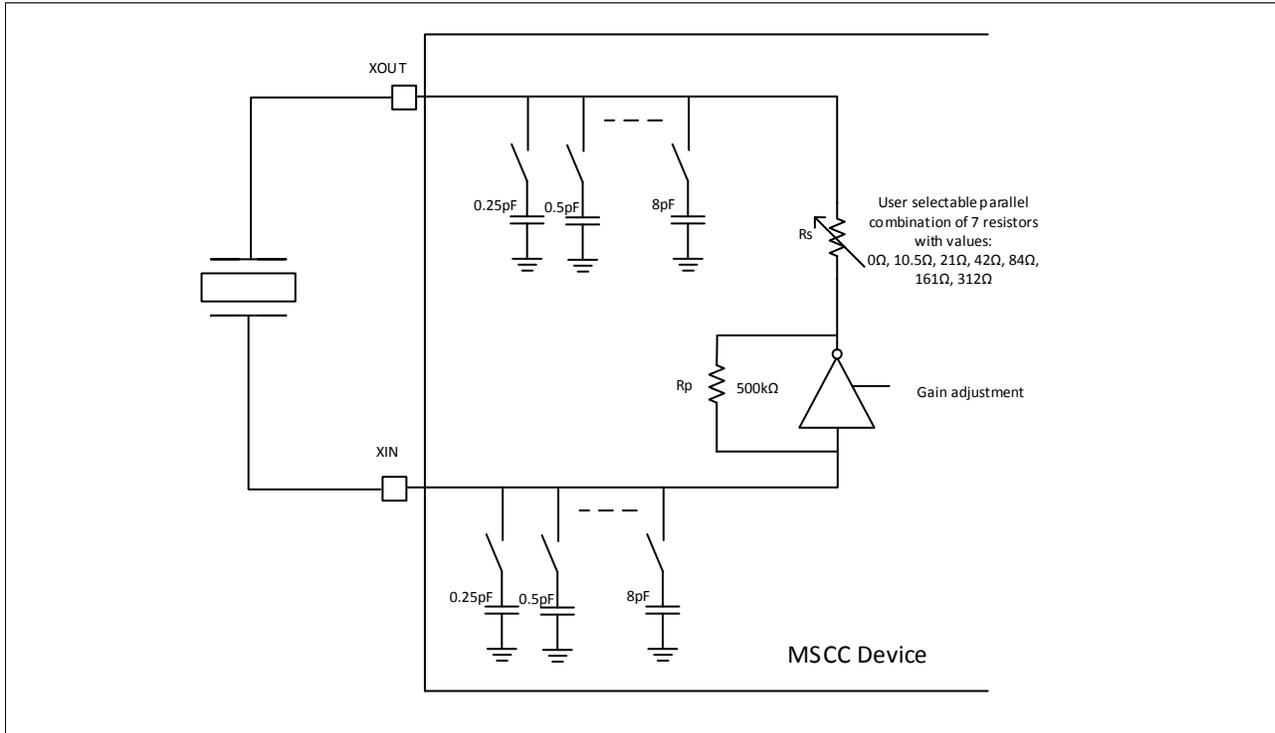
The device is designed to drive differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single ended output (for example driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 12. This is to provide a nominal common mode impedance of 10Ω or higher which is typical for differential terminations.



**Figure 12. Driving a load via transformer**

### Crystal Oscillator Input

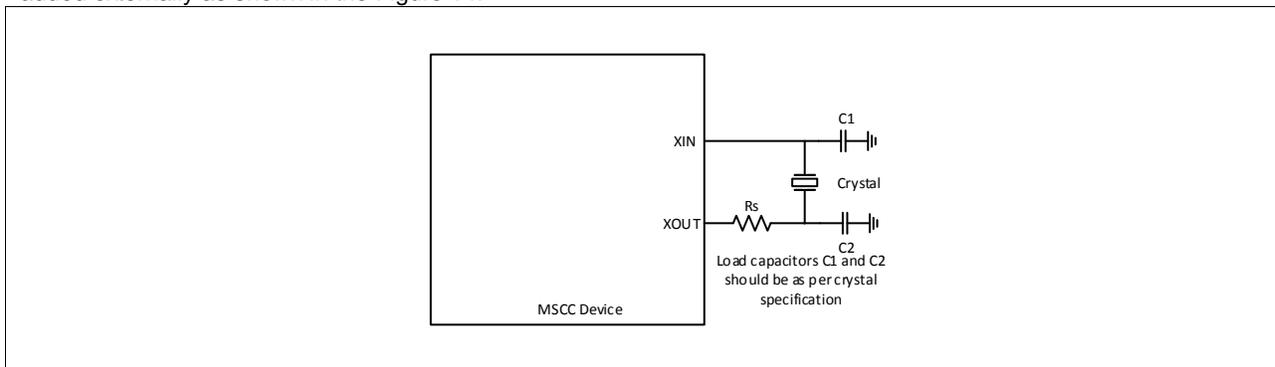
The crystal oscillator circuit can work with crystal resonators from 8MHz to 160MHz. As can be seen in the following figure only crystal resonator is required and all the other components are built-in the device. To be able support crystal resonators with different characteristics all internal components are programmable.



**Figure 13. Crystal Oscillator Circuit**

The load capacitors can be programmed from 0 to 21.75 pF (4pF default) with resolution of 0.25pF which not only meets load requirement for most crystal resonator but also allows for fine tuning of the crystal resonator frequency. The amplifier gain can be adjusted in five steps and series resistor can be adjusted as parallel combination of seven different resistors: 0Ω, 10.5Ω, 21Ω, 42Ω, 84Ω, 161Ω and 312Ω. (84Ω default) Although the first resistor is 0Ω the series resistance  $R_s$  will be slightly higher than 0Ω due to parasitic resistance of the switch which connects resistor. Hence the minimum series resistance is achieved when all seven resistors are connected in parallel. The shunt resistor is fixed and its value is 500kΩ.

In Hardware Controlled mode the capacitive load is set at 4pF, internal series resistance to 84Ω and they cannot be changed. For Crystal requiring higher load or series resistance additional capacitance and/or series resistance can be added externally as shown in the Figure 14.



**Figure 14. Crystal Oscillator Circuit in Hardware Controlled Mode**

## Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN\_0/1 can be pulled-down by 1kΩ resistor. Unused outputs should be left unconnected.

## Power Consumption

The device total power consumption can be calculated as:

$$P_T = P_S + P_{XTAL} + P_C + P_{O\_DIF} + P_{O\_LVCMOS}$$

Where:

$$P_S = V_{DD} \times I_S$$

is core power consumed by input buffers. If XTAL is running this power should be set to zero. where the static current ( $I_S$ ) is specified in Table 7.

$$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$$

is core power consumption of XTAL circuit. The current of the XTAL circuit is provided in Table 7. If XTAL is not used the power consumption is equal to zero.

$$P_C = V_{DDO} \times I_{DD\_CM}$$

Common output power shared among all ten outputs. The current  $I_{DD\_CM}$  is specified Table 7.

$$P_{O\_DIF} = V_{DDO} \times (I_{DD\_LVDS} \times N_1 + I_{DD\_LVPECL} \times N_2 + I_{DD\_HCSL} \times N_3)$$

Output power where the output currents are specified Table 7.  $N_1$ ,  $N_2$  and  $N_3$  are number of enabled LVPECL, LVDS and HCSL outputs respectively and  $N_1+N_2+N_3$  is less or equal to 10.

$$P_D = V_{DD\_LVCMOS} \times (I_{DD} \times f / 100\text{MHz} + V_{DD\_LVCMOS} \times C_{LOAD} \times f)$$

Dynamic LVCMOS output power.  $I_{DD}$  is specified in Table 7. If LVCMOS output is disabled this term is equal to zero.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption.

$$P_D = P_T - N_1 \times P_{LVPECL} - N_2 \times P_{LVDS} - N_3 \times P_{HCSL}$$

Where  $N_1$ ,  $N_2$  and  $N_3$  are the number of enabled LVPECL, LVDS and HCSL outputs respectively. Since there are ten differential outputs  $N_1 + N_2 + N_3$  will be less or equal to 10.

$$P_{LVPECL} = V_{SW} / 50 \times (V_{SW} + V_B)$$

$V_{SW}$  is voltage swing of LVPECL output.  $V_B$  is LVPECL bias voltage equal to  $V_{DD} - 2V$

$$P_{LVDS} = V_{SW} / 100$$

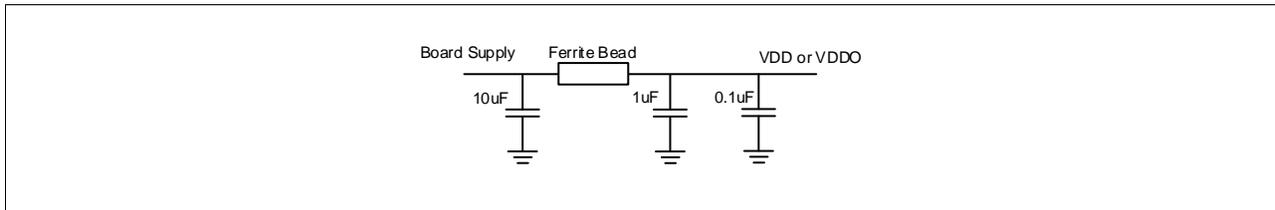
$V_{SW}$  is voltage swing of LVDS output.

$$P_{HCSL} = V_{SW} / 50 \times (V_{SW} + V_{SW} / 50 \times 33)$$

$V_{SW}$  is voltage swing of HCSL output. 50 ohm is termination resistance and 33 ohm is series resistance of the HCSL output.

### Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulated with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling for each power pin.



**Figure 15. Power Supply Filtering**

### Power Supplies and Power-up Sequence

The device has four different power supplies: VDD, VDDO\_A, VDDO\_B and VDD\_LVCMOS which are mutually independent. Voltages supported by each of these power supplies are specified in Table 1.

The device is not sensitive to the power-up sequence. For example commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence).

### Host Interface

ZL30230 can be controlled via hardware pins (SEL pin tied low) or via SPI port (SEL pin tied high). The mode shall be selected during power up and it cannot be changed on the fly.

#### Hardware Control Mode

In this mode, ZL40230 is controlled via Input Select (IN\_SEL0/1) pins which select which one of three inputs is fed to the output and show in Table 2 and OUTA/B\_TYPE\_SEL0/1 pins which select signal level (LVPECL, LVDS, HCSL or Hi-Z) for each of two (A and B) output banks as shown in Table 3.

All input control pins have low input threshold voltage so they can be driven from the device with low output voltage (FPGA/CPLD). Supported voltages are between 1.2V and VDD (2.5V or 3.3V).

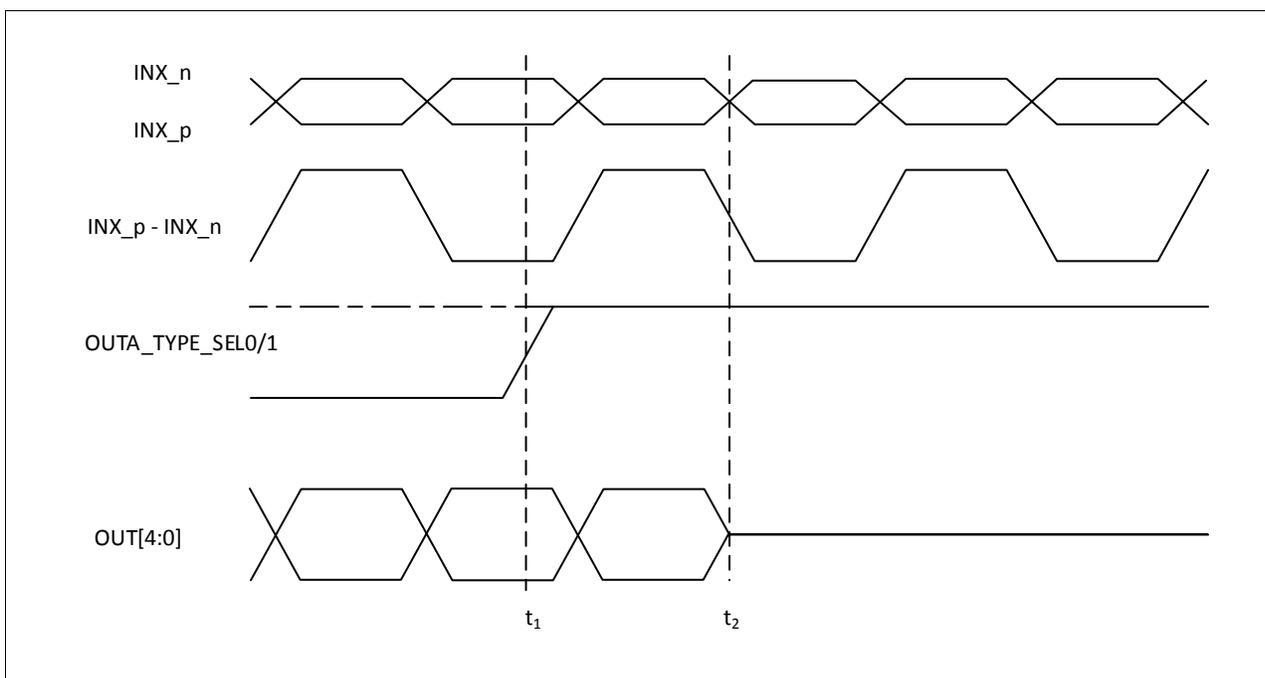
**Table 2 Input clock selection**

IN_SEL1	IN_SEL0	Selected Input
0	0	IN0_p, IN0_n
0	1	IN1_p, IN1_n
1	X	XIN

**Table 3 Output Type Selection**

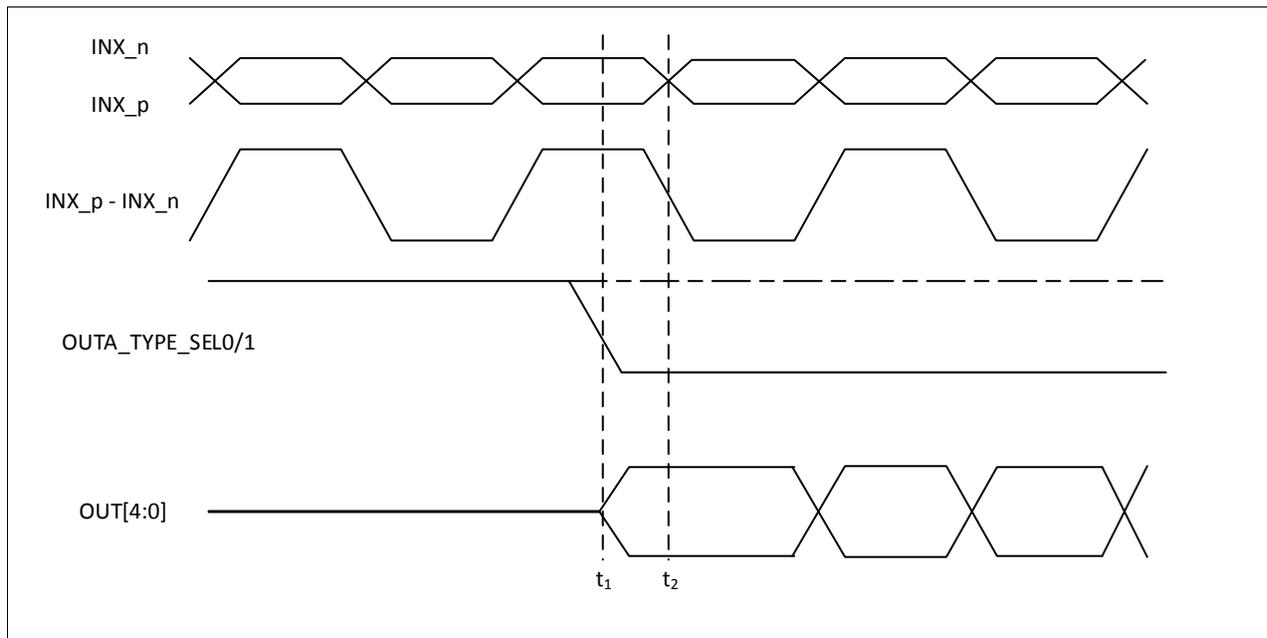
OUTA/B_TYPE_SEL1	OUTA/B_TYPE_SEL0	Output
0	0	LVPECL
1	1	LVDS
1	0	HCSL
1	1	High-Z (Output Disabled)

Output is disabled synchronously on the falling edge of the input ( $t_2$ ) as shown in Figure 16.



**Figure 16. Output Disable**

Outputs can be enabled by toggling one or both OUTA/B\_TYPE\_SEL0/1 pins low depending on which type of interface needs to be enabled for particular bank. As soon as one or both OUTA/B\_TYPE\_SEL0/1 pins go low ( $t_1$ ) the outputs will go from high-Z to low ( $OUT_{X_p} = \text{low}$ ,  $OUT_{X_n} = \text{high}$ ) and will start to track the input after the first falling edge ( $t_2$ ) of the input signal as shown in Figure 17.

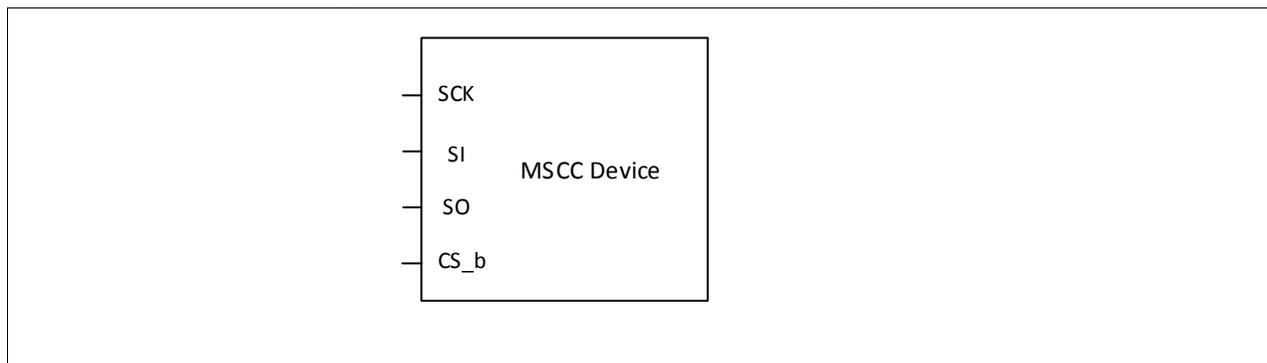


**Figure 17. Output Enable**

Figures above show enable/disable waveform for the output bank A (OUT[4:0]). The waveforms are equivalent for the output bank B (OUT[9:5]) which is controlled by OUTB\_TYPE\_SEL0/1 pins.

**SPI Control Mode**

ZL40230 is controlled via four pin SPI slave interface as shown in the following figure.



**Figure 18. SPI slave interface**

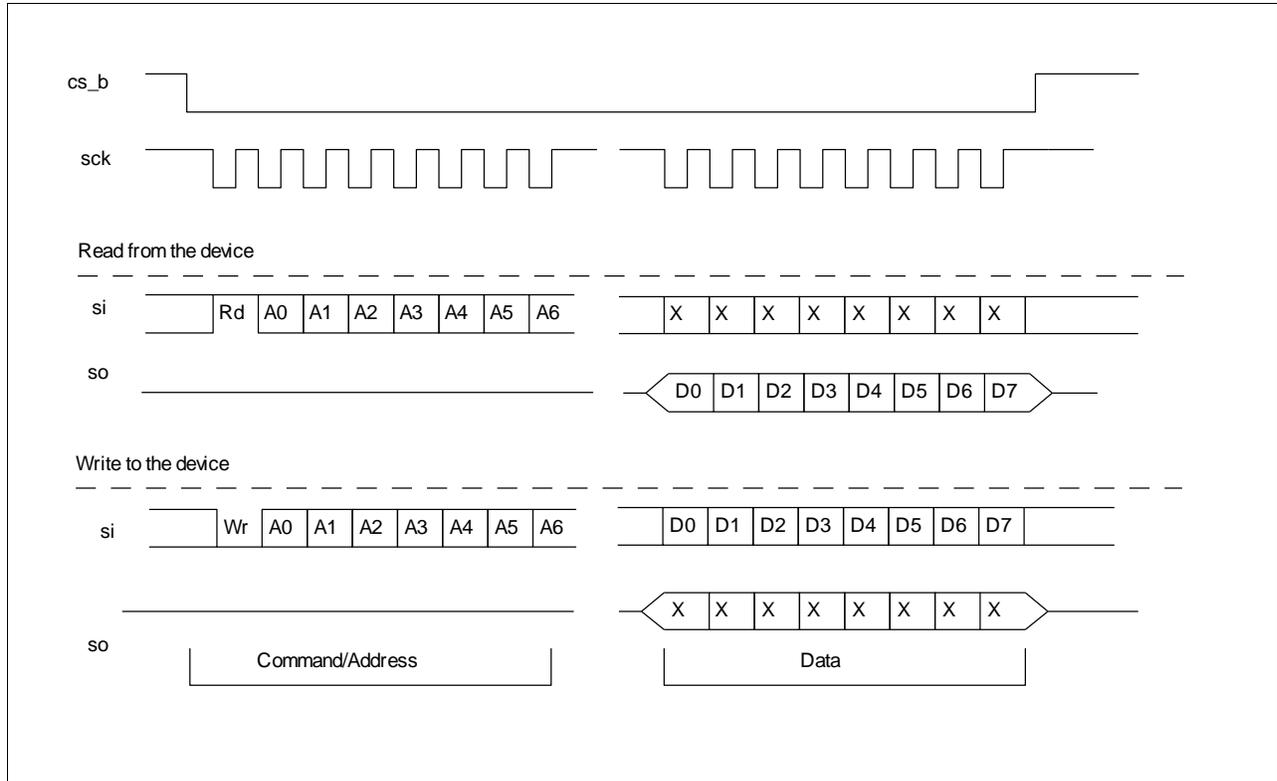
All SPI input pins have low threshold voltage so they can be driven from low output voltage SPI master device. Supported voltages are between 1.2V and VDD (2.5V or 3.3V). This allows device to be controlled from an FPGA with low voltage I/O supply.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **SO** pin must be ignored. Similarly, the input data on the **SI** pin is ignored by the device during a read cycle.

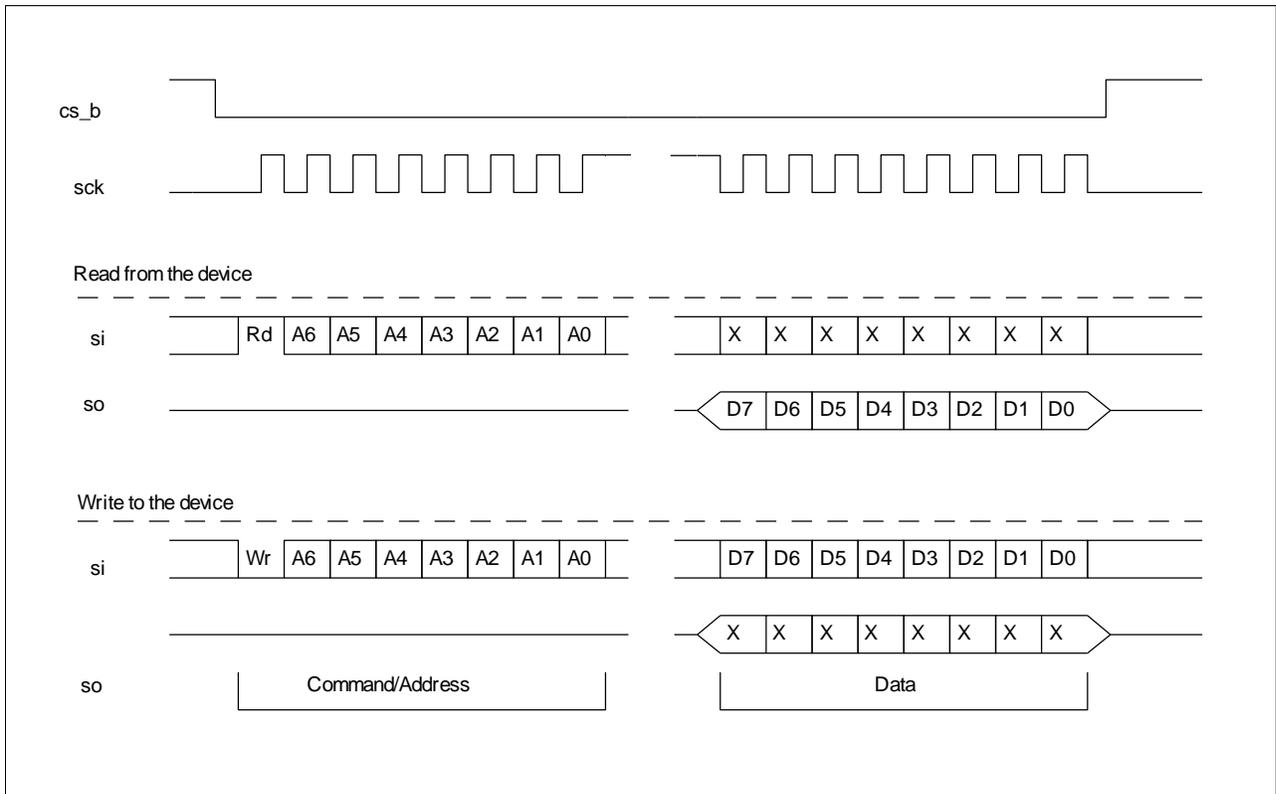
The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **SCK** pin when the **CS\_b** pin is active. If the **SCK** pin is low during **CS\_b** activation, then MSb first timing is selected. If the **SCK** pin is high during **CS\_b** activation, then LSb first timing is assumed.

The SPI port expects 1-bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **CS\_b** pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal **CS\_b** is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

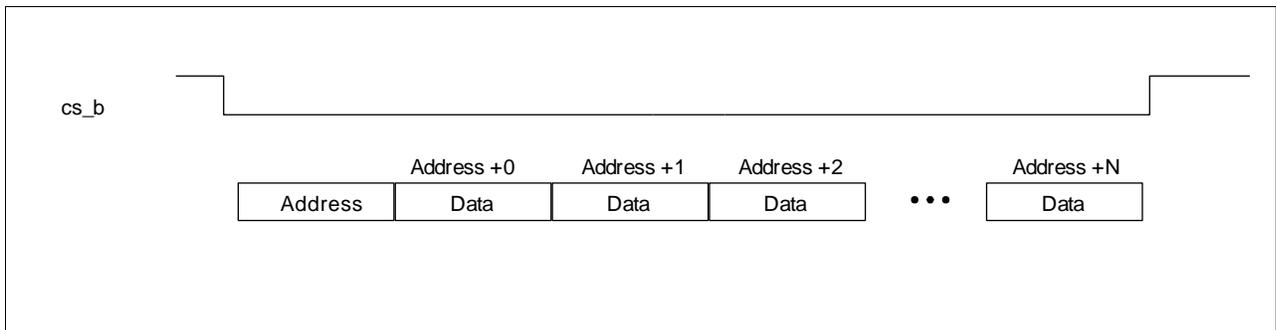
Functional waveforms for the LSB and MSb first mode, and burst mode are shown in Figure 19 and Figure 20 respectively. Figure 21 shows an example of burst mode operation which allows user to read or write consecutive location in the register map.



**Figure 19. Serial Peripheral Interface Functional Waveform – LSB First Mode**



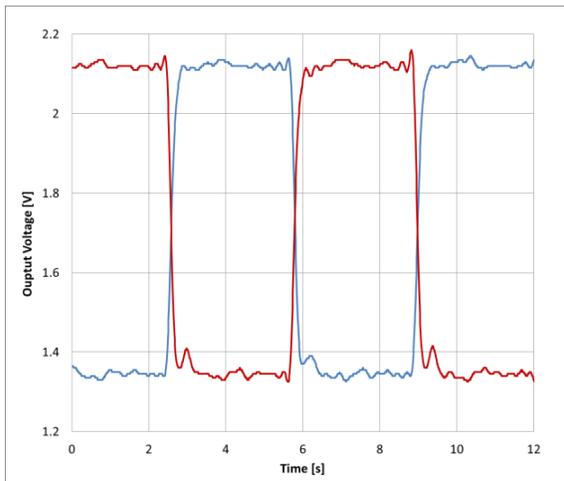
**Figure 20. Serial Peripheral Interface Functional Waveform – MSB First Mode**



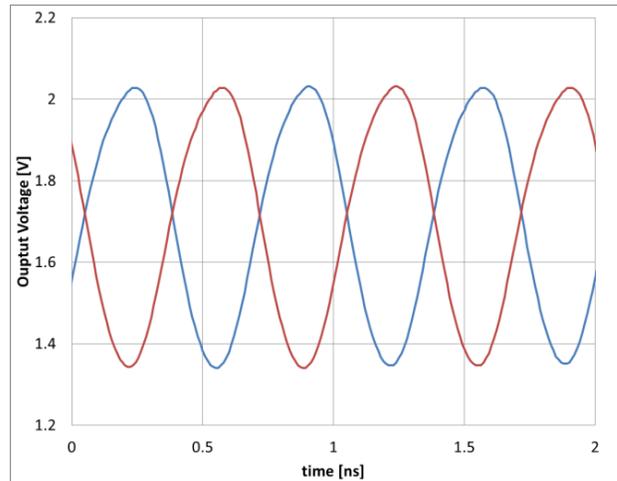
**Figure 21. Example of the Burst Mode Operation**

## Typical device performance

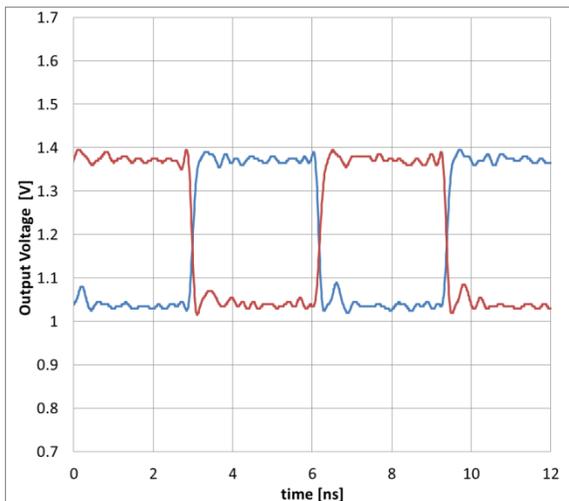
The following plots show typical device performances



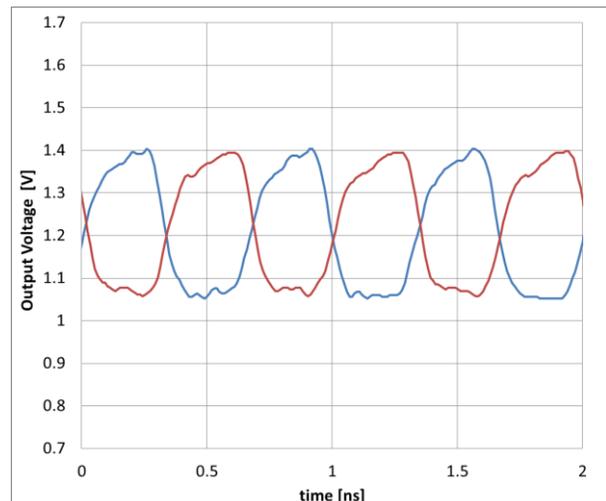
**Figure 22. 156.25MHz LVPECL**



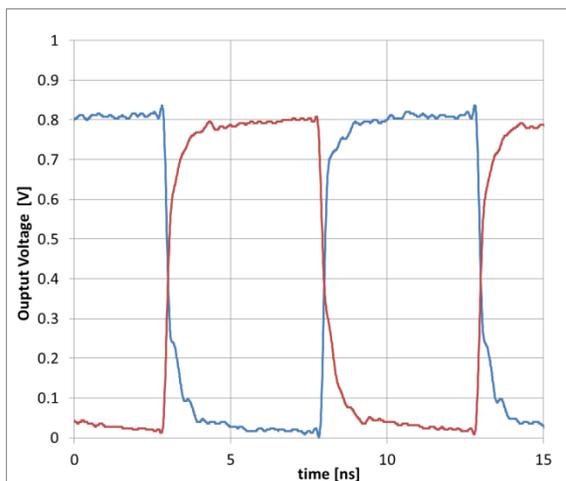
**Figure 23. 1.5GHz LVPECL**



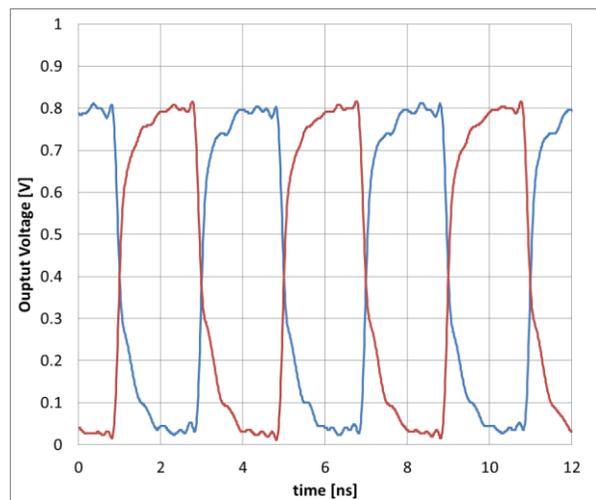
**Figure 24. 156.25MHz LVDS**



**Figure 25. 1.5GHz LVDS**



**Figure 26. 100MHz HCSSL**



**Figure 27. 250MHz HCSSL**

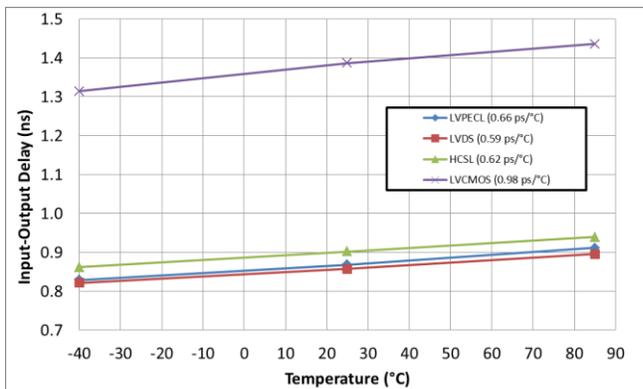


Figure 28. I/O delay vs temperature

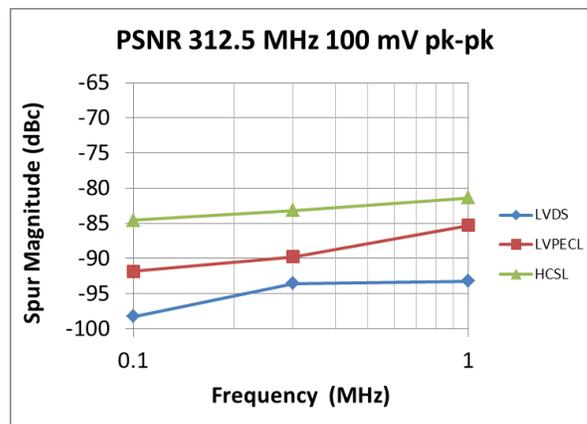


Figure 29. PSNR vs noise frequency

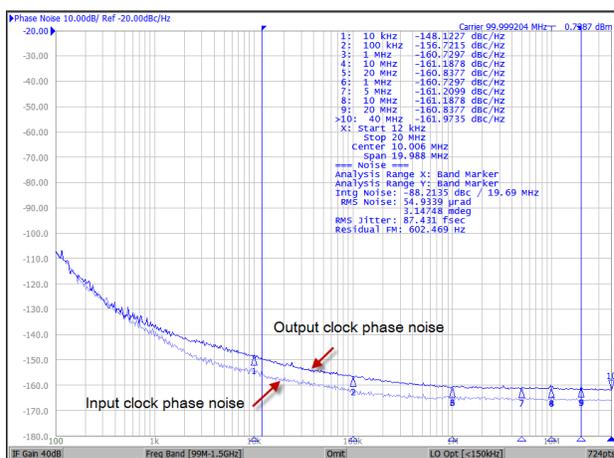


Figure 30. 100MHz LVPECL Phase Noise

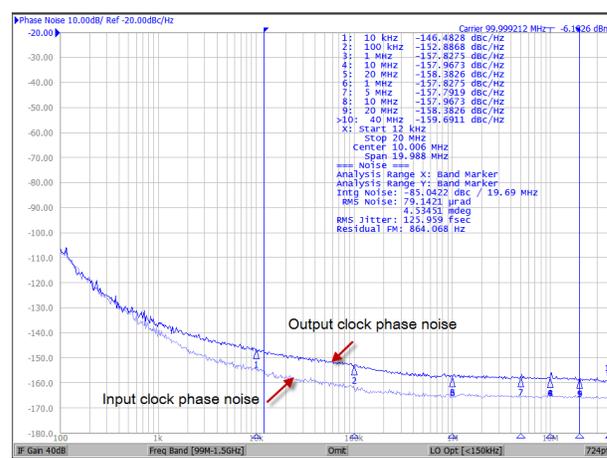


Figure 31. 100MHz LVDS Phase Noise

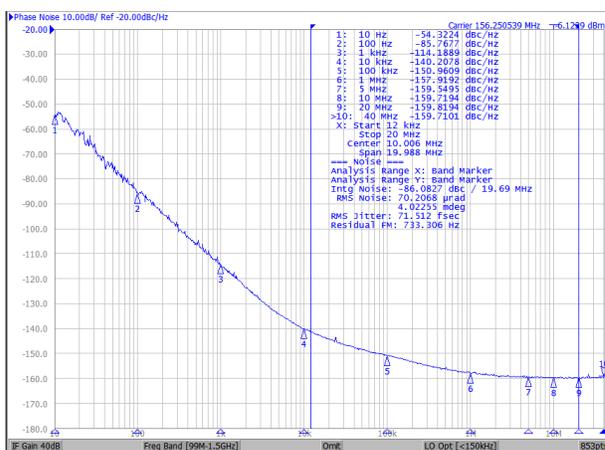


Figure 32. 156.25MHz LVDS Phase Noise in Xtal mode

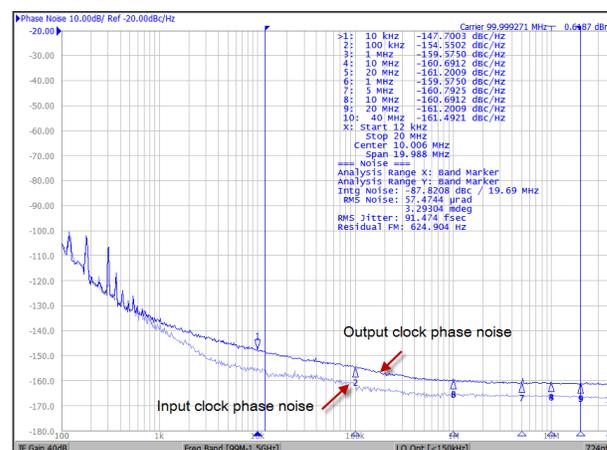


Figure 33. 100MHz HCSL Phase Noise

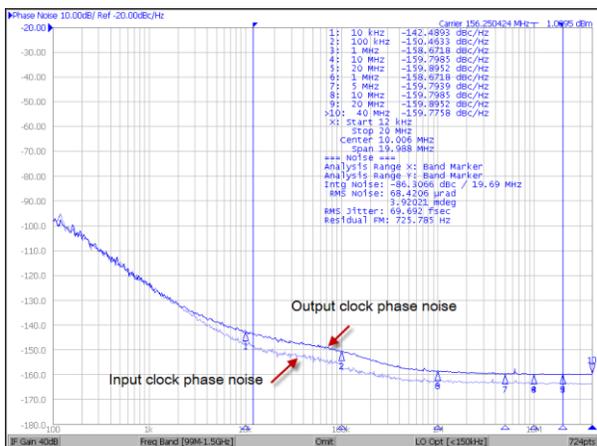


Figure 34. 156.25MHz LVPECL Phase Noise

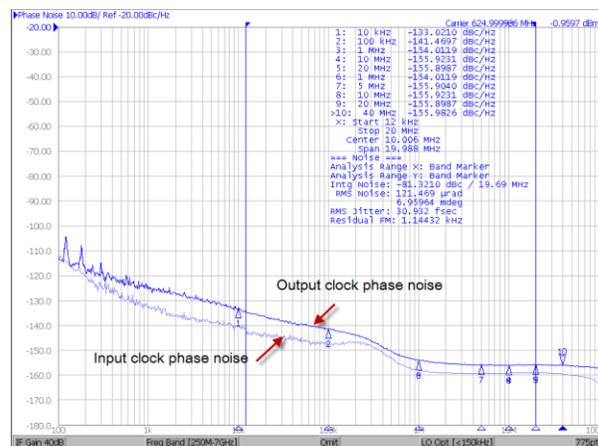


Figure 35. 625MHz LVPECL Phase Noise

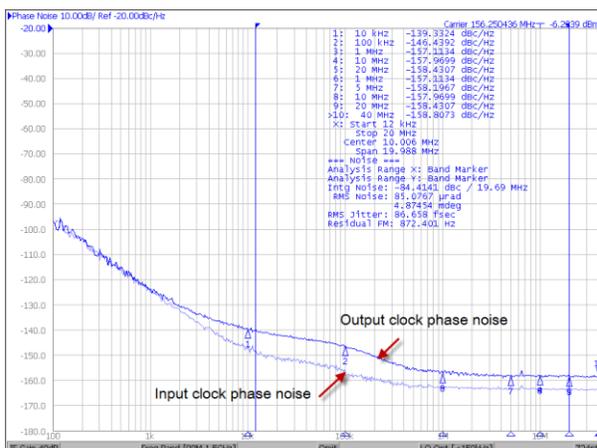


Figure 36. 156.25MHz LVDS Phase Noise

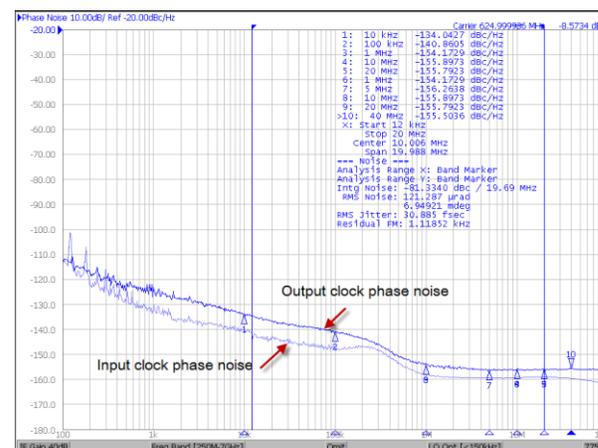


Figure 37. 625MHz LVDS Phase Noise

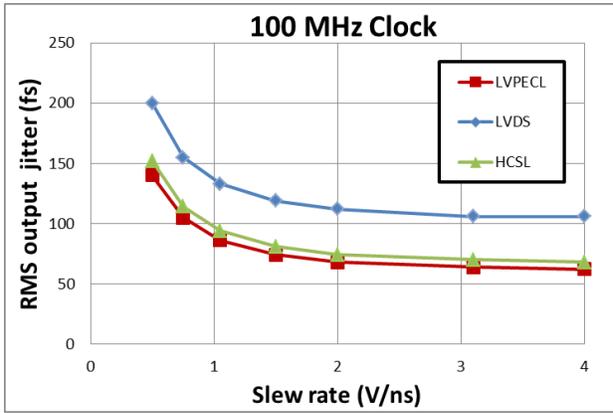


Figure 38. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

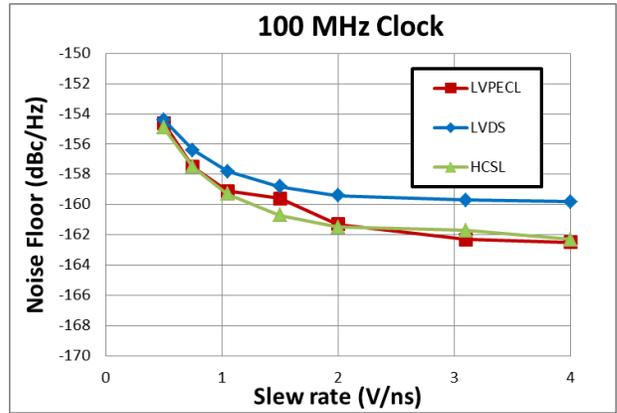


Figure 39. Output clock noise floor vs input clock slew-rate

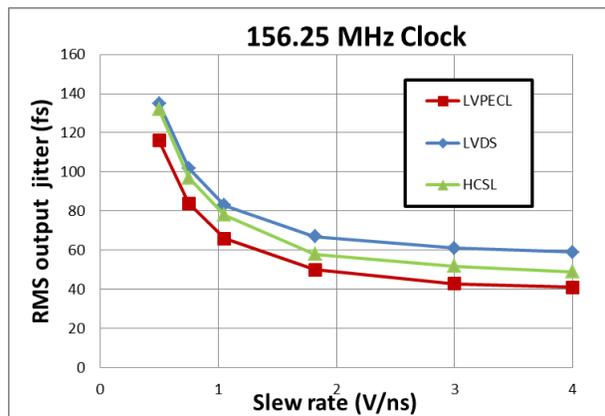


Figure 40. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

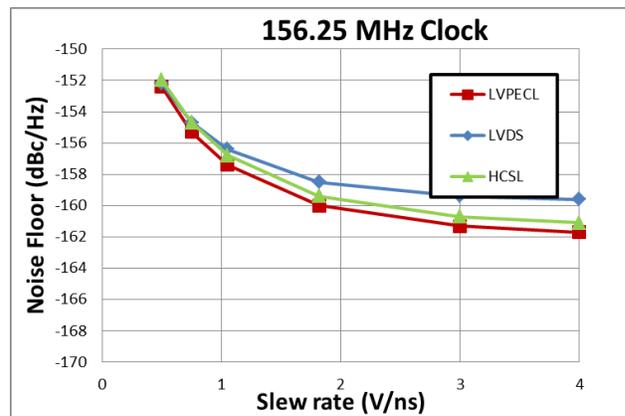


Figure 41. Output clock noise floor vs input clock slew-rate

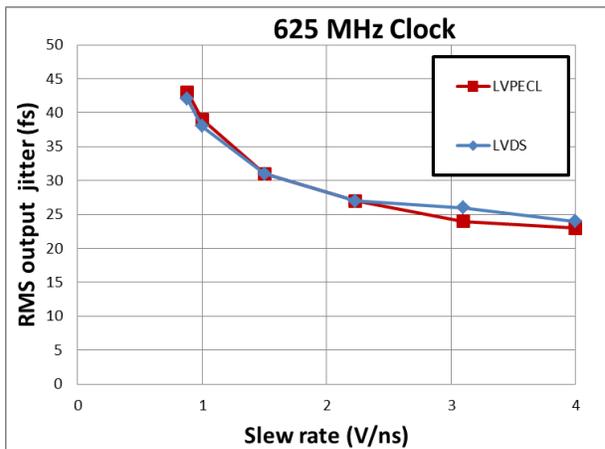


Figure 42. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

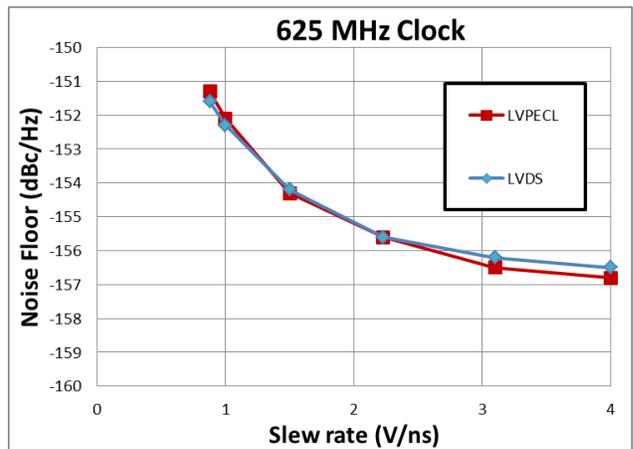


Figure 43. Output clock noise floor vs input clock slew-rate

## Register Map

The device is controlled by accessing registers through the serial interface. The following table provides a summary of the registers available for the configuration of the device.

**Table 4 Register Map**

Address SPI A[6:0] Hex (0x)	Name	Data D[7:0]
00	XTALBG	xtal_buf_gain[7:0]
01	XTALDL	xtal_drive_level[7:0]
02	XTALLC	xtal_load_cap[7:0]
03	XTALNR	xtal_normal_run
04	-	Not used
05	INSEL	input_select[1:0]
06	OUTLOW	output_drive_low
07	DRVTYPEA0	driver_type[7:0] (differential output OUT3, OUT2, OUT1, OUT0)
08	DRVTYPEA1	driver_type[9:8] (differential output OUT4)
09	DRVTYPEB0	driver_type[17:10] (differential output OUT8, OUT7, OUT6, OUT5)
0A	DRVTYPEB1	driver_type[19:18] (differential output OUT9)
0B	CMOSDIV	cmos_div[2:0] (cmos)
0C	CMOSOUTEN	output_enable (cmos)
0D	CMOSDRVSTR	driver_strength (cmos)
0E	-	Not used
0F and 10	Reserved	Leave as default
11	DEVID	Device ID
12 to 1F	Reserved	Leave as default

Address	0x00			Hex
XTALBG		XTAL Buffer Gain		
Bit	Name	Description	Type	Reset
7:0	xtal_buf_gain[7:0]	<p>Programs crystal buffer (inverting amplifier) gain. Every bit pair (bits: 01, 23, 45, 67) of this register correspond to additional equal gain block which can be added (bits set) or removed (bits cleared).</p> <p>Minimum gain is 0x00 (default) and 0xFF is maximum gain. When reference input mode is "bypass XTAL mode" or "differential input modes" with HIGH xtal_normal_run bit, the buffer is disabled and follows "Input Selection". When xtal_normal_run bit is LOW, XTAL buffer is in the "xtal forced run" mode and keep running.</p> <p><b>8'b0000_0000: default crystal buffer strength.</b>                      8'b0000_0011: enable additional buffer strength                      8'b0000_1100: enable additional buffer strength                      8'b0011_0000: enable additional buffer strength                      8'b1100_0000: enable additional buffer strength</p>	RW	FF

Address	0x01			Hex
XTALDL		XTAL Drive Level		
Bit	Name	Description	Type	Reset
7:0	xtal_drive_level[7:0]	<p>Internal damping resistance of crystal circuit to limit external crystal's drive level uW. The value of damping resistor is determined by crystal's motion resistance of crystal's equivalent circuit. Drive level should be lower than crystal manufacturer's specification. Crystal's equivalent values should be requested to the manufacturer, (motion resistance and shunt capacitance). The selected resistors are connected to XOUT. Multiple bit combinations available by 7-bit control. Because they use parallel connections, 0xFF is the smallest resistance and 0x01 is the highest resistance.</p> <p>8'b0000_0000: disable all resistors                      8'b0000_0001: 312 Ohm resistor                      8'b0000_0010: 161 Ohm resistor                      8'b0000_0100: 84 Ohm resistor                      8'b0000_1000: 42 Ohm resistor                      8'b0001_0000: 21 Ohm resistor                      8'b0010_0000: 10.5 Ohm resistor                      8'b0100_0000: 0 Ohm connection                      8'b1000_0000: not used</p>	RW	04

Address	0x02			Hex
<b>XTALLC</b>		<b>XTAL Load Capacitance</b>		
Bit	Name	Description	Type	Reset
7:0	xtal_load_cap[7:0]	Internal load capacitance of crystal circuit (0 pF to 21.75 pF with the resolution of 0.25 pF). XIN and XOUT have each capacitor connected to GND. Multiple bit combinations available between 8 capacitors.  8'b0000_0000: disable all xtal load capacitors 8'b0000_0001: enable capacitor 0.25 pF 8'b0000_0010: enable capacitor 0.5 pF 8'b0000_0100: enable capacitor 1 pF 8'b0000_1000: enable capacitor 2 pF 8'b0001_0000: enable capacitor 2 pF 8'b0010_0000: enable capacitor 4 pF 8'b0100_0000: enable capacitor 4 pF 8'b1000_0000: enable capacitor 8 pF	RW	40

Address	0x03			Bin
<b>XTALNR</b>		<b>XTAL Normal Run</b>		
Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	1111111
0	xtal_normal_run	When this bit is set high crystal oscillator circuit is running only if input_select[1:0] register at address 0x05 selects crystal mode (2'b10). This value is recommended because it provides best jitter performance--XO circuit is running only when it is needed.  When this bit is set low the crystal oscillator will keep running even if crystal oscillator is not selected in input_select[1:0] register at address 0x05. This mode should only be used when fast switching between input references and crystal oscillator is required.	RW	1

Address	0x05			Bin
<b>INSEL</b>		<b>Input Select Register</b>		
Bit	Name	Description	Type	Reset
7:2	Unused	Unused	R	1111111
1:0	input_select[1:0]	Input reference clock selection. Proper external coupling and termination are required.  2'b00: differential input from IN0_p and IN0_n 2'b01: differential input from IN1_p and IN1_n 2'b10: fundamental XTAL mode with XIN and XOUT (Use internal crystal oscillator circuits) or XTAL overdrive mode (single-ended clock signal fed to XIN) 2'b11: XTAL bypass mode (single-ended clock signal with XIN and disabled internal crystal buffer circuit in the analog block)	RW	00

Address	0x06			Bin
<b>OUTLOW</b>		<b>Output Drive Low</b>		
Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	1111111
0	output_drive_low	<p>Forces all disabled outputs to drive low in LVPECL mode.</p> <p>1'b1: All differential outputs that are disabled in DRVTYPE registers (addresses 0x07, 0x08, 0x09 and 0x0A) will drive low in LVPECL mode. Hence, LVPECL biasing/termination resistors are required for proper functionality of this feature.</p> <p>1'b0: This feature is ignored and all outputs that are disabled in DRVTYPE registers (addresses 0x07, 0x08, 0x09 and 0x0A) will stay in disabled (high-Z) mode.</p>	RW	0

Address	0x07			Bin
<b>DRVTYPEA0</b>		<b>Output Type Select Bank-A 0</b>		
Bit	Name	Description	Type	Reset
7:6	driver_type[7:6]	<p>Output driver type of differential OUT3.</p> <p>The same bit configuration with OUT0.</p>	RW	11
5:4	driver_type[5:4]	<p>Output driver type of differential OUT2.</p> <p>The same bit configuration with OUT0.</p>	RW	11
3:2	driver_type[3:2]	<p>Output driver type of differential OUT1.</p> <p>The same bit configuration with OUT0.</p>	RW	11
1:0	driver_type[1:0]	<p>Output driver type of differential OUT0.</p> <p>2'b00: LVPECL outputs                  2'b01: LVDS outputs                  2'b10: HCSL outputs                  2'b11: outputs disabled (Disabled state is dependent on "out_drive_low" control bit of register OUTLOW.)</p>	RW	11

Address	0x08			Bin
<b>DRVTYPEA1</b>		<b>Output Type Select Bank-A 1</b>		
Bit	Name	Description	Type	Reset
7:2	Unused	Unused	R	1111111
1:0	driver_type[9:8]	<p>Output driver type of differential OUT4.</p> <p>The same bit configuration with OUT0.</p>	RW	11

Address	0x09			Hex
<b>DRVTYPEB0</b>		<b>Output Type Select Bank-B 0</b>		
Bit	Name	Description	Type	Reset
7:6	driver_type[17:16]	Output driver type of differential OUT8. The same bit configuration with OUT0.	RW	11
5:4	driver_type[15:14]	Output driver type of differential OUT7. The same bit configuration with OUT0.	RW	11
3:2	driver_type[13:12]	Output driver type of differential OUT6. The same bit configuration with OUT0.	RW	11
1:0	driver_type[11:10]	Output driver type of differential OUT5. The same bit configuration with OUT0.	RW	11

Address	0x0A			Bin
<b>DRVTYPEB1</b>		<b>Output Type Select Bank-B 1</b>		
Bit	Name	Description	Type	Reset
7:2	Unused	Unused	R	111111
1:0	driver_type[19:18]	Output driver type of differential OUT9. The same bit configuration with OUT0.	RW	11

Address	0x0B			Bin
<b>CMOSDIV</b>		<b>CMOS Output Divider</b>		
Bit	Name	Description	Type	Reset
7:3	Unused	Unused	R	11111
2:0	cmos_div[2:0]	Integer divider from a selected input reference clock for OUT_LVCMOS (1 to 8).  <b>3'b000: division ratio = 1</b> 3'b001: division ratio = 2 3'b010: division ratio = 3 3'b011: division ratio = 4 3'b100: division ratio = 5 3'b101: division ratio = 6 3'b110: division ratio = 7 3'b111: division ratio = 8	RW	000

Address	0x0C			Bin
<b>CMOSOUTEN</b>		<b>LVC MOS Output Enable</b>		
Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	111111
0	output_enable	Output enable of OUT_LVCMOS. Disabled state is dependent on "out_drive_low" control bit.  1'b0: Disable OUT_LVCMOS output 1'b1: Enable OUT_LVCMOS output	RW	0

Address	0x0D			Bin
<b>CMOSDRVSTR</b>		<b>CMOS Driver Strength</b>		
Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	1111111
0	driver_strength	OUT_LVCMOS output strength.  1'b0: low strength 1'b1: high strength	RW	0

Address	0x11			Bin
<b>DEVID</b>		<b>Device Identification</b>		
Bit	Name	Description	Type	Reset
7	Unused	Unused	R	0
6:5	Reserved	Leave as default		01
4:0	dev_id	Device ID <b>5'h02: ZL40230</b>	RO	00010

## AC and DC Electrical Characteristics

### Absolute Maximum Ratings

**Table 5 Absolute Maximum Ratings\***

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage (3.3V)	$V_{DD}/V_{DDO}$	-0.5		4.6	V	
2	Supply voltage (2.5V)	$V_{DD}/V_{DDO}$	-0.5		3.5	V	
3	Storage temperature	$T_{ST}$	-55		125	°C	

- \* Exceeding these values may cause permanent damage
- \* Functional operation under these conditions is not implied
- \* Voltages are with respect to ground (GND) unless otherwise stated

### Recommended Operating Conditions

**Table 6 Recommended Operating Conditions\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	$V_{DD}/V_{DDO}/V_{DD,LVCMOS}$	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	$V_{DD}/V_{DDO}/V_{DD,LVCMOS}$	2.375	2.50	2.625	V	
3	Supply voltage 1.8V	$V_{DD,LVCMOS}$	1.6	1.8V	2	V	
4	Supply voltage 1.5V	$V_{DD,LVCMOS}$	1.35	1.5	1.65	V	
5	Operating temperature	$T_A$	-40	25	85	°C	
6	Input voltage	$V_{DD-IN}$	- 0.3		$V_{DD} + 0.3$	V	

- \* Voltages are with respect to ground (GND) unless otherwise stated
- \* The device core supports two power supply modes (3.3V and 2.5V)

**Table 7 Current consumption**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Core device current (all outputs and XTAL disabled)	$I_{s,3.3V}$		163	197	mA	$V_{DD} = 3.3V \pm 5\%$
		$I_{s,2.5V}$		153	187	mA	$V_{DD} = 2.5V \pm 5\%$
2	Core device current (all outputs disabled) XTAL circuit enabled with 25MHz Crystal connected between XIN and XOUT	$I_{DD,XTAL,3.3V}$		128	154	mA	$V_{DD} = 3.3V \pm 5\%$
		$I_{DD,XTAL,2.5V}$		124	150	mA	$V_{DD} = 2.5V \pm 5\%$
3	Common output current	$I_{DD,CM,3.3V}$		13.44	15.05	mA	$V_{DDO} = 3.3V \pm 5\%$
		$I_{DD,CM,2.5V}$		12.18	13.65	mA	$V_{DDO} = 2.5V \pm 5\%$
4	Dynamic LVCMOS current for high strength output (f = 100MHz) Needs to be scaled for different frequencies by f/100MHz	$I_{DD,3.3V}$		4.08	4.74	mA	$V_{DDO} = 3.3V \pm 5\%$
		$I_{DD,2.5V}$		2.90	3.29	mA	$V_{DDO} = 2.5V \pm 5\%$
5	Dynamic LVCMOS current for high strength output (f = 100MHz) Needs to be scaled for different frequencies by f/100MHz	$I_{DD,3.3V}$		2.38	2.68	mA	$V_{DDO} = 3.3V \pm 5\%$
		$I_{DD,2.5V}$		1.74	1.96	mA	$V_{DDO} = 2.5V \pm 5\%$
6	Current dissipation per LVPECL output	$I_{DD,LVPECL,3.3V}$		19.36	23.26	mA	$V_{DDO} = 3.3V \pm 5\%$
		$I_{DD,LVPECL,2.5V}$		19.38	22.17	mA	$V_{DDO} = 2.5V \pm 5\%$
7	Current dissipation per LVDS output	$I_{DD,LVDSL,3.3V}$		6.73	8.00	mA	$V_{DDO} = 3.3V \pm 5\%$
		$I_{DD,LVDS,2.5V}$		6.87	7.83	mA	$V_{DDO} = 2.5V \pm 5\%$
8	Current dissipation per HCSL output	$I_{DD,HCSL,3.3V}$		16.43	19.87	mA	$V_{DDO} = 3.3V \pm 5\%$
		$I_{DD,HCSL,2.5V}$		17.14	19.18	mA	$V_{DDO} = 2.5V \pm 5\%$

**Table 8 Input Characteristics\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage for control inputs	$V_{CIH}$	1.05			V	
2	CMOS low-level input voltage for control inputs	$V_{CIL}$			0.45	V	
3	CMOS input leakage current for control inputs (includes current due to pull down resistors)	$I_L$	-25		50	$\mu A$	$V_i = V_{DD}$ or 0 V
4	Differential input common mode voltage for IN0_p/n and IN1_p/n	$V_{CM}$	1		2	V	
5	Differential input voltage difference for IN0_p/n and IN1_p/n	$V_{ID}$	0.15		1.3	V	
6	Differential input voltage difference for IN0_p/n and IN1_p/n for $1GHz < f < 1.6GHz$	$V_{ID}$	0.35		1.3		
7	Differential input leakage current for IN0_p/n and IN1_p/n (includes current due to pull-up and pull-down resistors)	$I_L$	-150		150	$\mu A$	$V_i = 2V$ or 0V
8	Single ended input voltage for IN0_p and IN1_p	$V_{SI}$	-0.3		2.7	V	$V_{DD} = 3.3V$ or $2.5V$
9	Single ended input common mode voltage (IN0_p/n and IN1_p/n)	$V_{SIC}$	1		2	V	$V_{DD} = 3.3V$ or $2.5V$
10	Single ended input voltage swing for IN0_p and IN1_p	$V_{SID}$	0.3		1.3	V	$V_{DD} = 3.3V$ or $2.5V$
11	Input frequency (differential)	$f_{IN}$	0		1600	MHz	
12	Input frequency (LVCMOS)	$f_{IN\_CMOS}$	0		250	MHz	
13	Input duty cycle	dc	35%		65%		
14	Input slew rate	slew		2		V/ns	
15	Input pull-up/ pull-down resistance	$R_{PU}/R_{PD}$		60k $\Omega$			
16	Input pull-down resistance for INx_p	$R_{PD}$		30k $\Omega$			
17	Input multiplexer isolation IN0_p/n to IN1_p/n and vice versa Power on both inputs 0dBm, $f_{OFFSET} > 50kHz$	Iso			-84 -82 -71 -67	dBc	$f_{IN} = 100$ MHz $f_{IN} = 200$ MHz $f_{IN} = 400$ MHz $f_{IN} = 800$ MHz

\* Values are over Recommended Operating Conditions

\* Values are over all two power supply modes ( $V_{DD} = 3.3V$  and  $V_{DD} = 2.5V$ )

\* Input mux isolation is measured as amplitude of  $f_{OFFSET}$  spur in dBc on the output clock phase noise plot

**Table 9 Crystal Oscillator Characteristics\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Mode of oscillation	mode	Fundamental				
2	Frequency	f	8		160	MHz	
3	On chip load capacitance in SPI controlled mode	$C_L$	0		21.75	pF	Programmable
4	On chip load capacitance in pin controlled mode			4		pF	Fixed
5	On chip series resistor in SPI controlled mode	$R_S$	0		312	$\Omega$	Programmable
6	On chip series resistor in pin controlled mode			84		$\Omega$	Fixed
7	On chip shunt resistor	R		500		k $\Omega$	
8	Frequency in overdrive mode <sup>(1)</sup>	$f_{OV}$	0.1		250	MHz	Functional but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1 $\mu F$ assumed)
9	Frequency in bypass mode <sup>(2)</sup>	$f_{BP}$	0		250	MHz	Functional but may not meet AC parameters

\* Values are over Recommended Operating Conditions

\* Values are over all two power supply modes ( $V_{DD} = 3.3V$  and  $V_{DD} = 2.5V$ )

(1) Maximum input level is 2V

(2) Maximum output level is VDD

**Table 10 Power Supply Rejection Ratio for VDD = VDDO = 3.3V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	PSRR for LVPECL output	PSRR <sub>LVPECL</sub>		-71.75		dBc	f <sub>IN</sub> = 156.25 MHz
				-84.45			f <sub>IN</sub> = 312.5 MHz
				-82.11			f <sub>IN</sub> = 625 MHz
2	PSRR for LVDS output	PSRR <sub>LVDS</sub>		-95.16		dBc	f <sub>IN</sub> = 156.25 MHz
				-97.77			f <sub>IN</sub> = 312.5 MHz
				-79.23			f <sub>IN</sub> = 625 MHz
3	PSRR for HCSSL output	PSRR <sub>HCSSL</sub>		-77.15		dBc	f <sub>IN</sub> = 100 MHz
				-76.75			f <sub>IN</sub> = 156.25 MHz
				-80.44			f <sub>IN</sub> = 312.5 MHz

\* Values are over Recommended Operating Conditions

\* Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp

\* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot

**Table 11 Power Supply Rejection Ratio for VDD = VDDO = 2.5V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	PSRR for LVPECL output	PSRR <sub>LVPECL</sub>		-73.68		dBc	f <sub>IN</sub> = 156.25 MHz
				-78.88			f <sub>IN</sub> = 312.5 MHz
				-71.82			f <sub>IN</sub> = 625 MHz
2	PSRR for LVDS output	PSRR <sub>LVDS</sub>		-90.04		dBc	f <sub>IN</sub> = 156.25 MHz
				-79.99			f <sub>IN</sub> = 312.5 MHz
				-73.45			f <sub>IN</sub> = 625 MHz
3	PSRR for HCSSL output	PSRR <sub>HCSSL</sub>		-92.16		dBc	f <sub>IN</sub> = 100 MHz
				-74.08			f <sub>IN</sub> = 156.25 MHz
				-91.88			f <sub>IN</sub> = 312.5 MHz

\* Values are over Recommended Operating Conditions

\* Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp

\* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot

**Table 12 LVCMOS Output Characteristics for VDDO = 3.3V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage (1 mA load)	V <sub>OH</sub>	VDDO-0.1			V	DC Measurement
2	Output low voltage (1 mA load)	V <sub>OL</sub>			0.1	V	DC Measurement
3	Output High Current (Load adjusted to V <sub>out</sub> = VDDO/2)	I <sub>OH</sub>		30		mA	DC Measurement
4	Output Low Current (Load adjusted to V <sub>out</sub> = VDDO/2)	I <sub>OL</sub>		34		mA	DC Measurement
5	Output impedance	R <sub>O</sub>		15		Ω	DC Measurement
6	Rise time (20% to 80%)	t <sub>r</sub>		220	310	ps	
7	Fall time (20% to 80%)	t <sub>f</sub>		320	365	ps	
8	Output frequency	F <sub>O</sub>	0		250	MHz	
9	Input to output delay	t <sub>IOD</sub>	1.07	1.28	2.07	ns	
10	Output enable time	t <sub>EN</sub>			3	cycles	
11	Output disable time	T <sub>DIS</sub>			3	cycles	
12	Additive RMS jitter in 1MHz to 5MHz band	T <sub>J,1M,5M</sub>		46	80	fs	Input Clock 25MHz
13	Additive RMS jitter in 12kHz to 5MHz band	T <sub>J,12K,5M</sub>		56	90	fs	Input Clock 25MHz
14	Additive RMS jitter in 1MHz to 20MHz band	T <sub>J,1M,20M</sub>		60	79	fs	Input Clock 125MHz
15	Additive RMS jitter in 12kHz to 20MHz band	T <sub>J,12K,20M</sub>		65	86	fs	Input Clock 125MHz
16	Additive RMS jitter in 1MHz to 20MHz band	T <sub>J,1M,20M</sub>		61	94	fs	Input Clock 156.25MHz
17	Additive RMS jitter in 12kHz to 20MHz band	T <sub>J,12K,20M</sub>		66	100	fs	Input Clock 156.25MHz
18	Noise floor	N <sub>F</sub>		-165	-162	dBc/Hz	Input clock: 25 MHz
19				-160	-156	dBc/Hz	Input clock: 125 MHz
20				-158	-153	dBc/Hz	Input clock: 156.25 MHz

\* Values are over Recommended Operating Conditions

**Table 13 LVCMOS Output Characteristics for VDDO = 2.5V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage (1 mA load)	$V_{OH}$	VDDO-0.1			V	DC Measurement
2	Output low voltage (1 mA load)	$V_{OL}$			0.1	V	DC Measurement
3	Output High Current (Load adjusted to $V_{out} = VDDO/2$ )	$I_{OH}$		21		mA	DC Measurement
4	Output Low Current (Load adjusted to $V_{out} = VDDO/2$ )	$I_{OL}$		25		mA	DC Measurement
5	Output impedance	$R_O$		15		$\Omega$	DC Measurement
6	Rise time (20% to 80%)	$t_r$		225	310	ps	
7	Fall time (20% to 80%)	$t_f$		320	365	ps	
8	Output frequency	$F_O$	0		250	MHz	
9	Input to output delay	$t_{IOD}$	1.10	1.41	2.30	ns	
10	Output enable time	$t_{EN}$			3	cycles	
11	Output disable time	$T_{DIS}$			3	cycles	
12	Additive RMS jitter in 1MHz to 5MHz band	$T_{j,1M,5M}$		51	104	fs	Input Clock 25MHz
13	Additive RMS jitter in 12kHz to 5MHz band	$T_{j,12k,5M}$		62	111	fs	Input Clock 25MHz
14	Additive RMS jitter in 1MHz to 20MHz band	$T_{j,1M,20M}$		64	81	fs	Input Clock 125MHz
15	Additive RMS jitter in 12kHz to 20MHz band	$T_{j,12k,20M}$		70	88	fs	Input Clock 125MHz
16	Additive RMS jitter in 1MHz to 20MHz band	$T_{j,1M,20M}$		62	94	fs	Input Clock 156.25MHz
17	Additive RMS jitter in 12kHz to 20MHz band	$T_{j,12k,20M}$		68	100	fs	Input Clock 156.25MHz
18	Noise floor	$N_F$		-164	-161	dBc/Hz	Input clock: 25 MHz
19				-159	-155	dBc/Hz	Input clock: 125 MHz
20				-158	-153	dBc/Hz	Input clock: 156.25 MHz

\* Values are over Recommended Operating Conditions

**Table 14 LVPECL Output Characteristics for VDDO = 3.3V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	$V_{LVPECL\_OH}$	1.9	2.08	2.4	V	DC Measurement
2	Output low voltage	$V_{LVPECL\_OL}$	1.2	1.36	1.7	V	DC Measurement
3	Output differential swing**	$V_{LVPECL\_SW}$	0.6	0.72	0.9	V	DC Measurement
4	Variation of $V_{LVPECL\_SW}$ for complementary output states	$\Delta V_{LVPECL\_SW}$	0	0.02	0.07	V	
5	Common mode output	$V_{CM}$	1.6	1.72	2.1	V	
7	Output frequency when $V_{LVPECL\_SW} \geq 0.6V$	$F_{MAX\_0.6VSW}$			800	MHz	
8	Output frequency when $V_{LVPECL\_SW} \geq 0.4V$	$F_{MAX\_0.4VSW}$			1600	MHz	
9	Rise or fall time (20% to 80%)	$t_r, t_f$		110	170	ps	
10	Output frequency	$F_O$	0		1600	MHz	
11	Output to output skew	$t_{OOSK}$			40	ps	
12	Device to device output skew	$t_{DOOSK}$			120	ps	
13	Input to output delay	$t_{IOD}$	0.73	0.87	1.1	ns	
14	Output enable time	$t_{EN}$			3	cycles	
15	Output disable time	$t_{DIS}$			3	cycles	
16	Additive RMS jitter in 1MHz to 20MHz band	$T_{L1M,20M}$		68	96	fs	Input clock: 100 MHz
				52	102	fs	Input clock: 156.25MHz
				20	32	fs	Input clock: 625 MHz
17	Additive RMS jitter in 12kHz to 20MHz band	$T_{L12k,20M}$		71	101	fs	Input clock: 100 MHz
				57	106	fs	Input clock: 156.25MHz
				25	39	fs	Input clock: 625 MHz
18	Noise floor	$N_F$		-161	-159	dBc/Hz	Input clock: 100 MHz
				-160	-155	dBc/Hz	Input clock: 156.25 MHz
				-155	-151	dBc/Hz	Input clock: 625 MHz

\* Values are over Recommended Operating Conditions

\*\*Output differential swing is calculated as  $V_{SW} = V_{OH} - V_{OL}$ . It should not be confused with  $V_{SW} = 2 * (V_{OH} - V_{OL})$  sometimes used in some datasheets

**Table 15 LVPECL Output Characteristics for VDDO = 2.5V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	$V_{LVPECL\_OH}$	1.1	1.28	1.7	V	DC Measurement
2	Output low voltage	$V_{LVPECL\_OL}$	0.4	0.57	0.9	V	DC Measurement
3	Output differential swing**	$V_{LVPECL\_SW}$	0.6	0.71	0.9	V	DC Measurement
4	Variation of $V_{LVPECL\_SW}$ for complementary output states	$\Delta V_{LVPECL\_SW}$	0	0.02	0.05	V	
5	Common mode output	$V_{CM}$	0.8	0.92	1.2	V	
7	Output frequency when $V_{LVPECL\_SW} \geq 0.6V$	$F_{MAX\_0.6VSW}$			800	MHz	
8	Output frequency when $V_{LVPECL\_SW} \geq 0.4V$	$F_{MAX\_0.4VSW}$			1600	MHz	
9	Rise or fall time (20% to 80%)	$t_r, t_f$		120	170	ps	
10	Output frequency	$F_O$	0		1600	MHz	
11	Output to output skew	$t_{OOSK}$			40	ps	
12	Device to device output skew	$t_{DOOSK}$			120	ps	
13	Input to output delay	$t_{IOD}$	0.75	0.87	1.1	ns	
14	Output enable time	$t_{EN}$			3	cycles	
15	Output disable time	$t_{DIS}$			3	cycles	
16	Additive RMS jitter in 1MHz to 20MHz band	$T_{JL1M,20M}$		65	91	fs	Input clock: 100 MHz
				50	95	fs	Input clock: 156.25MHz
				20	30	fs	Input clock: 625 MHz
17	Additive RMS jitter in 12kHz to 20MHz band	$T_{JL12k,20M}$		69	99	fs	Input clock: 100 MHz
				55	101	fs	Input clock: 156.25MHz
				26	41	fs	Input clock: 625 MHz
18	Noise floor	$N_F$		-161	-159	dBc/Hz	Input clock: 100 MHz
				-160	-156	dBc/Hz	Input clock: 156.25 MHz
				-155	-151	dBc/Hz	Input clock: 625 MHz

\* Values are over Recommended Operating Conditions

\*\*Output differential swing is calculated as  $V_{SW} = V_{OH} - V_{OL}$ . It should not be confused with  $V_{SW} = 2 * (V_{OH} - V_{OL})$  used in some datasheets

**Table 16 LVDS Outputs for VDDO = 3.3V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	$V_{LVDS\_OH}$	1.3	1.39	1.47	V	DC Measurement
2	Output low voltage	$V_{LVDS\_OL}$	1.0	1.07	1.15	V	DC Measurement
3	Output differential swing**	$V_{LVDS\_SW}$	0.25	0.32	0.39	V	DC Measurement
4	Variation of $V_{LVDS\_SW}$ for complementary output states	$\Delta V_{LVDS\_SW}$	0	0.002	0.01	V	
5	Common mode output	$V_{CM}$	1.15	1.23	1.3	V	
6	Variation of $V_{CM}$ for complementary output states	$\Delta V_{CM}$	0	0.001	0.01	V	
7	Output frequency when $V_{LVDS\_SW} \geq 250mV$	$F_{MAX\_0.25VSW}$			800	MHz	
8	Output frequency when $V_{LVDS\_SW} \geq 200mV$	$F_{MAX\_0.2VSW}$			1600	MHz	
9	Rise or fall time (20% to 80%)	$t_r, t_f$		110	170	ps	
10	Output frequency	$F_O$	0		1600	MHz	
11	Output to output skew	$t_{OOSK}$			20	ps	
12	Device to device output skew	$t_{DOOSK}$			130	ps	
13	Input to output delay	$t_{IOD}$	0.76	0.86	1.1	ns	
14	Output Short Circuit Current Single Ended	$I_S$	-24		24	mA	Single ended outputs shorted to GND
15	Output Short Circuit Current Differential	$I_{SD}$	-24		24	mA	Complementary outputs shorted
16	Output enable time	$t_{EN}$			3	cycles	
17	Output disable time	$t_{DIS}$			3	cycles	
18	Additive RMS jitter in 1MHz to 20MHz band	$T_{L1M,20M}$		110	144	fs	Input clock: 100 MHz
				65	112	fs	Input clock: 156.25MHz
				21	33	fs	Input clock: 625 MHz
19	Additive RMS jitter in 12kHz to 20MHz band	$T_{L12k,20M}$		115	150	fs	Input clock: 100 MHz
				73	143	fs	Input clock: 156.25MHz
				26	40	fs	Input clock: 625 MHz
20	Noise floor	$N_F$		-158	-156	dBc/Hz	Input clock: 100 MHz
				-158	-155	dBc/Hz	Input clock: 156.25 MHz
				-154	-151	dBc/Hz	Input clock: 625 MHz

\* Values are over Recommended Operating Conditions

\*\*Output differential swing is calculated as  $V_{SW} = V_{OH} - V_{OL}$ . It should not be confused with  $V_{SW} = 2 * (V_{OH} - V_{OL})$  used in some datasheets

**Table 17 LVDS Outputs for VDDO = 2.5V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	$V_{LVDS\_OH}$	1.3	1.4	1.5	V	DC Measurement
2	Output low voltage	$V_{LVDS\_OL}$	0.97	1.05	1.13	V	DC Measurement
3	Output differential swing**	$V_{LVDS\_SW}$	0.25	0.35	0.44	V	DC Measurement
4	Variation of $V_{LVDS\_SW}$ for complementary output states	$\Delta V_{LVDS\_SW}$	0	0.001	0.01	V	
5	Common mode output	$V_{CM}$	1.15	1.23	1.3	V	
6	Variation of $V_{CM}$ for complementary output states	$\Delta V_{CM}$	0	0.001	0.01	V	
7	Output frequency when $V_{LVDS\_SW} \geq 250mV$	$F_{MAX\_0.25VSW}$			800	MHz	
8	Output frequency when $V_{LVDS\_SW} \geq 200mV$	$F_{MAX\_0.2VSW}$			1600	MHz	
9	Rise or fall time (20% to 80%)	$t_r, t_f$		110	170	ps	
10	Output frequency	$F_O$	0		1600	MHz	
11	Output to output skew	$t_{OOSK}$			20	ps	
12	Device to device output skew	$t_{DOOSK}$			130	ps	
13	Input to output delay	$t_{IOD}$	0.78	0.86	1.12	ns	
14	Output Short Circuit Current Single Ended	$I_S$	-24		24	mA	Single ended outputs shorted to GND
15	Output Short Circuit Current Differential	$I_{SD}$	-24		24	mA	Complementary outputs shorted
16	Output enable time	$t_{EN}$			3	cycles	
17	Output disable time	$t_{DIS}$			3	cycles	
18	Additive RMS jitter in 1MHz to 20MHz band	$T_{L1M,20M}$		107	140	fs	Input clock: 100 MHz
				61	103	fs	Input clock: 156.25MHz
				20	31	fs	Input clock: 625 MHz
19	Additive RMS jitter in 12kHz to 20MHz band	$T_{L12k,20M}$		111	146	fs	Input clock: 100 MHz
				66	106	fs	Input clock: 156.25MHz
				24	36	fs	Input clock: 625 MHz
20	Noise floor	$N_F$		-158	-156	dBc/Hz	Input clock: 100 MHz
				-159	-155	dBc/Hz	Input clock: 156.25 MHz
				-155	-151	dBc/Hz	Input clock: 625 MHz

\* Values are over Recommended Operating Conditions

\*\*Output differential swing is calculated as  $V_{SW} = V_{OH} - V_{OL}$ . It should not be confused with  $V_{SW} = 2 * (V_{OH} - V_{OL})$  used in some datasheets

**Table 18 HCSL Outputs for VDDO = 3.3V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	$V_{HCSL\_OH}$	0.6	0.85	1.1	V	DC Measurement
2	Output low voltage	$V_{HCSL\_OL}$	-0.05	0	0.05	V	DC Measurement
3	Output differential swing**	$V_{HCSL\_SW}$	0.6	0.85	1.1	V	DC Measurement
4	Variation of $V_{HCSL\_SW}$ for complementary output states	$\Delta V_{HCSL\_SW}$	0	0.003	0.05	V	
5	Common mode output	$V_{CM}$	0.28	0.43	0.55	V	
6	Variation of $V_{CM}$ for complementary output states	$\Delta V_{CM}$	0	0.002	0.05	V	
7	Absolute Crossing Voltage	$V_{CROSS}$	0.320	0.384	0.447	V	
8	Total Variation of $V_{CROSS}$	$\Delta V_{CROSS}$			0.127	V	
9	Output frequency	$F_{MAX}$	0		400	MHz	
10	Rise or fall time (20% to 80%)	$t_r, t_f$		143	309	ps	
11	Output to output skew	$t_{OOSK}$			21	ps	
12	Device to device output skew	$t_{DOOSK}$			129	ps	
13	Input to output delay	$t_{IOD}$	0.73	0.90	1.08	ns	
14	Output enable time	$t_{EN}$			3	cycles	
15	Output disable time	$t_{DIS}$			3	cycles	
16	Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{JPCIE\_3.0}$		20	40	fs	Input clock: 100MHz
17	Additive RMS jitter in 1MHz to 20MHz band	$T_{L1M\_20M}$		73	104	fs	Input clock: 100 MHz
				56	106	fs	Input clock: 156.25MHz
18	Additive RMS jitter in 12kHz to 20MHz band	$T_{L12K\_20M}$		77	112	fs	Input clock: 100 MHz
				66	114	fs	Input clock: 156.25MHz
19	Noise floor	$N_F$		-161	-159	dBc/Hz	Input clock: 100 MHz
				-159	-155	dBc/Hz	Input clock: 156.25 MHz

\* Values are over Recommended Operating Conditions

\*\*Output differential swing is calculated as  $V_{SW} = V_{OH} - V_{OL}$ . It should not be confused with  $V_{SW} = 2 * (V_{OH} - V_{OL})$  used in some datasheets

**Table 19 HCSL Outputs for VDDO = 2.5V\***

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	$V_{HCSL\_OH}$	0.6	0.83	1.1	V	DC Measurement
2	Output low voltage	$V_{HCSL\_OL}$	-0.05	0	0.05	V	DC Measurement
3	Output differential swing**	$V_{HCSL\_SW}$	0.5	0.83	1.1	V	DC Measurement
4	Variation of $V_{HCSL\_SW}$ for complementary output states	$\Delta V_{HCSL\_SW}$	0	0.003	0.05	V	
5	Common mode output	$V_{CM}$	0.28	0.42	0.55	V	
6	Variation of $V_{CM}$ for complementary output states	$\Delta V_{CM}$	0	0.002	0.05	V	
7	Absolute Crossing Voltage	$V_{CROSS}$	0.260	0.316	0.372	V	
8	Total Variation of $V_{CROSS}$	$\Delta V_{CROSS}$			0.108	V	
9	Output frequency	$F_{MAX}$	0		400	MHz	
10	Rise or fall time (20% to 80%)	$t_r, t_f$		125	162	ps	
11	Output to output skew	$t_{OOSK}$			21	ps	
12	Device to device output skew	$t_{DOOSK}$			129	ps	
13	Input to output delay	$t_{IOD}$	0.76	0.92	1.10	ns	
14	Output enable time	$t_{EN}$			3	cycles	
15	Output disable time	$t_{DIS}$			3	cycles	
16	Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{JPCIE\_3.0}$		20	40	fs	Input clock: 100MHz
17	Additive RMS jitter in 1MHz to 20MHz band	$T_{L1M\_20M}$		68	95	fs	Input clock: 100 MHz
				52	96	fs	Input clock: 156.25MHz
18	Additive RMS jitter in 12kHz to 20MHz band	$T_{L12K\_20M}$		72	102	fs	Input clock: 100 MHz
				57	102	fs	Input clock: 156.25MHz
19	Noise floor	$N_F$		-161	-158	dBc/Hz	Input clock: 100 MHz
				-160	-153	dBc/Hz	Input clock: 156.25 MHz

\* Values are over Recommended Operating Conditions

\*\*Output differential swing is calculated as  $V_{SW} = V_{OH} - V_{OL}$ . It should not be confused with  $V_{SW} = 2 * (V_{OH} - V_{OL})$  used in some datasheets

**Table 20 LVCMOS Output Phase Noise with 25 MHz XTAL\***

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 5MHz band		103		fs	VDD = 3.3V, VDDO = 3.3V
			117		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-75		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-107		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-132		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-150		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-162		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-166		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-166		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-70		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-102		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-130		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-149		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-161		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-165		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
	-165		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V		

\* Values are over Recommended Operating Conditions

**Table 21 LVPECL Output Phase Noise with 25 MHz XTAL\***

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 5MHz band		265		fs	VDD = 3.3V, VDDO = 3.3V
			213		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-75		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-107		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-133		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-152		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-158		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-71		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-103		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-130		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-151		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-160		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
	-159		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V		

\* Values are over Recommended Operating Conditions

**Table 22 LVDS Output Phase Noise with 25 MHz XTAL**

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 5MHz band		178		fs	VDD = 3.3V, VDDO = 3.3V
			190		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-75		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-107		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-133		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-154		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-161		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-161		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-160		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-68		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-103		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-130		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-152		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-161		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
	-160		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V		
	-159		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V		

\* Values are over Recommended Operating Conditions

**Table 23 HCSL Output Phase Noise with 25 MHz XTAL**

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		269		fs	VDD = 3.3V, VDDO = 3.3V
			228		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-76		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-107		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-133		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-152		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-73		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-105		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-131		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-151		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
	-159		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V		
	-159		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V		

\* Values are over Recommended Operating Conditions

**Table 24 LVCMOS Output Phase Noise with 125 MHz XTAL\***

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		92		fs	VDD = 3.3V, VDDO = 3.3V
			105		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-58		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-90		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-118		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-136		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-150		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-158		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-159		dBc/Hz	@10MHz, VDD = 3.3V, VDDO = 3.3V
			-53		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-86		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-113		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-134		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-148		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-157		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@10MHz, VDD = 2.5V; VDDO = 2.5V

\* Values are over Recommended Operating Conditions

**Table 25 LVPECL Output Phase Noise with 125 MHz XTAL\***

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		76		fs	VDD = 3.3V, VDDO = 3.3V
			86		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-58		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-90		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-118		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-140		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-154		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-159		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-161		dBc/Hz	@10MHz, VDD = 3.3V, VDDO = 3.3V
			-54		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-86		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-114		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-137		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-152		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-160		dBc/Hz	@10MHz, VDD = 2.5V; VDDO = 2.5V

\* Values are over Recommended Operating Conditions

**Table 26 LVDS Output Phase Noise with 125 MHz XTAL**

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		98		fs	VDD = 3.3V, VDDO = 3.3V
			100		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-57		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-90		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-118		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-140		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-152		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-158		dBc/Hz	@10MHz, VDD = 3.3V, VDDO = 3.3V
			-54		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-86		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-114		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-137		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-153		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-157		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@10MHz, VDD = 2.5V; VDDO = 2.5V

\* Values are over Recommended Operating Conditions

**Table 27 HCSL Output Phase Noise with 125 MHz XTAL**

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		83		fs	VDD = 3.3V, VDDO = 3.3V
			85		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-58		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-90		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-118		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-140		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-152		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-158		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-160		dBc/Hz	@10MHz, VDD = 3.3V, VDDO = 3.3V
			-54		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-86		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-114		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-137		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-153		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-159		dBc/Hz	@10MHz, VDD = 2.5V; VDDO = 2.5V

\* Values are over Recommended Operating Conditions

**Table 28 LVCMOS Output Phase Noise with 156.25 MHz XTAL\***

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		79		fs	VDD = 3.3V, VDDO = 3.3V
			88		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-53		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-81		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-111		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-135		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-149		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-159		dBc/Hz	@10MHz, VDD = 3.3V, VDDO = 3.3V
			-53		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-82		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-113		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-135		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-148		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-156		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@10MHz, VDD = 2.5V; VDDO = 2.5V

\* Values are over Recommended Operating Conditions

**Table 29 LVPECL Output Phase Noise with 156.25 MHz XTAL\***

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		61		fs	VDD = 3.3V, VDDO = 3.3V
			68		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-52		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-80		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-111		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-140		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-153		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-159		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-161		dBc/Hz	@10MHz, VDD = 3.3V, VDDO = 3.3V
			-53		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-81		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-114		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-140		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-151		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-160		dBc/Hz	@10MHz, VDD = 2.5V; VDDO = 2.5V

\* Values are over Recommended Operating Conditions

**Table 30 LVDS Output Phase Noise with 156.25 MHz XTAL**

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		79		fs	VDD = 3.3V, VDDO = 3.3V
			76		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-52		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-81		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-111		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-138		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-148		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-159		dBc/Hz	@10MHz, VDD = 3.3V, VDDO = 3.3V
			-52		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-82		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-113		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-140		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-151		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-157		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-159		dBc/Hz	@10MHz, VDD = 2.5V; VDDO = 2.5V

\* Values are over Recommended Operating Conditions

**Table 31 HCSSL Output Phase Noise with 156.25 MHz XTAL**

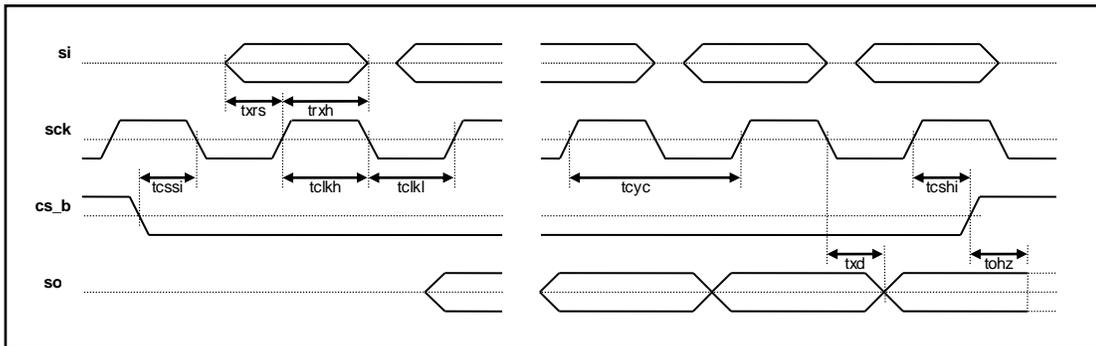
	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		72		fs	VDD = 3.3V, VDDO = 3.3V
			72		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-53		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-86		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-114		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-139		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-148		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-160		dBc/Hz	@10MHz, VDD = 3.3V, VDDO = 3.3V
			-53		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-86		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-115		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-140		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-151		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-157		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-160		dBc/Hz	@10MHz, VDD = 2.5V; VDDO = 2.5V

\* Values are over Recommended Operating Conditions

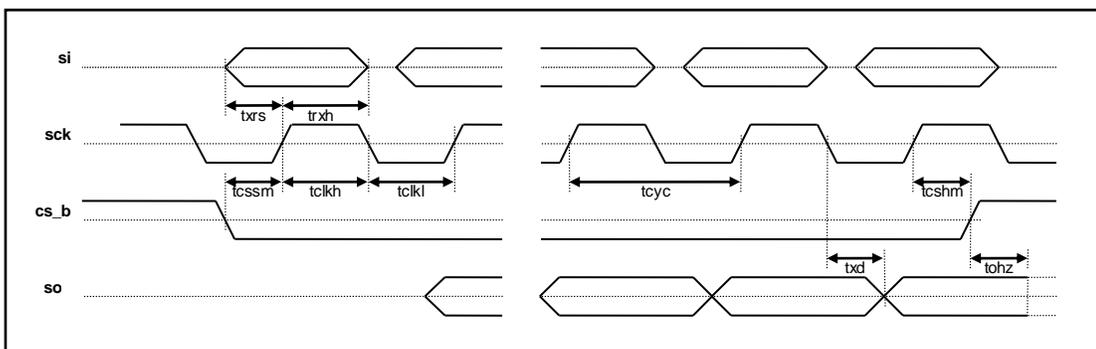
**Table 32 AC Electrical Characteristics\* - SPI (Serial Peripheral Interface) Timing**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	sck period	tcyc	124			ns	See Figure 44& Figure 45
2	sck pulse width low	tccl	62			ns	
3	sck pulse width high	tcch	62			ns	
4	si setup (write) from sck rising edge	trxs	10			ns	
5	si hold (write) from sck falling edge	trxh	10			ns	
6	so delay (read) from sck falling edge	txd			25	ns	
7	cs_b to output high impedance	tohz			60	ns	
8	cs_b setup from sck falling edge (LSB first)	tcssi	20			ns	See Figure 44
9	cs_b hold from sck falling edge (LSB first)	tcshl	10			ns	See Figure 45
10	cs_b setup from sck falling edge (MSB first)	tcssm	20			ns	
11	cs_b hold from sck falling edge (MSB first)	tcshm	10			ns	

\* Values are over Recommended Operating Conditions  
 \* For LSB first mode timing diagram, refer to Figure 44  
 \* For MSB first mode timing diagram, refer to Figure 45  
 \* Values shown are proposed for the data sheet, these values are to be confirmed



**Figure 44. SPI (Serial Peripheral Interface) Timing - LSB First Mode**



**Figure 45. SPI (Serial Peripheral Interface) Timing - MSB First Mode**

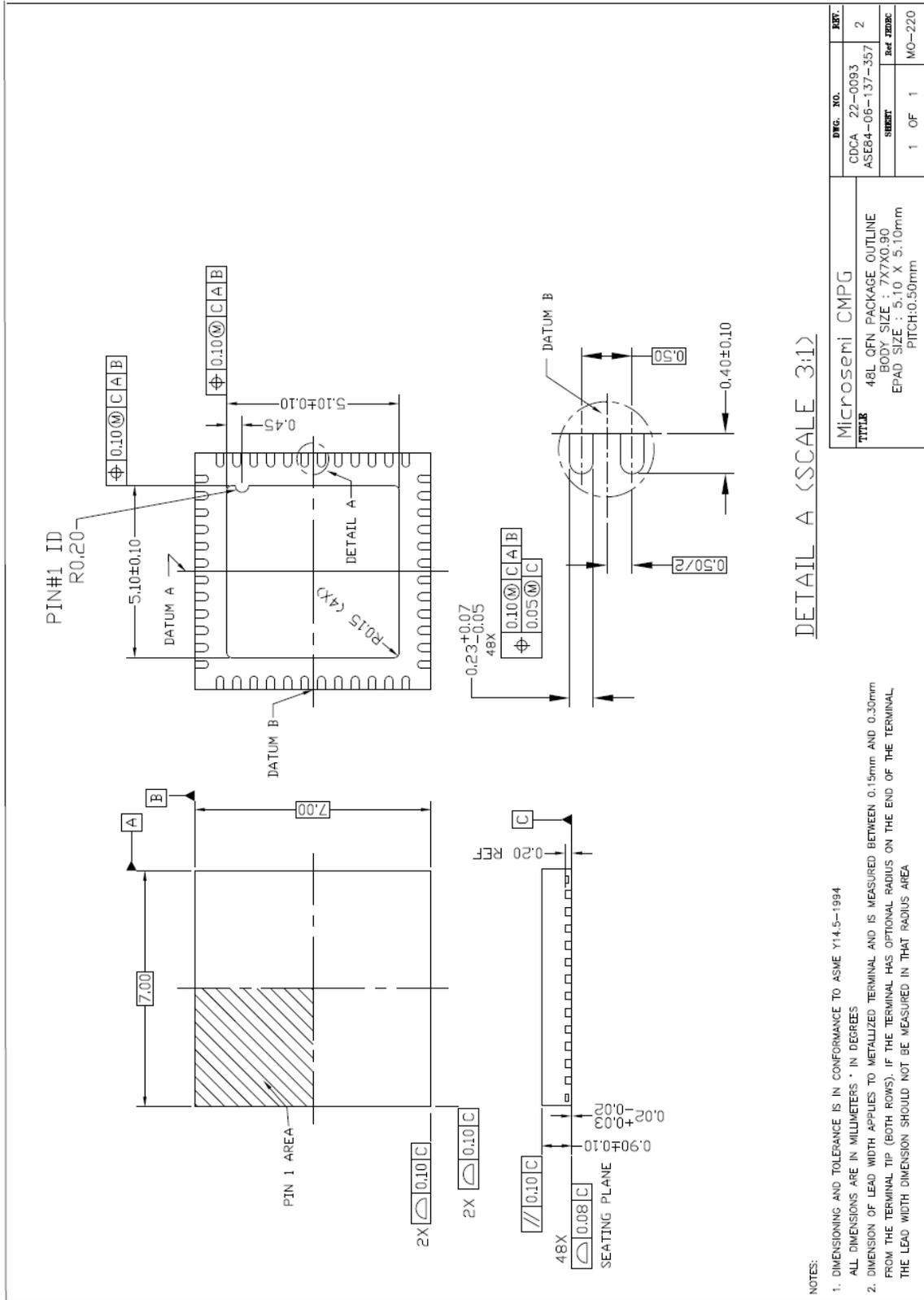
**Table 33 7x7mm QFN Package Thermal Properties**

Parameter	Symbol	Condition	Value	Units
Maximum Ambient Temperature	$T_A$		85	°C
Maximum Junction Temperature	$T_{JMAX}$		125	°C
Junction to Ambient Thermal Resistance <sup>(1)</sup>	$\theta_{JA}$	still air	21.1	°C/W
		1 m/s airflow	16.9	
		2.5 m/s airflow	15.0	
Junction to Board Thermal Resistance	$\theta_{JB}$		6.9	°C/W
Junction to Case Thermal Resistance	$\theta_{JC}$		12.8	°C/W
Junction to Pad Thermal Resistance <sup>(2)</sup>	$\theta_{JP}$	Still air	3.9	°C/W
Junction to Top-Center Thermal Characterization Parameter	$\Psi_{JT}$	Still air	0.2	°C/W

(1) Theta-JA ( $\theta_{JA}$ ) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power

(2) Theta-JP ( $\theta_{JP}$ ) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

Package Outline



DRG. NO.	REV.
CDCA 22-0093	2
ASE64-06-137-357	
SUBJECT	
1 OF 1	MO-220

**Microsemi CMPG**  
**TITLE**  
 48L QFN PACKAGE OUTLINE  
 BODY SIZE : 7X7X0.90  
 EPAD SIZE : 5.10 X 5.10mm  
 PITCH:0.50mm

DETAIL A (SCALE 3:1)

- NOTES:
1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS \* IN DEGREES
  3. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA



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