

Ten LVCMOS Output Low Additive Jitter Fanout Buffer

Features

- 3 to 1 input Multiplexer: Two inputs accept any differential (LVPECL, HCSSL, LVDS, SSTL, CML, LVCMOS) or a single ended signal and the third input accepts a crystal or a single ended signal
- Ten 1.5V/1.8V/2.5V/3.3V LVCMOS outputs
- Supports frequencies from 0 to 200MHz
- Supports crystals from 8MHz to 60MHz
- Ultra-low additive jitter: 25fs (12kHz to 20MHz)
- Ultra-low noise floor of -165dBc/Hz
- Supports 2.5V or 3.3V power supplies
- Output to output skew of 30ps (typical)
- Input to output delay of 2ns (typical)

Ordering Information

ZL40241LDG1	32 Pin QFN	Trays
ZL40241LDF1	32 pin QFN	Tape and Reel

Package size: 5 x 5 mm
-40°C to +85°C

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired and Wireless communications
- High performance microprocessor clock distribution
- Medical Imaging
- Test equipment

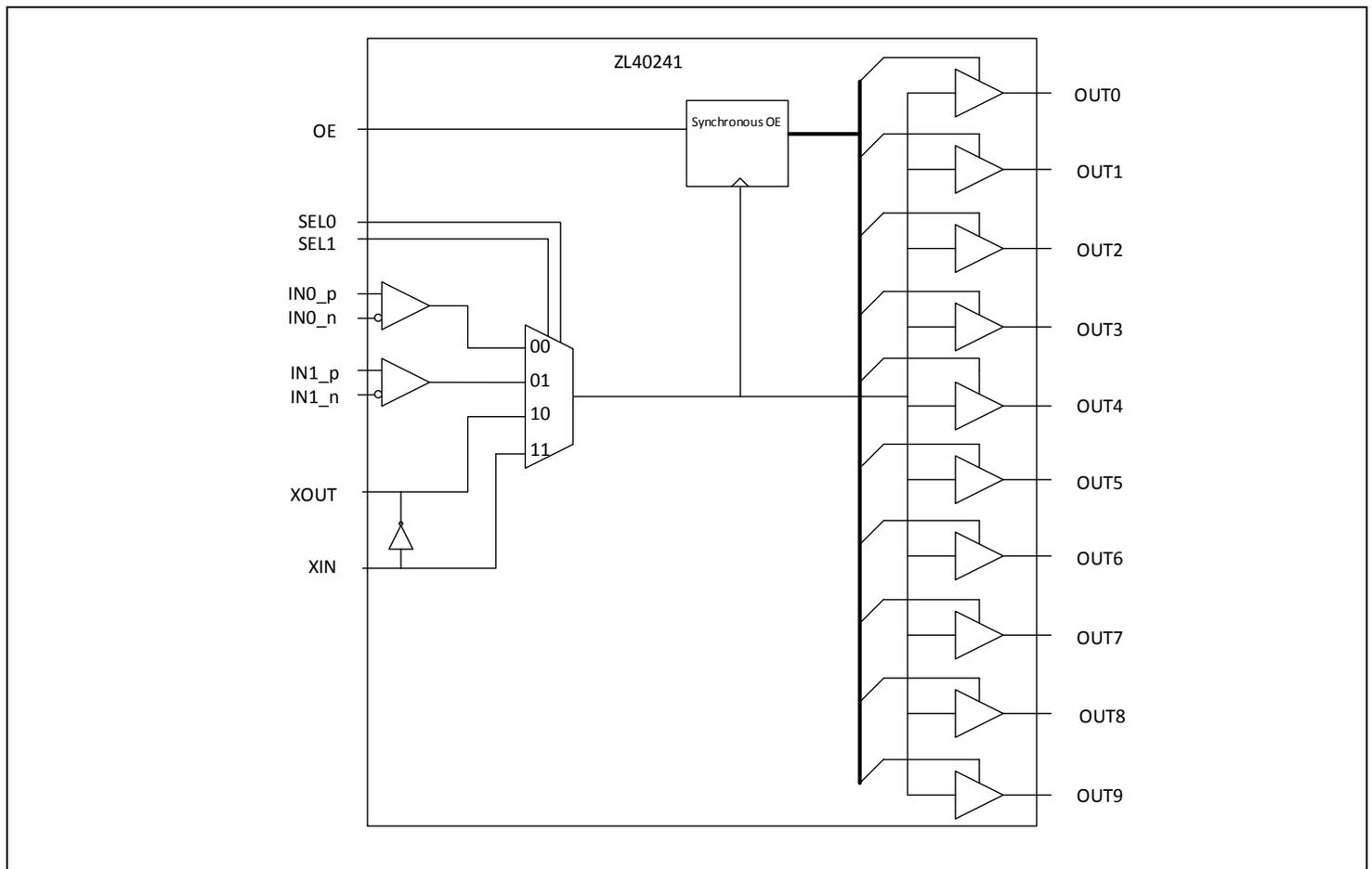


Figure 1. Functional Block Diagram

Table of Contents

Features.....	1
Table of Contents	2
Pin Diagram	5
Pin Descriptions.....	6
Functional Description	8
Clock Inputs	8
Clock Outputs	11
Crystal Oscillator Input.....	11
Termination of unused inputs and outputs	12
Device Control	12
AC and DC Electrical Characteristics	14
Absolute Maximum Ratings.....	14
Recommended Operating Conditions	14
Package Outline	19

List of Figures

Figure 1.	Functional Block Diagram.....	1
Figure 2.	Pin Diagram	5
Figure 3.	Input driven by a single ended output	8
Figure 4.	Input driven by DC coupled LVPEVCL output	8
Figure 5.	Input driven by DC coupled LVPEVCL output (alternative termination).....	9
Figure 6.	Input driven by AC coupled LVPECL output.....	9
Figure 7.	Input driven by HCSL output	9
Figure 8.	Input driven by LVDS output	10
Figure 9.	Input driven by AC coupled LVDS.....	10
Figure 10.	Input driven by an SSTL output	10
Figure 11.	Termination for 3.3V LVPECL outputs.....	11
Figure 12.	Crystal Oscillator Circuit.....	11
Figure 13.	Phase Noise Plot with 25MHz Crystal	12
Figure 14.	OE Output Disable	13
Figure 15.	OE Output Enable	13

List of Tables

<i>Table 1 · Pin Descriptions</i>	6
<i>Table 2 · Absolute Maximum Ratings*</i>	14
<i>Table 3 · Recommended Operating Conditions*</i>	14
<i>Table 4 · Current consumption</i>	14
<i>Table 6 · Crystal Oscillator Characteristics*</i>	15
<i>Table 7 · LVCMOS Output Characteristics*</i>	16
<i>Table 8 · LVCMOS Output Additive Jitter and Phase Noise*</i>	17
<i>Table 9 · LVCMOS Output Jitter Phase Noise with XTAL*</i>	18
<i>Table 10 · 5x5mm QFN Package Thermal Properties</i>	18

Pin Diagram

The device is packaged in a 5x5mm 32-pin QFN.

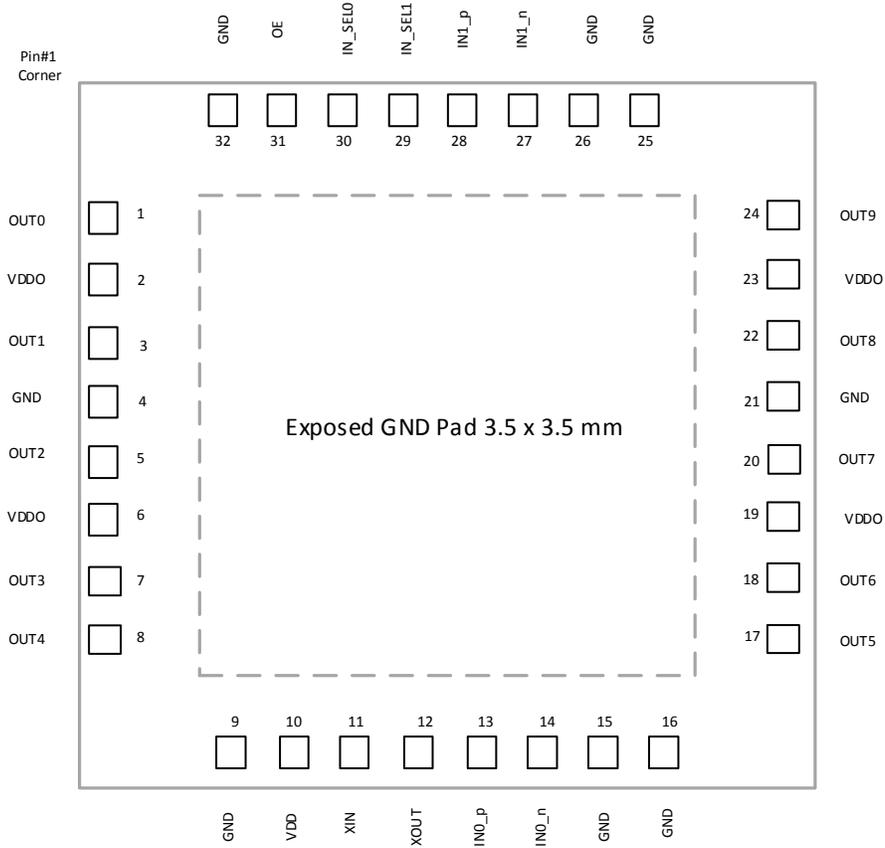


Figure 2. Pin Diagram

Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 300kΩ internal pull-up resistor, I_{PD} – input with 300kΩ internal pull-down resistor, I_{APU} – input with 31kΩ internal pull-up resistor, I_{APD} – input with 31kΩ internal pull-down resistor, I_{APU/APD} – input with 31kΩ internal pull-up and pull-down resistors, O – output, I/O – Input/Output pin, P – power supply pin.

Table 1 - Pin Descriptions

#	Name	I/O	Description															
Input Reference																		
13 14 28 27	IN0_p IN0_n IN1_p IN1_n	I _{APD} I _{APU/APD} I _{APD} I _{APU/APD}	<p>Input Differential or Single Ended References 0 and 1</p> <p>Input frequency range 0Hz to 200MHz.</p> <p>Non inverting inputs (_p) are pulled down with internal 31kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 31kΩ internal resistors to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference)</p>															
Output Clocks																		
1 3 5 7 8 17 18 20 22 24	OUT0 OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7 OUT8 OUT9	O	<p>Ultra Low Additive Jitter LVCMOS Outputs 0 to 9</p> <p>Output frequency range 0 to 200MHz</p>															
Control																		
30 29	IN_SEL0 IN_SEL1	I _{PD}	<p>Input select pins. Logic level on these pins selects which input will be passed to the output.</p> <table border="1"> <thead> <tr> <th>IN_SEL1</th> <th>IN_SEL0</th> <th>OUTN</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Input 0 (IN0)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Input 1 (IN1)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Crystal Oscillator or overdrive</td> </tr> <tr> <td>1</td> <td>1</td> <td>Crystal Bypass</td> </tr> </tbody> </table>	IN_SEL1	IN_SEL0	OUTN	0	0	Input 0 (IN0)	0	1	Input 1 (IN1)	1	0	Crystal Oscillator or overdrive	1	1	Crystal Bypass
IN_SEL1	IN_SEL0	OUTN																
0	0	Input 0 (IN0)																
0	1	Input 1 (IN1)																
1	0	Crystal Oscillator or overdrive																
1	1	Crystal Bypass																

31	OE	I	Output Enable When high outputs are enabled. When low outputs are high-Z.
Crystal Oscillator			
11	XIN	I	Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode
12	XOUT	O	Crystal Oscillator Output
Power and Ground			
10	VDD	P	Positive Supply Voltage. Connect to 3.3V or 2.5V supply.
2 6 19 23	VDDO	P	Positive Supply Voltage for LVCMOS Outputs Connect 3.3V, 2.5V, 1.8V or 1.5V power supply
4 9 15 16 21 25 26 32	GND	P	Ground Connect to the ground
E-Pad	GND	P	Ground. Connect to the ground

Functional Description

The ZL40241 is a pin controlled low additive jitter, low power 3 x 10 LVCMOS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins. .

The ZL40241 has ten LVCMOS outputs which can be powered from 3.3V, 2.5V, 1.8V or 1.5V supply. Output can be synchronously enabled/disabled via OE pin.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40241 inputs.

Figure 3 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each so that the transmission line is terminated with matched impedance (50Ω). However, if the driving strength of the output driver is not sufficient resistor values should be increased

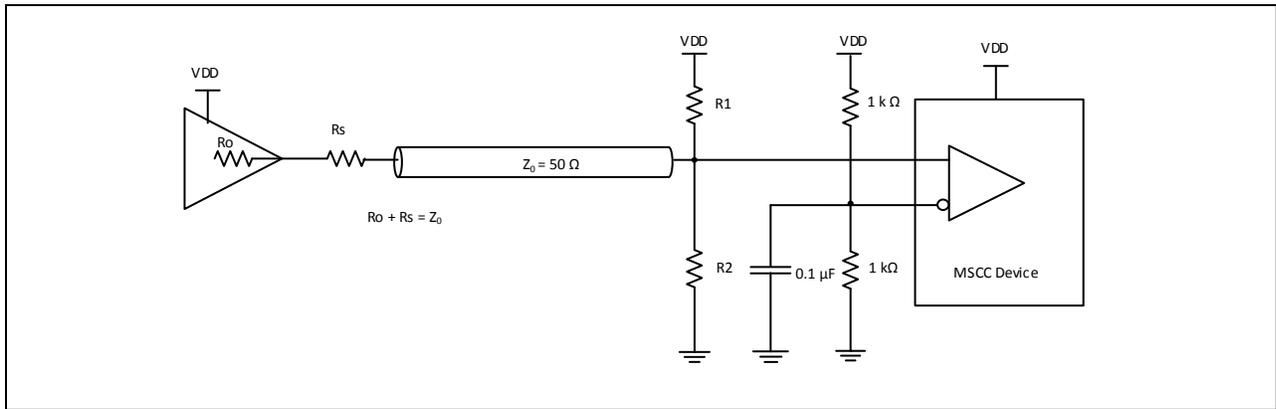


Figure 3. Input driven by a single ended output

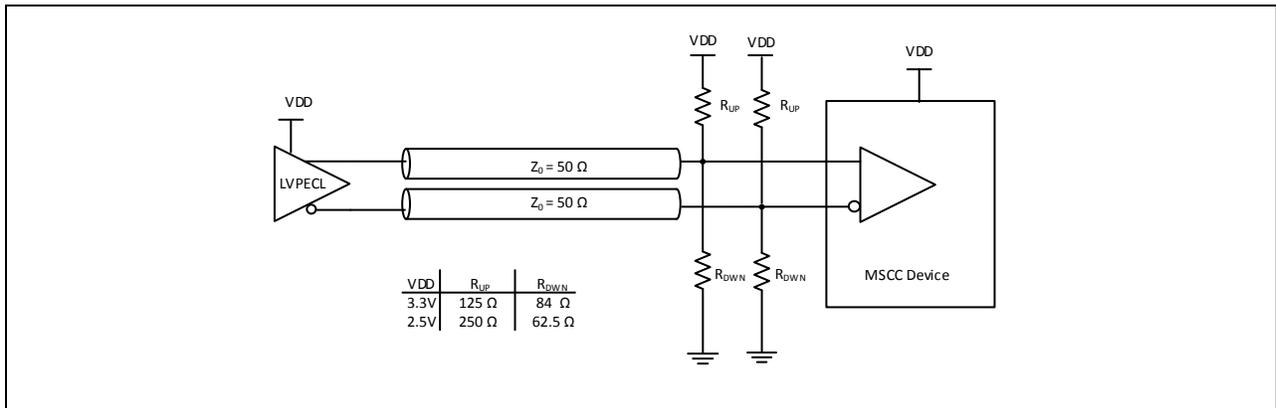


Figure 4. Input driven by DC coupled LVPEVCL output

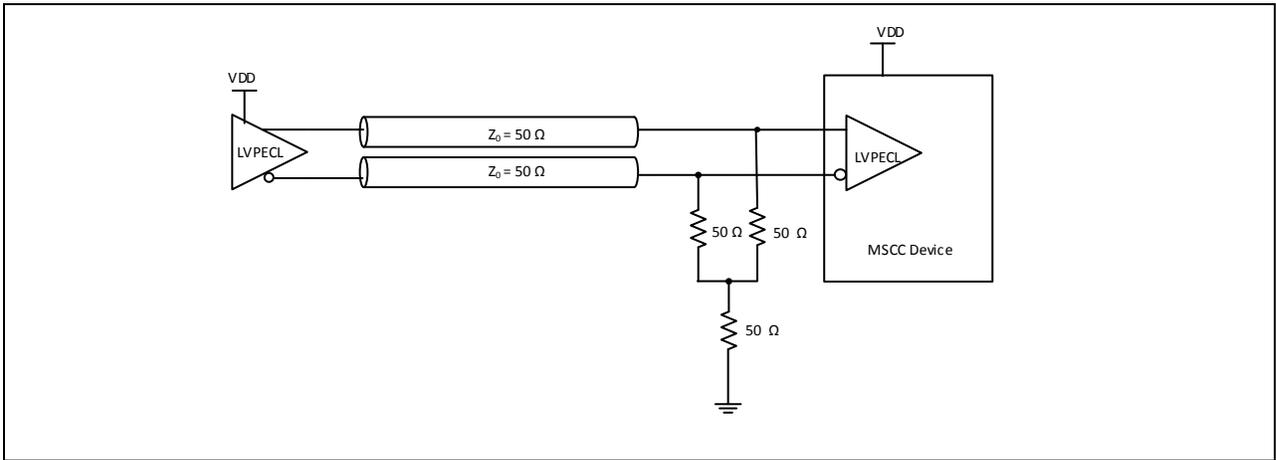


Figure 5. Input driven by DC coupled LVPEVCL output (alternative termination)

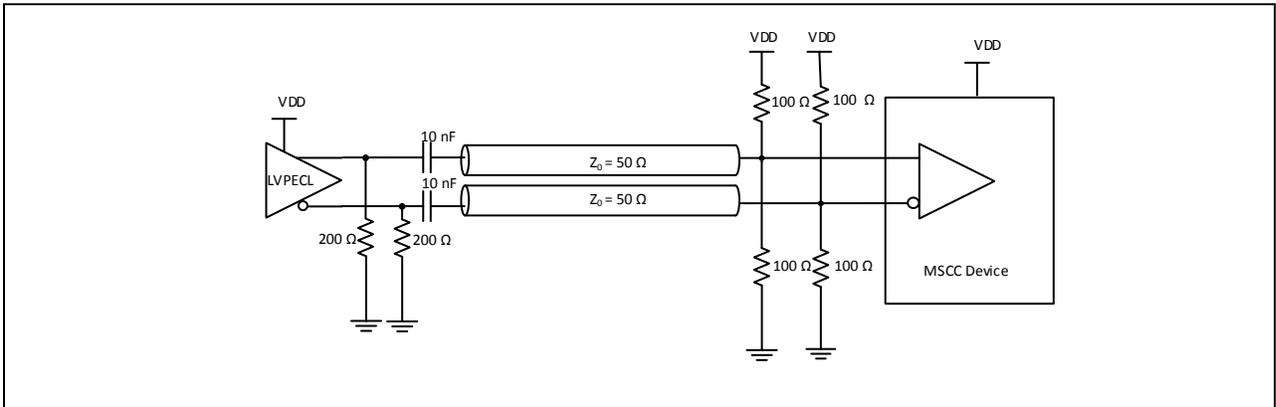


Figure 6. Input driven by AC coupled LVPECL output

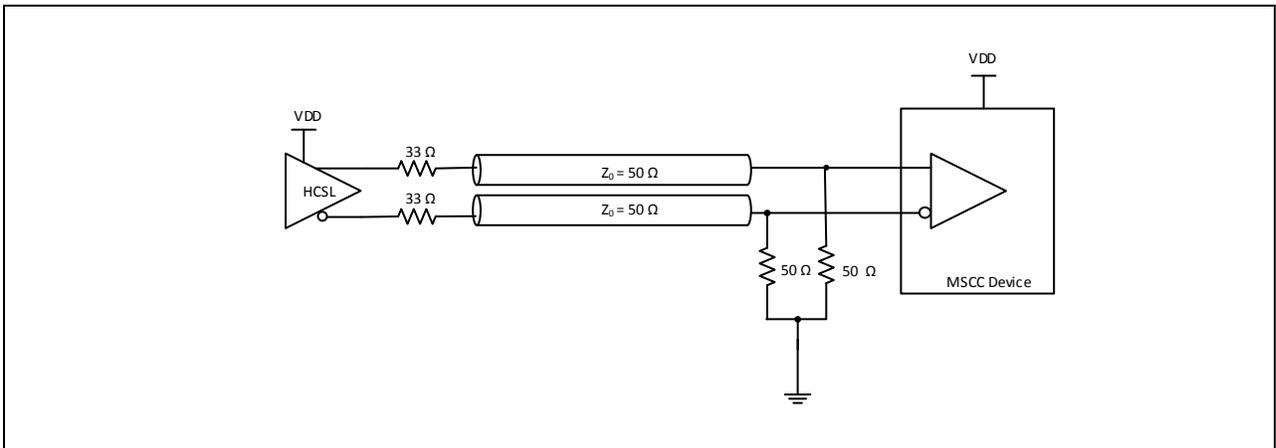


Figure 7. Input driven by HCSL output

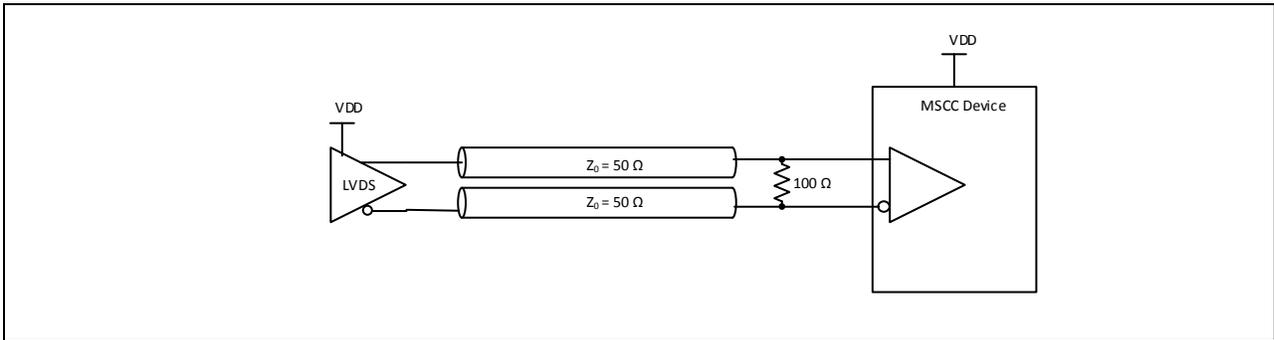


Figure 8. Input driven by LVDS output

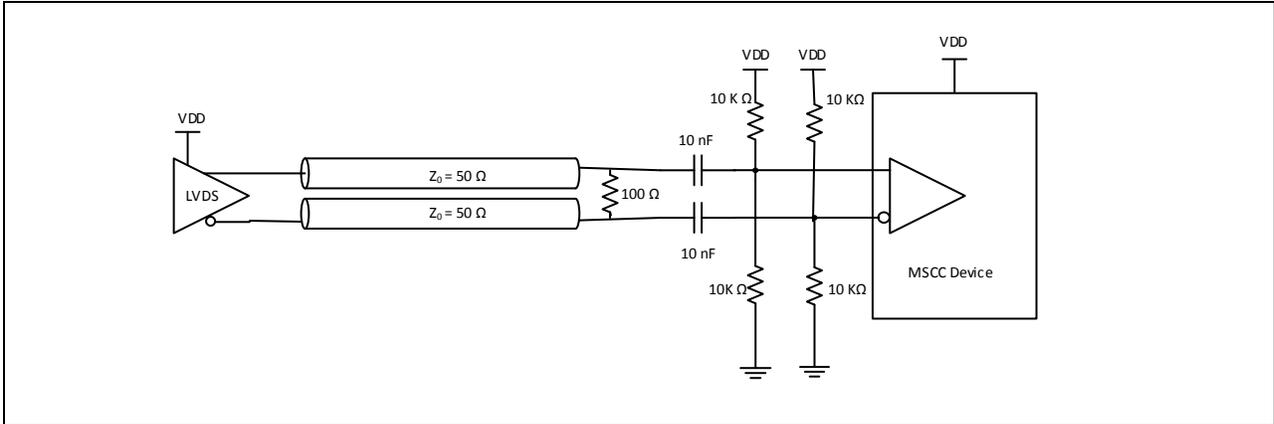


Figure 9. Input driven by AC coupled LVDS

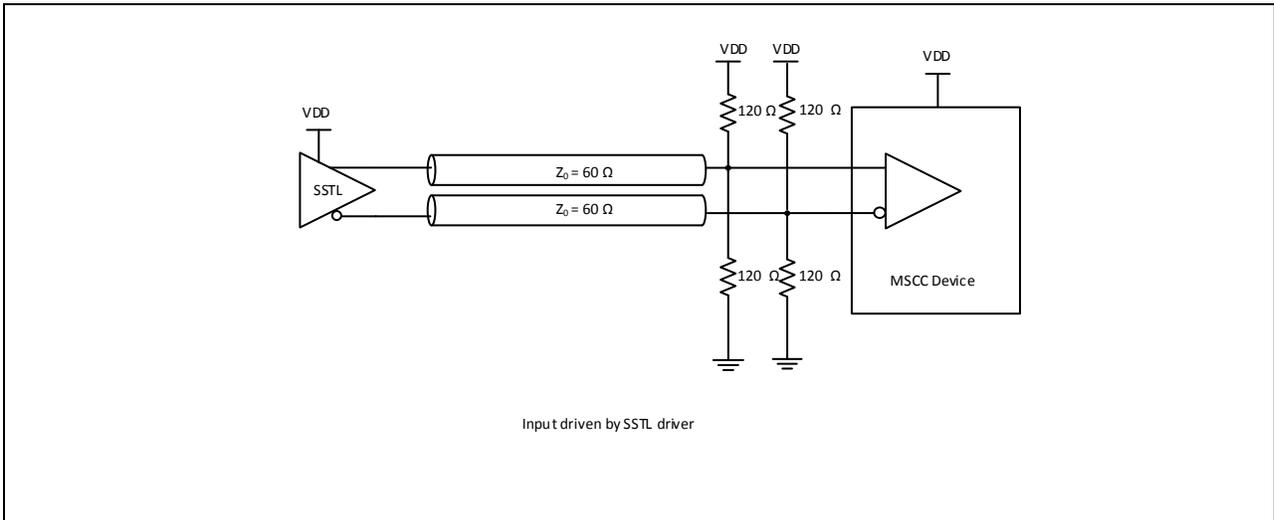


Figure 10. Input driven by an SSTL output

Clock Outputs

LVC MOS outputs require only series termination resistor whose value is depending on LVC MOS output voltage as shown in Figure 11.

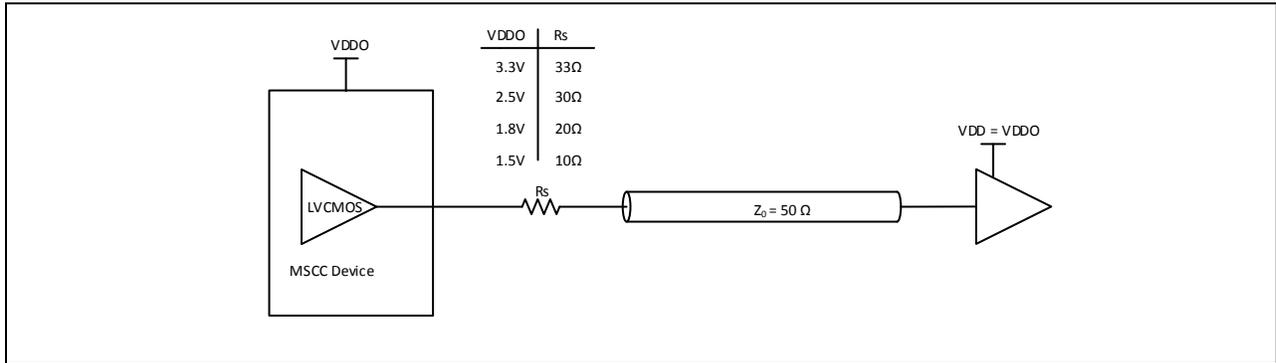


Figure 11. Termination for 3.3V LVPECL outputs

Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8MHz to 60MHz. Load capacitors C1 and C2 shall be selected as per crystal vendor recommendation. Shunt resistor is implemented inside the device.

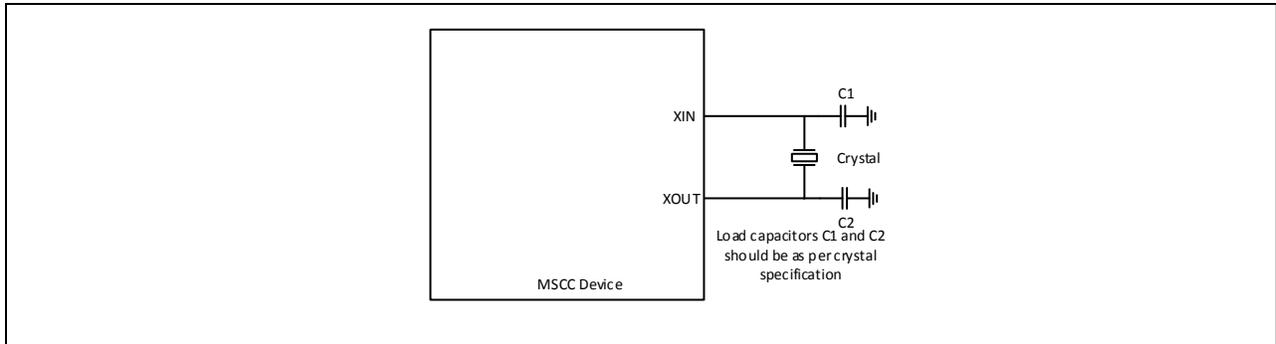


Figure 12. Crystal Oscillator Circuit

The phase noise plot for 25MHz crystal is shown in Figure 13. The phase noise floor of the device is below -170dBc/Hz as can be seen on the figure.

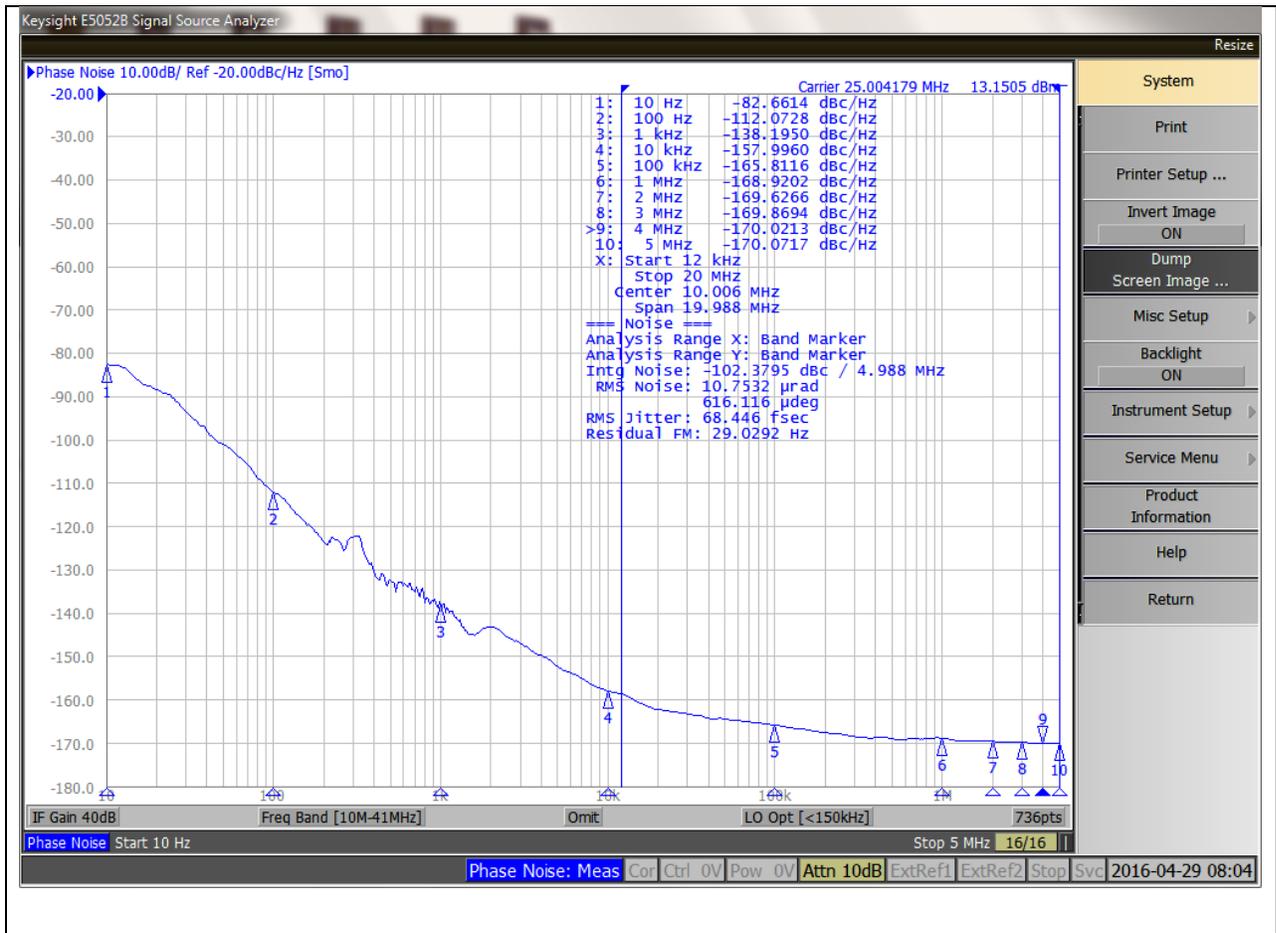


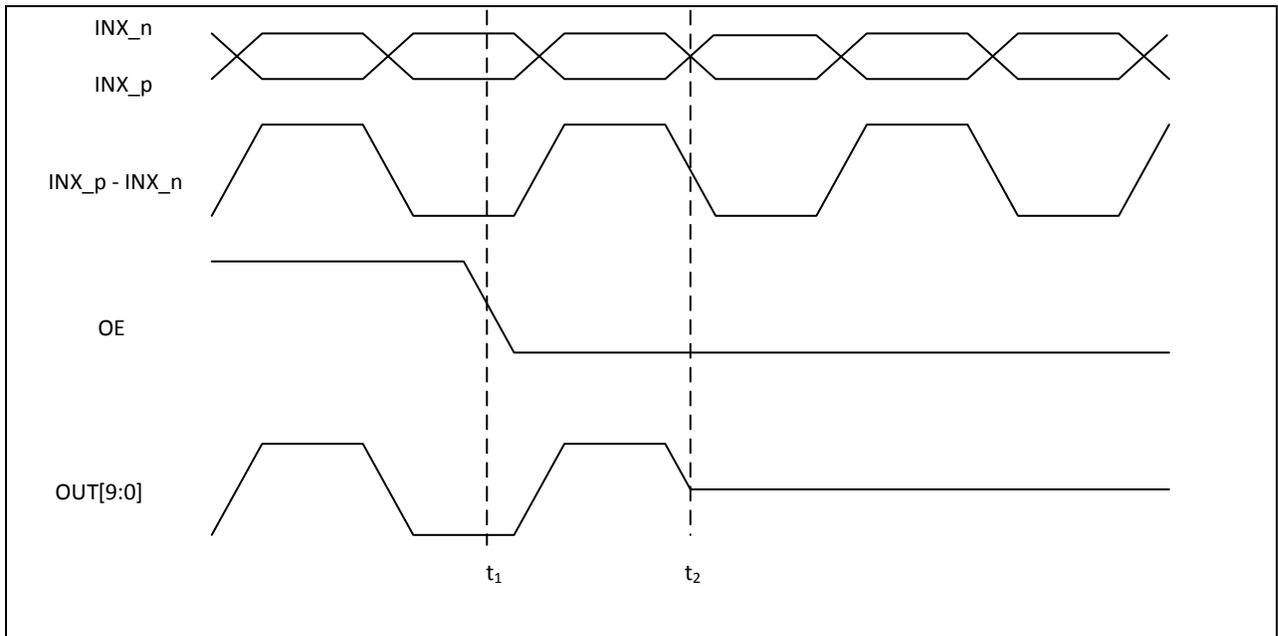
Figure 13. Phase Noise Plot with 25MHz Crystal

Termination of unused inputs and outputs

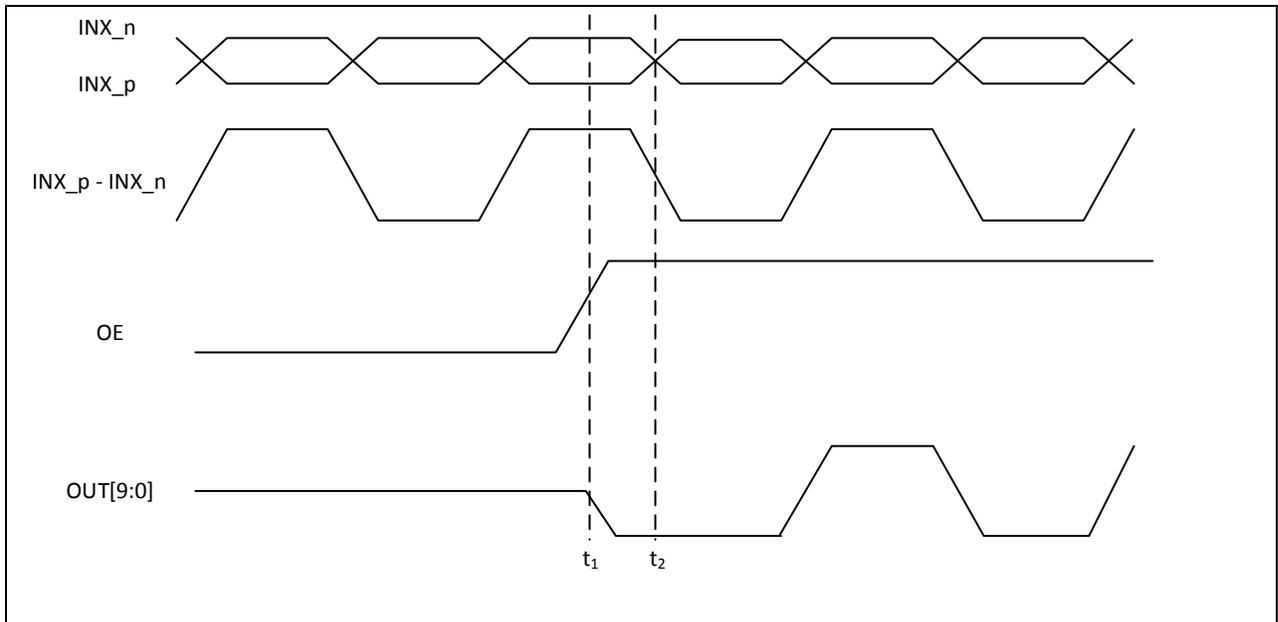
Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by 1k Ω resistor. Unused outputs should be left unconnected.

Device Control

ZL40241 is controlled via Output Enable (OE) and Input Select (SEL0/1) input pins. Output is disabled synchronously on the falling edge of the input (t_2) as shown in Figure 14.


Figure 14. OE Output Disable

Outputs can be enabled by toggling OE pin high. As soon as OE pin goes high (t_1) the outputs will go from high-Z to low and will start to track the input after the first falling edge (t_2) of the input signal as shown in Figure 15.


Figure 15. OE Output Enable

AC and DC Electrical Characteristics

Absolute Maximum Ratings

Table 2 - Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage (3.3V)	V_{DD}/V_{DDO}	-0.5		4.6	V	
2	Supply voltage (2.5V)	V_{DD}/V_{DDO}	-0.5		4.6	V	
3	Supply voltage (1.8V)	V_{DDO}	-0.5		2.5	V	
4	Supply voltage (1.5V)	V_{DDO}	-0.5		2.0	V	
5	Storage temperature	T_{ST}	-55		125	°C	

- * Exceeding these values may cause permanent damage
- * Functional operation under these conditions is not implied
- * Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions

Table 3 - Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V_{DD}/V_{DDO}	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	V_{DD}/V_{DDO}	2.375	2.50	2.625	V	
3	Supply voltage 1.8V	V_{DDO}	1.6	1.8V	2	V	
4	Supply voltage 1.5V	V_{DDO}	1.35	1.5	1.65		
5	Operating temperature	T_A	-40	25	85	°C	
6	Input voltage	V_{DD-IN}	-0.3		$V_{DD} + 0.3$	V	

- * Voltages are with respect to ground (GND) unless otherwise stated
- * The device supports two power supply modes (3.3V and 2.5V)

Table 4 - Current consumption

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Static device current	$I_{s_3.3V}$		14	TBD	mA	VDD= 3.465V
		$I_{s_2.5V}$		8	TBD	mA	VDD = 2.625V
2	Device current with XTAL input	$I_{DD_XTAL_3.3V}$		20	TBD	mA	VDD= 3.465V
		$I_{DD_XTAL_2.5V}$		12	TBD	mA	VDD= 2.625V
3	Dynamic current per output (f = 100MHz) ⁽¹⁾⁽²⁾ Needs to be scaled for different frequencies by f/100MHz	$I_{DD_3.3V}$			TBD	mA	VDDO= 3.465V
		$I_{DD_2.5V}$			TBD	mA	VDDO= 2.625V
		$I_{DD_1.8V}$			TBD	mA	VDDO= 2V
		$I_{DD_1.5V}$			TBD	mA	VDDO= 1.65V

- (1) Needs to be scaled for different frequencies by f/100MHz
- (2) To calculate total current consumption use following formula: $I = I_s + I_{DD_XTAL} + I_{DD} * n * f/100MHz + VDDO * C_{LOAD} * f * n$, where
 I_{DD_XTAL} : should be set to zero if XTAL is not used
 n: number of active outputs
 f: frequency of the clock
 C_{LOAD} : is capacitive load driven by an output.

Table 5 - Input Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage for SEL0/1 and OE	V_{CIH}	0.45			V	
2	CMOS low-level input voltage for SEL0/1 and OE	V_{CIL}			1.05	V	
3	CMOS input leakage current for SEL0/1 and OE	I_{IL}	-10		10	μA	$V_i = V_{DD}$ or 0 V
4	Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	0.5		$V_{DD} - 0.85$	V	
5	Differential input voltage difference for IN0_p/n and IN1_p/n	V_{ID}	0.15		1.3	V	
6	Differential input leakage current for IN0_p/n and IN1_p/n	I_{IL}	-10		10	μA	$V_i = V_{DD}$ or 0 V
7	Single ended input high voltage for IN_0_p and IN_1_p	V_{SIH}	2		$V_{DD} + 0.3V$	V	$V_{DD} = 3.3V$
		V_{SIH}	1.6		$V_{DD} + 0.3V$	V	$V_{DD} = 2.5V$
8	Single ended input high voltage for IN_0_p and IN_1_p	V_{SIL}	-0.3		1.3	V	$V_{DD} = 3.3V$
		V_{SIL}	-0.3		0.9	V	$V_{DD} = 2.5V$
9	Input frequency	f_{IN}	0		200	MHz	
10	Input duty cycle	dc	30%		70%		
11	Input slew rate	slew		2		V/ns	
12	Input pull-up/ pull-down resistance	R_{PU}/R_{PD}		31k Ω			

* Values are over Recommended Operating Conditions

* Values are over all two power supply modes ($V_{DD} = 3.3V$ and $V_{DD} = 2.5V$)

Table 6 - Crystal Oscillator Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Mode of oscillation	mode	Fundamental				
2	Frequency	f	8		60	MHz	
3	On chip shunt resistor	R		0.5		M Ω	
4	On chip capacitance	C		12		pF	
5	Frequency in overdrive mode ⁽¹⁾	f_{OV}	0.1		200	MHz	Functional but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1 μF assumed)
6	Frequency in bypass mode ⁽²⁾	f_{BP}			200	MHz	Functional but may not meet AC parameters

* Values are over Recommended Operating Conditions

* Values are over all two power supply modes ($V_{DD} = 3.3V$ and $V_{DD} = 2.5V$)

(1) Maximum input level is 2V

(2) Maximum output level is VDD

Table 7 - LVCMOS Output Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	V_{OH}	$0.8 \cdot V_{DDO}$			V	$V_{DDO} = 3.3V \pm 5\%$
		V_{OH}	$0.8 \cdot V_{DDO}$			V	$V_{DDO} = 2.5V \pm 5\%$
		V_{OH}	$0.7 \cdot V_{DDO}$			V	$V_{DDO} = 1.8V \pm 10\%$
		V_{OH}	$0.7 \cdot V_{DDO}$			V	$V_{DDO} = 1.5V \pm 10\%$
2	Output low voltage	V_{OL}			$0.2 \cdot V_{DDO}$	V	$V_{DDO} = 3.3V \pm 5\%$
		V_{OL}			$0.2 \cdot V_{DDO}$	V	$V_{DDO} = 2.5V \pm 5\%$
		V_{OL}			$0.3 \cdot V_{DDO}$	V	$V_{DDO} = 1.8V \pm 10\%$
		V_{OL}			$0.3 \cdot V_{DDO}$	V	$V_{DDO} = 1.5V \pm 10\%$
3	Output impedance	R_o		15		Ω	$V_{DDO} = 3.3V$
		R_o		20		Ω	$V_{DDO} = 2.5V$
		R_o		25		Ω	$V_{DDO} = 1.8V$
		R_o		30		Ω	$V_{DDO} = 1.5V$
4	Output slew rate-- rise or fall (20% to 80%)	t_r, t_f	TBD	7.3	TBD	V/ns	$V_{DDO} = 3.3V \pm 5\%$
		t_r, t_f	TBD	4.8	TBD	V/ns	$V_{DDO} = 2.5V \pm 5\%$
		t_r, t_f	TBD	2.1	TBD	V/ns	$V_{DDO} = 1.8V \pm 10\%$
		t_r, t_f	TBD	1.1	TBD	V/ns	$V_{DDO} = 1.5V \pm 10\%$
5	Output frequency	F_o	0		200	MHz	
6	Output to output skew	t_{OOSK}		30	TBD	ps	
7	Device to device output skew	t_{DOOSK}			TBD	ns	
8	Input to output delay	t_{IOD}		1.9		ns	$V_{DD} = 3.3V$
		t_{IOD}		2.4		ns	$V_{DD} = 2.5V$
9	Input multiplexer isolation	iso	55			dB	125MHz

* Values are over Recommended Operating Conditions

* Values are over all two power supply modes ($V_{DD} = 3.3V$ and $V_{DD} = 2.5V$)

* Load 50 Ohm to $V_{DDO}/2$

Table 8 - LVCMOS Output Additive Jitter and Phase Noise*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	System level additive jitter ⁽¹⁾		25		fs-RMS	VDD = 3.3V, VDDO = 3.3V f _{in} = 125MHz, single ended input
			30		fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V f _{in} = 125MHz, single ended input
			30		fs-RMS	VDD = 3.3V, VDDO = 3.3V f _{in} = 125MHz, differential input
			30		fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V f _{in} = 125MHz, differential input
2	Additive jitter ⁽²⁾		25		fs-RMS	VDD = 3.3V, VDDO = 3.3V f _{in} = 125MHz, single ended input
			30		fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V f _{in} = 125MHz, single ended input
			30		fs-RMS	VDD = 3.3V, VDDO = 3.3V f _{in} = 125MHz, differential input
			30		fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V f _{in} = 125MHz, differential input
3	Phase Noise floor		-145		dBc/Hz	@10kHz f _{in} = 125MHz, single ended input
			-156		dBc/Hz	@100kHz f _{in} = 125MHz, single ended input
			-163		dBc/Hz	@1MHz f _{in} = 125MHz, single ended input
			-163		dBc/Hz	@10MHz f _{in} = 125MHz, single ended input
			-163		dBc/Hz	@20MHz f _{in} = 125MHz, single ended input
			-145		dBc/Hz	@10kHz f _{in} = 125MHz, differential input
			-155		dBc/Hz	@100kHz f _{in} = 125MHz, differential input
			-160		dBc/Hz	@1MHz f _{in} = 125MHz, differential input
			-161		dBc/Hz	@10MHz f _{in} = 125MHz, differential input
	-162		dBc/Hz	@20MHz f _{in} = 125MHz, differential input		

* Values are over Recommended Operating Conditions

* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)

(1) System level additive jitter is calculated as $J_{RMS_SYS_AJ} = \sqrt{J_{RMS_OUT}^2 - J_{RMS_IN}^2}$

(2) Additive jitter is calculated as $J_{RMS_AJ} = \sqrt{J_{RMS_OUT}^2 - J_{RMS_IN}^2}$

Table 9 - LVCMOS Output Jitter Phase Noise with XTAL*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		80		fs	VDD = 3.3V, VDDO = 3.3V
			115		fs	VDD = 2.5V; VDDO = 2.5V
2	Phase Noise floor		-90		dBc/Hz	@10Hz, VDD = 3.3V, VDDO = 3.3V
			-117		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-138		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-160		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-168		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			--168		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-168		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-90		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-117		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-138		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-160		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-168		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			--168		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-168		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V

* Values are over Recommended Operating Conditions

* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)

* Xtal frequency is 25 MHz

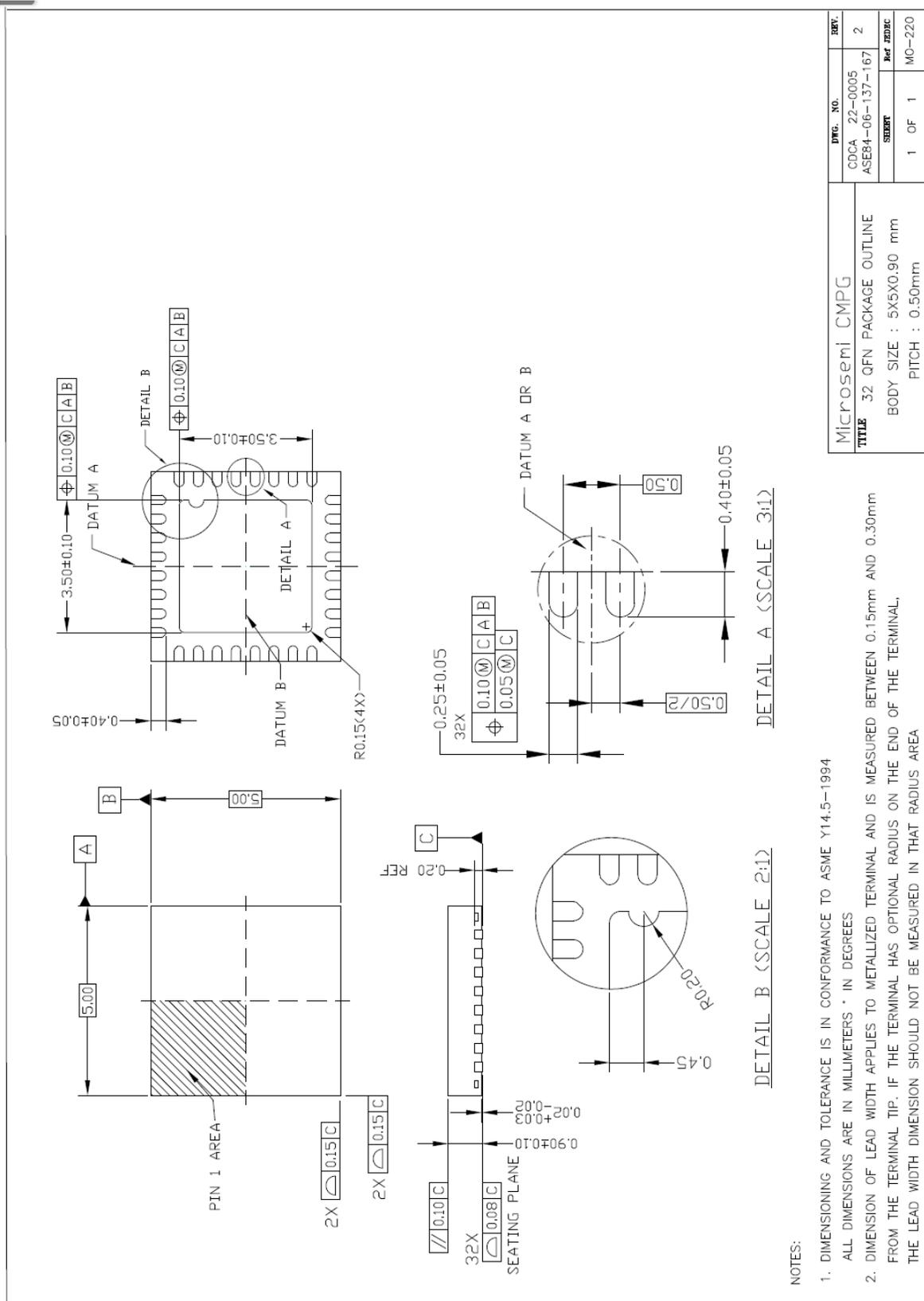
Table 10 - 5x5mm QFN Package Thermal Properties

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T _A		85	°C
Maximum Junction Temperature	T _{JMAX}		125	°C
Junction to Ambient Thermal Resistance ⁽¹⁾ (Note 1)	θ _{JA}	still air	26.8	°C/W
		1m/s airflow	21.8	
		2.5m/s airflow	19.9	
Junction to Board Thermal Resistance	θ _{JB}		10.8	°C/W
Junction to Case Thermal Resistance	θ _{JC}		19.5	°C/W
Junction to Pad Thermal Resistance ⁽²⁾	θ _{JP}	Still air	6.5	°C/W
Junction to Top-Center Thermal Characterization Parameter	ψ _{JT}	Still air	0.6	°C/W

(1) Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power

(2) Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

Package Outline



Microsemi CMPG		DWG. NO.	REV.
TITLE 32 QFN PACKAGE OUTLINE		CDCA 22-0005	2
BODY SIZE : 5X5X0.90 mm		ASEB4-06-137-167	Ref JESD8C
PITCH : 0.50mm		SEBPT	Ref JESD8C
		1 OF 1	MO-220

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
ALL DIMENSIONS ARE IN MILLIMETERS * IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA



Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

© 2016 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,400 employees globally. Learn more at www.microsemi.com.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.