Low Skew, Low Additive Jitter 2 x10 LVPECL Fanout Buffer

Features

- Two inputs accept any differential (LVPECL, HCSL, LVDS, SSTL, CML) or single ended LVCMOS signal
- Ten 2.5V/3.3V LVPECL outputs
- Ultra-low additive jitter: 30fs (12KHz to 20MHz)
- Supports clock frequencies from 0 to 1.6GHz
- Supports 2.5V or 3.3V power supplies
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 50ps
- Maximum input to output delay of 645ps

Ordering Information

ZL40260LDG1	32 Pin QFN	Trays
ZL40260LDF1	32 pin QFN	Tape and Reel
ZL40260QGG1	32 pin eTQFP	Trays
ZL40260QGF1	32 pin eTQFP	Tape and Reel

Package size: 5 x 5 mm QFN and 7 x 7 mm eTQFP
-40°C to +85°C

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3 clock distribution
- Wireless communications
- High performance microprocessor clock distribution
- Test equipment

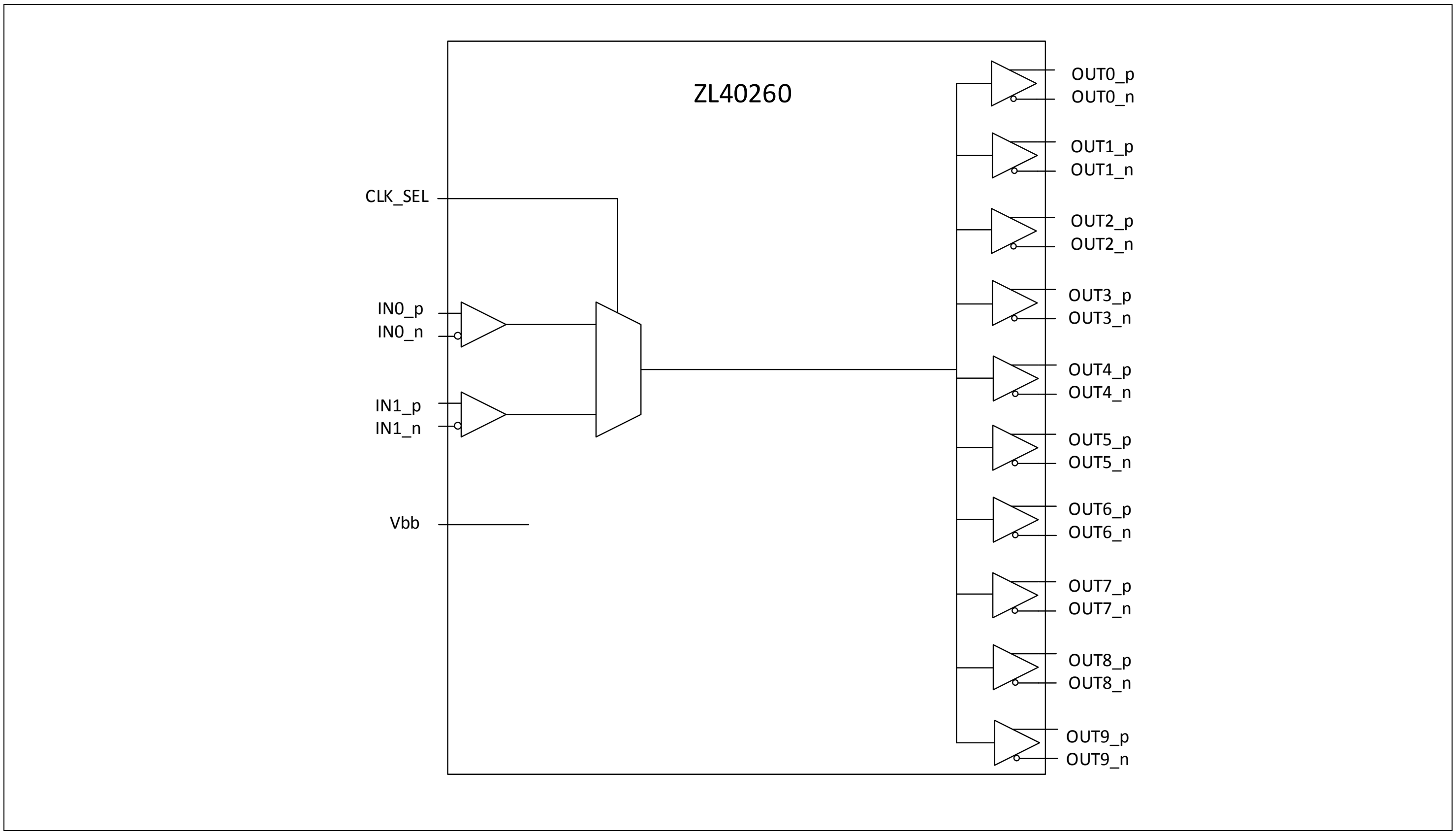

Figure 1. Functional Block Diagram

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Pin Diagram

The device is packaged in a 5x5mm 32-pin QFN and 7x7mm 32-pin eTQFP.

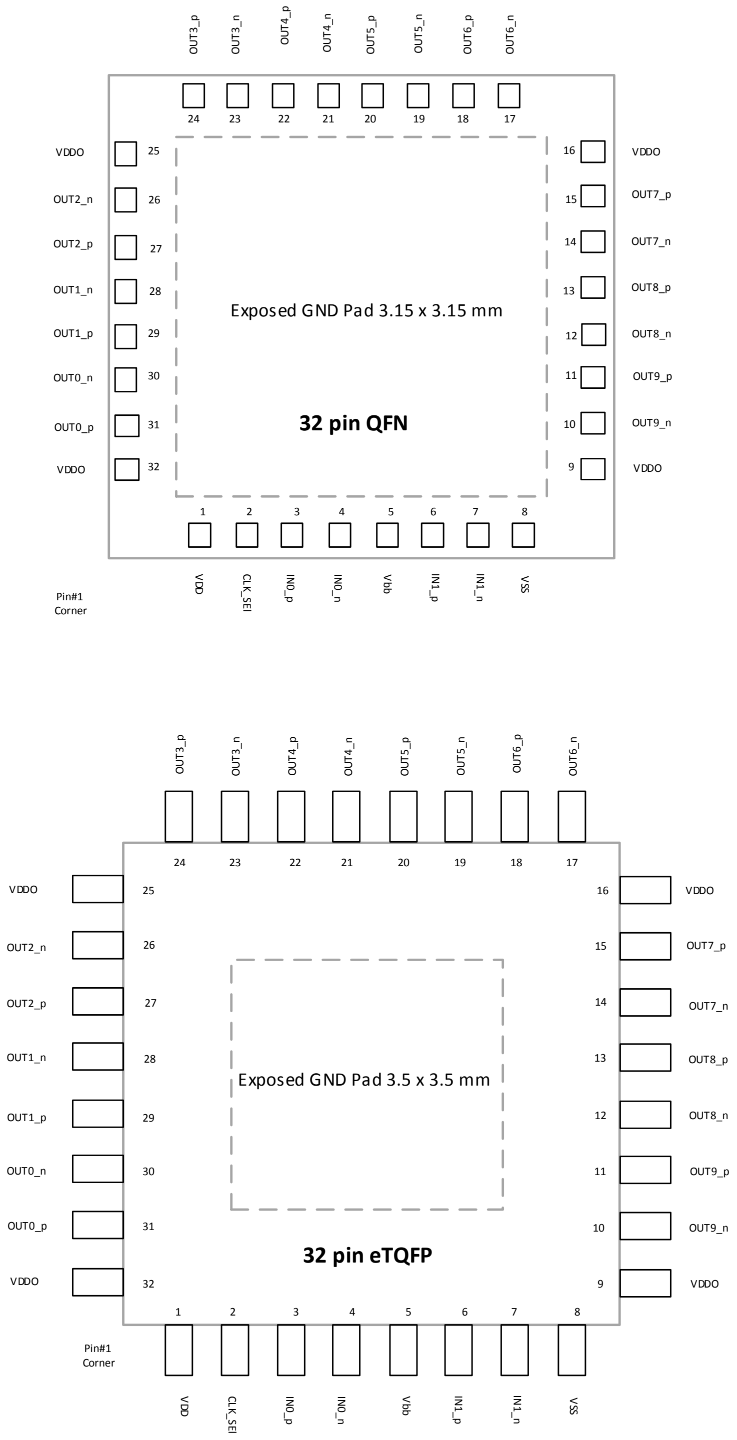


Figure 2. Pin Diagram (not to scale)

Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 31kΩ internal pull-up resistor, I_{PD} – input with 30kΩ internal pull-down resistor, $I_{PU/PD}$ – input biased to VDD/2 with 60kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, P – power supply pin.

Table 1 Pin Descriptions

#	Name	I/O	Description
Input Reference			
3 4 6 7	IN0_p IN0_n IN1_p IN1_n	I_{PD} $I_{PU/PD}$ I_{PD} $I_{PU/PD}$	**Differential/Single Ended References 0 and 1** Input frequency range 0Hz to 1.6GHz. Non inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60kΩ internal resistors (30kΩ equivalent) to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).
Output Clocks			
31 30 29 28 27 26 24 23 22 21 20 19 18 17 15 14 13 12 11 10	OUT0_p OUT0_n OUT1_p OUT1_n OUT2_p OUT2_n OUT3_p OUT3_n OUT4_p OUT4_n OUT5_p OUT5_n OUT6_p OUT6_n OUT7_p OUT7_n OUT8_p OUT8_n OUT9_p OUT9_n	O	**Ultra Low Additive Jitter Differential LVPECL Outputs 0 to 9** Output frequency range 0 to 1.6GHz
Control			
2	CLK_SEL	I_{PD}	**Clock select input.** Logic level at this pin selects one of input references. When low selects IN0_p/IN0_n. When high selects IN1_p/IN1_n Accepts LVPECL and LVCMOS logic levels. This pin is pulled down with 31kΩ resistor.

Input Biasing			
5	Vbb	O	**Bias Output Voltage** Provides power output to bias IN0_n and/or IN1_n when input are fed by a single ended LVPECL inputs or if differential inputs signal is AC coupled (see application section).
Power and Ground			
1	VDD	P	**Positive Supply Voltage.** Connect to 3.3V or 2.5V supply. VDD does not have to be connected to the same voltage level as VDDO pins.
9 16 25 32	VDDO	P	**Positive Supply Voltage for LVPECL Outputs** Connect 3.3V or 2.5V. VDDO pins do not have to be connected to the same voltage level as VDD pin.
8	VSS	P	**Ground** Connect to the ground
E-Pad	VSS	P	**Ground** Connect to the ground

Functional Description

The ZL40260 is a 2x10 LVPECL clock fan out buffer shown in Figure 1with ten identical output clock drivers capable of operating at frequencies up to 1600MHz.

The ZL40260 has two inputs. Each input can accpet differential (LVPECL, SSTL, LVDS, HSTL, CML) or a single ended LVPECL input or a CMOS input. The voltage level at CLK_SEL pin selects which input will be passed to the output drivers. LVPECL input must be externally biased and terminated with resistors. The device provides biasing voltage at the output pin Vbb which can minimize number of external resistors.

The ZL40260 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40260 inputs. Please note that value of AC coupling capacitors needs to be increased for frequencies below 10MHz to reduce voltage drop. When driven from an AC coupled driver, the input voltage biasing is provided from Vbb output.

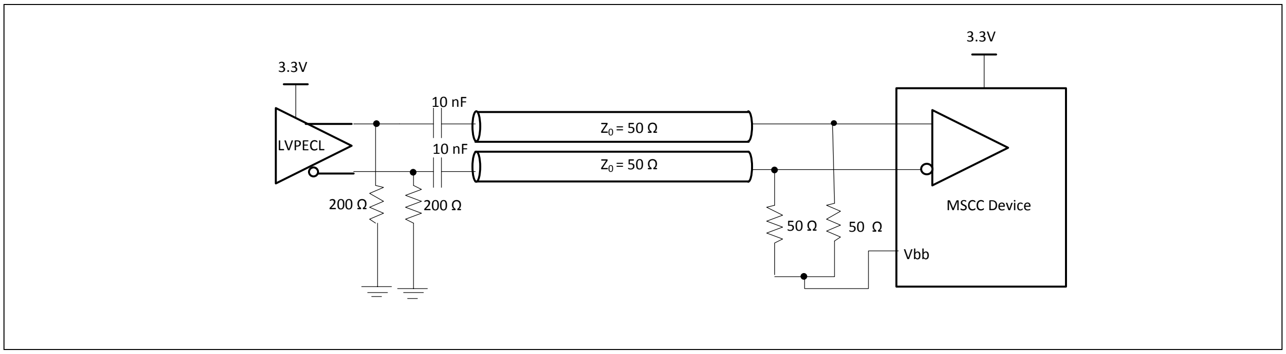
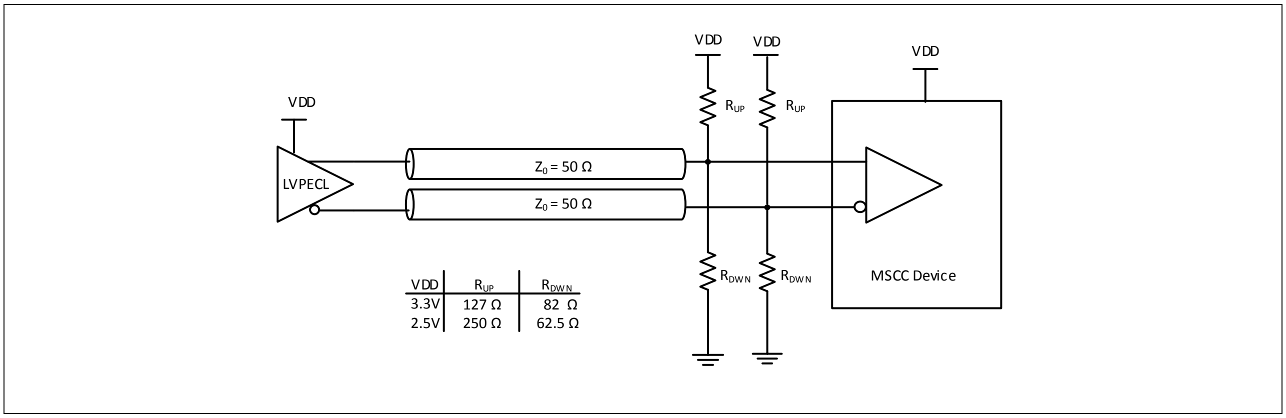


Figure 3. Input driven by a AC coupled LVPECL output



VDD	R_{UP}	R_{DWN}
3.3V	127 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure 4. Input driven by a DC coupled LVPEVCL output

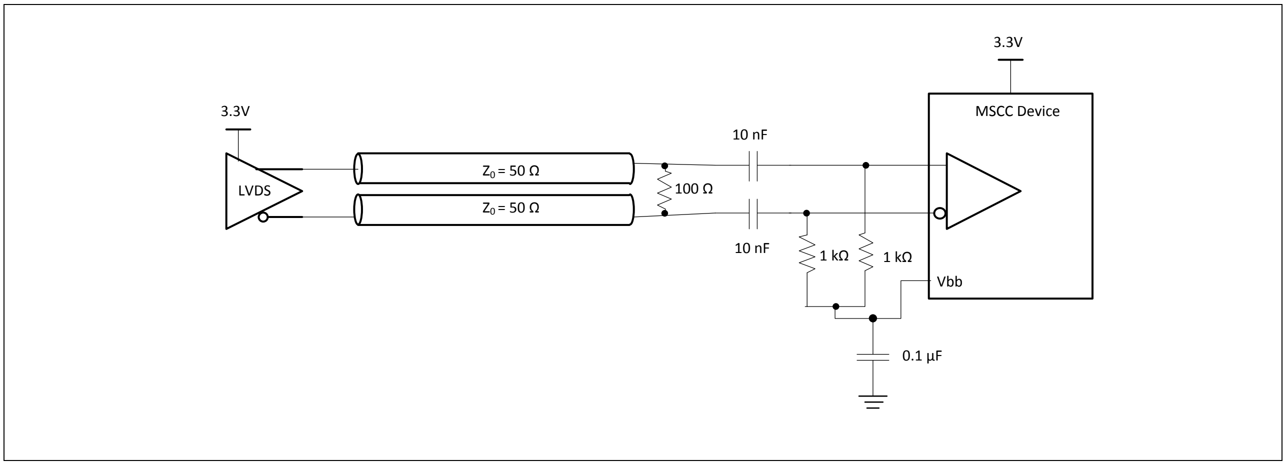


Figure 5. Input driven by AC coupled LVDS output

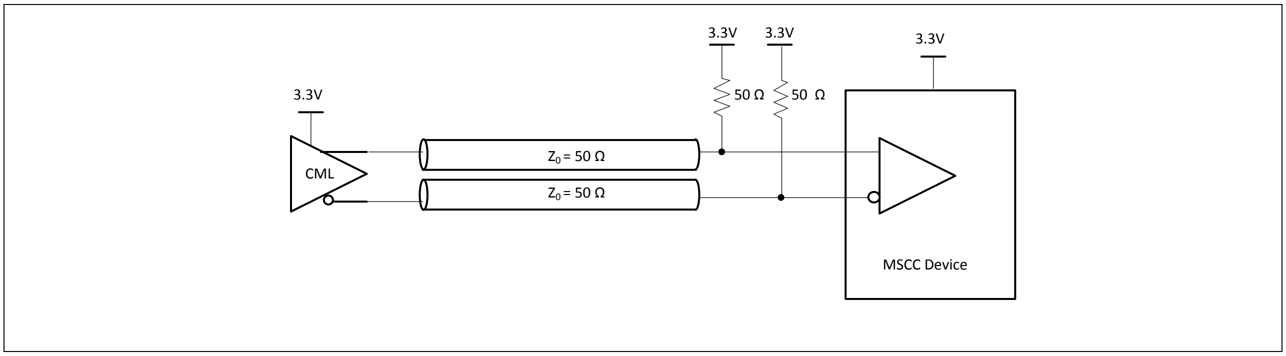


Figure 6. Input driven by 3.3V CML output

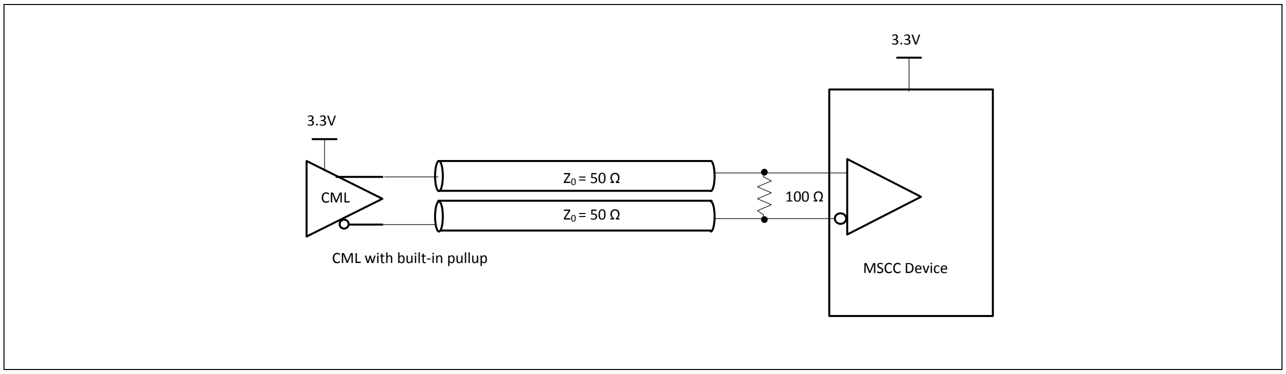


Figure 7. Input driven by 3.3V CML output with internal pull-ups

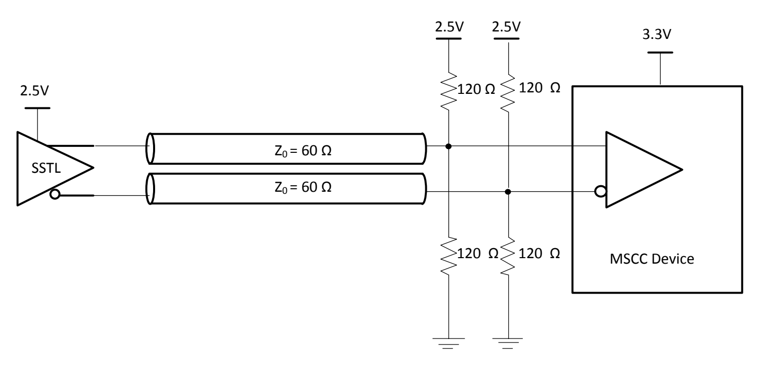


Figure 8. Input driven by SSTL output

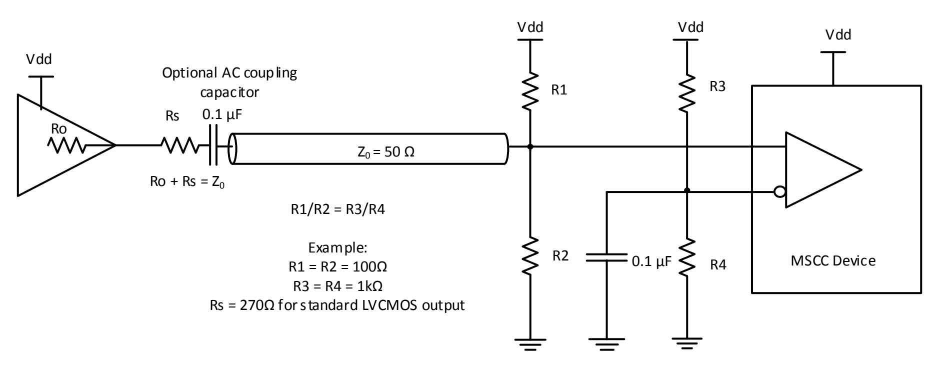


Figure 9. Input driven by single-ended output

Figure 9 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and Ro + Rs should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 4). The source resistors of Rs = 270Ω could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

Clock Outputs

Termination for 3.3V LVPECL outputs is shown in following figures:

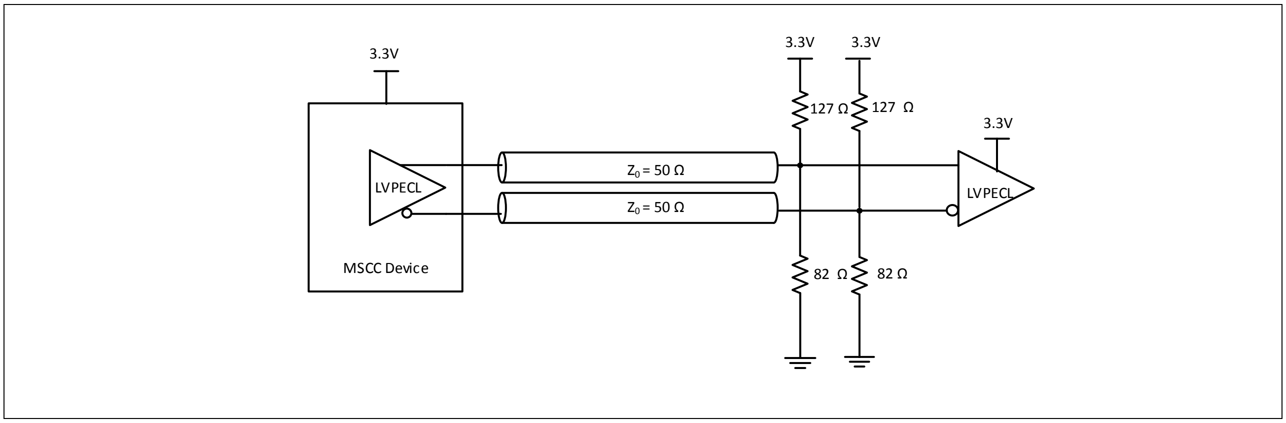


Figure 10. Termination for 3.3V LVPECL outputs

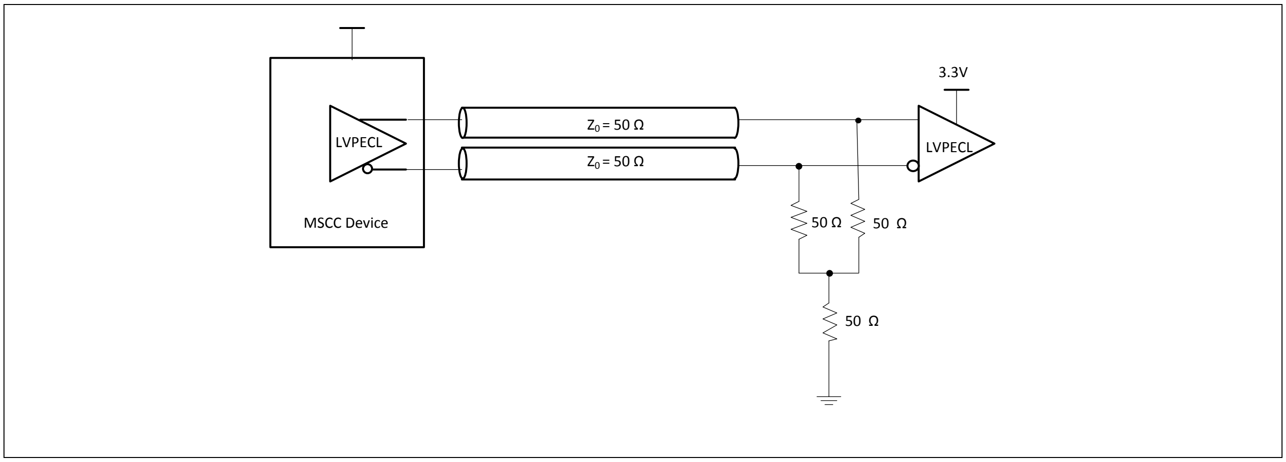


Figure 11. Alternative termination for 3.3V LVPECL outputs

Termination for 2.5V LVPECL outputs is shown in following figures:

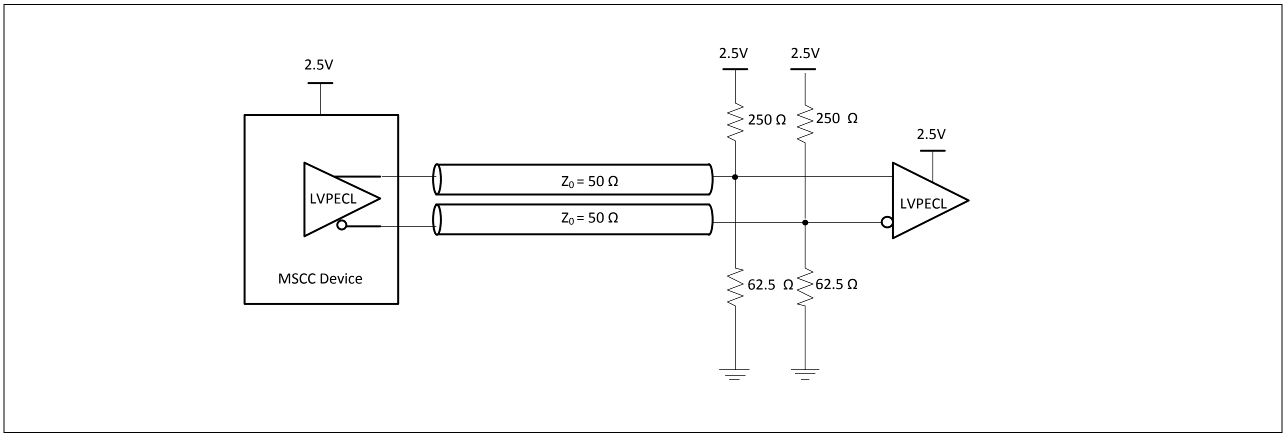


Figure 12. Termination for 2.5V LVPECL output

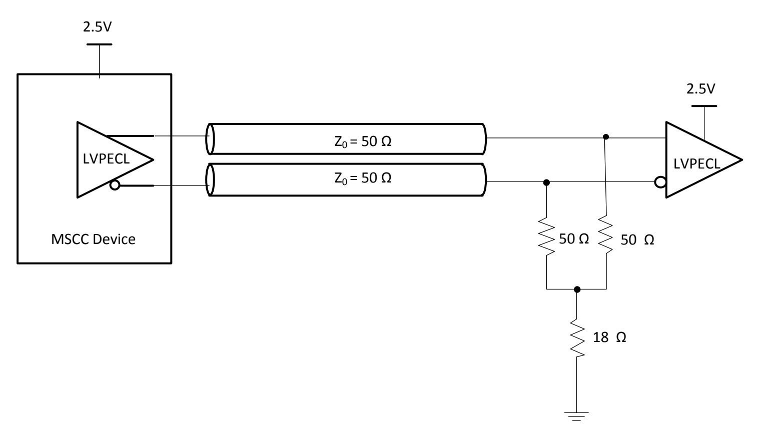


Figure 13. **Alternative termination for 2.5V LVPECL output**

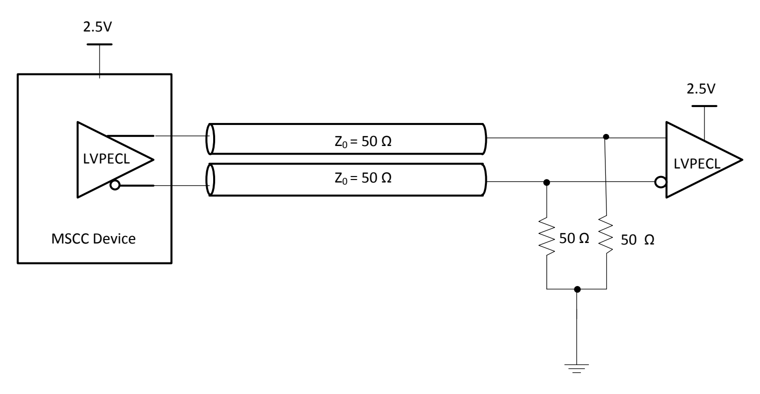


Figure 14. **Alternative termination for 2.5V LVPECL output**

Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by 1KΩ resistor. Unused outputs should be left unconnected.

AC and DC Electrical Characteristics

Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage (3.3V)	V_{DD}	-0.5		4.6	V	
2	Supply voltage (2.5V)	V_{DD}	-0.5		4.6	V	
3	Storage temperature	T_{ST}	-55		125	°C	

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated
*

Recommended Operating Conditions

Table 3 Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V_{DD}/ V_{DDO}	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	V_{DD}/ V_{DDO}	2.375	2.50	2.625	V	
3	Operating temperature	T_A	-40	25	85	°C	
4	Input voltage	V_{IN}	-0.3		V_{DD} + 0.3	V	
5	Core current	I_{CORE}				mA	
6	Power per output	P_{OUT}				mW	

* Voltages are with respect to ground (GND) unless otherwise stated
* The device supports two power supply modes (3.3V and 2.5V)

DC Electrical Characteristics

Table 4 DC Electrical Characteristics vdd_core=vddo=3.3V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
VOH	Output High Voltage; NOTE 1			2.07			2.05			1.98		V
VOL	Output Low Voltage; NOTE 1			1.37			1.35			1.34		V
VIH	Input High Voltage (Single-ended)			1.8<			1.8<			1.8<		V
VIL	Input Low Voltage (Single-ended)			<1.64			<1.64			<1.64		V
VBB	Output Voltage Reference; NOTE 2		1.94		1.98	1.88		1.97	1.81		1.92	V
VPP	Peak-to-Peak Input Voltage NOTE 3		150	800	1300	150	800	1200	150	800	1200	mV
VCMR	Input Common Mode (VCM) NOTE 3, 4		1	1.5	2	1	1.5	2	1	1.5	2	V
IIH	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1		56			56			56		µA
IIL	Input Low Current	PCLK0, PCLK1		36			36			36		µA
		nPCLK0, nPCLK1		20			20			20		µA

NOTE1: Outputs terminated each side with 50Ω to vddo – 2V and in parallel with a 1pF cap
NOTE 2: Single-ended input operation is limited. Vdd_core ≥3.3V in LVPECL mode.
NOTE 3: VCM = {1V .. 2V} for vdd_core = 3.3V +-5%
NOTE 4: VCM = {1V .. 1.5V} for vdd_core = 2.5V +-5%

Table 5 LVPECL DC characteristics; vdd_core=vddo=2.5V

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
VOH	Output High Voltage; NOTE 1		1.27			1.25			1.18		V
VOL	Output Low Voltage; NOTE 1		0.57			0.55			0.54		V
VIH	Input High Voltage (Single-ended)		1.05<			1.05<			1.05<		V
VIL	Input Low Voltage (Single-ended)		<0.8			<0.8			<0.8		V
VBB	Output Voltage Reference at 500uA	1.14		1.2	1.08		1.18	1.01		1.13	V
VPP	Peak-to-Peak Input Voltage; NOTE 2	150	800	1100	150	800	1100	150	800	1100	mV
VCMR	Input Voltage Common Mode	1		1.5	1		1.5	1		1.5	V
I_{IH}	Input High Current		56			56			56		µA
I_{IL}	Input Low Current		56			56			56		µA

NOTE 1: Outputs terminated each side with 50Ω to vddo – 2V and in parallel with a 1pF
NOTE 2: Single-ended input operation is limited. Vdd_core ≥2.5V in LVPECL mode.
NOTE 3: VCM = {1V .. 2V} for vdd_core = 3.3V +-5%
NOTE 4: VCM = {1V .. 1.5V} for vdd_core = 2.5V +-5%

Table 6 AC Electrical Characteristics – 3.3V LVPECL Outputs

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
fOUT	Output Frequency			1.6			1.6			1.6	GHz
tPD	Propagation Delay (from IN0_p/n)	TBD	632	TBD	TBD	785	TBD	TBD	1025	TBD	ps
tsk(o)	Output Skew		TBD	50		TBD	50		TBD	50	ps
tsk(pp)	Part-to-Part Skew			150			150			150	ps
Pn1K	Phase noise at 125MHz; Offset=1KHz **		-142			-138			-135		dBc/Hz
Pn10K	Phase noise at 125MHz; Offset=10KHz**		-152			-149			-145		dBc/Hz
Pn100K	Phase noise at 125MHz; Offset=100KHz**		-161			-158			-155		dBc/Hz
Pn1M	Phase noise at 125MHz; Offset=1MHz**		-165			-165			-162		dBc/Hz
Pn10M	Phase noise at 125MHz; Offset=10MHz**		-166			-166.5			-163		dBc/Hz
Pn20M	Phase noise at 125MHz; Offset=20MHz**		-166			-166.5			-163		dBc/Hz
tjit	Buffer Additive Phase Jitter, RMS Carrier=125MHz		41	TBD		41	TBD		60	TBD	fs 12K-20M
tR / t F	Output Rise/Fall Time (125MHz) 20% to 80% Zero track; CL=1p		60	TBD		80	TBD		125	TBD	ps
Duty-Cycle	Output differential duty cycle		50.17			50.17			50.13		%

NOTE: All parameters are measured at f < 800MHz, unless otherwise noted.

Table 7 AC Electrical Characteristics – 2.5V LVPECL Output

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Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{OUT}	Output Frequency			TBD			TBD			TBD	GHz
t_{PD}	Propagation Delay (from IN0_p/n)		TBD			TBD			TBD		ps
$t_{sk(o)}$	Output Skew			TBD			TBD			TBD	ps
$t_{sk(pp)}$	Part-to-Part Skew			TBD			TBD			TBD	ps
P_{n1K}	Phase noise at 125MHz; Offset=1KHz **		TBD			TBD			TBD		dBc/Hz
P_{n10K}	Phase noise at 125MHz; Offset=10KHz**		TBD			TBD			TBD		dBc/Hz
P_{n100K}	Phase noise at 125MHz; Offset=100KHz**		TBD			TBD			TBD		dBc/Hz
P_{n1M}	Phase noise at 125MHz; Offset=1MHz**		TBD			TBD			TBD		dBc/Hz
P_{n10M}	Phase noise at 125MHz; Offset=10MHz**		TBD			TBD			TBD		dBc/Hz
P_{n20M}	Phase noise at 125MHz; Offset=20MHz**		TBD			TBD			TBD		dBc/Hz
t_{jit}	Buffer Additive Phase Jitter, RMS Carrier=125MHz		TBD			TBD			TBD		fs 12K-20M
t_R / t_F	Output Rise/Fall Time (125MHz) 20% to 80% Zero track; CL=1pF		TBD			TBD			TBD		ps
Duty Cycle	Output differential duty cycle		TBD			TBD			TBD		%

NOTE: All parameters are measured at f < 800MHz, unless otherwise noted.

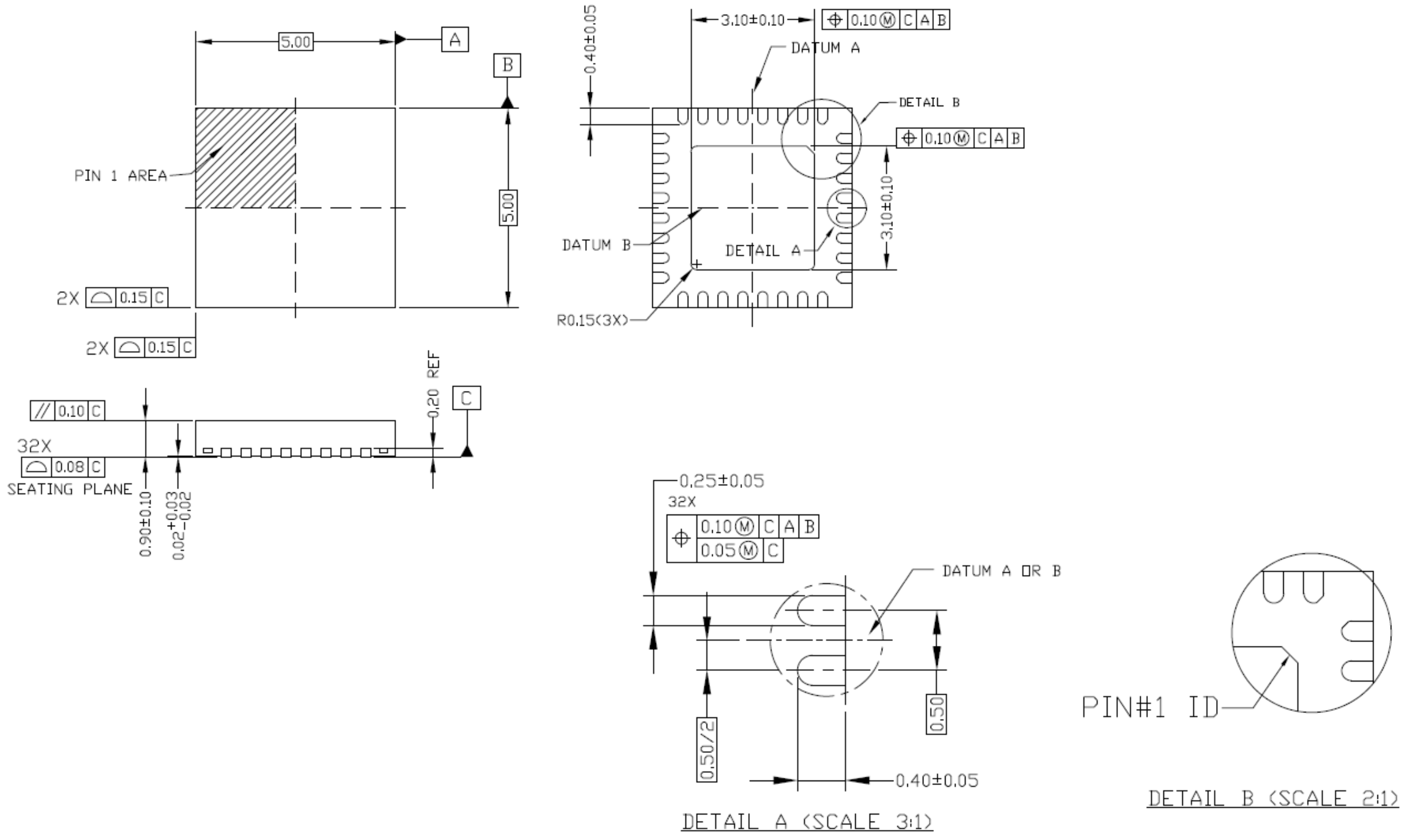
Table 8 5x5mm QFN Package Thermal Properties

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance	θ_{JA}	still air	25.2	°C/W
		1m/s airflow	20.6	
		2.5m/s airflow	18.8	
Junction to Board Thermal Resistance	θ_{JB}		10.9	°C/W
Junction to Case Thermal Resistance	θ_{JC}		18.9	°C/W
Junction to Pad Thermal Resistance	θ_{JP}	Still air	6.5	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.6	°C/W

Table 9 7x7mm eTQFP Package Thermal Properties

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance	θ_{JA}	still air	TBD	°C/W
		1m/s airflow	TBD	
		2.5m/s airflow	TBD	
Junction to Board Thermal Resistance	θ_{JB}		TBD	°C/W
Junction to Case Thermal Resistance	θ_{JC}		TBD	°C/W
Junction to Pad Thermal Resistance	θ_{JP}	Still air	TBD	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	TBD	°C/W

Packages Outline



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5−1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Microsemi CMPG	DWG. NO.	REV.
TITLE 32L QFN PACKAGE OUTLINE BODY SIZE : 5x5X0.90 EPAD SIZE : 3.10 X 3.10mm PITCH:0.50mm	CDCA 22−0100 84−06−137−528	1
	SHEET	Ref JEDEC
	1 OF 1	MO−220

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	0.05	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
D2	3.50 REF			0.138 REF		
E2	3.50 REF			0.138 REF		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L 1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

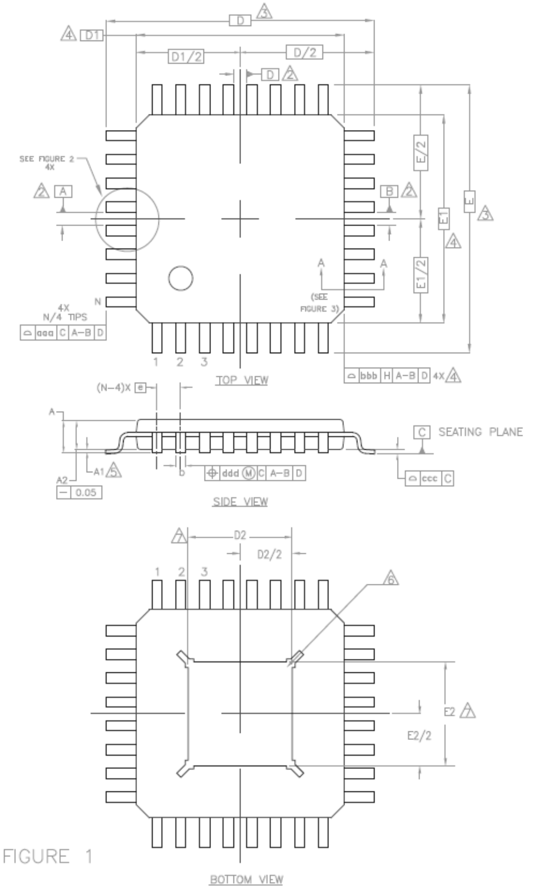


FIGURE 1

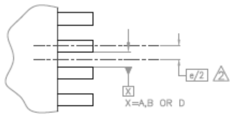


FIGURE 2: EVEN LEAD SIDES
TOP VIEW

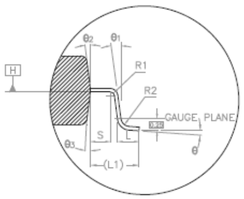


FIGURE 3: SECTION A–A

NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.

2. DATUMS A–B AND D TO BE DETERMINED AT DATUM PLANE H.

3. TO BE DETERMINED AT SEATING DATUM PLANE C.

4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

5. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

6. THE EXPOSED PAD IS COINCIDENT WITH THE BOTTOM SIDE OF THE PACKAGE AND NOT ALLOWED TO PROTRUDE BEYOND THAT SURFACE. THE SIZE DEPENDENT ON DIE ATTACH PAD.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.40	0.012	0.014	0.016
e	0.80 BSC.			0.031 BSC.		
N	32L					
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.20			0.008		

Microsemi CMPG	DWG. NO.	REV.
TITLE 32 eTQFP PACKAGE OUTLINE BODY SIZE : 7x7X1.0 mm 2.0 mm Footprint 0.8 pitch	CDCA 22–0104 84–06–117–020	2
	SHEET	SIZE
	1 OF 1	A4

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