Brief Description

The ZSSC3123 is a CMOS integrated circuit for accurate capacitance-to-digital conversion and sensor-specific correction of capacitive sensor signals. Digital compensation of sensor offset, sensitivity, and temperature drift is accomplished via an internal digital signal processor running a correction algorithm with calibration coefficients stored in a non-volatile EEPROM.

The ZSSC3123 is configurable for capacitive sensors with capacitances up to 260pF and a sensitivity of 125aF/LSB to 1pF/LSB depending on resolution, speed, and range settings. It is compatible with both single capacitive sensors (both terminals must be accessible) and differential capacitive sensors. Measured and corrected sensor values can be output as I²C™*, SPI, PDM, or alarms.

The I²C™ interface can be used for a simple PC-controlled calibration procedure to program a set of calibration coefficients into an on-chip EEPROM. The calibrated ZSSC3123 and a specific sensor are mated digitally: fast, precise, and without the cost overhead of trimming by external devices or laser.

Features

- Maximum target input capacitance: 260pF
- Sampling rates as fast as 0.7ms at 8-bit resolution; 1.6ms at 10-bit; 5.0ms at 12-bit; 18.5ms at 14-bit
- Digital compensation of sensor: piece-wise 1st and 2nd order sensor compensation or up to 3rd order single-region sensor compensation
- Digital compensation of 1st and 2nd order temperature gain and offset drift
- Internal temperature compensation reference (no external components)
- Programmable capacitance span and offset
- Layout customized for die-die bonding with sensor for low-cost, high-density chip-on-board assembly
- Accuracy † as high as
  ±0.25% FSO@ -40 to 125°C, 3V, 5V, Vsupply ±10%

Benefits

- Minimized calibration costs: no laser trimming, one-pass calibration using a digital interface
- Wide capacitance range to support a broad portfolio of different sensor elements
- Excellent for low-power battery applications

Interfaces

- I²C™ or SPI interface—easy connection to a µC
- PDM outputs (Filtered Analog Ratiometric) for both capacitance and temperature
- Up to two alarms that can act as full push-pull or open-drain switches

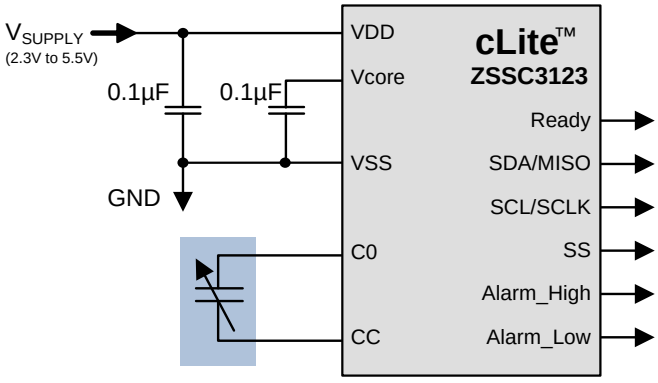
Physical Characteristics

- Supply voltage: 2.3V to 5.5V
- Typical current consumption 650µA down to 60µA depending on configuration
- Typical Sleep Mode current: ≤ 1µA at 85°C
- Operation temperature: –40°C to +125°C
- Die or TSSOP14 package

Available Support

- ZSSC3123 SSC Evaluation Kit available: SSC Evaluation Board, samples, software, documentation.
- Support for industrial mass calibration available.
- Quick circuit customization option for large production volumes.

Application: Digital Output, Alarms

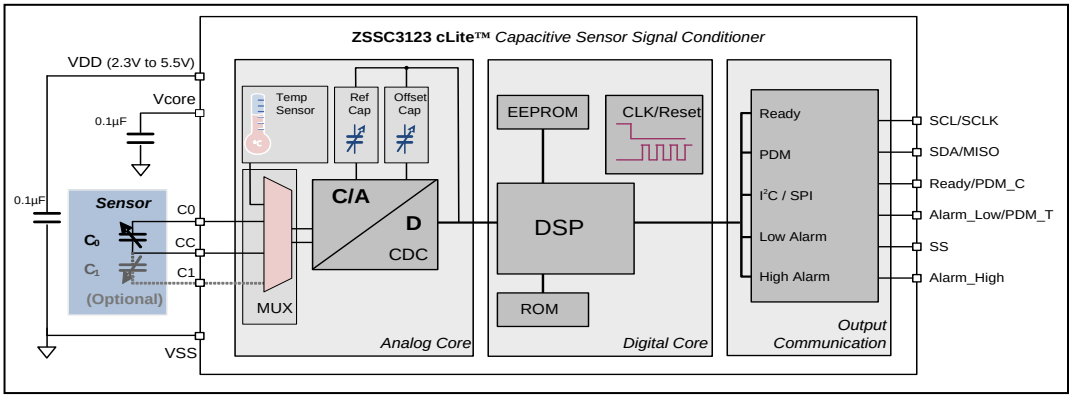


* I²C™ is a registered trademark of NXP.

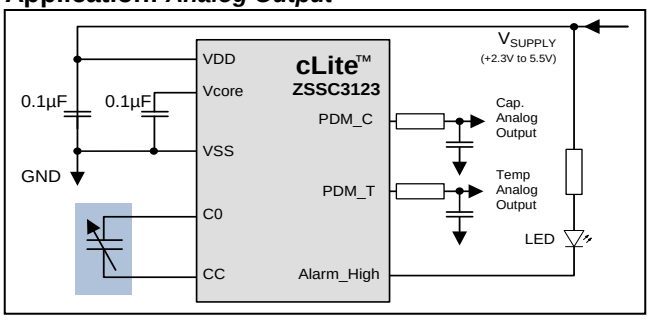
† See data sheet section 1.3 for restrictions.

ZSSC3123

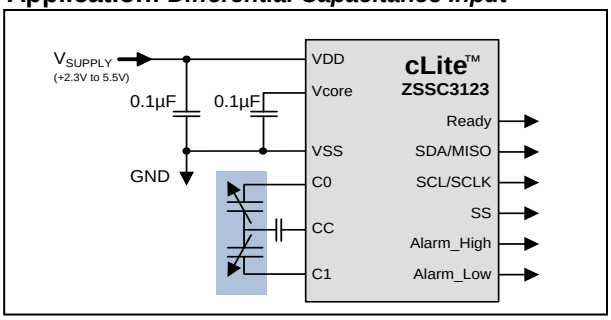
Block Diagram



Application: *Analog Output*



Application: *Differential Capacitance Input*



Ordering Codes

Sales Code	Description	Package
ZSSC3123AA1B	ZSSC3123 die — Temperature range: -40°C to +125°C	*Tested dice on un-sawn wafer*
ZSSC3123AI1B	ZSSC3123 die — Temperature range: -40°C to +85°C	*Tested dice on un-sawn wafer*
ZSSC3123AA1C	ZSSC3123 die — Temperature range: -40°C to +125°C	*Tested dice on frame*
ZSSC3123AI1C	ZSSC3123 die — Temperature range: -40°C to +85°C	*Tested dice on frame*
ZSSC3123AA2	ZSSC3123 TSSOP14 — Temperature range: -40°C to +125°C – Lead-free package	Tube: add “T” to code; reel: add “R”
ZSSC3123AI2	ZSSC3123 TSSOP14 — Temperature range: -40°C to +85°C – Lead-free package	Tube: add “T” to code; reel: add “R”
ZSSC3123KIT	ZSSC3123 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples (software can be downloaded from www.IDT.com/ZSSC3123)	Kit

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Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

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1 IC Characteristics

1.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply Voltage	V_{DD}	-0.3		6.0	V
Voltages at Analog I/O – In Pin	V_{INA}	-0.3		V_{DD}+0.3	V
Voltages at Analog I/O – Out Pin	V_{OUTA}	-0.3		V_{DD}+0.3	V
Storage Temperature Range	T_{STOR}	-55		150	°C

1.2 Operating Conditions

See important footnotes at the end of the following table.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage to Gnd	V_{SUPPLY}	2.3		5.5	V
Ambient Temperature Range [1)]	T_{AMB}	-40		125	°C
Output Pads/Pins Drive Strength [2)]	I_{OUT}	1.5		20	mA
External Capacitance between V_{DD} pin and Gnd	$C_{VSUPPLY}$	100	220	470	nF
External Capacitance between Vcore and Gnd—Sleep Mode	C_{VCORE_SM}	10		110	nF
External Capacitance between Vcore and Gnd—Update Mode	C_{VCORE_UM}	90		330	nF
Input Capacitance Span (Full Scale Values)	C_0	2		260	pF
External Reference Capacitance	C_1	2		260	pF
External Isolating Capacitance (Mult1)‡ (CC pin to sensor common node) [3)]	C_{CC}			16	pF
I^2C™ Pull-Up Resistor [3)]	R_{PU}	1	2.2		kΩ
SDA/MISO Load Capacitance	C_{SDA}			200	pF

1 *Caution: If buying die, select the proper package to ensure that the maximum junction temperature is not exceeded.*

2 See section 1.5 for full details on output pad drive strengths.

3 An external isolating capacitor allows a non-galvanic connection to special differential or external reference sensor types. Ccc could also be used to lower the overall capacitance level to a value that is supported by the ZSSC3123 because it limits the maximum capacitance seen by the ZSSC3123 input to CC even if C0 and C1 have higher values.

‡ The series combination of sensor and CC must not exceed the maximum capacitance allowed for the chosen Mult setting.

1.3 Electrical Parameters

See important footnotes at the end of the following table.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Update Mode Current (varies with part configuration) [1]	I_{DD}	Best case settings: * Mult 1, 8-bit, 125ms Power Down		60	100	µA
		Worst case settings: Mult 1, 14-bit, 0ms Power Down		750	1100	
Extra Current with PDM enabled *	I_{PDM}			150		µA
Sleep Mode Current [1]	I_{SLEEP}	-40 to 85°C		0.6	1	µA
		-40 to 125°C		1	3	µA
Voltage Levels						
Power-On-Reset Level	V_{POR}		1.6	1.7	2.2	V
Active Regulated Voltage	V_{REG}	Note: Regulated voltage can be measured on the Vcore pin.	2.4	2.55	2.7	V
CAPACITANCE-TO-DIGITAL CONVERTER (CDC)						
Resolution	RES_{CDC}		8		14	Bits
Excitation Frequency of External Capacitances C0 and C1 (for a system frequency f_{SYS})	f_{MULT1}	Mult 1		$f_{SYS}/2$		kHz
	f_{MULT2}	Mult 2		$f_{SYS}/4$		
	f_{MULT4}	Mult 4		$f_{SYS}/8$		
	f_{MULT8}	Mult 8		$f_{SYS}/16$		
Integral Nonlinearity (INL) [2]	INL_{CDC}	Mult 1, 10% to 90% input, 14-bit			0.2	%
Differential Nonlinearity (DNL) *	DNL_{CDC}	Mult 1, 10% to 90% input, 14-bit			0.9	LSB
EEPROM						
Number of Erase/Write Cycles	n_{WRI_EEP}	@85°C			100k	
Data Retention	t_{WRI_EEP}	@100°C			10	Year
TEMPERATURE CONVERSION						
Resolution in °C *	RES_{TEMP}	-40 to 125°C, 8-bit mode	0.64	0.96	1.6	°C
		-40 to 125°C, 14-bit mode	0.01	0.015	0.025	
Nonlinearity First Order Fit *, [3]	INL_{CDC}	-40 to 125°C		±0.5	±1	°C
Nonlinearity Second Order Fit *, [4]	INL_{CDC}	-40 to 125°C		±0.2	±0.4	°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Dependency *	PSR_{TEMP}	$V_{SUPPLY} > V_{REG}+0.25V$		0.03	0.1	°C/V
		$2.3V \le V_{SUPPLY} \le V_{REG} + 0.25V$		1.25	2.25	
PDM Output						
Output Range *	V_{PDM_Range}		10		90	$\%V_{SUPPLY}$
PDM Frequency	f_{PDM}			$f_{SYS}/8$		kHz
Filter Settling Time *, [5]	t_{SETT}	0% to 90% LPFilter 10kΩ/400nF			9.2	ms
Ripple *, [5]	V_{RIPP}	0% to 90% LPFilter 10kΩ/400nF			1.0	mV/V
PDM Additional Error (Including Ratiometricity Error) *	E_{PDM}	-40 to 125°C		0.1	0.5	%
DIGITAL I/O						
Voltage Output Level Low	V_{OL}			0	0.2	V_{SUPPLY}
Voltage Output Level High	V_{OH}		0.8	1		V_{SUPPLY}
Voltage Input Level Low	V_{IL}			0	0.2	V_{SUPPLY}
Voltage Input Level High	V_{IH}		0.8	1		V_{SUPPLY}
Communication Pin Input Capacitance *	C_{IN}				10	pF
TOTAL SYSTEM						
Capacitive Tolerance Between Parts *	C_{tol}	All capacitive values in the specification are subject to this variation			±10	%
Trimmed System Frequency	f_{SYS}	All timing in this specification is subject to this variation.	1.76	1.85	1.94	MHz
Frequency Variation Over Voltage and Temperature	f_{var}	All timing in this specification is subject to this variation.			±10	%
Start-Up-Time *, [6, 7] Power-on (POR) to data ready	t_{STA}	Fastest and slowest settings	4.25		173	ms
Update Rate (Update Mode) *, [6, 7]	t_{RESP_UP}	Fastest and slowest settings	0.70		288	ms
Response Time (Sleep Mode) *, [6, 7]	t_{RESP_SL}	Fastest and slowest settings	1.25		163	ms
Parasitic to Gnd Tolerance Including package parasitics (Pins C0, CC, and C1) *		Mult 1			10	pF
		Mult 2			20	
		Mult 4			40	
		Mult 8			80	
Peak-to-Peak Noise @ output (100 measurements in 14 bit) *	N_{OUT}	Mult 1, 2, 4, 8		5	20	LSB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Error Mult 1, -40 to 125°C *[8, 9,10]	AE_{out}	3V±10%, 3.3V±10%, 5V±10%		±0.25	±0.75	%FSO
		2.5V±10%		±0.50	±1.25	
Mult 2, 4, 8, -40 to 125°C *[8, 9, 10]	AE_{out}	3V±10%, 3.3V±10%, 5V±10%		±0.50	±1.25	%FSO
		2.5V±10%		±1.50	±3.00	

** Parameter not tested during production but guaranteed by design.*

1 *See section 1.4 for full details for current consumption in each mode.*

2 *Parameter measured using internal test capacitors (0pF to 7pF in Mult 1).*

3 *Assumes optimal calibration points of 0°C and 100°C; see section 1.6 for more details.*

4 *Assumes optimal calibration points of -20°C, 40°C and 100°C; see section 1.6 for more details.*

5 *See section 3.7 for more details.*

6 *See section 3 for more details.*

7 *Timing values are for a nominal oscillator, for worst case, ±10% total frequency variation, multiply by 0.9 (min time) or 1.1 (max time).*

8 *Accuracy specification includes a 2-point temperature calibration for correcting the internal TC.*

9 *Accuracy specification assumes maximum parasitics of 10pF to ground.*

10 *Accuracy specification does not include PDM errors, see the PDM Output electrical parameters for additional errors when using PDM.*

1.4 Current Consumption Graphs

Part current consumption depends on a number of different factors including voltage, temperature, capacitive input, Mult, resolution, and power down time. The best way to calculate the ZSSC3123's power consumption is to measure the current consumption with the actual setup. If measurement is not possible, then the graphs in this section can provide a starting point for estimating the current consumption.

1.4.1 Update Mode Current Consumption

Figure 1.1 Best Case Settings *(Typical Part)*

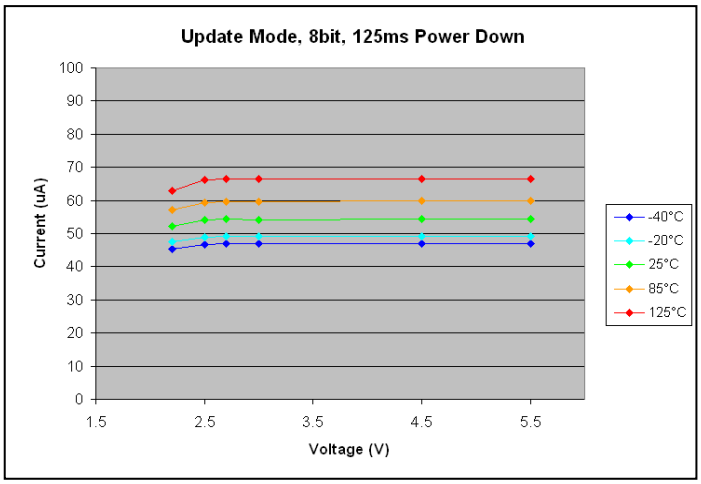
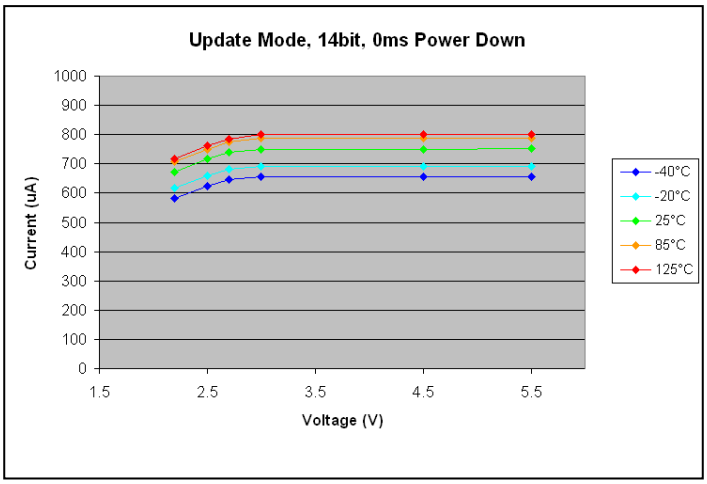
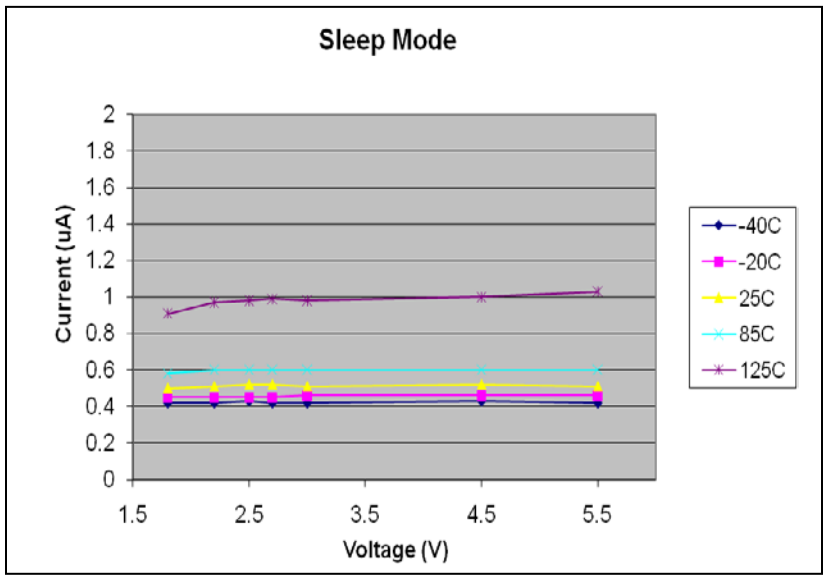


Figure 1.2 Worst Case Settings *(Typical Part)*



1.4.2 Sleep Mode Current Consumption

Figure 1.3 Typical Current Consumption during Sleep Mode *(No Measurements)*



1.5 Output Pad Drive Strength

Figure 1.4 Output High Drive Strength Graph

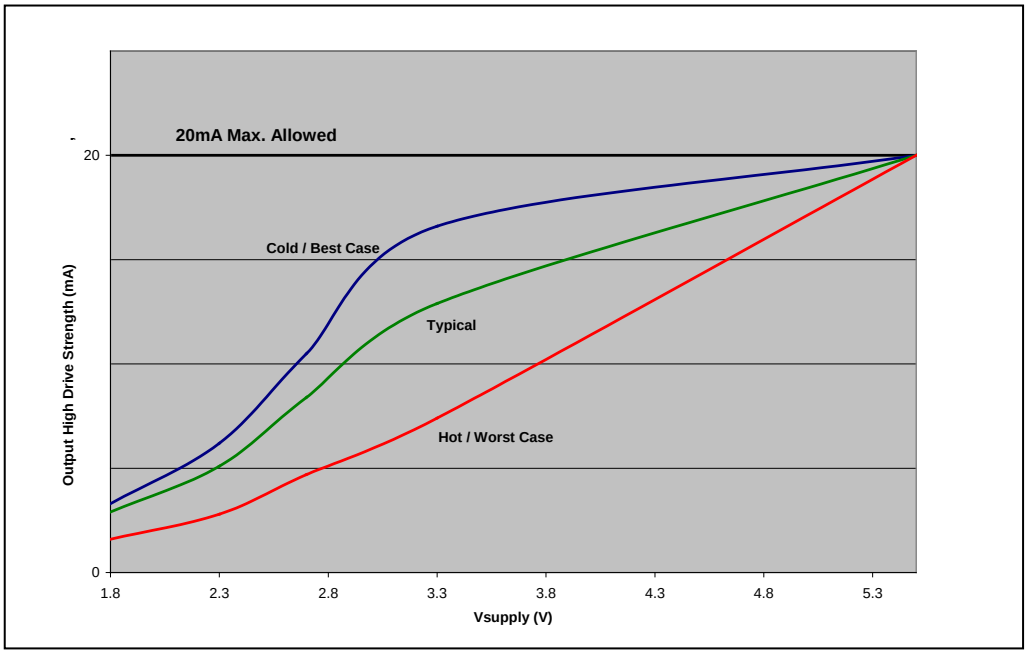
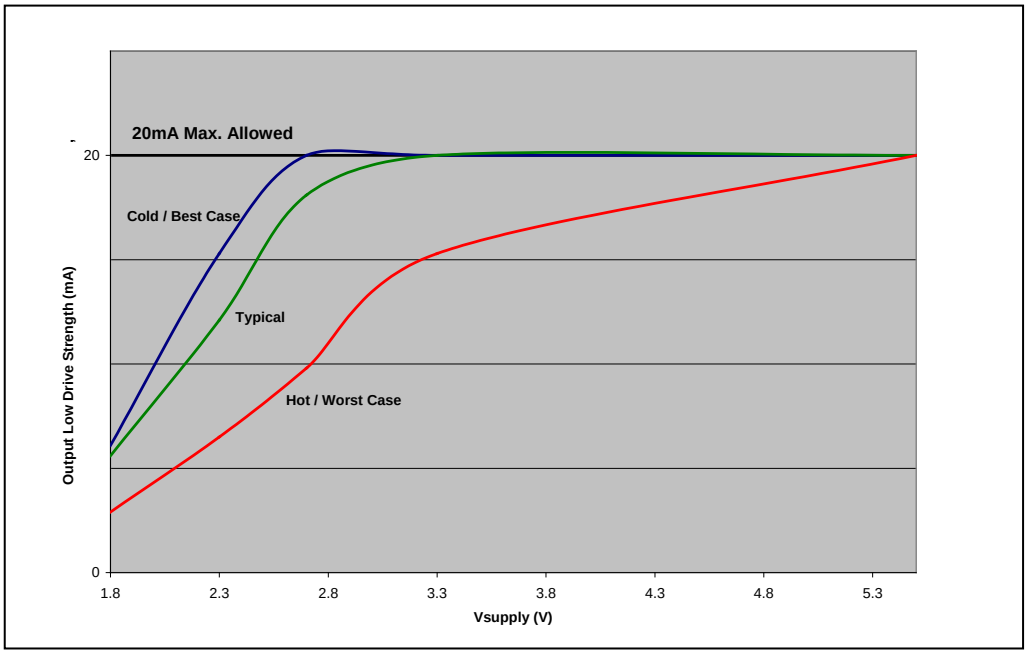


Figure 1.5 Output Low Drive Strength Graph



1.6 Temperature Sensor Nonlinearity

Temperature sensor nonlinearity can vary depending on the type of calibration and the selected calibration points. It is highly recommended that a temperature calibration is done with calibration points at least 20°C apart from each other. Figure 1.6 and Figure 1.7 show the resulting nonlinearity error for the full temperature range (-40°C to 125°C) using the optimal calibration points, 0°C and 100°C for a first-order fit and -20°C, 40°C, and 100°C for a second-order fit.

***Figure 1.6 First Order Fit** (Typical Part)*

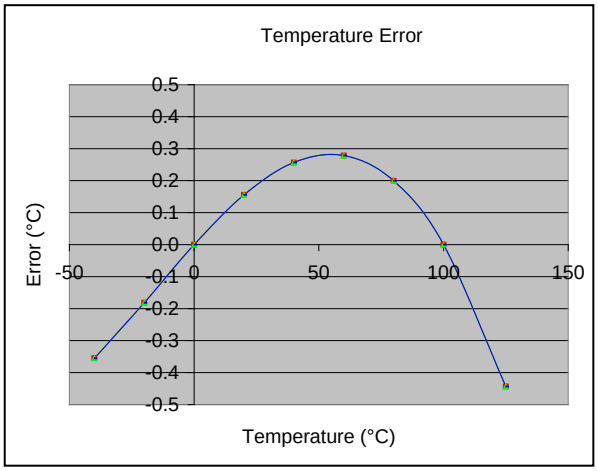
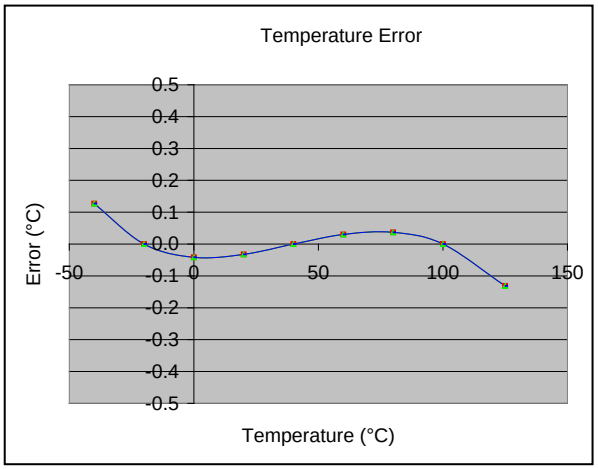


***Figure 1.7 Second Order Fit** (Typical Part)*



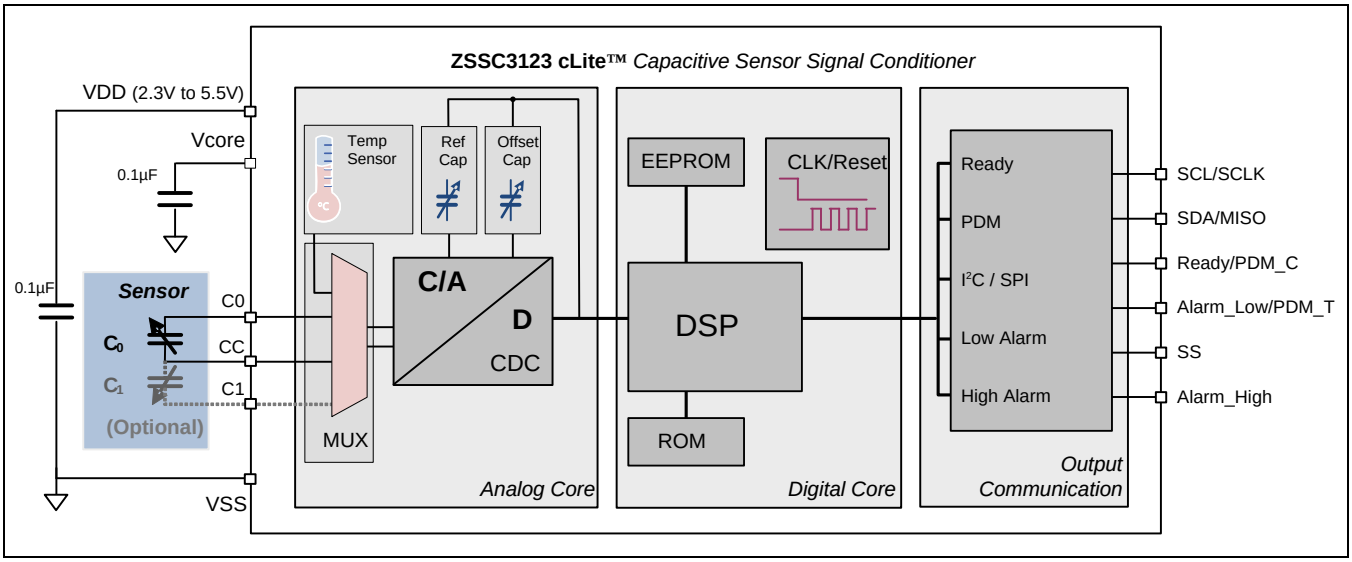
2 Circuit Description

2.1 Signal Flow and Block Diagram

As seen in Figure 2.1, the ZSSC3123 comprises three main blocks: the analog core, digital core, and output communication. The capacitive input is first sampled by the analog core using a charge-balancing CDC and is adjusted for the appropriate capacitance range using the CDC_Offset, and CDC_Reference, and CDC_Mult settings. The digital core corrects the digital sample with an on-chip digital signal processor (DSP), which uses coefficients stored in EEPROM for precise conditioning. An internal temperature sensor can be used to compensate for temperature effects of the capacitive input. A temperature value can also be calibrated and output as a 14-bit reading.

The corrected capacitance value can be read using four different output types, I²C™, SPI, PDM, and alarms. They can all be directly interfaced with a microcontroller, and optional filtering of the PDM output can provide a ratiometric analog output. The alarm pins can also be used to control a variety of analog circuitry.

Figure 2.1 ZSSC3123 Block Diagram



2.2 Analog Front End

2.2.1 Capacitance-to-Digital Converter

A 1st order charge-balancing capacitance-to-digital converter (CDC) is used to convert the input capacitance to the digital domain. The CDC uses a chopper-stabilized design to decrease any drift over temperature. The CDC interfaces to the sensor capacitor through the input multiplexer that controls whether the measurement is a capacitance or a temperature measurement. The input multiplexer also allows for two sensor capacitance configurations: a single sensor capacitance or a ratio based differential capacitive sensor, two-sensor, capacitor configuration, where the reference capacitor is part of the sensor.

As part of a switched-capacitor network the reference capacitor C_1 is driven by a square wave voltage of the frequency f_{EXC} (refer to section 1.3). The sensor capacitance C_0 is not exposed to DC voltages in order to prevent aging effects of some sensor types. The configuration of the CDC is controlled by programming settings in EEPROM word C_Config. (See Table 5.3 for settings.)

2.2.1.1. Single Ended

In the case of a single-sensor capacitor, the CDC output is proportional to the ratio of the sensor capacitor to an internal reference capacitor (**C_{REF}**). This internal reference capacitor value can be adjusted using the 3-bit trim CDC_Reference and a 2-bit range selection CDC_Mult (bit settings in Table 5.3). To optimize the measured end-resolution further, another internal capacitor (**C_{OFF}**) allows the subtraction of a defined offset capacitance using the 3-bit trim CDC_Offset (bit setting in Table 5.3). Equations (1) to (2) describe the CDC output for a single sensor capacitance measurement. For C_{MULT}, use the multiplier in the "Total Capacitance Multiplier (C_{MULT})" column in Table 2.1 in section 2.2.1.4. Select the values of CDC_Offset, and CDC_Reference by using the settings given in Table 2.2 a through d, depending on the Mult value. NOTE: Use the bit settings (0-7) and not the value in pF.

$$Z_{SENSOR} = \frac{(C_0 - C_{OFF})}{C_{REF}} \quad (1)$$

$$Z_{CDC} = 2^{RES} * Z_{SENSOR} \quad (2)$$

With

$$C_{OFF} = C_{MULT} * CDC\_Offset * 1pF \quad (3)$$

And

$$C_{REF} = C_{MULT} * CDC\_\text{Reference} * 1pF \quad (4)$$

Where:

Symbol	Description
Z_{SENSOR}	Measured sensor ratio, must be in the range [0 to 1]
C_0	Input sensor capacitance
C_{OFF}	Zero shift of CDC
C_{REF}	Reference capacitance
Z_{CDC}	Digital raw converted capacitance value
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 5.3)
C_{MULT}	Capacitance range multiplier (see Table 2.1)
CDC_Offset	CDC offset trim setting (selection see section 2.2.1.4 and bit setting see Table 5.3)
CDC_Reference	CDC reference setting (selection see section 2.2.1.4 and bit setting see Table 5.3)

2.2.1.2. Single Ended with External Reference

Some sensors include an external reference capacitor as part of the sensor construction. If the external reference capacitance (**C_1**) is constant or increases with increasing input sensor capacitance (**C_0**), then use CDC output equations (5) to (7). In this case the CDC_Reference should be set to zero (bit setting in Table 5.3).

$$Z_{SENSOR} = \frac{(C_0 - C_{OFF})}{C_1} \quad \textbf{(5)}$$

$$Z_{CDC} = 2^{RES} * Z_{SENSOR} \quad \textbf{(6)}$$

$$C_{OFF} = C_{MULT} * CDC\_Offset * 1pF \quad \textbf{(7)}$$

Where

Symbol	Description
Z_{SENSOR}	Measured sensor ratio, must be in the range [0 to 1]
C_0	Input sensor capacitance
C_{OFF}	Zero shift of CDC
C_1	External reference capacitance
Z_{CDC}	Digital raw converted capacitance value
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 5.3)
C_{MULT}	Capacitance range multiplier (see Table 2.1)
CDC_Offset	CDC offset trim setting (selection see section 2.2.1.4 and bit setting see Table 5.3)

2.2.1.3. Differential

A differential capacitive sensor includes two capacitors C_0 and C_1 that are captured as a ratio. The differential sensor is built so that the sensor input capacitance C_0 increases while the external reference capacitance C_1 decreases over the input signal range, but the total sum always remains constant. Equations describe the CDC output for a differential sensor capacitance measurement. The CDC_Reference and CDC_Offset capacitor trim bits need to be set to zero, and the Differential bit needs to be set to one. (See Table 5.3 for bit numbers and settings). The Mult bits should be set so that the total capacitance (C_0 + C_1) falls in the corresponding capacitance range (see Table 2.1). The sum of C_0 and C_1 must not be bigger than the selected mult's maximum input range, except when CC is used as a decoupling capacitor.

In differential mode special sensor types can allow a non-galvanic connection with an external isolating capacitor C_{CC} between the sensor and the CC pin to avoid wear caused by mechanical moving parts.

$$Z_{SENSOR} = \frac{C_0}{(C_0 + C_1)} \quad \textbf{(8)}$$

$$Z_{CDC} = 2^{RES} * Z_{SENSOR} \quad \textbf{(9)}$$

Where

Symbol	Description
Z_{SENSOR}	Measured sensor ratio, must be in the range [0 to 1]
C_0	Input sensor capacitance (moves in the opposite direction of C_1)
C_1	External reference capacitance (moves in the opposite direction of C_0)
Z_{CDC}	Digital raw converted capacitance value
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 5.3)

2.2.1.4. Capacitive Range Selection

Whether one is using a single-ended or a differential sensor the correct capacitance range must be selected using the Mult bits as seen in Table 2.1. (See Table 5.3 for bit numbers). If using a single-ended sensor, then the minimum and maximum capacitance inputs should fall into the specified ranges. If using a differential sensor then the total capacitance (C_0 + C_1) needs to fall into this range. The Mult range affects the conversion time (see section 3.2)

Note: If the range is set to a lower input value and a higher input capacitance value is applied, the output can come back into range. The limit is about 500% of the selected maximum input value, e.g. for capacitance setting mult1, CDC_Offset at zero and CDC_Reference at 7, an input value above 117pF will give a non-saturated input value.

Table 2.1 CDC Multiplier

EEPROM Encoding (CDC_Mult)	Frequency Multiplier (Mult)	Reference Multiplier	Total Capacitance Multiplier (C_{MULT})	Capacitance Range (Full Scale Values)
00_B	1	1.44	1.44	2pF to 8pF
01_B	2	2.88	5.76	8pF to 32pF
10_B	4	5.76	23.04	32pF to 130pF
11_B	8	11.52	92.16	130pF to 260pF

For single ended sensors use Table 2.2 as guidance to select appropriate values for the CDC (C_{OFF}) and (C_{REF}) for a particular capacitance input range. The CDC_Offset and CDC_Reference bits are found in EEPROM word C_Config. (See Table 5.3 for bit numbers). Using Table 2.2, the CDC input range can be adjusted to optimize the coverage of the sensor signal and offset values to give the maximum sensor span that can be processed without losing resolution. Choose a range by fitting the input sensor span within the narrowest range in the table, but note that these tables are only approximate, so the range should be experimentally chosen with the actual setup. Also note that since internal capacitance values can vary over process (see spec parameter C_{tol} in section 1.3), the minimum and maximum sensor span should be at least ±10% within the min and max of the chosen range respectively. In addition, be aware of the effects of parasitics; if the parasitics for a particular Mult range exceed the parasitic to ground tolerance given in section 1.3, then the next Mult range should be considered since the CDC frequency is reduced by the Mult factor.

Note: A C_{REF} setting of 0 (marked with * in the following tables) is only supported with an external reference capacitor (C1) for single-ended sensors. C1 capacitance values should be within the defined range for each Mult setting.

Table 2.2 Selection Settings for C_{REF}, and C_{OFF}, and Mult (Capacitance ranges are nominal values[§])

(a) Mult 1: Sensor Capacitors Ranging from 2pF to 10pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	1.4	0.0	2.9	0.0	4.3	0.0	5.8	0.0	7.2	0.0	8.6	0.0	10.1
	1	1.4	C1	1.4	2.9	1.4	4.3	1.4	5.8	1.4	7.2	1.4	8.6	1.4	10.1	1.4	11.5
	2	2.9	C1	2.9	4.3	2.9	5.8	2.9	7.2	2.9	8.6	2.9	10.1	2.9	11.5		
	3	4.3	C1	4.3	5.8	4.3	7.2	4.3	8.6	4.3	10.1	4.3	11.5				
	4	5.8	C1	5.8	7.2	5.8	8.6	5.8	10.1	5.8	11.5						
	5	7.2	C1	7.2	8.6	7.2	10.1	7.2	11.5								
	6	8.6	C1	8.6	10.1	8.6	11.5										
	7	10.1	C1	10.1	11.5												

PROHIBITED

not recommended

[§] Production-related tolerances can change the nominal capacitance values by ±10%

(b) Mult 2: Sensor Capacitors Ranging from 8pF to 32pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	5.8	0.0	11.5	0.0	17.3	0.0	23.0	0.0	28.8	0.0	34.6	0.0	40.3
	1	5.8	C1	5.8	11.5	5.8	17.3	5.8	23.0	5.8	28.8	5.8	34.6	5.8	40.3		
	2	11.5	C1	11.5	17.3	11.5	23.0	11.5	28.8	11.5	34.6	11.5	40.3				
	3	17.3	C1	17.3	23.0	17.3	28.8	17.3	34.6	17.3	40.3						
	4	23.0	C1	23.0	28.8	23.0	34.6	23.0	40.3								
	5	28.8	C1	28.8	34.6	28.8	40.3										
	6	34.6	C1	34.6	40.3												
	7																

PROHIBITED

not recommended

(c) Mult 4: Sensor Capacitors Ranging from 32pF to 130pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	23.0	0.0	46.1	0.0	69.1	0.0	92.2	0.0	115.2	0.0	138.2	0.0	161.3
	1	23.0	C1	23.0	46.1	23.0	69.1	23.0	92.2	23.0	115.2	23.0	138.2	23.0	161.3		
	2	46.1	C1	46.1	69.1	46.1	92.2	46.1	115.2	46.1	138.2	46.1	161.3				
	3	69.1	C1	69.1	92.2	69.1	115.2	69.1	138.2	69.1	161.3						
	4	92.2	C1	92.2	115.2	92.2	138.2	92.2	161.3								
	5	115.2	C1	115.2	138.2	115.2	161.3										
	6	138.2	C1	138.2	161.3												
	7																

PROHIBITED

not recommended

(d) Mult 8: Sensor Capacitors Ranging from 130pF to 260pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	92.2	0.0	184.3	0.0	276.5								
	1	92.2	C1	92.2	184.3	92.2	276.5										
	2	184.3	C1	184.3	276.5												
	3																
	4																
	5																
	6																
	7																

PROHIBITED

not recommended

2.2.2 Temperature Measurement

The temperature signal comes from an internal PTAT (proportional to absolute temperature) circuit that is a measure of the die temperature. The PTAT (V_{PTAT}) voltage is used in the CDC to charge an internal capacitor (C_T), while the bandgap voltage (V_{BG}) is used to charge the offset and the reference trimmable capacitors. The CDC temperature output (Z_{TEMP}) is defined by equations (10) to (13):

$$Z_{TEMP} = 2^{RES} * \frac{(V_{PTAT} / V_{BG}) * C_T - C_{TOFF}}{C_{TREF}} \quad \textbf{(10)}$$

With

$$C_T = 1.44 * Temp\_Trim * 1pF \quad \textbf{(11)}$$

With

$$C_{TOFF} = 1.44 * CDC\_Offset * 1pF \quad \textbf{(12)}$$

And

$$C_{TREF} = 1.44 * CDC\_Reference * 1pF \quad \textbf{(13)}$$

Where

Symbol	Description
Z_{TEMP}	Measured internal temperature
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 5.4)
V_{PTAT}	Internal PTAT voltage
V_{BG}	Internal bandgap voltage
C_T	Temperature measurement capacitor
C_{TOFF}	Temperature CDC zero shift
C_{TREF}	Temperature reference capacitance
Temp_Trim	Temperature trim setting (bit setting in Table 5.4)
CDC_Offset	CDC offset trim setting (bit setting in Table 5.4)
CDC_Reference	CDC reference setting (bit setting in Table 5.4)

Note: The factory settings for Temp_Trim, CDC_Offset, and CDC_Reference are optimized for the full temperature range of -40°C to 125°C guaranteeing a minimum effective resolution of 13 bits when 14 bits of resolution is selected. Unless a different temperature range is needed, it is strongly recommended that these settings not be changed.

2.3 Digital Core

The digital core provides control logic for the analog front-end, performs input signal conditioning, and handles external communication. A digital signal processor (DSP) is used for conditioning and correcting the converted sensor and temperature inputs. The DSP can correct for up to a two-region piece-wise non-linear sensor input, and up to a second order non-linear temperature input. Alternatively a third-order correction of the sensor input for one region and up to a second-order non-linear temperature input can be selected. Refer to section 6 for details on the signal conditioning and correction math. The analog front-end configuration and correction coefficients for both the capacitive sensor and the temperature sensor are stored in an on-chip EEPROM (see section 5).

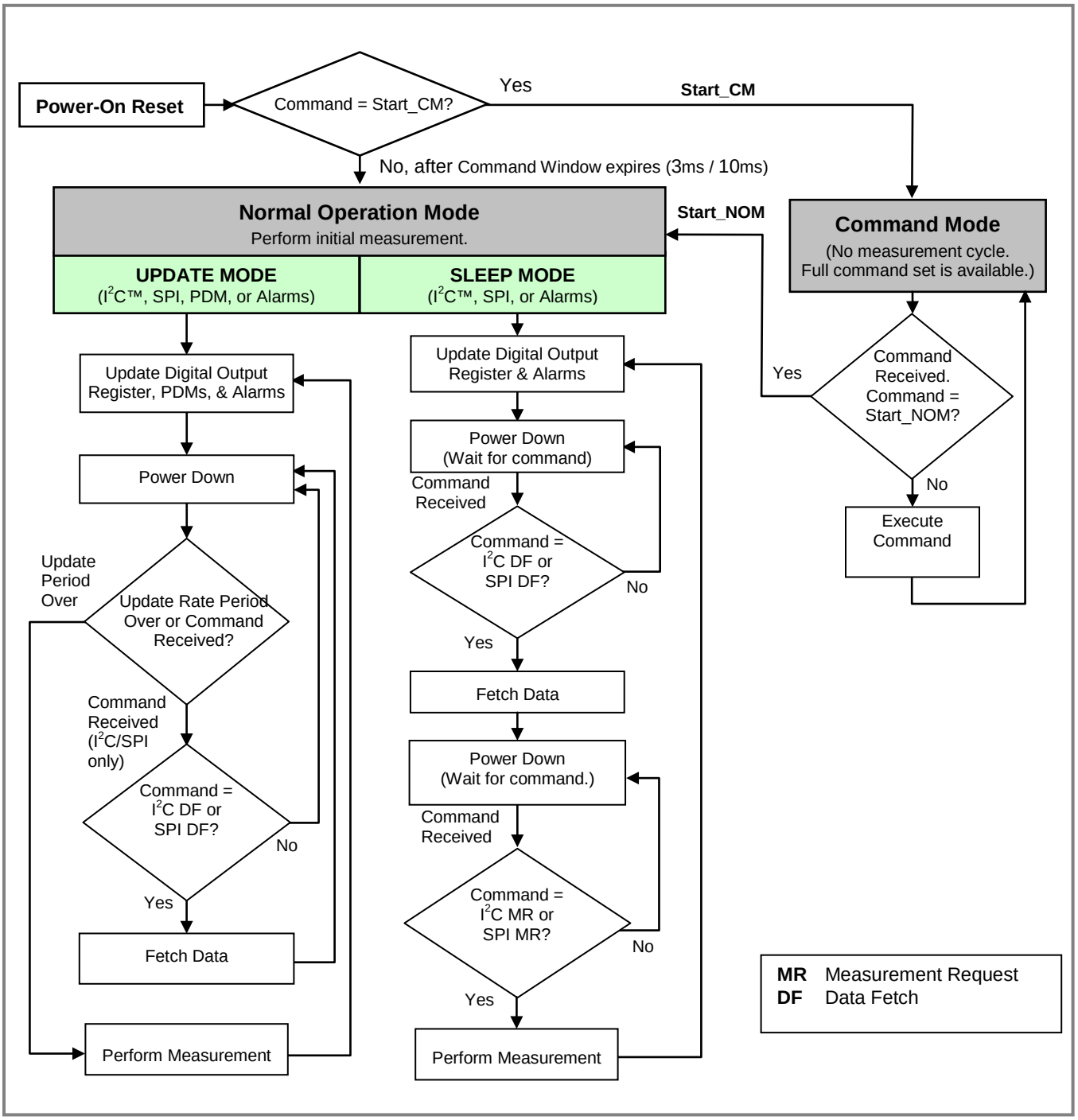
Four different types of outputs are available: I^2C™, SPI, PDM, and the Alarms. These output modes are used in combination with the two measurement modes: Update Mode and Sleep Mode. For a full description of normal operation in each mode, refer to section 3.

The ZSSC3123 has an internal 1.85 MHz temperature-compensated oscillator that provides the time base for all operations. When VDD exceeds the POR level, the reset signal de-asserts and the clock generator starts. See section 3.1 for the subsequent power-up sequence. The exact clock frequency influences the measurement cycle time (see the frequency variation spec in section 1.3). To minimize the oscillator error as the VDD voltage changes, an on-chip regulator supplies the oscillator block.

3 Normal Operation Mode

Figure 3.1 gives a general overview of ZSSC3123 operation. Details of operation, including the power-up sequence, measurement modes, output modes, diagnostics, and commands, are given in the subsequent sections.

Figure 3.1 General Operation

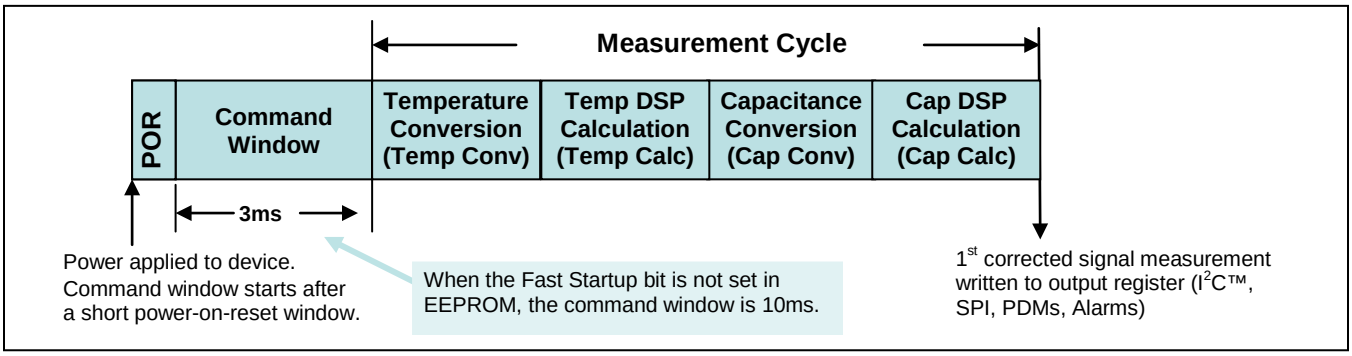


3.1 Power-On Sequence

Figure 3.2 shows the power-on sequence of the ZSSC3123. On system power-on reset (POR), the ZSSC3123 wakes as an I²C™ device regardless of the output protocol programmed in EEPROM. After power-on reset, the ZSSC3123 enters the command window. It then waits for a Start_CM command for 3ms if the Fast_Startup EEPROM bit is set or 10ms otherwise (see Table 5.5). If the ZSSC3123 receives the Start_CM command during the command window, it enters and remains in Command Mode. Command Mode is primarily used in the calibration environment. See section 4 for details on Command Mode.

If during the power-on sequence, the command window expires without receiving a Start_CM or if the part receives a Start_NOM command in Command Mode, the device will immediately assume its programmed output mode and will perform one complete measurement cycle. Timing for the initial measurement is described in section 3.2. At the end of the capacitance DSP calculation, the first data is written to the output register. Beyond this point, conversions are performed according to the programmed measurement mode settings (see section 3.3).

Figure 3.2 Power-On Sequence with Fast Startup Bit Set in EEPROM



***Note**: See section 3.2 for timing of the measurement cycle. Timing values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).*

3.2 Measurement Cycle

Figure 3.3 shows a typical measurement cycle. At the start of a measurement, there is a small wakeup period and then an internal temperature conversion/temperature DSP calculation is performed followed by a capacitance conversion/capacitance DSP calculation. The length of these conversions depends on the setting of the Resolution bits (see Table 3.1). For capacitance measurements, conversion time also depends on the Mult selected by the CDC_Mult bits (see Table 2.1). Both The resolution and the CDC_Mult bits can be found in EEPROM words C_Config and T_Config (see Table 5.3 and Table 5.4 for bit numbers). Each conversion cycle is followed by a DSP calculation, which uses the programmed calibration coefficients to calculate corrected temperature and capacitance measurements. In Update Mode, a temperature conversion is not performed every measurement cycle because it is considered a slower moving quantity. In this case, the measurement cycle timing is the same as Figure 3.3 without the temperature conversion/ temperature DSP calculation (see section 3.3.1 for more information).

Figure 3.3 Measurement Cycle Timing **

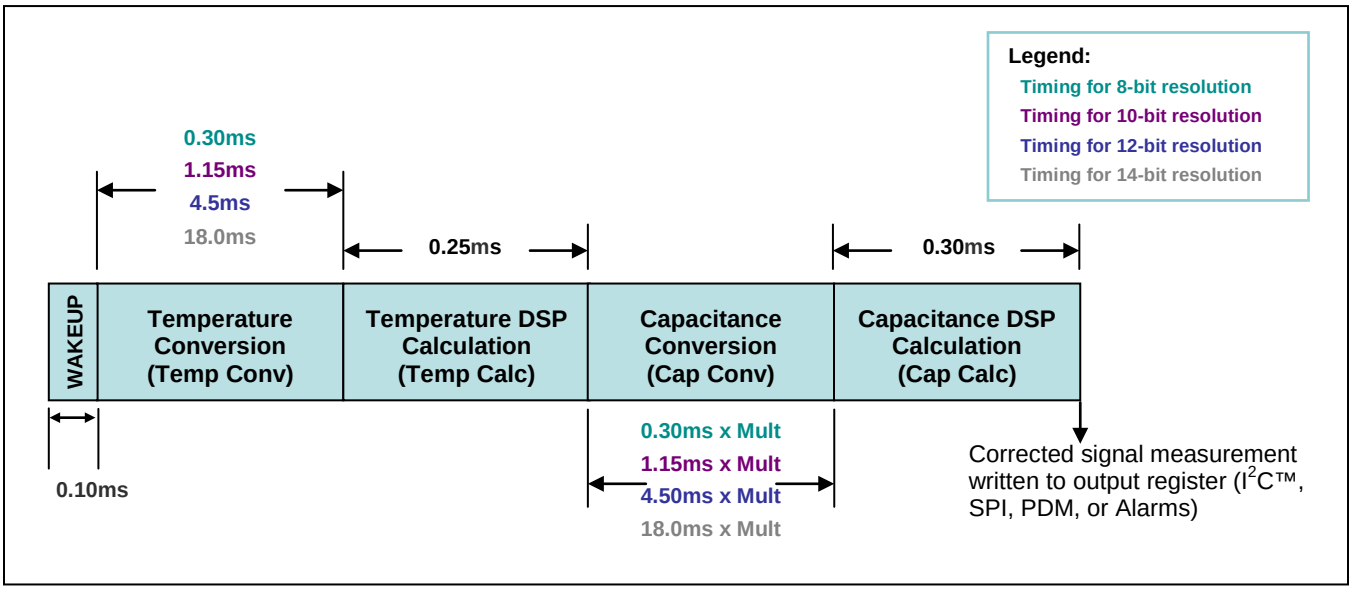


Table 3.1 CDC Resolution and Conversion Times

EEPROM Encoding	CDC Resolution (Bits)	Temperature Conversion Time ** (ms)	Capacitance Conversion Time ** (ms)
00_B	8	0.30	0.30 * Mult
01_B	10	1.15	1.15 * Mult
10_B	12	4.50	4.50 * Mult
11_B	14	18.0	18.0 * Mult

3.3 Measurement Modes

The ZSSC3123 can be programmed to operate in either Sleep Mode or Update Mode. The measurement mode is selected with the Measurement_Mode bit in the ZMDI_Config EEPROM word (see Table 5.2). In Update Mode, measurements are taken at a fixed, selectable rate (see section 3.3.1). In Sleep Mode, the part waits for commands from the master before taking measurements (see section 3.3.2). Figure 3.1 shows the differences in operation between the two measurement modes.

3.3.1 Update Mode

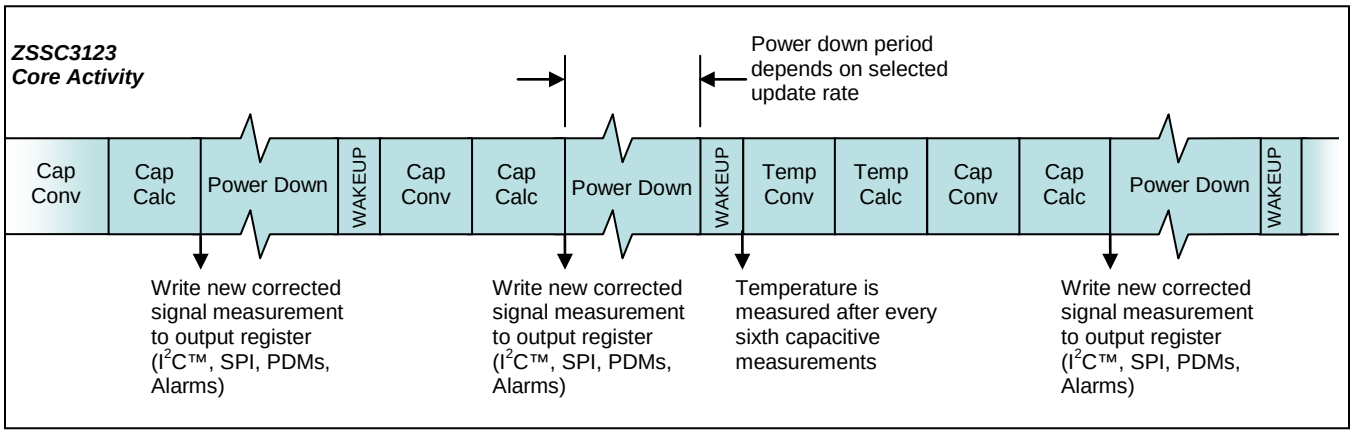
In Update Mode, the digital core will perform conversions at an update rate selected with the Update_Rate bits in the ZMDI_Config EEPROM word (see Table 5.2). Table 3.2 shows the power-down periods between conversions for the four Update_Rate settings. The benefit of slower update rates is power savings. Update Mode is compatible with all the different output modes; I²C™, SPI, PDMs, and the Alarms. As shown in Figure 3.4, at the completion of a measurement cycle, the digital output register, PDMs, and/or Alarms will be updated before powering down. When the power-down period expires, the ZSSC3123 will wake up and perform another measurement cycle. If the part is programmed for the fastest update rate, there is no power down period, and measurements happen continuously.

** All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

Table 3.2 Update Rate Settings [††]

Update_Rate	Power Down Period (ms)
00_B	0
01_B	5
10_B	25
11_B	125

Figure 3.4 Measurement Sequence in Update Mode



***Note**: See section 3.2 for measurement cycle timing.*

To calculate the total time between capacitive measurements in Update Mode, add the measurement cycle timing from section 3.2 and the power down timing from Table 3.2. For example typical settings might be a capacitance measurement resolution of 12-bits with a Mult of 1.

In this example, the time between measurements = (4.5ms*1+ 0.1ms+ 0.3ms) + (power down period). Table 3.3 shows the time between measurements for the different update rate settings and bit resolutions.

Temperature measurements are performed every six capacitive measurements. The actual frequency of temperature conversions varies with the update rate and AFE configuration settings. As shown in Figure 3.4 when a temperature measurement is performed, a capacitance measurement occurs immediately after, so the total measurement cycle time is increased by the length of the temperature conversion/temperature DSP calculation.

To calculate the total time between temperature measurements in Update Mode, take the time between capacitive measurements as calculated in the above text and multiply that number by six (there are six capacitive measurements to every temperature measurement) and then add the temperature conversion time/temperature DSP calculation time from Table 3.1 For example a temperature measurement with a resolution of 12-bits has a conversion time/DSP calculation time of 4.5ms +0.25ms (from Table 3.1) Continuing with the above example (12-bit capacitive measurement with a multiplier of 1) the time between temperature measurements is (capacitance update time * 6) + 4.75ms.

[††] All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

Table 3.3 Time Periods between Capacitance Measurements and Temperature Measurements for Different Mult, Resolution and Update Rates

Mult1	Total Time between Capacitance Measurements (ms)				Total Time between Temperature Measurements (ms)			
CDC Resolution (Bits)	Update Rate 00_B	Update Rate 01_B	Update Rate 10_B	Update Rate 11_B	Update Rate 00_B	Update Rate 01_B	Update Rate 10_B	Update Rate 11_B
8	0.70	5.70	25.70	125.70	4.75	34.75	154.75	754.75
10	1.55	6.55	26.55	126.55	10.70	40.70	160.70	760.70
12	4.90	9.90	29.90	129.90	34.15	64.15	184.15	784.15
14	18.40	23.40	43.40	143.40	128.65	158.65	278.65	878.65
Mult2	**Total Time between Capacitance Measurements (ms)**				**Total Time between Temperature Measurements (ms)**			
CDC Resolution (Bits)	Update Rate 00_B	Update Rate 01_B	Update Rate 10_B	Update Rate 11_B	Update Rate 00_B	Update Rate 01_B	Update Rate 10_B	Update Rate 11_B
8	1.00	6.00	26.00	126.00	6.55	36.55	156.55	756.55
10	2.70	7.70	27.70	127.70	17.60	47.60	167.60	767.60
12	9.40	14.40	34.40	134.40	61.15	91.15	211.15	811.15
14	36.40	41.40	61.40	161.40	236.65	266.65	386.65	986.65
Mult4	**Total Time between Capacitance Measurements (ms)**				**Total Time between Temperature Measurements (ms)**			
CDC Resolution (Bits)	Update Rate 00_B	Update Rate 01_B	Update Rate 10_B	Update Rate 11_B	Update Rate 00_B	Update Rate 01_B	Update Rate 10_B	Update Rate 11_B
8	1.60	6.60	26.60	126.60	10.15	40.15	160.15	760.15
10	5.00	10.00	30.00	130.00	31.40	61.40	181.40	781.40
12	18.40	23.40	43.40	143.40	115.15	145.15	265.15	865.15
14	72.40	77.40	97.40	197.40	452.65	482.65	602.65	1202.65

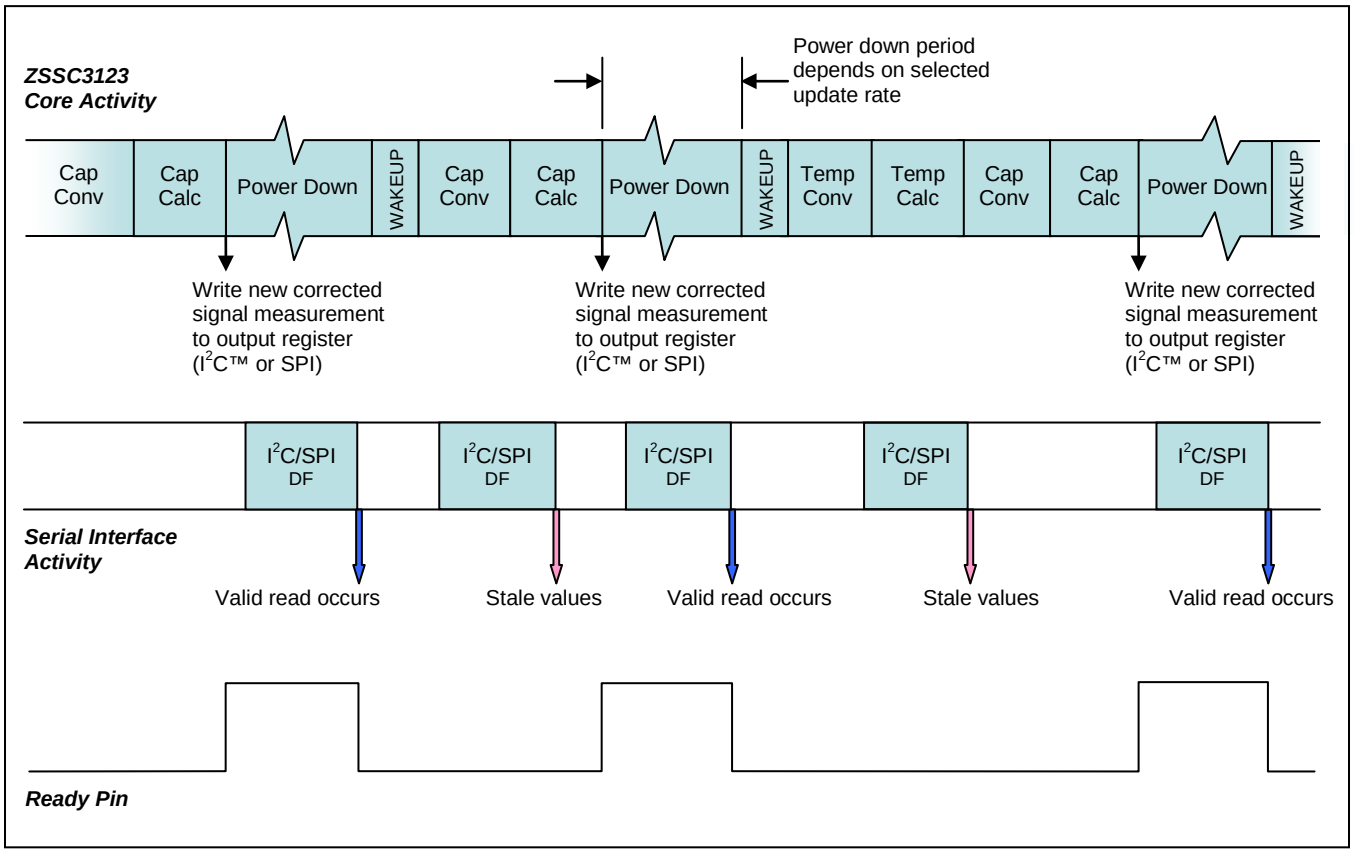
Mult8	Total Time between Capacitance Measurements (ms)				Total Time between Temperature Measurements (ms)			
CDC Resolution (Bits)	Update Rate 00_B	Update Rate 01_B	Update Rate 10_B	Update Rate 11_B	Update Rate 00_B	Update Rate01_B	Update Rate 10_B	Update Rate 11_B
8	2.80	7.80	27.80	127.80	17.35	47.35	167.35	767.35
10	9.60	14.60	34.60	134.60	59.00	89.00	209.00	809.00
12	36.40	41.40	61.40	161.40	223.15	253.15	373.15	973.15
14	144.40	149.40	169.40	269.40	884.65	914.65	1034.65	1634.65

3.3.1.1. Data Fetch in Update Mode

In Update Mode, I²C™ and SPI are used to fetch data from the digital output register using a Data Fetch (DF) command (see section 3.6.3).

Detecting when data is ready to be fetched can be handled either by polling or by monitoring the Ready pin (see section 3.6.6 for details on the Ready pin). The status bits of a DF tell whether or not the data is valid or stale (see section 3.4 regarding the status bits). As shown in Figure 3.5 after a measurement cycle is complete, valid data can be fetched. If the next data fetch is performed too early, the data will be the same as the previous fetch with stale status bits. As shown in Figure 3.5, a rise on the Ready pin can also be used to tell when valid data is ready to be fetched.

Figure 3.5 I²C™ and SPI Data Fetching in Update Mode



***Note**: See section 3.2 for timing of measurements.*

3.3.2 Sleep Mode

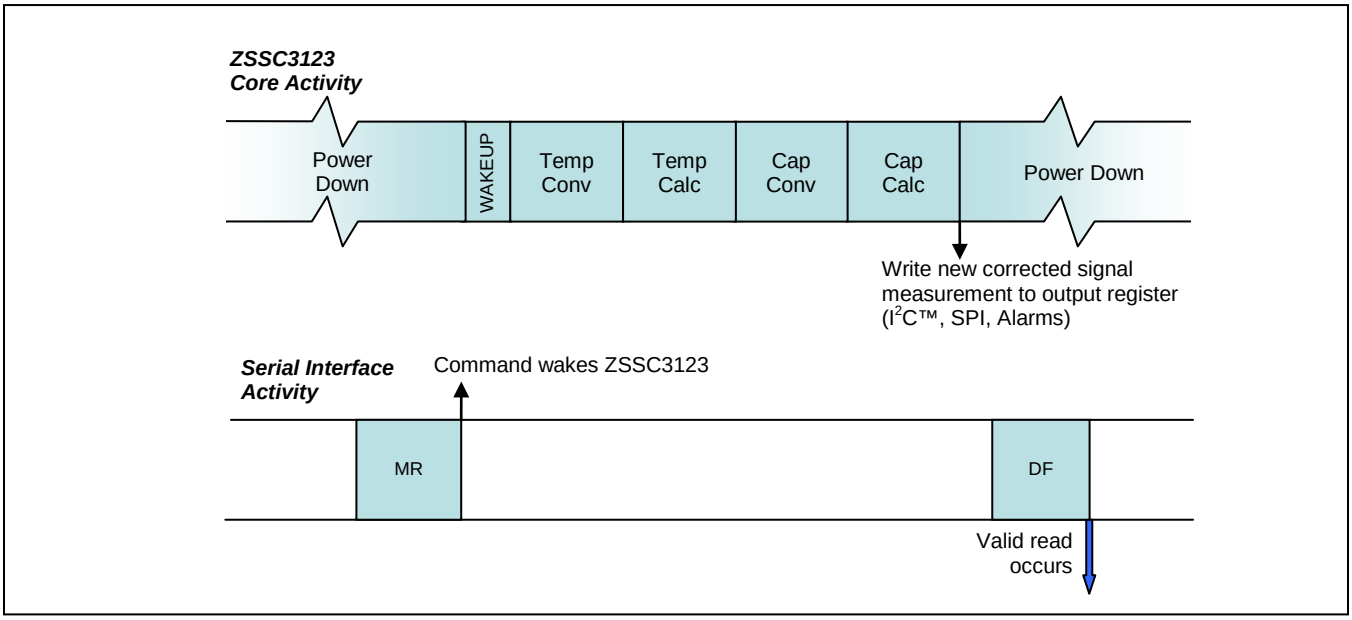
In Sleep Mode, the digital core will only perform conversions when the ZSSC3123 receives a Measurement Request command (MR); otherwise, the ZSSC3123 is always powered down. Measurement Request commands can only be sent using I²C™ or SPI, so PDM is not available. The Alarms can be used in Sleep Mode but only in combination with I²C™ or SPI. More details about MR commands in Sleep Mode operation can be found in section 3.3.2.1.

Note: Sleep Mode power consumption is significantly lower than Update Mode power consumption (see section 1.3 for exact values).

Figure 3.6 shows the measurement and communication sequence for Sleep Mode. The master sends an MR command to wake the ZSSC3123 from power down. After the ZSSC3123 wakes up, a measurement cycle is performed consisting of both a temperature and a capacitance conversion followed by the DSP correction calculations.

At the end of a measurement cycle, the digital output register and Alarms will be updated before powering down. An I²C™ or SPI data fetch (DF) is performed during the power-down period to fetch the data from the output register. In I²C™ the user can send another MR to start a new measurement cycle without fetching the previous data, but in SPI, a DF must be done before another MR can be sent. After the data has been fetched, the ZSSC3123 remains powered down until the master sends an MR command. The timing for measurements can be found in section 3.2.

Figure 3.6 Measurement Sequence in Sleep Mode (Only I²C™, SPI, or Alarms)



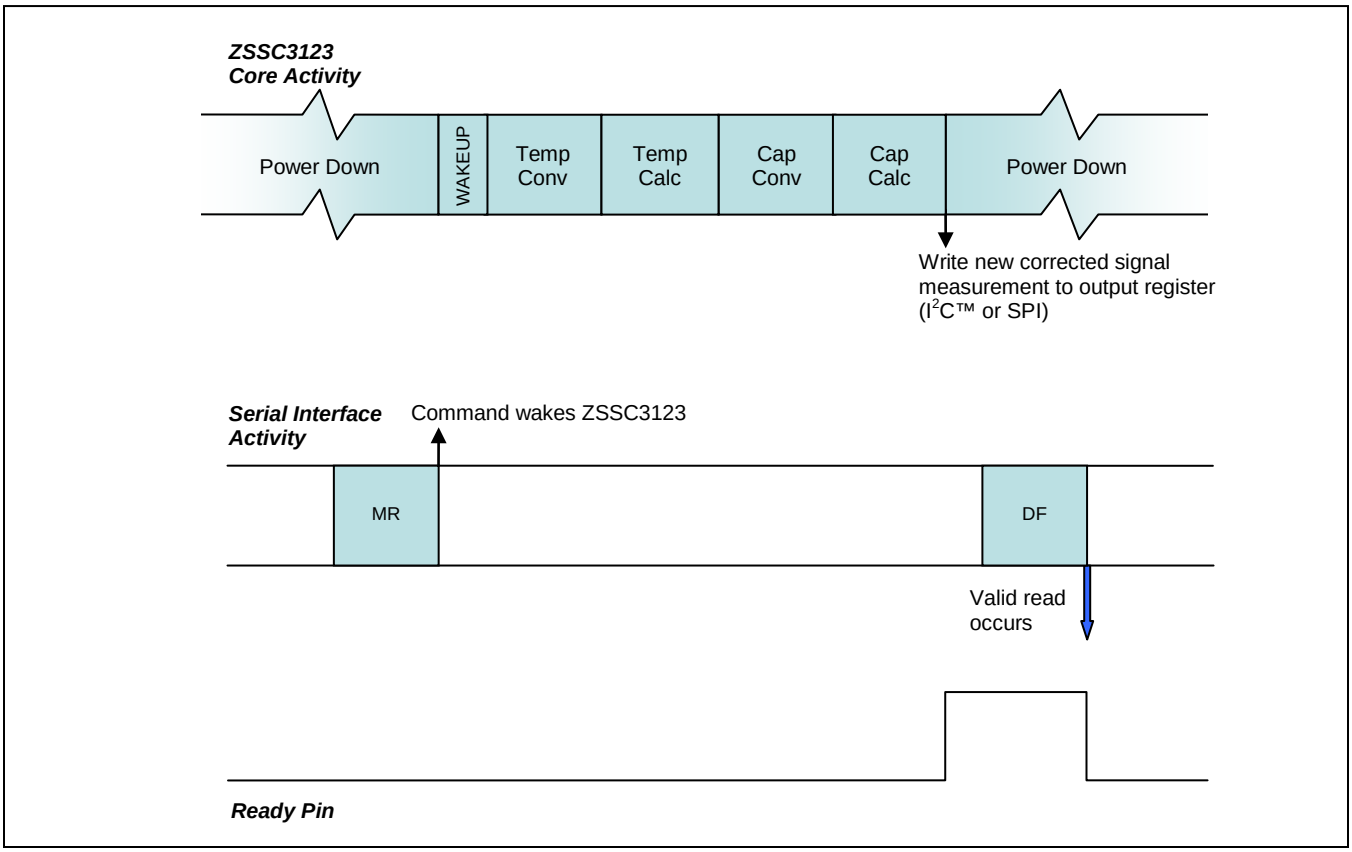
***Note**: See section 3.2 for timing of measurements.*

3.3.2.1. Data Fetch in Sleep Mode

In Sleep Mode, I²C™ and SPI are used to request a measurement with a MR command and to fetch data from the digital output register using a Data Fetch (DF) command (see section 3.6.3).

As shown in Figure 3.7, after a measurement cycle is complete, valid data can be fetched. The preferred method of detecting valid data is to wait for a rise on the Ready pin (see section 3.6.6 for details on the Ready pin). If the Ready pin is not available, the user must wait for the measurements to complete before performing the DF (see section 3.2 for measurement timing). The status bits of the DF can be used to tell whether the data is valid or stale (see section 3.4 regarding the status bits), but polling for the result must not be done before the time required for conversion has elapsed.

Figure 3.7 I²C™ and SPI Data Fetching in Sleep Mode



***Note**: See section 3.2 for timing of measurements.*

3.4 Status and Diagnostics

Status bits (the two MSBs of the fetched high data byte, see Table 3.4) are provided in I²C™ and SPI but not in PDM. The status bits are used to indicate the current state of the fetched data. Diagnostic detection is available in I²C™, SPI and PDM. In I²C™ and SPI diagnostics are reported as a saturated high capacitance and temperature output (see Table 3.5). In PDM, diagnostics are reported as a railed high output level for both PDM_C (capacitive PDM) and PDM_T (temperature PDM). If a diagnostic value is reported then one or more of the errors shown in Table 3.6 occurred in normal operation.

Configuration EEPROM diagnostics are detected at initial power-up of the ZSSC3123 or a wakeup in Sleep Mode and are permanent diagnostics. All other diagnostics are detected during a measurement cycle and reported in the subsequent data fetch for I²C™ or SPI or output register update for PDM.

Table 3.4 Status Table

Status Bits (I^2C™ or SPI)	PDM Output	Definition
00_B	Clipped normal output	Valid data: Data that has not been fetched since the last measurement cycle.
01_B	Not applicable	Stale data: Data that has already been fetched since the last measurement cycle. **Note**: If a data fetch is performed before or during the first measurement after power-on reset, then Stale will be returned, but this data is actually invalid since the first measurement has not been completed.
10_B	Not applicable	Command Mode: The ZSSC3123 is in Command Mode.
11_B	Not used	Not used

Table 3.5 Diagnostic Detection

I^2C™ or SPI Output	PDM Output	Definition
Saturated output $3FFF_H$	High output (railed) level	A diagnostic has occurred in normal operation (see Table 3.6).

Table 3.6 Normal Operation Diagnostic Table

Diagnostic	Type	Definition
Configuration Error	Permanent	An EEPROM or RAM Parity Error occurred in the initial loading of the configuration registers.
RAM Parity Error	Transient	A RAM Parity Error occurred during a microcontroller instruction in the last measurement cycle.
EEPROM Error	Transient	A DED EEPROM error occurred in the last measurement cycle (see section 3.4.1).
Math Warning	Transient	An internal math overflow has occurred in the last measurement cycle and the output might be invalid.

3.4.1 EEPROM Error Detection and Correction

The contents of the EEPROM are protected via error checking and correction (ECC). Each of the 32 16-bit words contains 6 parity bits enabling single-bit error correction and double-bit error detection (SEC and DED) per word. In Command Mode both SEC and DED errors are reported in the response byte (see section 4.3). If the fetched EEPROM data has a DED error then the fetched data will be incorrect; however, if a SEC error was reported then the fetched data has been corrected, and it is the user's choice to write the data back to attempt to correct the error. During Normal Operation Mode, a diagnostic will be flagged on any DED error, but an SEC error will be automatically corrected and not flagged as a diagnostic.

3.4.2 Alarm Diagnostics

The alarm outputs do not report diagnostics. If diagnostics are needed with alarm outputs, then either digital or PDM outputs must also be used.

3.5 Output Modes

The ZSSC3123 has four different output modes as shown in Table 3.7. See the corresponding reference sections for specifics on each mode.

Table 3.7 Output Modes

Output Mode	Reference Sections
I^2C	Section 3.6
Read only SPI	
PDM	Section 3.7
Alarms	Section 3.8

As illustrated in the pin configuration in section 9, the output communication modes share pins. The Output_Selection bits in EEPROM word ZMDI_Config (see section 5.1.1) select which of these outputs will be enabled. Table 3.8 shows the pin configuration for the different output selections.

Table 3.8 Pin Assignment for Output Selections

	Output Selection			
	I^2C™ (001_B)	**SPI (011_B)**	**PDM_C (100_B)**	**PDM_C+T (110_B)**
Pin 08	Alarm_ Low	Alarm_Low	Alarm_Low	PDM_T
Pin 09	Alarm_High	Alarm_High	Alarm_High	Alarm_High
Pin 10	Ready	Ready	PDM_C	PDM_C
Pin 12	SDA	MISO	SDA	SDA
Pin 13	SCL	SCLK	SCL	SCL
Pin 14	No input	SS	No input	No Input

3.6 I^2C™ and SPI

Two wire I^2C™ and three-wire read-only SPI are available for fetching data from the ZSSC3123. I^2C™ is used to send calibration commands to ZSSC3123. To choose I^2C™ or SPI, set the corresponding Output_Selection Bits in EEPROM word ZMDI_Config.

3.6.1 I^2C™ Features and Timing

The ZSSC3123 uses an I^2C™-compatible communication protocol[‡‡] with support for 100kHz and 400kHz bit rates. The ZSSC3123 I^2C™ slave address (00_H to $7F_H$) is selected by the Device_ID bits in the Cust_Config EEPROM word (see Table 5.5 for bit assignments). The device will respond only to this address if the communication lock is set by programming 011_B in the Comm_lock bits in the ZMDI_Config EEPROM word (see Table 5.2 for bit assignments); otherwise, the device will respond to all I^2C™ addresses. The factory setting for the I^2C™ slave address is 28_H with Comm_lock set.

See Figure 3.8 for the I^2C™ timing diagram and Table 3.9 for definitions of the parameters shown in the diagram.

[‡‡] For details, refer to http://www.standardics.nxp.com/literature/books/i2c/pdf/i2c.bus.specification.pdf or other websites for this specification.

Figure 3.8 I²C™ Timing Diagram

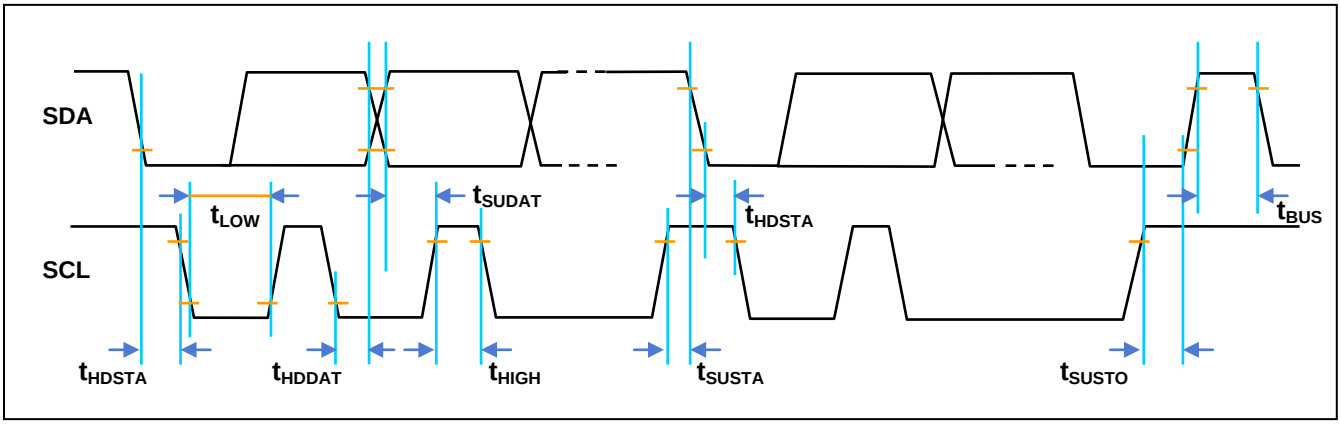


Table 3.9 I²C™ Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCL clock frequency [1)]	f_{SCL}	20		400	kHz
Start condition hold time relative to SCL edge	t_{HDSTA}	0.1			µs
Minimum SCL clock low width [2)]	t_{LOW}	0.6			µs
Minimum SCL clock high width [2)]	t_{HIGH}	0.6			µs
Start condition setup time relative to SCL edge	t_{SUSTA}	0.1			µs
Data hold time on SDA relative to SCL edge	t_{HDDAT}	0		0.5	µs
Data setup time on SDA relative to SCL edge	t_{SUDAT}	0.1			µs
Stop condition setup time on SCL	t_{SUSTO}	0.1			µs
Bus free time between stop condition and start condition	t_{BUS}	1			µs

1 *The min. frequency of 20kHz applies to calibration/test only (required to meet Command Window timing). There is no minimum for NOM.*
2 *Combined low and high widths must equal or exceed minimum SCL period.*

3.6.2 SPI Features and Timing

SPI is available only as half duplex (read-only from the ZSSC3123). SPI speeds of up to 800kHz can be supported. The SPI interface can be programmed to allow the master to sample MISO on the falling-edge or rising-edge of SCL via the SPI_Phase bit in EEPROM word Cust_Config (see Table 5.5 for bit assignments). See Figure 3.9 for the SPI timing diagram and Table 3.10 for definitions of the parameters shown in the timing diagram.

Figure 3.9 SPI Timing Diagram

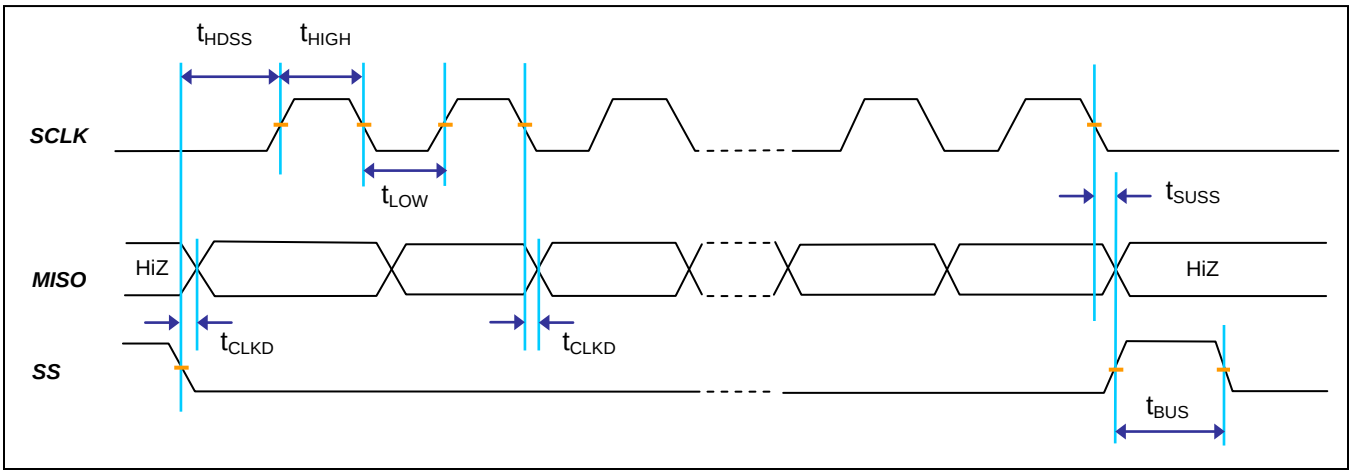


Table 3.10 SPI Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK clock frequency	f_{SCL}	50		800	kHz
SS drop to first clock edge	t_{HDSS}	2.5			µs
Minimum SCLK clock low width [1)]	t_{LOW}	0.6			µs
Minimum SCLK clock high width [1)]	t_{HIGH}	0.6			µs
Clock edge to data transition	t_{CLKD}	0		0.5	µs
Rise of SS relative to last clock edge	t_{SUSS}	0.1			µs
Bus free time between rise and fall of SS	t_{BUS}	2			µs

1 *Combined low and high widths must equal or exceed minimum SCLK period.*

3.6.3 I²C™ and SPI Commands

As detailed in Table 3.11, there are three types of commands which allow the user to interface with the ZSSC3123 in the I²C™ or SPI modes.

Table 3.11 I²C™ and SPI Command Types

Type	Description	Communication Supported	Reference Sections
Data Fetch (DF)	Used to fetch data in any digital mode	I²C™ and SPI	Section 3.6.4
Measurement Request (MR)	Used to start measurements in Sleep Mode	I²C™ and SPI	Section 3.6.5
Calibration Commands	Used in Command Mode during the calibration process	I²C™ Only	Section 4.2

3.6.4 Data Fetch (DF)

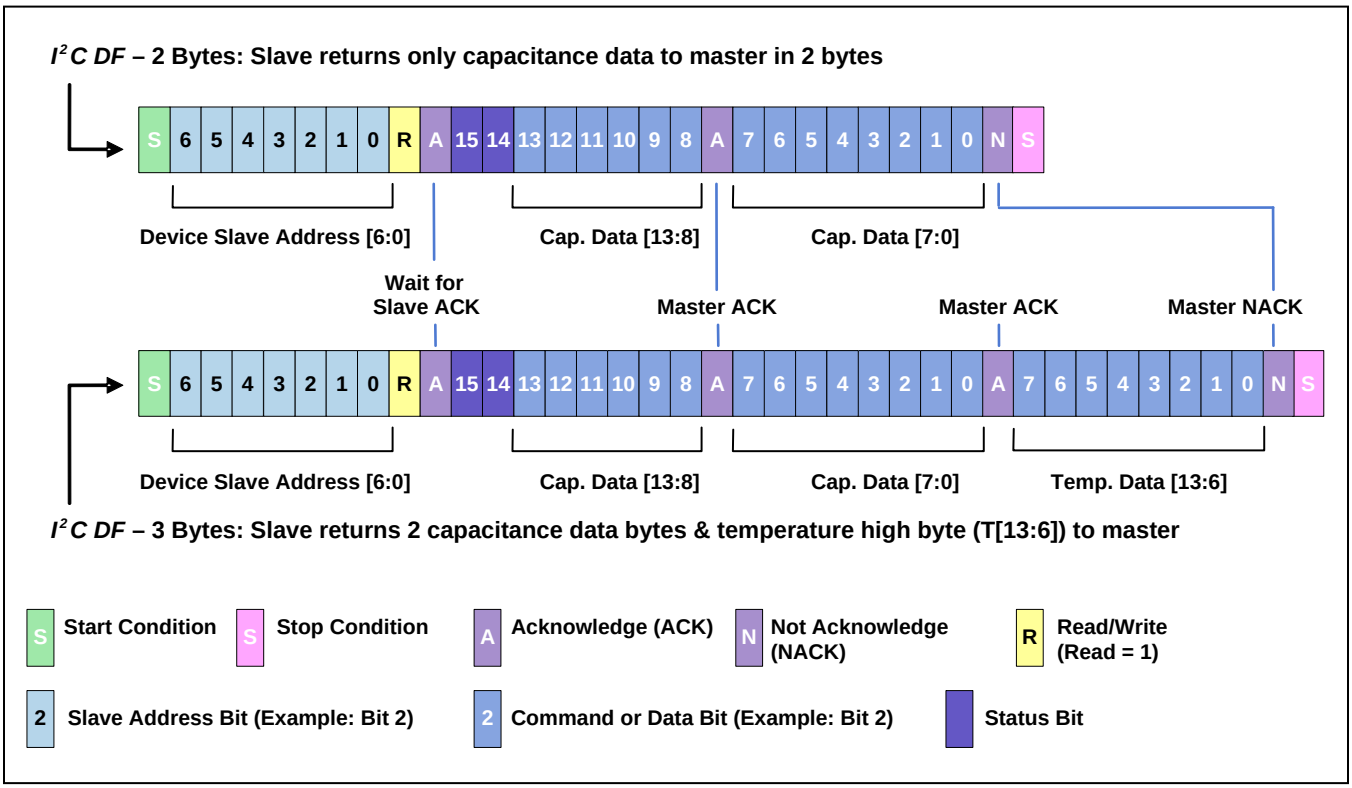
The Data Fetch (DF) command is used to fetch data in any digital output mode. With the start of communication (for I²C™ after reading the slave address; for SPI at the falling edge of SS) the entire output packet will be loaded in a serial output register. The register will be updated after the communication is finished. The output is always scaled to 14 bits independent of the programmed resolution. The ordering of the bits is big-endian.

3.6.4.1. I²C™ Data Fetch

An I²C™ Data Fetch command starts with the 7-bit slave address and the 8th bit = 1 (READ). The ZSSC3123 as the slave sends an acknowledge (ACK) indicating success. The number of data bytes returned by the ZSSC3123 is determined by when the master sends the NACK and stop condition. Figure 3.10 shows examples of fetching two and three bytes respectively. The full 14 bits of capacitive data are fetched in the first two bytes. The MSBs of the first byte are the status bits.

If temperature data is needed, additional temperature bytes can be fetched. In Figure 3.10, the three-byte data fetch returns 1 byte of temperature data (8-bit accuracy) after the capacitive data. A fourth byte can be fetched where the six MSBs of the fetched byte are the six LSBs of a 14-bit temperature measurement. The last two bits of the fourth byte are undetermined and should be masked off in the application.

Figure 3.10 I²C™ Measurement Packet Reads

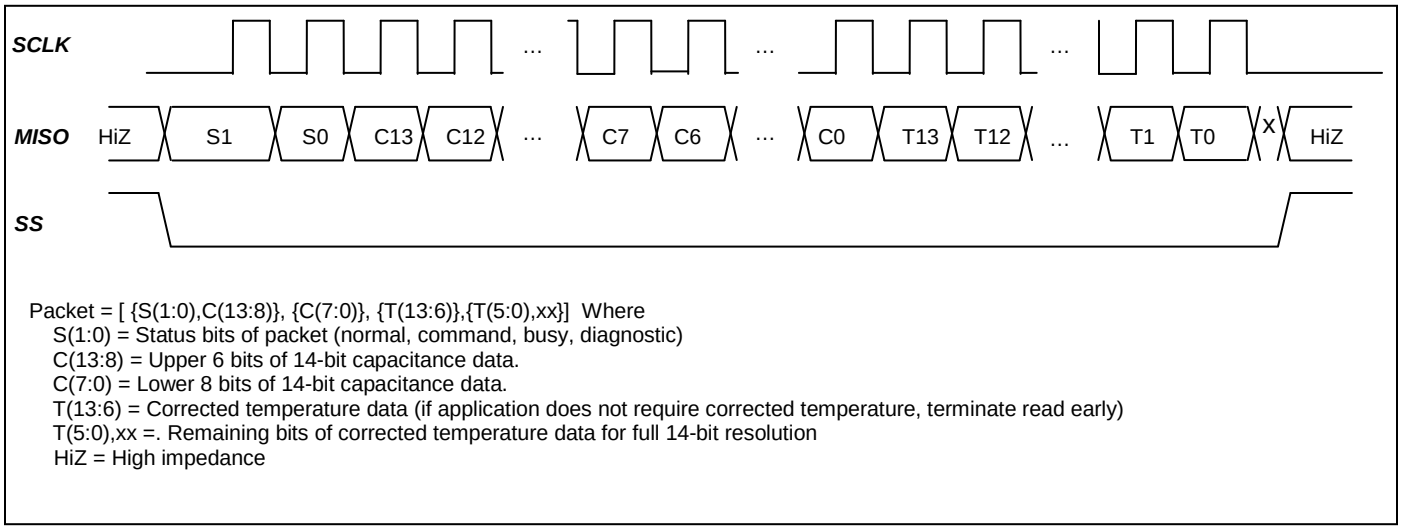


3.6.4.2. SPI Data Fetch

By default the SPI interface will have data change after the falling edge of SCLK. The master should sample MISO on the rising (opposite) edge of SCLK. This is configurable via the SPI_Phase bit in EEPROM word Cust_Config (see Table 5.5 for bit assignments). The SPI protocol can handle high and low polarity of the clock line without configuration change.

As seen in Figure 3.11 the entire output packet is 4 bytes (32 bits). The high capacitive data byte comes first, followed by the low byte. Then 14 bits of corrected temperature (T[13:0]) are sent: first the T[13:6] byte and then the {T[5:0],xx} byte. The last 2 bits of the final byte are undetermined and should be masked off in the application. If the user only requires the corrected capacitance value, the read can be terminated after the 2nd byte. If the corrected temperature is also required but only at an 8-bit resolution, the read can be terminated after the 3rd byte is read.

Figure 3.11 SPI Output Packet with Positive Edge Sampling



Packet = [{S(1:0),C(13:8)}, {C(7:0)}, {T(13:6)},{T(5:0),xx}] Where
S(1:0) = Status bits of packet (normal, command, busy, diagnostic)
C(13:8) = Upper 6 bits of 14-bit capacitance data.
C(7:0) = Lower 8 bits of 14-bit capacitance data.
T(13:6) = Corrected temperature data (if application does not require corrected temperature, terminate read early)
T(5:0),xx =. Remaining bits of corrected temperature data for full 14-bit resolution
HiZ = High impedance

3.6.5 Measurement Request (MR)

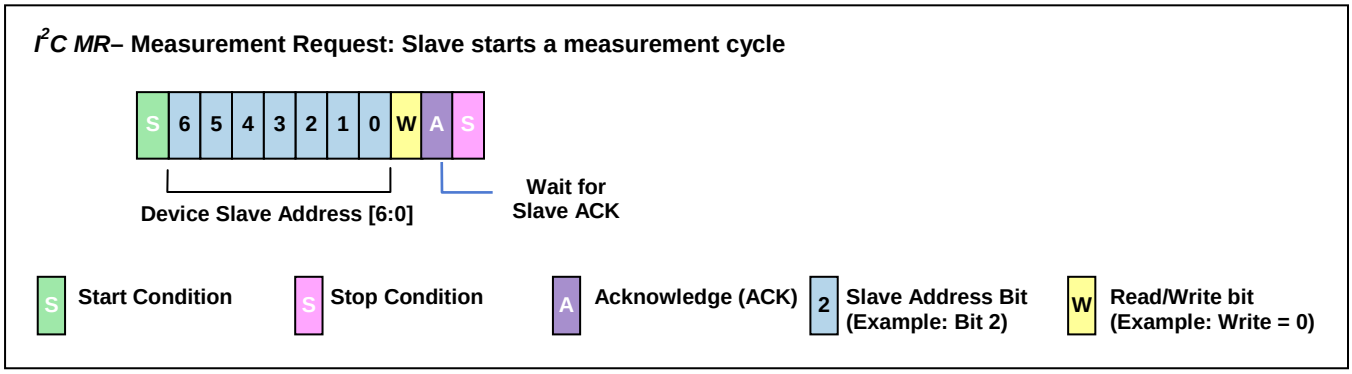
A measurement request (MR) is a Sleep-Mode-only command sent by the master to wake up the ZSSC3123 and start a new measurement cycle in both I²C™ and SPI modes. See section 3.3.2 for more information on Sleep Mode.

3.6.5.1. I²C™ Measurement Request

The I²C™ MR is used to wake up the device in Sleep Mode and start a complete measurement cycle starting with a temperature measurement, followed by a capacitance measurement, followed by the DSP calculations, and then the results are written to the digital output register. As shown in Figure 3.12, the communication contains only the slave address and the WRITE bit (0) sent by the master. After the ZSSC3123 responds with the slave ACK, the master creates a stop condition.

Note: The I²C™ MR function can also be accomplished by sending “don’t care” data after the address instead of immediately sending a stop bit.

Figure 3.12 I²C™ MR

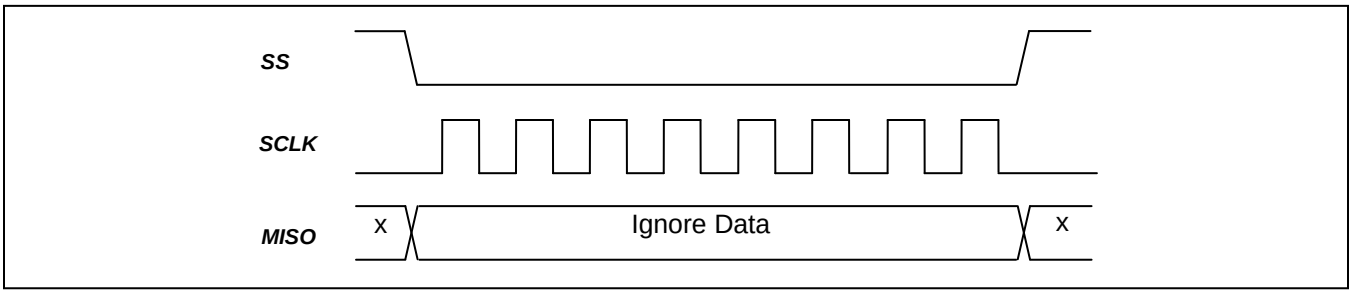


3.6.5.2. SPI Measurement Request

The SPI MR is used to wake up the device in Sleep Mode and start a complete measurement cycle starting with a temperature measurement/temperature DSP calculation, followed by a capacitance measurement / capacitance DSP calculations, and then the results are written to the digital output register. As shown in Figure 3.13, executing an SPI MR command is a read of 8 bits, ignoring the data that is returned.

Note: The SPI MR function can also be accomplished by performing a full SPI Data Fetch (see section 3.6.4.2) and ignoring the invalid data that will be returned.

Figure 3.13 SPI MR



3.6.6 Ready Pin

A rise on the Ready pin indicates that new data is ready to be fetched from either the I²C™ or SPI interface. The Ready pin stays high until a Data Fetch (DF) command is sent (see section 3.6.3); it stays high even if additional measurements are performed before the DF. In Sleep Mode, sending a Measurement Request (MR) command resets the Ready pin.

The Ready pin's output driver type is selectable as either full push-pull or open drain via the Ready_Open_Drain bit in EEPROM word Cust_Config (see Table 5.5 for bit assignments and settings). Point-to-point communication most likely uses the full push-pull driver. If an application requires interfacing to multiple parts, then the open drain option can allow for just one wire and one pull-up resistor to connect all the parts in a bus format.

3.7 PDM (Pulse Density Modulation)

PDM outputs for both corrected capacitance and temperature are available. PDM_C (capacitance PDM) appears on the READY/PDM_C pin, and PDM_T (temperature PDM) appears on the ALARM_LOW/PDM_T pin if enabled using the Output_Selection bits (see Table 5.2). The PDM frequency is 231.25kHz ± 10% (i.e., the oscillator frequency 1.85MHz ± 10% divided by 8). Both PDM signals are 14-bit values. In PDM Mode, the ZSSC3123 must be programmed to Update Mode (see section 3.3.1). Every time a conversion cycle has finished, the PDM will begin outputting the new value.

An analog output value is created by low-pass filtering the output; a simple first-order RC filter will work in this application.

Select the time constant of the filter based on the requirements for settling time and/or peak-to-peak ripple.

Important: The resistor of the RC filter must be ≥10kΩ.

Table 3.12 shows some filter examples using a 10kΩ resistor.

Table 3.12 Low Pass Filter Example for R = 10kΩ

Filter Capacitance (nF)	PDM_C		Desired Analog Output Resolution
	VPP Ripple (mV/V)	0 to 90% Settling Time (ms)	
100	4.3	2.3	8
400	1.0	9.2	10
1600	0.3	36.8	12
6400	0.1	147.2	14

For a different (higher) resistor, the normalized ripple VPP[mV/V] can be calculated as

$$VPP[mV/V] = \frac{4324}{(R[k\Omega] * C[nF])} \quad (14)$$

or the settling time t_{SETT} for a 0% to 90% settling can be calculated as

$$t_{SETT}[ms] = 0.0023 * R[k\Omega] * C[nF] \quad (15)$$

ZSSC3123 provides high and low clipping limits for the PDM output. EEPROM words PDM_Clip_High and PDM_Clip_Low (EEPROM registers 16_{HEX} and 17_{HEX}; see Table 5.1) are the 14-bit high and low clipping limit registers respectively. The 14-bit values map directly to the output of the IC and can be calculated as

$$PDM\_Clip = ROUND\left(\frac{2^{14} * clip\_level\_\%}{100}\right) \quad (16)$$

These registers apply to both PDM_C and PDM_T. Since diagnostics are reported in the PDM pin (see section 3.4), clipping limits allow diagnostics to be differentiated from the normal output. For detection of the diagnostic signal, a PDM_Clip_High limit of 97.5% ($3E66_{HEX}$) or lower is recommended.

Important: The default values for the high and low clipping limits (00_{HEX}) are not compatible with PDM output, so the clipping limits must be changed if the PDM output is used. Otherwise, the PDM output will not work as expected. If the PDM output is not used, it is important to retain the default values of 00_{HEX} for the clipping limits.

3.8 Alarm Output

The alarm output can be used to monitor whether a corrected capacitance reading has exceeded or fallen below pre-programmed values. The alarm can be used to drive an open-drain load connected to VDD, as demonstrated in section 7.2, or it can function as a full push-pull driver. If a high voltage application is required, external devices can be controlled with the Alarm pins, as demonstrated in section 7.3.

The two alarm outputs can be used at the same time, and these alarms can be used in combination with any of the other three modes; I²C™, SPI, or PDM.

Note: When both PMD_C and PDM_T are selected only Alarm_High is available (see section 3.5).

The alarm outputs are updated when a conversion cycle is completed. The alarm outputs can be used in both Update Mode and Sleep Mode, but if Sleep Mode is used, I²C™ or SPI must also be used to control the measurements (see section 3.3).

3.8.1 Alarm Registers

Four registers are associated with the alarm functions: Alarm_High_On, Alarm_High_Off, Alarm_Low_On, and Alarm_Low_Off (see Table 5.1 for EEPROM addresses). Each of these four registers is a 14-bit value that determines where the alarms turn on or off. The two high alarm registers form the output with hysteresis for the Alarm_High pin, and the two low alarm registers form the output with hysteresis for the Alarm_Low pin. Each of the two alarm pins can be configured independently using Alarm_Low_Cfg and Alarm_High_Cfg located in EEPROM word Cust_Config (see Table 5.5 for bit assignments).

Note: If two high alarms or two low alarms are needed, see section 3.8.4.

3.8.2 Alarm Operation

As shown in Figure 3.14, the Alarm_High_On register determines where the high alarm trip point is and the Alarm_High_Off register determines where the high alarm turns off if the high alarm has been activated. The high alarm hysteresis value is equal to Alarm_High_On – Alarm_High_Off. The same is true for the low alarm where Alarm_Low_On is the low alarm trip point with Alarm_Low_Off determining the alarm shut off point. The low alarm hysteresis value is equal to Alarm_Low_Off – Alarm_Low_On. Figure 3.15 shows output operation flowcharts for both the Alarm_High and Alarm_Low pins.

Figure 3.14 Example of Alarm Function

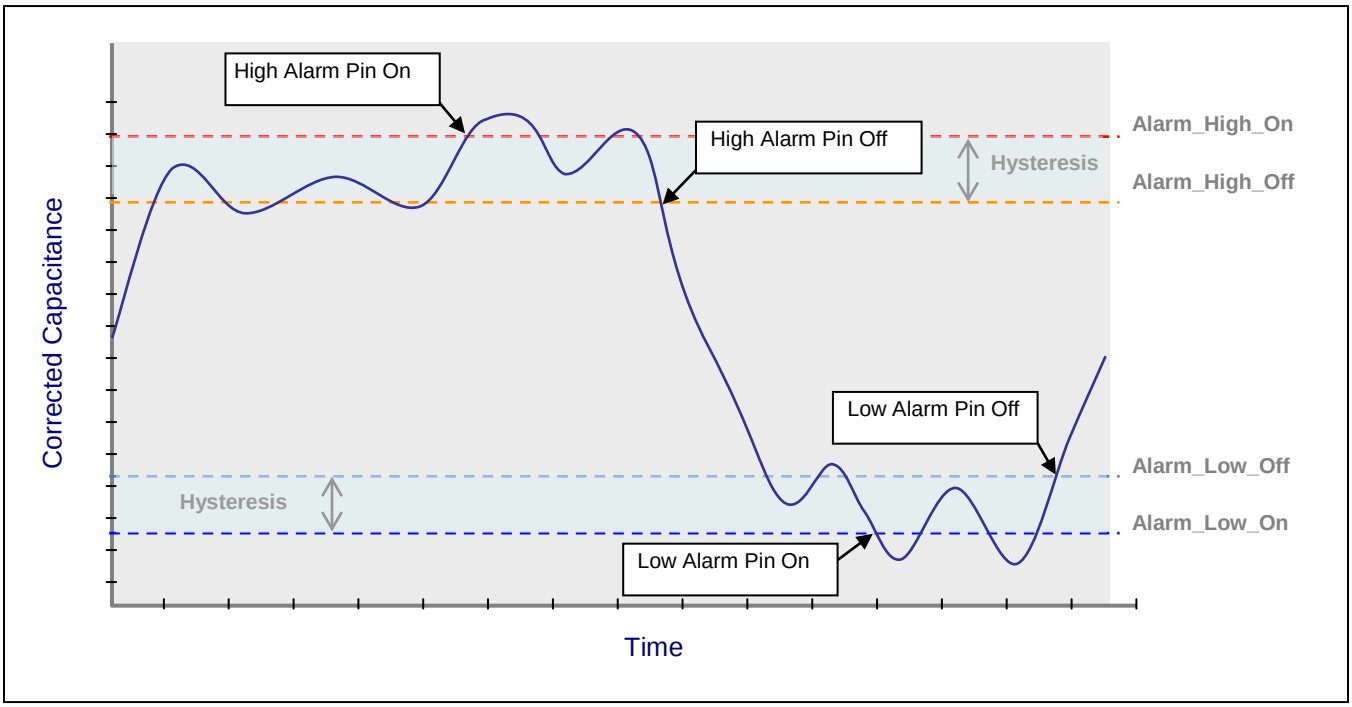
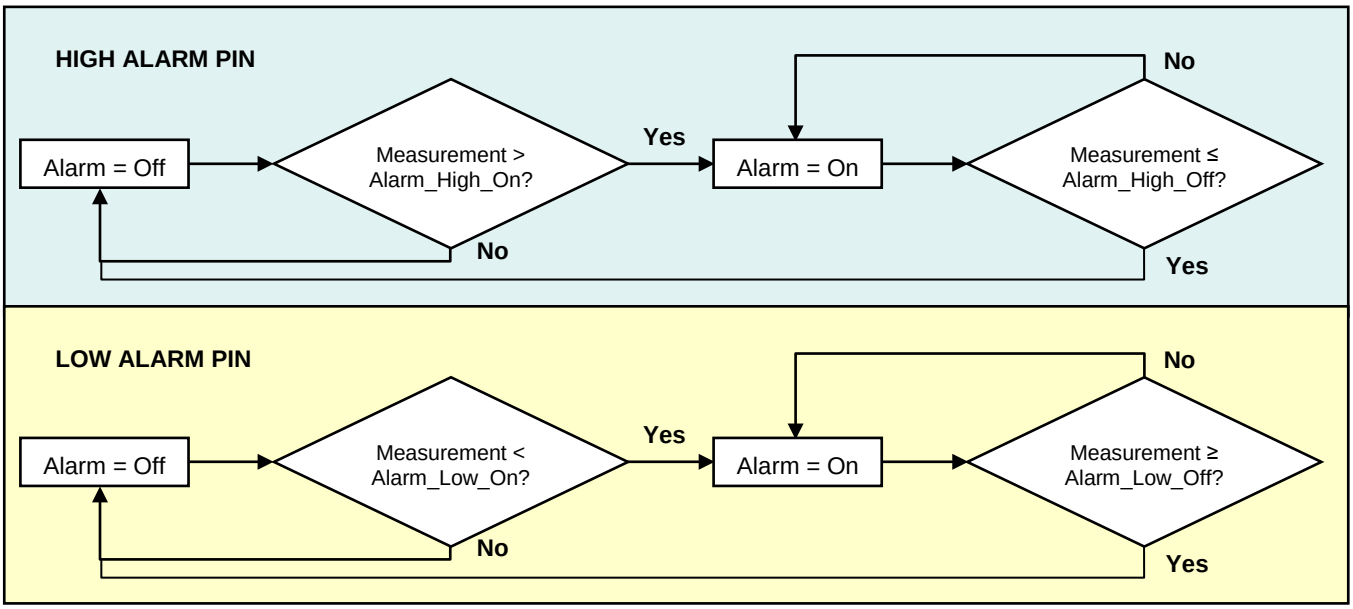


Figure 3.15 Alarm Output Flow Chart



3.8.3 Alarm Output Configuration

The user can select the output driver configuration for each alarm using the Output Configuration bit in the Alarm_High_Cfg and Alarm_Low_Cfg registers in EEPROM word Cust_Config (see Table 5.5 for bit assignments). For applications, such as interfacing with a microcontroller or controlling an external device (as seen in section 7.3), select the full push-pull driver for the alarm output type. For an application that directly drives a load connected to VDD, as demonstrated in section 7.2, the typical selection is the open-drain output type.

An advantage of making an alarm output open drain is that in a system with multiple devices, the alarm outputs of each ZSSC3123 can be connected together with a single pull-up resistance so that one can detect an alarm on any device with a single wire.

3.8.4 Alarm Polarity

For both alarm pins, the polarity of the alarm output is selected using the Alarm Polarity bit in the Alarm_High_Cfg and Alarm_Low_Cfg registers in EEPROM word Cust_Config (see Table 5.5 for bit assignments). As shown in the example in section 7.3, the alarms can be used to drive a high voltage humidity control system. Since the humidifier or dehumidifier relays must be on when the alarms are on, the alarm polarity bits are set to 0 (active high). In the example given in section 7.2, an alarm is used to turn on an LED in an open drain configuration. In order for the LED to be on when the alarm is on, the output must be low, so the alarm polarity bit is set to 1 (active low).

Another feature of the polarity bits is the ability to create two high alarms or two low alarms. For example, with applications requiring two high alarms, flip the polarity bit of the Alarm_Low pin, and it will act as a high alarm. However, in this case, the effect of the alarm low registers is also changed: the Alarm_Low_On register would act like the Alarm_High_Off register and the Alarm_Low_Off register would act like the Alarm_High_On register. The same can be done to achieve two low alarms: the Alarm_High pin would have the polarity bit flipped, and the two Alarm_High registers would have opposite meanings.

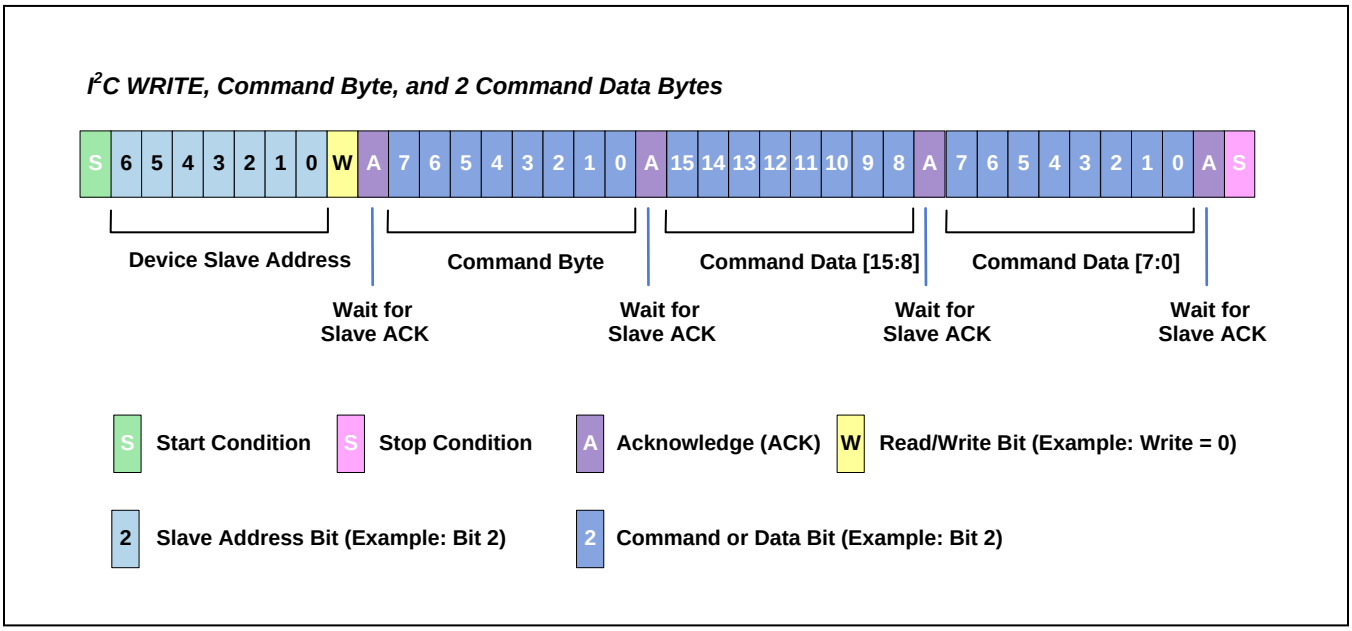
4 Command Mode

Command Mode is primarily used for calibrating the ZSSC3123. Command Mode is entered by sending a Start_CM during the command window (see section 3.1 for more details on how to enter Command Mode). In Command Mode, a set of commands are available to the user to calibrate the part (see Table 4.1).

4.1 Command Format

Command Mode commands are only supported for the I²C™ protocol. As shown in Figure 4.1, commands are 4-byte packets with the first byte being a 7-bit slave address followed by 0 for write. The second byte is the command byte and the last two bytes form a 16-bit data field.

Figure 4.1 I²C™ Command Format



4.2 Command Encodings

Table 4.1 describes all the commands that are offered in Command Mode.

Note: Only the commands listed in Table 4.1 are valid. Other encodings might cause unpredictable results. If data is not needed for the command, zeros must be supplied as data to complete the 4-byte packet.

Table 4.1 Command List and Encodings

Command Byte 8 Command Bits (Hex)	Third and Fourth Bytes 16 Data Bits(Hex)	Description	Response Time [§§]
00_H to $1F_H$	0000_H	EEPROM Read of addresses 00_H to $1F_H$ After this command has been sent and executed, a data fetch must be performed (see section 3.6.4).	100µs
40_H to $5F_H$	$YYYY_H$ (Y = data)	Write to EEPROM addresses 00_H to $1F_H$ The 2 bytes of data sent will be written to the address specified in the 6 LSBs of the command byte.	12ms
80_H	0000_H	Start_NOM Ends Command Mode and transitions to Normal Operation Mode.	Length of initial conversions depends on temperature and capacitance resolution settings and the capacitance “mult” setting (see section 3).
$A0_H$	0000_H	Start_CM Start Command Mode: used to enter the command interpreting mode. Start_CM is only valid during the power-on command window (see section 3.1).	100µs
$B0_H$	0000_H	Get Revision Get the revision of the part. After this command has been sent and executed, a data fetch must be performed (see section 3.6.4).	100µs

4.3 Command Response and Data Fetch

After a command has been sent and the execution time defined in Table 4.1 has expired, an I^2C™ Data Fetch (DF) can be performed to fetch the response. As shown in Figure 4.2, after the slave address has been sent, the first byte fetched is the response byte. The upper two status bits will always be 10_B to represent Command Mode (see section 3.4). The lower two bits are the response bits. Table 4.2 describes the different responses that can be fetched.

[§§] All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

To determine if a command has finished executing, poll the part until a Busy response is no longer received. The middle four bits of the response byte are command diagnostic bits where each bit represents a different diagnostic (see Table 4.3). For more information on EEPROM errors see section 3.4.1.

Note: Regardless of what the response bits are, one or more of the diagnostic bits may be set indicating an error occurred during the execution of the command.

Note: Only one command can be executed at a time. After a command is sent another command must not be sent until the execution time of the first command defined in Table 4.1 has expired.

For all commands except EEPROM Read and Get Revision, the data fetch should be terminated after the response byte is read. If the command was a Get Revision, then the user will fetch a one byte Revision as shown in Figure 4.2, example 2. The revision is coded with the upper nibble being the letter corresponding to a full layer change and the lower nibble being the metal change number, for example A0. If the command was an EEPROM Read, then the user will fetch two more bytes as shown in Figure 4.2, example 3. If a Corrected EEPROM Error diagnostic was flagged after an EEPROM read, the user has the option to write this data back to attempt to fix the error.

Instead of polling to determine if a command has finished executing, the user can use the Ready pin. In this case, wait for the Ready pin to rise, which indicates that the command has executed. Then a data fetch can be performed to get the response and data (see Figure 4.2). See section 3.6.6 for more information on the Ready pin.

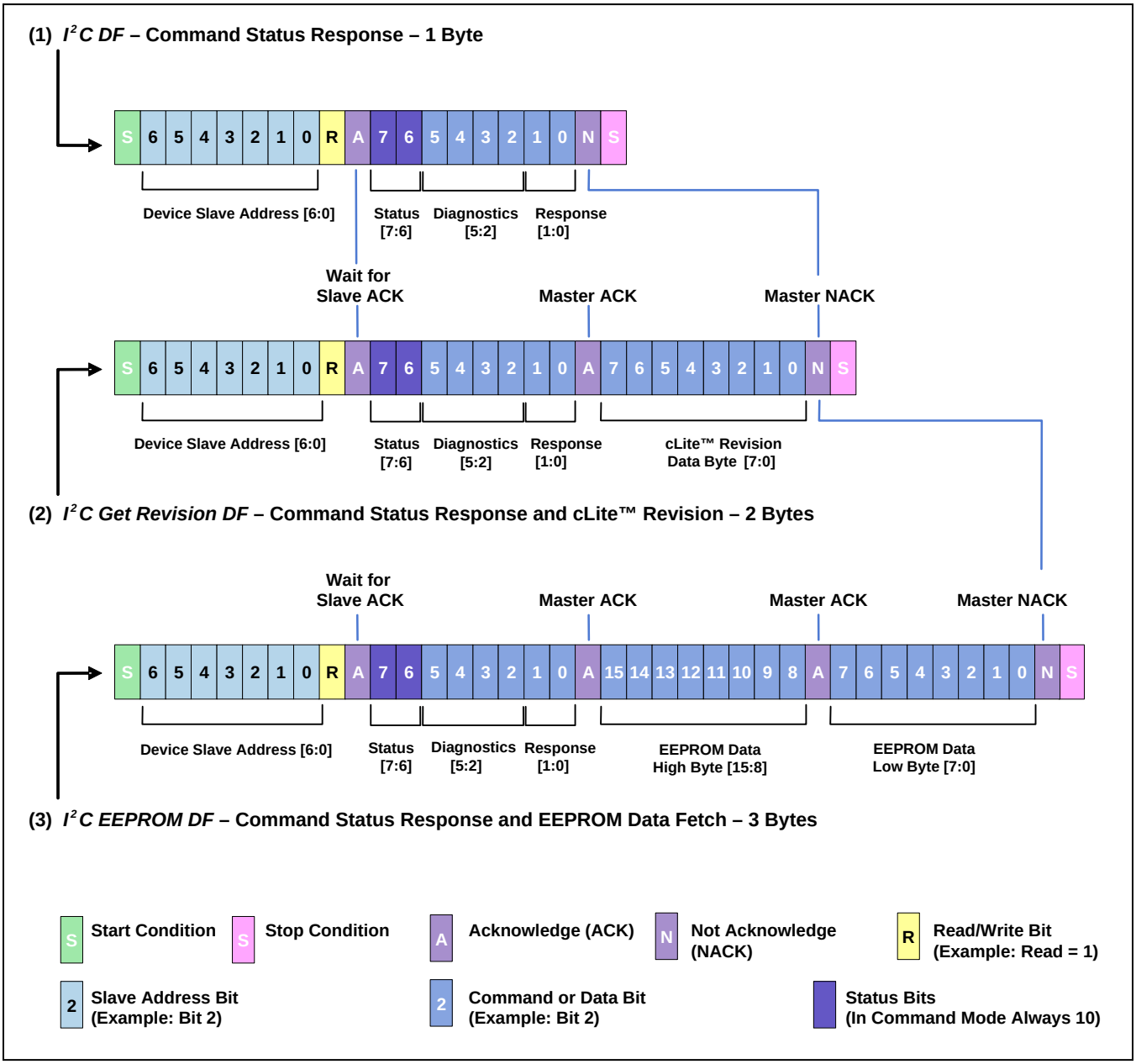
Table 4.2 Response Bits

Encoding	Name	Description
00_B	Busy	The command is busy executing.
01_B	Positive Acknowledge	The command executed successfully.
10_B	Negative Acknowledge	The command was not recognized or an EEPROM write was attempted while the EEPROM was locked.

Table 4.3 Command Diagnostic Bits

Bit Position	Name	Description
2	Corrected EEPROM Error	A corrected EEPROM error occurred in execution of the last command.
3	Uncorrectable EEPROM Error	An uncorrectable EEPROM error occurred in execution of the last command.
4	RAM Parity Error	A RAM parity error occurred during a microcontroller instruction in the execution of the last command.
5	Configuration Error	An EEPROM or RAM parity error occurred in the initial loading of the configuration registers.

Figure 4.2 Command Mode Data Fetch



5 EEPROM

The EEPROM array contains the calibration coefficients for gain and offset, etc., and the configuration bits for the analog front end, output modes, measurement modes, etc. The ZSSC3123 EEPROM is arranged as 32 16-bit words (see Table 5.1). The EEPROM is divided into two sections. Words 0_H to 15_H can only be written to if the EEPROM is unlocked. After the EEPROM is locked these locations can no longer be written to. The EEPROM lock bits are in the ZMDI_Config register (see Table 5.2 for the bit assignment). Words 16_H to $1F_H$ (highlighted blue in Table 5.1) are always unlocked and available to write to at all times. See section 4 for instructions on reading and writing to the EEPROM in Command Mode via the I²C™ interface. When programming the EEPROM, an internal charge pump voltage is used; therefore a high voltage supply is not needed.

Note: If the EEPROM was accidentally locked, it can be unlocked with the following instructions (see section 4 for how to send commands).

1. Enter Command Mode with a Start_CM command.
2. Send an $A2_H$ for the command byte and 0000_H for the command data.
3. Send an $F0_H$ for the command byte and 0021_H for the command data.
4. Clear the EEPROM_Lock bits in the ZMDI_Config register with an EEPROM Write command.
5. Reset the part.

There are four Customer_ID words available for customer use, two in the locked region and two in the unlocked region. They can be used as a customer serial number for module traceability. (see Table 5.1 for Customer_ID EEPROM addresses.) The integrity of the contents of the EEPROM array is ensured via ECC (see section 3.4.1).

Table 5.1 provides a summary of the EEPROM contents. The configuration register bits are explained in detail in the following subsections.

Table 5.1 EEPROM Word Assignments

EEPROM Word	Bit Range	IC Default	Name	Description and Notes
00_H	15:0	$XXXX_H$	Cust_ID0	Customer ID byte 0: For use by customer (default value is the upper 16 bits of the lot number)
01_H	15:0	$XXXX_H$ ($LLLLLLLL_B$ $0000ssss_B$)	Cust_ID1	Customer ID byte 1: For use by customer (default value is the lower 8 bits of the lot number and an 8 bit wafer number)
02_H	15:0	$0B00_H$	ZMDI_Config	IDT Configuration Register (See section 5.1.1)
03_H	15:0	0006_H	Not Available	**Do Not Change**; must leave at factory settings
04_H	15:0	$00FT_H$	Not Available	**Do Not Change**; must leave at factory settings***
05_H	15:0	0000_H	Not Available	**Do Not Change**; must leave at factory settings
06_H	15:0	$0C06_H$	C_Config	AFE Capacitance Configuration Register: See Table 5.3.
07_H	15:0	0000_H	SOT_tco	2nd order temperature offset correction for capacitance
08_H	15:0	0000_H	Tco	Temperature offset correction for capacitance
09_{HH}	15:0	0000_H	SOT_tcg	2nd order temperature gain correction for capacitance
$0A_H$	15:0	0000_H	Tcg	Temperature gain correction for capacitance

*** The T in the default setting for EEPROM word 04_H represents the custom trim value determined by final test. Do not change this setting.

EEPROM Word	Bit Range	IC Default	Name	Description and Notes
$0B_H$	15:0	0000_H	Offset	Offset correction for capacitance
$0C_H$	15:0	2000_H	Gain_1	Gain correction for capacitance (region 1)
$0D_H$	15:0	0000_H	SOT_1	2nd order correction for capacitance (region 1)
$0E_H$	15:0	2000_H	Gain_2	Gain correction for capacitance (region 2)
$0F_H$	15:0	0000_H	SOT_2 Or TOT_1	2nd order correction for capacitance (region 2) alternatively 3rd order correction (only one region)
10_H	15:0	$7FFF_H$	Raw_Break	Break point dividing region 1 from region 2
11_H	15:0	$8D92_H$	T_Config	AFE Temperature Configuration Register (See Table 5.4)
12_H	15:0	0000_H	Offset_T	Offset correction for temperature
13_H	15:0	2000_H	Gain_T	Gain correction for temperature
14_H	15:0	0000_H	SOT_T	2nd order correction for temperature
15_H	15:0	0000_H	T_{REF}	Raw temperature reading reference point
16_H	13:0	0000_H	PDM_Clip_High	PDM high clipping limit (keep at zero unless PDM is enabled; must change default if PDM is used)
17_H	13:0	0000_H	PDM_Clip_Low	PDM low clipping limit (keep at zero unless PDM is enabled; may be changed if PDM is used)
18_H	13:0	$3FFF_H$	Alarm_High_On	High alarm on trip point
19_H	13:0	$3FFF_H$	Alarm_High_Off	High alarm off trip point
$1A_H$	13:0	0000_H	Alarm_Low_On	Low alarm on trip point
$1B_H$	13:0	0000_H	Alarm_Low_Off	Low alarm off trip point
$1C_H$	15:0	0028_H	Cust_Config	Customer Configuration Register (See section 5.1.4.)
$1D_H$	15:0	0000_H	Not Available	**Do Not Change**; must leave at factory settings
$1E_H$	15:0	$XXXX_H$	Cust_ID2	Customer ID byte 2: For use by customer (default value is the 8 bit x and 8 bit y coordinates on the wafer)
$1F_H$	15:0	0000_H	Cust_ID3	Customer ID byte 3: For use by customer

5.1.1 IDT Configuration Register (ZMDI_Config, EEPROM Word 02_{HEX})

This register is loaded at power-on reset and upon exiting Command Mode using a Start_NOM command.

Table 5.2 ZMDI_Config Bit Assignments

Bit Range	IC Default	Name	Description and Notes
0	0_B	Measurement_Mode	0 = Update Mode 1 = Sleep Mode
2:1	00_B	Power_Down_Period	Power Down Period: ††† 00_B = 0ms 01_B = 5ms 10_B = 25ms 11_B = 125ms
3	0_B	Scale_Sot_Tc	Scales the SOT TC Terms: 0 = Scale x 1 1 = Scale x 2
4	0_B	Gain4x_C	Multiply Gain_1 and Gain_2 by 0 = multiply by 1 1 = multiply by 4
7:5	000_B	EEPROM_lock	011_B = locked All other = unlocked When EEPROM is locked, the internal charge pump is disabled and the EEPROM can no longer be programmed. **Note:** If the EEPROM was accidentally locked, see section 5 for instructions for unlocking it.
10:8	011_B	Comm_lock	011_B = locked All other = unlocked When communication is locked, I^2C™ communication will only respond to its programmed address. Otherwise if communication is unlocked, I^2C™ will respond to any address.

††† All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

Bit Range	IC Default	Name	Description and Notes
13:11	001_B	Output_Selection	001_B = I^2C™ 011_B = SPI 100_B = PDM Capacitance (+ 2 alarms) 110_B = PDM Capacitance + Temperature (+ 1 alarm) All other configurations are not allowed See Table 3.8 for more details.
14	0_B	Third_order	0 = Piece-wise linear calibration with breakpoint 1 = Third-order calibration
15	0_B	Not Available	**Do Not Change** – must leave at factory settings

5.1.2 Capacitance Analog Front End Configuration (C_Config, EEPROM Word 06_{HEX})

This register is loaded immediately before a capacitance measurement is taken, so a power cycle is not needed for changes to take effect.

Table 5.3 C_Config Bit Assignments

Bit Range	IC Default	Name	Description and Notes
2:0	110_B	CDC_Reference	CDC reference capacitor selection (see Table 2.2)
5:3	000_B	CDC_Offset	CDC offset capacitor selection (see Table 2.2)
9:6	0000_B	Not Available	**Do Not Change** – must leave at factory settings
11:10	11_B	Resolution	CDC resolution and sample rate: ‡‡‡ 00_B = 8 bits at 0.7 ms rate 01_B = 10 bits at 1.6 ms rate 10_B = 12 bits at 5.0 ms rate 11_B = 14 bits at 18.5 ms rate
13:12	00_B	CDC_Mult Not Available	CDC Multiplier: 00_B = 1 (2pF to 8pF) 01_B = 2 (8pF to 32pF) 10_B = 4 (32pF to 130pF) 11_B = 8 (130pF to 260pF)

‡‡‡ All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%). See section 3.2 for additional timing factors.

Bit Range	IC Default	Name	Description and Notes
14	0_B	Differential	Differential input capacitance selection: 0 = Single-ended 1 = Differential
15	0_B	Not Available	**Do Not Change** – must leave at factory settings

5.1.3 Temperature Analog Front End Configuration (T_Config, EEPROM Word 11_{HEX})

This register is loaded immediately before a capacitance measurement is taken, so a power cycle is not needed for changes to take effect.

Table 5.4 T_Config Bit Assignments

Bit Range	IC Default	Name	Description and Notes
2:0	010_B	CDC_Reference	CDC reference capacitor selection. The factory settings are set for a full span temperature range from -40°C to +125°C. **Note:** Do not change this setting from the factory setting unless a different temperature range is needed.
5:3	010_B	CDC_Offset	CDC offset capacitor selection. The factory settings are set for a full span temperature range from -40°C to +125°C. **Note:** Do not change this setting from the factory setting unless a different temperature range is needed.
8:6	110_B	Temp_Trim	Trim setting used for the temperature measurement. The factory settings are set for a full span temperature range from -40°C to +125°C. **Note:** Do not change this setting from the factory setting unless a different temperature range is needed.
9	0_B	Not Available	**Do Not Change** – must leave at factory settings
11:10	11_B	Resolution	Temperature resolution and sample rate: §§§ 00_B = 8 bits at 0.7 ms rate 01_B = 10 bits at 1.6 ms rate 10_B = 12 bits at 5.0 ms rate 11_B = 14 bits at 18.5 ms rate
15:12	1000_B	Not Available	**Do Not Change** – must leave at factory settings

§§§ All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

5.1.4 Customer Configuration Register (Cust_Config, EEPROM Word $1C_{HEX}$)

This register is loaded at power-on reset and upon exiting Command Mode after receiving a Start_NOM command.

Table 5.5 Cust_Config Bit Assignments

<table>
<tr><th>Bit Range</th><th>IC Default</th><th>Name</th><th>Description and Notes</th></tr>
<tr><td>6:0</td><td>0101000_B</td><td>Device_ID</td><td>I²C™ slave address</td></tr>
<tr><td>8:7</td><td>00_B</td><td>Alarm_Low_Cfg</td><td>Configure the Alarm_Low output pin:
<table><tr><th>Bits</th><th>Description</th></tr><tr><td>7</td><td>Alarm Polarity:
0 = Active High
1 = Active Low</td></tr><tr><td>8</td><td>Output Configuration:
0 = Full push-pull
1 = Open drain</td></tr></table></td></tr>
<tr><td>10:9</td><td>00_B</td><td>Alarm_High_Cfg</td><td>Configure the Alarm_High output pin:
<table><tr><th>Bits</th><th>Description</th></tr><tr><td>9</td><td>Alarm Polarity:
0 = Active High
1 = Active Low</td></tr><tr><td>10</td><td>Output Configuration:
0 = Full push-pull
1 = Open drain</td></tr></table></td></tr>
<tr><td>11</td><td>0_B</td><td>SPI_Phase</td><td>The edge of SCLK that the master samples MISO on:
0 = positive edge
1 = negative edge</td></tr>
<tr><td>12</td><td>0_B</td><td>Ready_Open_Drain</td><td>Ready pin is
0 = Full push-pull
1 = Open drain</td></tr>
<tr><td>13</td><td>0_B</td><td>Fast_Startup</td><td>Sets the Command Window length:
0 = 10 ms Command Window
1 = 3 ms Command Window</td></tr>
<tr><td>15:14</td><td>00_B</td><td>Not Available</td><td>Do Not Change – must leave at factory settings</td></tr>
</table>

6 Calibration and Signal Conditioning Math

IDT can provide software and hardware with samples to perform the calibration. For a complete description and detailed examples, see *ZSSC3122/ZSSC3123_SSC_Modular_Evaluation_Kit_Description_RevX_xy.pdf*. For more details on the following equations, refer to *ZSSC3123 Technical Note—Detailed Equations for ZSSC3123 Rev C Silicon Math* (available on request).

Note For best results the calibration should be done with all settings set to the final application including supply voltage, measurement mode, update rate, output mode, resolution, and AFE settings in the final packaging.

6.1 Capacitance Signal Conditioning

The ZSSC3123 supports up to a two-region piece-wise, non-linear sensor input or a third-order correction selectable. The general form of the capacitance signal conditioning equation is provided below.

Note: The following equations are only meant to show the general form and capabilities of the ZSSC3123 sensor signal conditioning.

Two-region piece-wise, non-linear sensor input

$$RawTC = \frac{Raw\_C + OFFSET + \Delta T * (Tco + \Delta T * SOT\_tco)}{1 + \Delta T * (Tcg + \Delta T * SOT\_tcg)} \quad (17)$$

$$Raw_1 = MIN(RawTC, Raw\_Break) \quad (18)$$

$$Raw_2 = MAX(0, RawTC - Raw\_Break) \quad (19)$$

$$Out = SOT\_1 * (Gain\_1 * Raw_1)^2 + Gain\_1 * Raw_1 + SOT\_2 * (Gain\_2 * Raw_2)^2 + Gain\_2 * Raw_2 \quad (20)$$

Or alternatively

Non-linear sensor input up to third-order correction

$$Raw_1 = \frac{Raw\_C + OFFSET + \Delta T * (Tco + \Delta T * SOT\_tco)}{1 + \Delta T * (Tcg + \Delta T * SOT\_tcg)} \quad (21)$$

$$Out = TOT\_1 * (Gain\_1 * Raw_1)^3 + SOT\_1 * (Gain\_1 * Raw_1)^2 + Gain\_1 * Raw_1 \quad (22)$$

Where:

Symbol	Description
Raw_C	Raw sensor reading.
RawTC	Temperature corrected raw value.
Raw_1	Raw value to be used for region 1 correction.
Raw_2	Raw value used for region 2 correction.
Raw_Break	Raw value at which the transition from region 1 to region 2 occurs.
Offset	Offset correction for sensor applied at 50% full scale input.
Gain_1	Gain correction for sensor applied to region 1.
SOT_1	Second-order correction for sensor region 1.
Gain_2	Gain correction for sensor applied to region 2 – not used if only 1 region is used.
SOT_2 alternatively TOT_1	Second-order correction for sensor region 2 – not used if only 1 region is used. Used as third-order term TOT_1 for third-order correction.
Tco	Correction for offset drift due to temperature.
Tcg	Correction for sensitivity (gain) change due to temperature.
SOT_tco	Second-order correction for offset drift due to temperature.
SOT_tcg	Second-order correction for sensitivity change due to temperature.
T_{REF}	Raw temperature reading used as a reference temperature for the removal of all TC components.
ΔT	Difference between current raw temperature and the reference temperature.
OUT	Corrected capacitance output value.

6.2 Temperature Signal Compensation

Temperature is measured internally. Temperature correction contains both linear gain and offset terms as well as a second-order term to correct for any nonlinearity.

Note: The following equation is only meant to show the general form and capabilities of the internal ZSSC3123 temperature signal conditioning.

$$T = SOT\_T * (Raw\_T)^2 + Gain\_T * Raw\_T + Offset\_T \quad (23)$$

Where:

Symbol	Range	Description
Raw_T	[0,16383]	Raw temperature reading
Gain_T	[-32768,32767]	Gain correction for internal temperature
Offset_T	[-32768,32767]	Offset correction for internal temperature
SOT_T	[-32768,32767]	Second-order correction for internal temperature
T	[-32768,32767]	Corrected temperature output value

6.3 Limits on Coefficient Ranges

There are range limits on some of the calibration coefficients that will be enforced by the calibration routine provided by IDT. These limits ensure the integrity of the internal calculations and would only limit the most extreme cases of sensor correction.

Note: For Alarm-only applications, it is critical that the coefficient verification feature of the calibration routine is used since diagnostics are not reported for the Alarms (see section 3.4 for more details)

Table 6.1 shows the limits for correction for the grade of temperature dependency and 2nd nonlinearity of this dependency

Table 6.1 Limits on Coefficient Ranges

Coefficient	Correction	Condition
TCO	6060 PPM/K	
SOT_TCO	74 PPM/K^2	
TCG	12120 PPM/K	Based on raw temperature values
SOT_TCG	147 PPM/K^2	Based on raw temperature values

7 Application Circuit Examples

The ZSSC3123 provides functionality for many different configurations. The following examples correspond to the example circuits shown at the beginning of the specification; however, there are many other possibilities. Combinations of these examples and many other options can give the user maximum design flexibility. Settings for the configuration registers are given with each example. See Table 5.1 for register addresses. In the examples below bits 3 and 4 of the ZMDI_Config register are marked with an X because they are calculated during calibration and are coefficient dependent (see section 6).

7.1 Digital Output with Optional Alarms

In this example, a single-ended input capacitance is converted to the digital domain, corrected, and output via I²C™. The configuration settings are shown in Table 7.1 below. The ZSSC3123 operates in Sleep Mode, in which measurement commands are used during normal operation. In this example, the I²C™ address is 28_H and the Comm_lock is set.

In this application, both Alarm_High and Alarm_Low are used for digital communication. As shown in Table 7.1 below, both alarms are configured as active high and full push-pull drivers for digital communication.

The AFE configuration registers select 14-bit resolution for capacitance with a capacitance range from 2.9pF to 7.2pF. The internal temperature is set to 14-bit resolution.

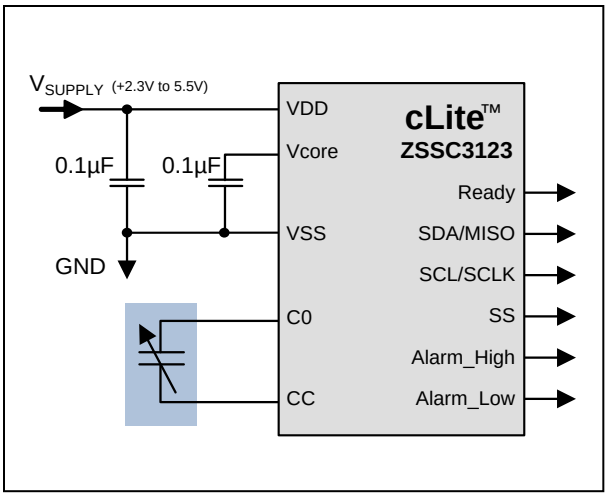


Figure 7.1 Digital Output with Optional Alarms Example

Table 7.1 Example 1: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 5.2)	0†	0	0	0	1	0	1	1	0	0	0	X	X	0	0	1
Cust_Config (Table 5.5)	0†	0†	0	0	0	0	0	0	0	0	1	0	1	0	0	0
C_Config (Table 5.3)	0†	0	0	0	1	1	0†	0†	0†	0†	0	1	0	0	1	1
T_Config (Table 5.4)	1†	0†	0†	0†	1	1	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*

* *The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.*

† *Reserved setting – do not change factory settings.*

7.2 Analog Output with Optional Alarms

In this example, a single-ended input capacitance is converted, corrected and then both capacitance and temperature are output via PDM, which are then low-pass filtered for analog outputs. One of the optional alarms controls an LED. The configuration settings are shown below in Table 7.2. In the ZMDI_Config register, the output selection bits are set to 10 to select PDM. Example low-pass filter values are given in section 3.7.

For PDM, Update Mode must be selected. In this application example, a 25ms power-down period has been used.

In this application, Alarm_High is used to turn on an LED in an open-drain configuration. The output must be low for the LED to be on, so the Alarm_High polarity bit is set to active low. The PDM clipping limits are set for 10% (666_{HEX}) to 90% (3999_{HEX}) output.

The AFE configuration registers show a resolution of 14 bits for capacitance; however, the PDM low pass filter may be set for a lower resolution with a faster settling time (See section 3.7). A capacitance range of 1.4pF to 8.6pF has been chosen, which requires a mult setting of 1. The internal temperature is set to 12-bit resolution.

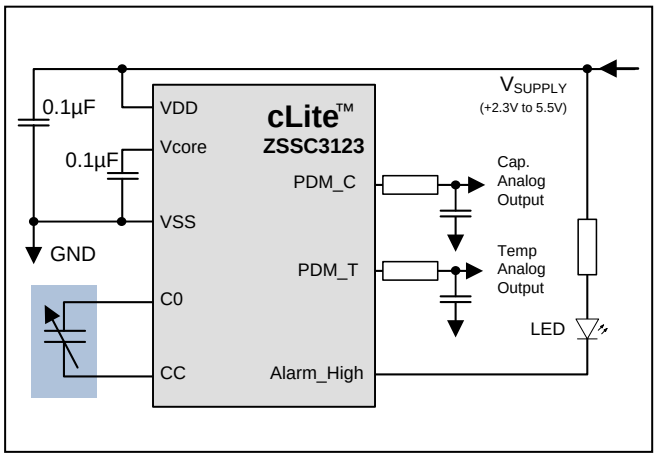


Figure 7.2 Analog Output with Optional Alarms Example

Table 7.2 Example 2: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 5.2)	0†	0	1	1	0	0	1	1	0	0	0	X	X	1	0	0
Cust_Config (Table 5.5)	0†	0†	0	0	0	0	1	0	0	0	1	0	1	0	0	0
C_Config (Table 5.3)	0†	0	0	0	1	1	0†	0†	0†	0†	0	0	1	1	0	1
T_Config (Table 5.4)	1†	0†	0†	0†	1	0	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*
PDM_Clip_High	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1
PDM_Clip_Low	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0

* *The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.*

† *Reserved setting – do not change factory settings.*

7.3 Bang-Bang Control System

In this example, the only outputs are the alarm pins. They are programmed to control a high voltage bang-bang humidity control system. External devices are not needed if not using high voltage.

If the humidity gets too high, the ZSSC3123 activates the dehumidifier using the Alarm_High pin. If the humidity gets too low, it activates the humidifier with the Alarm_Low pin. The alarm registers must be set to appropriate trip and hysteresis points (See section 3.8). The configuration settings are shown in Table 7.3.

The output selection bits should either be set to I²C™ or SPI since depending on the PDM configuration, both alarms are not supported. Additionally, I²C™ and SPI are lower power than PDM. This application does not use I²C™ or SPI, so Update Mode must be used because Sleep Mode commands cannot be sent. The fastest update rate is used for this example. External devices are needed to control the outputs because a voltage source greater than VDD is used.

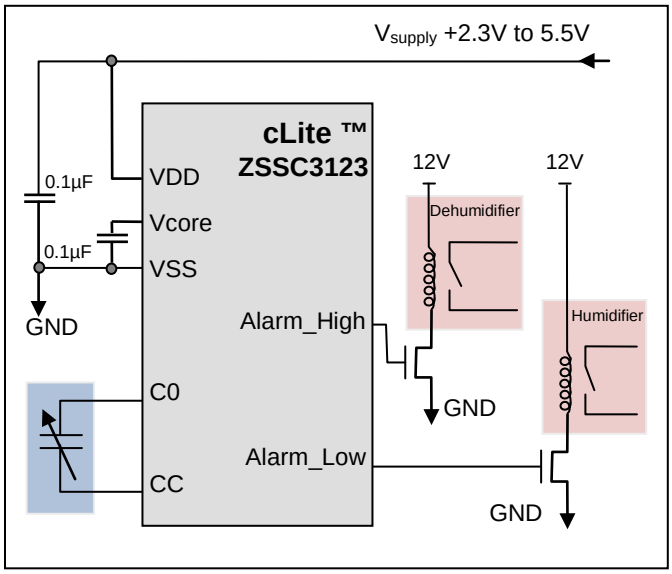


Figure 7.3 Bang-Bang Control System Example

The alarm pins control NMOS devices so the alarm pins must be full push-pull and output high when the alarm is on, so the polarity bits are set to 0 and the open drain bits are set to 0.

In this example application, a faster response time may be needed, so the AFE configuration settings show 10-bit resolution for both capacitance and internal temperature. C_Config settings have been selected for a capacitance range of 5.8pF to 7.2pF (see Table 2.2).

Table 7.3 Example 3: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 5.2)	0†	0	0	0	1	0	1	1	0	0	0	X	X	0	0	0
Cust_Config (Table 5.5)	0†	0†	0	0	0	0	0	0	0	0	1	0	1	0	0	0
C_Config (Table 5.3)	0†	0	0	0	0	1	0†	0†	0†	0†	1	0	0	0	0	1
T_Config (Table 5.4)	1†	0†	0†	0†	0	1	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*

* *The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.*

† *Reserved setting – do not change factory settings.*

7.4 Differential Input Capacitance

This example shows that the full functionality of the ZSSC3123 including the applications illustrated in examples 1, 2, and 3, can be implemented with a differential input capacitance. The capacitor C_{CC} allows a non-galvanic connection (e.g., to the moving part of a motion sensor as part of the sensor construction), but it is not needed for sensor types with existing galvanic connections.

The configuration settings are shown in Table 7.4. The differential bit is set to select differential input capacitance. In this example, SPI has been selected in Update Mode at the fastest update rate. The SPI phase is set to 1 so that the master samples MISO on the negative edge of SCLK. The EEPROM has been locked.

The AFE configuration registers select 14-bit resolution for capacitance and 10-bit resolution for internal temperature. Because this is the differential configuration, both the internal reference and offset capacitors are set to zero.

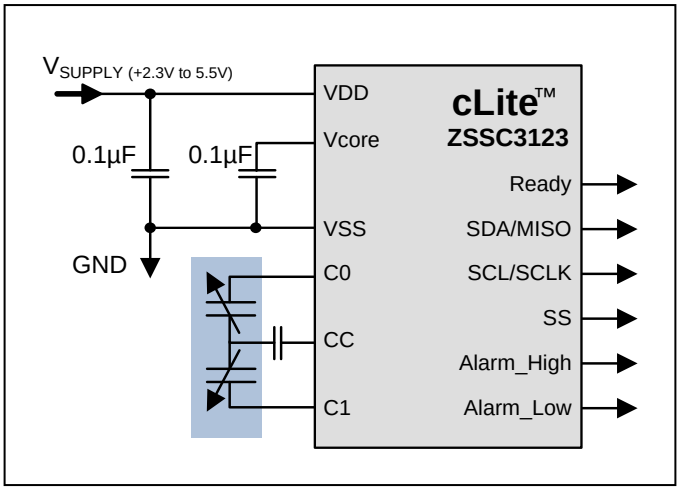


Figure 7.4 *Differential Input Capacitance Example*

Table 7.4 Example 4: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 5.2)	0†	0	0	1	1	0	0	0	0	1	1	X	X	0	0	0
Cust_Config (Table 5.5)	0†	0†	0	0	1	0	0	0	0	0	1	0	1	0	0	0
C_Config (Table 5.3)	0†	1	0	0	1	1	0†	0†	0†	0†	0	0	0	0	0	0
T_Config (Table 5.4)	1†	0†	0†	0†	0	1	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*

** The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.*

† Reserved setting – do not change factory settings.

7.5 External Reference Capacitor

This example demonstrates that the full functionality of the ZSSC3123, including the applications illustrated in examples 1, 2, and 3, can be implemented with an external reference capacitor in conjunction with a single-ended input capacitance. In this example, the digital output is used. The external reference is used. The configuration settings are shown in Table 7.5.

Example configuration settings show I²C™ in Sleep Mode with the Comm_lock off so that the ZSSC3123 can respond to any I²C™ slave address. Also the Ready pin is configured for open drain so that multiple devices can have their Ready lines connected together.

The AFE configuration registers select 12-bit resolution for capacitance and 12-bit resolution for internal temperature. This example also shows an offset setting of 4.3pF.

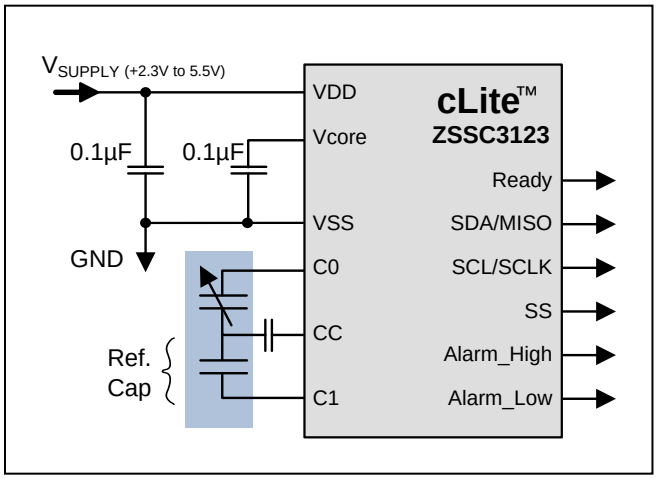


Figure 7.5 Ext. Reference Input Capacitance Example

Table 7.5 Example 5: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 5.2)	0†	0	0	0	1	0	0	0	0	0	0	X	X	0	0	0
Cust_Config (Table 5.5)	0†	0†	0	1	0	0	0	0	0	0	1	0	1	0	0	0
C_Config (Table 5.3)	0†	0	0	0	1	0	0†	0†	0†	0†	0	1	1	0	0	0
T_Config (Table 5.4)	1†	0†	0†	0†	1	0	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*

** The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.*

† Reserved setting – do not change factory settings.

8 ESD/Latch-Up-Protection

All external module pins have an ESD protection of >4000V and a latch-up protection of ±100mA or (up to +8V / down to –4V) relative to VSS/VSSA. The internal module pin VCORE has an ESD protection of > 2000V. ESD protection referenced to the Human Body Model is tested with devices in TSSOP14 packages during product qualification. The ESD test follows the Human Body Model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

9 Pin Configuration and Package

The standard package for the ZSSC3123 is a TSSOP-14 (4.4±0.1mm body wide) with lead-pitch 0.65mm. See the notes in Table 9.2 regarding connection requirements.

Table 9.1 Storage and Soldering Condition

Storage and Soldering TSSOP14						
Maximum Storage Temperature	$T_{max\_storage}$	Less than 10hrs, before mounting			150	°C
Minimum Storage Temperature:	$T_{min\_storage}$	at original packing only	-55			°C
Maximum Drybake Temperature	$T_{drybake}$	Less than100hrs in summary, before mounting			125	°C
Soldering Peak Temperature	T_{peak}	Less than 30s (IPC/JEDEC-STD-020 Standard)			260	°C

Figure 9.1 ZSSC3123 Pin-Out Diagram

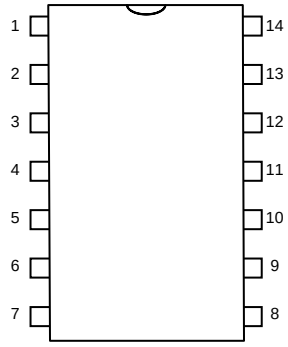


Table 9.2 ZSSC3123 Pin Assignments for TSSOP-14

Pin	Name	Description	Notes
1	VCORE	Core voltage	Always connect to an external capacitor to Gnd that is within the specifications given in section 1.3 for C_{VCORE_SM} and C_{VCORE_UM}. This is the only internal module pin. Refer to section 8 for ESD details.
2	C0	Capacitor input 0	
3	VSS	Ground supply	Connecting to GND for shielding is strongly recommended.
4	CC	Common capacitor input	
5	VSS	Ground supply	Connecting to GND for shielding is strongly recommended.

Pin	Name	Description	Notes
6	C1	Capacitor input 1	If not used, must be unconnected.
7	VDD	Supply voltage (1.8V to 5.5V) 2.3V to 5.5V for ZSSC3123	Must connect to Vsupply.
8	Alarm_Low/ PDM_T	Low alarm output Temperature PDM (see Table 3.8)	If not used, must be unconnected.
9	Alarm_High	High alarm output	If not used, must be unconnected.
10	Ready/ PDM_C	Ready signal (conversion complete output) Capacitance PDM (see Table 3.8)	If not used, must be unconnected.
11	VSS	Ground supply	Must connect to GND.
12	SDA/MISO	I^2C™ data if in I^2C™ Mode Master-In-Slave-Out if in SPI Mode (see Table 3.8)	If not used, must connect to VDD.
13	SCL/SCLK	I^2C™ clock if in I^2C™ Mode Serial clock if in SPI Mode (see Table 3.8)	If not used, must connect to VDD.
14	SS	Slave Select (input) if in SPI Mode (see Table 3.8)	If not used, must be unconnected.

10 Test

The test program is based on this datasheet. The final parameters, which will be tested during production, are listed in the tables and graphs of section 1.

11 Reliability

A reliability investigation according to the in-house non-automotive standard will be performed.

12 Customization

For high-volume applications that require an upgraded or downgraded functionality compared to the ZSSC3123, IDT can customize the circuit design by adding or removing certain functional blocks.

For this customization, IDT has a considerable library of sensor-dedicated circuitry blocks, which enable IDT to provide a custom solution quickly. Please contact IDT for further information.

13 Part Ordering Codes

Please contact IDT Sales for additional information.

Sales Code	Description	Package
ZSSC3123AA1B	ZSSC3123 die — Temperature range: -40°C to +125°C	*Tested dice on un-sawn wafer*
ZSSC3123AI1B	ZSSC3123 die — Temperature range: -40°C to +85°C	*Tested dice on un-sawn wafer*
ZSSC3123AA1C	ZSSC3123 die — Temperature range: -40°C to +125°C	*Tested dice on frame*
ZSSC3123AI1C	ZSSC3123 die — Temperature range: -40°C to +85°C	*Tested dice on frame*
ZSSC3123AA2	ZSSC3123 TSSOP14 — Temperature range: -40°C to +125°C – Lead-free package	Tube: add “T” to code; reel: add “R”
ZSSC3123AI2	ZSSC3123 TSSOP14 — Temperature range: -40°C to +85°C – Lead-free package	Tube: add “T” to code; reel: add “R”
ZSSC3123KIT	ZSSC3123 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples (software can be downloaded from www.IDT.com/ZSSC3123)	Kit

Contact IDT Sales for support and sales of the ZSSC3123 Mass Calibration System.

14 Related Documents

Document
ZSSC3122/ZSSC3123 SSC Evaluation Kit Description

Visit IDT’s website www.IDT.com or contact your nearest sales office for the latest version of these documents.

15 Glossary

Term	Description
ADC	Analog-to-Digital Converter
CDC	Capacitance-to-Digital Converter
DAC	Digital-to-Analog Converter
ECC	Error Checking and Correction
SSC	Sensor Signal Conditioner

16 Document Revision History

Revision	Date	Description
1.00	February 15, 2011	First release.
1.10	June 29, 2011	Added specification for “Excitation Frequency of External Capacitances C_0 and C_1” in section 1.3 and 2.2.1. Added “PDM frequency” specification to table in section 1.3. In section 3.7, clarified that clipping limit default values must be adjusted for PDM output functionality. Revised PDM frequency in sections 1.3 and 3.7. Revised PDM ripple and settling time specifications in section 1.3. Revised related examples in Table 3.12 and corrected equation (14) for calculating ripple. Revisions to text explaining equation (16) and subsequent text recommending limits for PDM_Clip_High. Revised Table 5.1 for PDM_Clip_High and PDM_Clip_Low. Added new settings for PDM clipping limits to section 7.2 and revised related settings in Table 7.2. Revised section 1.6 for addition of specifications for “Voltage Dependency” for the temperature channel to section 1.3. Revised section 2.2.1.3 regarding total capacitance. Revised default value for EEPROM word 04_H from $007T_H$ to $00FT_H$ in Table 5.1. Minor edits for clarity in section 7.3. Revised notes for VCORE pin 1 in Table 9.2. Revisions to section 3.3.2.1.
1.20	August 16, 2011	Added specifications in section 1.3 for V_{POR} maximum, V_{REG} typical and maximum, and $PSR_{TEMP.}$ Revisions to section 3.3.2.1 to explain preferred method for detecting valid data. Revised product ordering codes.
1.30	July 23, 2012	Added note for clarity to “Active Regulated Voltage” specification in section 1.3. Deleted redundant specification for f_{OSC} in section 1.3. Revised the “Excitation Frequency of External Capacitances C0 and C1” (f_{EXC}) specification in Table 1.3 to list a separate specification f_{MULTx} for each Mult setting. Deleted inapplicable row for 2.0V for the “Error Mult 1, -40 to 125°C” specification in section 1.3. Revised specifications for C_{VCORE_SM} and C_{VCORE_UM} in specifications in section 1.2. Updated IDT contact information.

Revision	Date	Description
1.40	October 15, 2012	Revision to maximum specifications for “Start-Up-Time,” “Update Rate (Update Mode),” and “Response Time (Sleep Mode)” in section 1.3. Revision to equations in section 2.2.1.1 and 2.2.1.2. Edits to text under Figure 3.4. Update for IDT contact information.
1.50	April 29, 2013	Updated part numbers with new parts. Update for IDT contact information.
1.60	May 20, 2013	Revisions to section 3.3.2.1 to explain preferred method for detecting valid data. Revision to section 3.6.6 to update Ready pin behavior in Sleep Mode. Revision to Figure 3.7.
1.61	July 4, 2013	Update for part order codes.
1.62	December 11, 2013	Update to kit description in the part order tables: software is no longer included in kit. Instead it is downloaded from the product page www.IDT.com/ZSSC3123. Minor edits to refer to product by alphanumeric name ZSSC3123, rather than cLite™.
	January 26, 2016	Changed to IDT branding

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