Brief Description

The ZSPM1025C and ZSPM1025D are true-digital single-phase PWM controllers optimally configured for use with the Murata Power Solutions 25A Power Block OKLP-X/25 in smart digital power solutions.

The ZSPM1025C and ZSPM1025D integrate a digital control loop, optimized for maximum flexibility and stability as well as load step and steady-state performance. In addition, a rich set of protection functions is provided.

To simplify the system design, a set of optimized configuration options have been pre-programmed in the devices. These configurations can be selected by setting the values of two external resistors.

Reference solutions are available complete with layout recommendations, example circuit board layouts, complete bill of materials and more.

Features

- Application-optimized digital control loop
- Advanced, digital control techniques
  - Tru-sample Technology™
  - State-Law Control™ (SLC)
  - Sub-cycle Response™ (SCR)
- Improved transient response and noise immunity
- Protection features
  - Over-current protection
  - Over-voltage protection (VIN, VOUT)
  - Under-voltage protection (VIN, VOUT)
  - Overloaded startup
  - Continuous retry (“hiccup”) mode for fault conditions
- Pre-programmed for optimized use with Murata Power Solutions 25A Power Block OKLP-X/25
- 2-pin configuration for loop compensation, output voltage, and slew rate.
- Operation from a single 5V or 3.3V supply

Benefits

- Fast time-to-market using off-the-shelf, optimally configured controller and power block
- Fast configuration and design flexibility
- Simplified design and integration
- FPGA designer-friendly solution
- Highest power density with smallest footprint
- Pin-to-pin compatible with the ZSPM1025A PWM controller enabling point-of-load platform designs with or without digital communication
- Higher energy efficiency across all output loading conditions

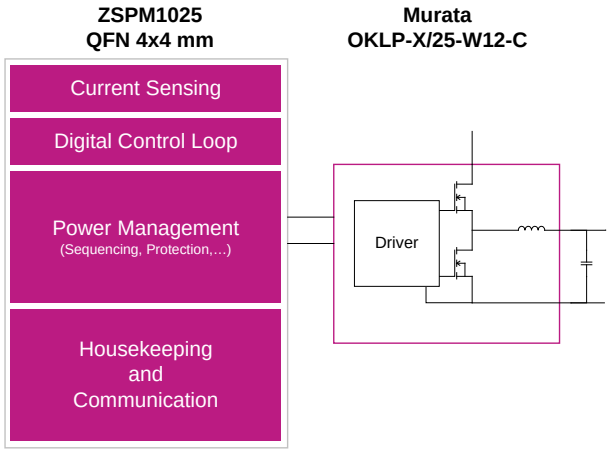
Available Support

- Evaluation Kit
- Reference Solutions
- PC-based Pink Power Designer™ Graphic User Interface (GUI)

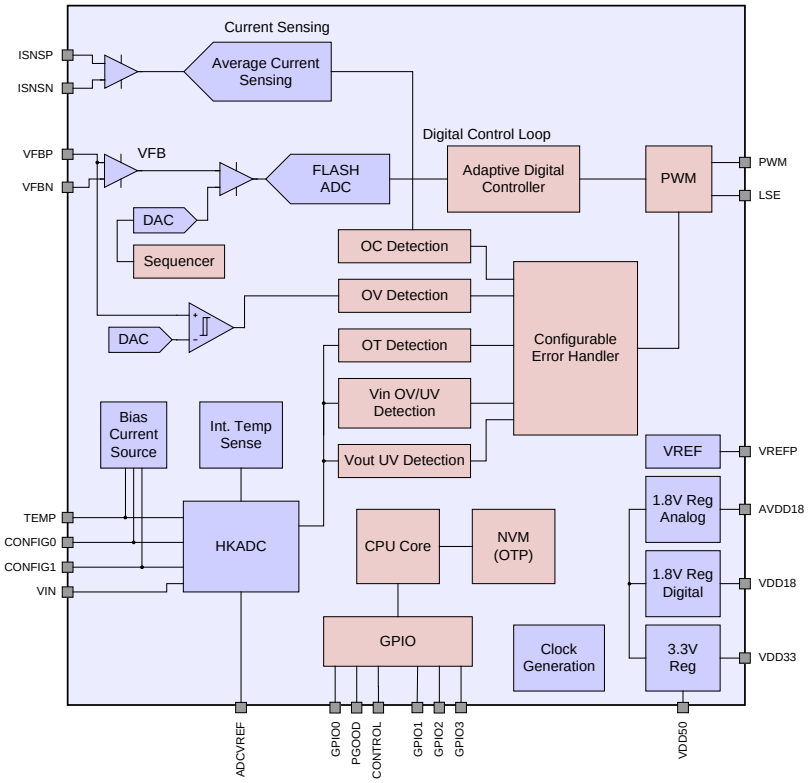
Physical Characteristics

- Operation temperature: -40°C to +125°C
- ZSPM1025C V_{OUT}: 0.62V to 1.20V
- ZSPM1025D V_{OUT}: 1.25V to 3.40V
- Lead free (RoHS compliant) 24-pin QFN package (4mm x 4mm)

ZSPM1025C/D Typical Application Diagram



ZSPM1025C/D Block Diagram



Typical Applications

- *Telecom Switches*
- *Servers and Storage*
- *Base Stations*
- *Network Routers*
- *Industrial Applications*
- *FPGA Designs*
- *Point-of-load power solutions*
- *Telecommunications*
- *Single-Rail/Single-Phase supplies for Processors, ASICs, DSP's, etc.*

Ordering Information

Sales Code	Description	Package
ZSPM1025CA1W 0	ZSPM1025C Lead-free QFN24 — Temperature range: -40°C to +125°C	7" Reel
ZSPM1025DA1W 0	ZSPM1025D Lead-free QFN24 — Temperature range: -40°C to +125°C	7" Reel
ZSPM8725-KIT	Evaluation Kit for ZSPM1025C with PMBus™ Communication Interface *	Kit
ZSPM8825-KIT	Evaluation Kit for ZSPM1025D with PMBus™ Communication Interface *	Kit

* Pink Power Designer™ GUI for kit can be downloaded from the IDT web site at www.IDT.com/ZSPM1025C or www.IDT.com/ZSPM1025D.

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Tech Support
www.IDT.com/go/support

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1 IC Characteristics

Note: The absolute maximum ratings are stress ratings only. The ZSPM1025C/D might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

1.1. Absolute Maximum Ratings

PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage	VDD50	dV/dt < 0.15V/µs	-0.3		5.5	V
Maximum slew rate					0.15	V/µs
3.3 V supply voltage	VDD33		-0.3		3.6	V
1.8 V supply voltage	VDD18 AVDD18		-0.3		2.0	V
Digital pins						
Digital I/O pins	GPIOx CONTROL PGOOD LSE PWM		-0.3		5.5	V
Analog pins						
Current sensing	ISNSP ISNSN		-0.3		5.5	V
Voltage feedback	VFBP VFBN		-0.3		2.0	V
All other analog pins	ADCVREF VREFP TEMP VIN CONFIGx		-0.3		2.0	V
Ambient conditions						
Storage temperature			-40		150	°C
Electrostatic discharge – Human Body Model [1)]					+/-2k	V
Electrostatic discharge – Charge Device Model [1)]					+/- 500	V

1) ESD testing is performed according to the respective JESD22 JEDEC standard.

1.2. Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient conditions						
Operation temperature	T_{AMB}		-40		125	°C
Thermal resistance junction to ambient	θ_{JA}			40		K/W

1.3. Electrical Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage—VDD50 pin	V_{VDD50}		4.75	5.0	5.25	V
5 V supply current	I_{VDD50}	VDD50=5.0 V		23		mA
3.3 V supply voltage	V_{VDD33}	Supply for both the VDD33 and VDD50 pins if the internal 3.3V regulator is not used.	3.0	3.3	3.6	V
3.3 V supply current	I_{VDD33}	VDD50=VDD33=3.3 V		23		mA
Internally generated supply voltages						
3.3 V supply voltage—VDD33 pin	V_{VDD33}	VDD50=5.0 V	3.0	3.3	3.6	V
3.3 V output current	I_{VDD33}	VDD50=5.0 V			2.0	mA
1.8 V supply voltages—AVDD18 and VDD18 pins	V_{AVDD18} V_{VDD18}	VDD50=5.0 V	1.72	1.80	1.98	V
1.8 V output current					0	mA
Power-on reset threshold for VDD33 pin – on	$V_{TH\_POR\_ON}$			2.8		V
Power-on reset threshold for VDD33 pin – off	$V_{TH\_POR\_OFF}$			2.6		V
Digital IO pins (GPIOx, CONTROL, PGOOD)						
Input high voltage		VDD33=3.3 V	2.0			V
Input low voltage		VDD33=3.3 V			0.8	V
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Input leakage current					±1	µA
Output current - high					2.0	mA
Output current - low					2.0	mA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital IO pins with tri-state capability (LSE, PWM)						
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Output current - high					2.0	mA
Output current - low					2.0	mA
Tri-state leakage current					±1.0	µA
Output voltage (without external feedback divider; see section 3.3.2)						
Set-point voltage			0		1.4	V
Set-point resolution				1.4		mV
Set-point accuracy		VOUT=1.2 V		1		%
Inductor current measurement						
Common mode voltage - ISNSP and ISNSN pins to AGND			0		5.0	V
Differential voltage range across ISNSP and ISNSN pins					±100	mV
Accuracy				10		%
Digital pulse width modulator						
Switching frequency	f_{SW}			500		kHz
Resolution				163		ps
Frequency accuracy				2.0		%
Duty Cycle			2.5		100	%
Over-voltage protection						
Reference DAC						
Set-point voltage			0		1.58	V
Resolution				25		mV
Set point accuracy				2		%
Comparator						
Hysteresis				35		mV
Housekeeping analog-to-digital converter (HKADC) input pins						
Input voltage—TEMP, VIN, CONFIG0, and CONFIG1 pins			0		1.44	V
Source impedance Vin sensing					3	kΩ
ADC resolution				0.7		mV
External temperature measurement (Note: Only PN-junction sense elements are supported)						

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bias currents for external temperature sensing—TEMP pin				60		µA
Resolution—TEMP pin				0.16		K
Accuracy of measurement—TEMP pin				±5.0		K
Internal temperature measurement						
Resolution				0.22		K
Accuracy of measurement				±5.0		K

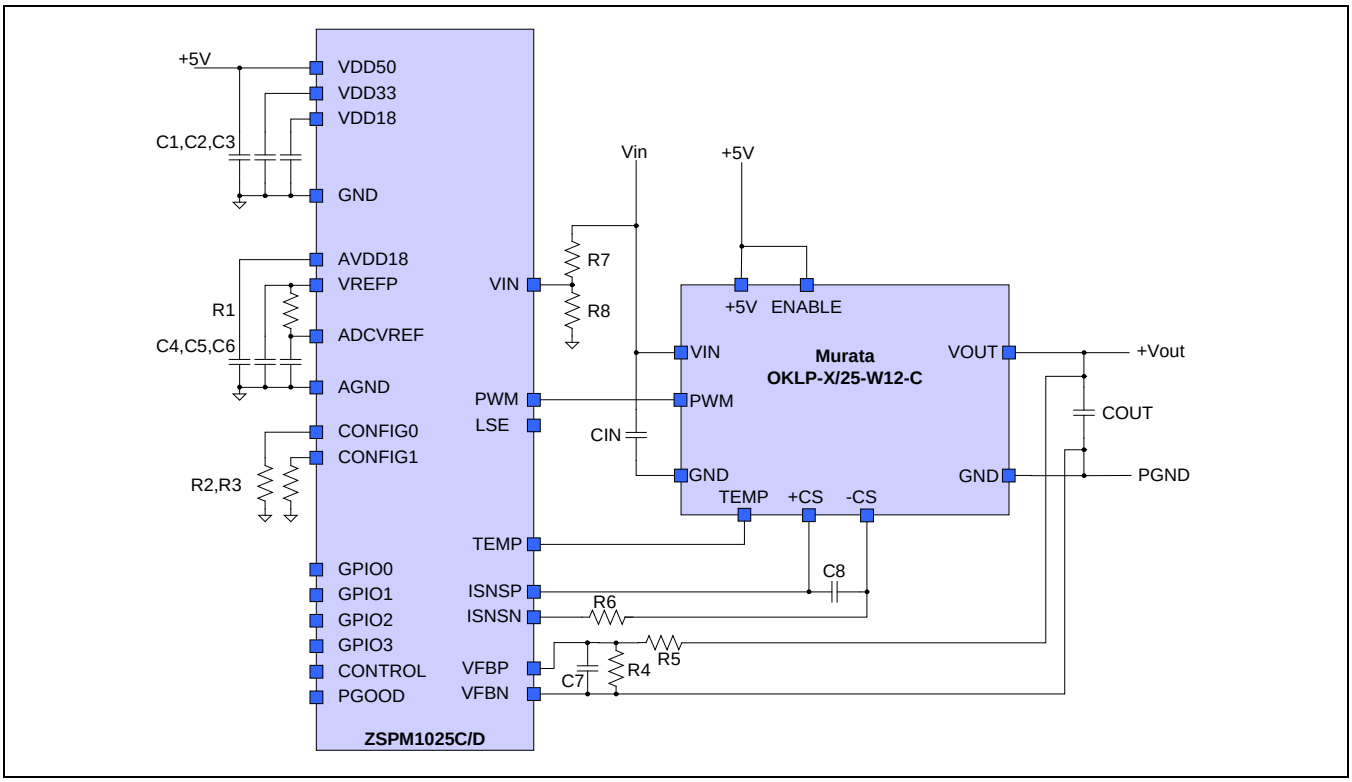
2 Product Summary

2.1. Overview

The ZSPM1025C and ZSPM1025D are true-digital single-phase PWM controllers optimally configured for use with the Murata Power Solutions 25A Power Block OKLP-X/25 in smart digital power solutions. The ZSPM1025C/D has a digital power control loop incorporating output voltage sensing, average inductor current sensing, and extensive fault monitoring and handling features. Several different functional units are integrated in the device. A dedicated digital control loop is used to provide fast loop response and optimal output voltage regulation. This includes output voltage sensing, average inductor current sensing, a digital control law, and a digital pulse-width modulator (DPWM). In parallel, a dedicated error handler allows fast and flexible detection of error signals and their appropriate handling. A housekeeping analog-to-digital converter (HKADC) ensures the reliable and efficient measurement of environmental signals, such as input voltage and temperature.

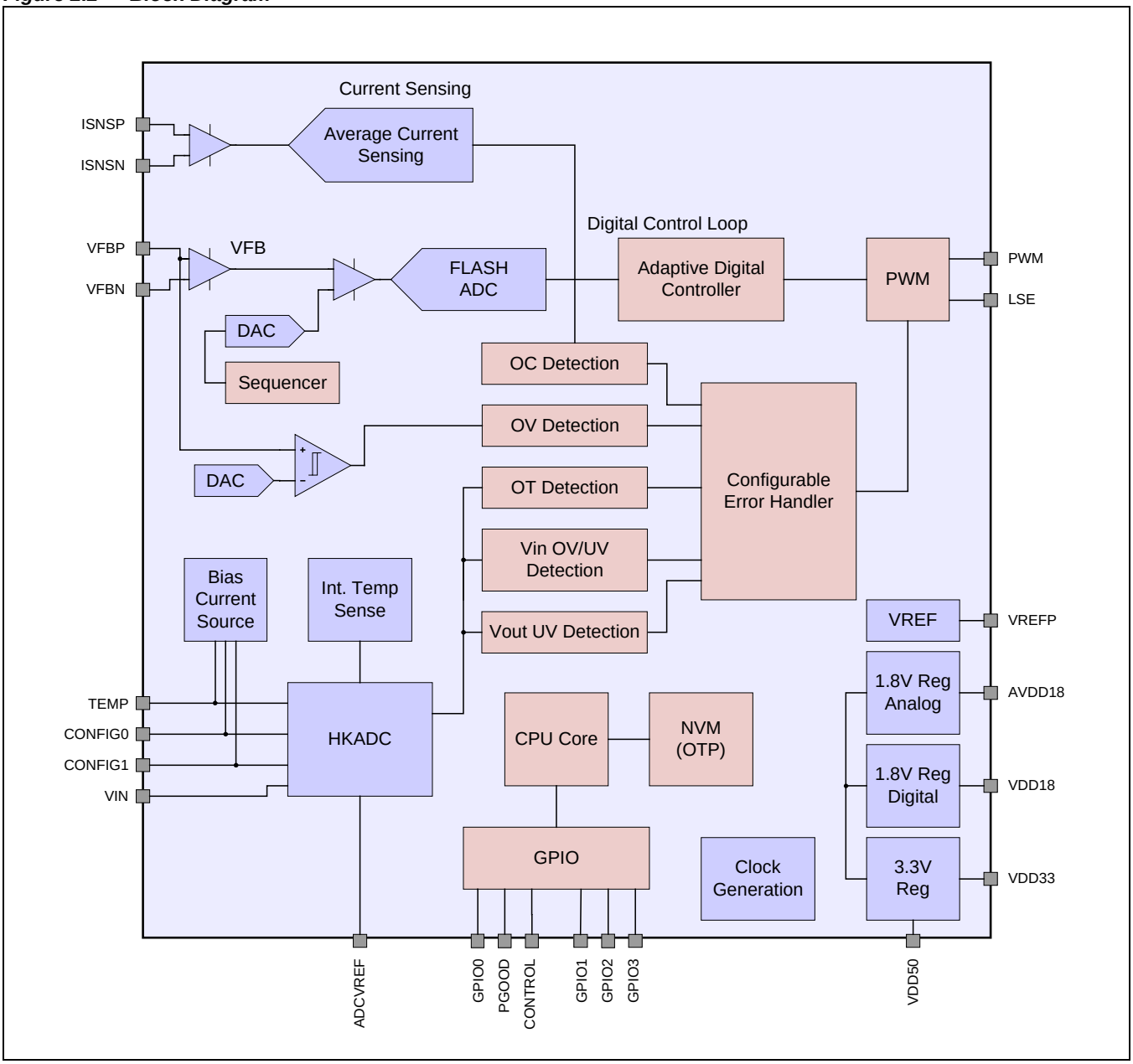
An application-specific, low-energy integrated microcontroller is used to control the overall system. It manages configuration of the various logic units according to the preprogrammed configuration look-up tables and the external configuration resistors connected to the CONFIG0 and CONFIG1 pins. These pin-strapping resistors expedite configuration of output voltage, compensation, and rise time without requiring digital communication. IDT's Pink Power Designer™ graphical user interface (GUI) allows the user to monitor the controller's measurements of the environmental signals and the status of the error handler via the GPIO2 and GPIO3 pins.

Figure 2.1 Typical Application Circuit with a 5 V Supply Voltage



A high-reliability, high-temperature one-time programmable memory (OTP) is used to store configuration parameters. All required bias and reference voltages are internally derived from the external supply voltage.

Figure 2.2 Block Diagram



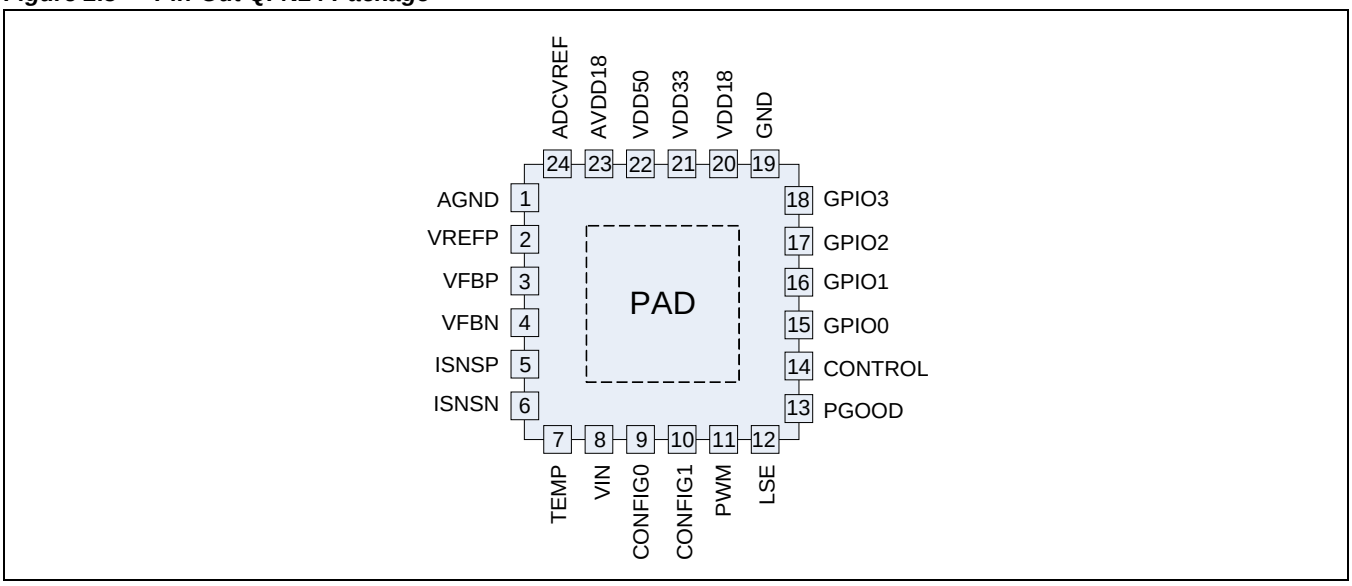
2.2. Pin Description

Pin	Name	Direction	Type	Description
1	AGND	Input	Supply	Analog Ground
2	VREFP	Output	Supply	Reference Terminal
3	VFBP	Input	Analog	Positive Input of Differential Feedback Voltage Sensing
4	VFBN	Input	Analog	Negative Input of Differential Feedback Voltage Sensing
5	ISNSP	Input	Analog	Positive Input of Differential Current Sensing
6	ISNSN	Input	Analog	Negative Input of Differential Current Sensing
7	TEMP	Input	Analog	Connection to External Temperature Sensing Element
8	VIN	Input	Analog	Power Supply Input Voltage Sensing
9	CONFIG0	Input	Analog	Configuration Selection 0
10	CONFIG1	Input	Analog	Configuration Selection 1
11	PWM	Output	Digital	High-Side FET Control Signal
12	LSE	Output	Digital	Low-Side FET Control Signal
13	PGOOD	Output	Digital	PGOOD Output (Internal Pull-Down)
14	CONTROL	Input	Digital	Control Input – Active High
15	GPIO0	Input/Output	Digital	General Purpose Input/Output Pin
16	GPIO1	Input/Output	Digital	General Purpose Input/Output Pin
17	GPIO2	Input/Output	Digital	General Purpose Input/Output Pin
18	GPIO3	Input/Output	Digital	General Purpose Input/Output Pin
19	GND	Input	Supply	Digital Ground
20	VDD18	Output	Supply	Internal 1.8 V Digital Supply Terminal
21	VDD33	Input/Output	Supply	3.3 V Supply Voltage Terminal
22	VDD50	Input	Supply	5.0 V Supply Voltage Terminal
23	AVDD18	Output	Supply	Internal 1.8 V Analog Supply Terminal
24	ADCVREF	Input	Analog	Analog-to-Digital Converter (ADC) Reference Terminal
PAD	PAD	Input	Analog	Exposed Pad, Digital Ground

2.3. Available Packages

The ZSPM1025C/D is available in a 24-pin QFN package. The pin-out is shown in Figure 2.3. The mechanical drawing of the package can be found in Figure 5.1.

Figure 2.3 Pin-Out QFN24 Package



3 Functional Description

3.1. Power Supply Circuitry, Reference Decoupling, and Grounding

The ZSPM1025C/D incorporates several internal power regulators in order to derive all required supply and bias voltages from a single external supply voltage. This supply voltage can be either 5V or 3.3V depending on whether the internal 3.3V regulator should be used. If the internal 3.3V regulator is not used, 3.3V must be supplied to the 3.3V and 5V supply pins. Decoupling capacitors are required at the VDD33, VDD18, and AVDD18 pins (1.0µF minimum; 4.7µF recommended). If the 5.0V supply voltage is used, i.e., the internal 3.3V regulator is used, a small load current can be drawn from the VDD33 pin. This can be used to supply pull-up resistors, for example.

The reference voltages required for the analog-to-digital converters are generated within the ZSPM1025C/D. External decoupling must be provided between the VREFP and ADCVREF pins. Therefore, a 4.7µF capacitor is required at the VREFP pin, and a 100nF capacitor is required at the ADCVREF pin. The two pins should be connected with approximately 50Ω resistance in order to provide sufficient decoupling between the pins.

Three different ground connections (the pad, AGND pin, and GND pin) are available on the outside of the package. These should be connected together to a single ground tie. A differentiation between analog and digital ground is not required.

3.2. Reset/Start-up Behavior

The ZSPM1025C/D employs an internal power-on-reset (POR) circuit to ensure proper start up and shut down with a changing supply voltage. Once the supply voltage increases above the POR threshold voltage (see section 1.3), the ZSPM1025C/D begins the internal start-up process. Upon its completion, the device is ready for operation.

3.3. Digital Power Control

3.3.1. Overview

The digital power control loop consists of the integral parts required for the control functionality of the ZSPM1025C/D. A high-speed analog front-end is used to digitize the output voltage. A digital control core uses the acquired information to provide duty-cycle information to the PWM that controls the drive signals to the power stage.

3.3.2. Output Voltage Feedback

The voltage feedback signal is sampled with a high-speed analog front-end. The feedback voltage is differentially measured and subtracted from the voltage reference provided by a reference digital-to-analog converter (DAC) using an error amplifier. A flash ADC is then used to convert the voltage into its digital equivalent. This is followed by internal digital filtering to improve the system's noise rejection.

3.3.2.1. ZSPM1025C

The ZSPM1025C has been designed for an output voltage range from 0.62 to 1.20V. The VFBP pin should be connected to the converter output through a 1.75kΩ resistor, and a small filter capacitor, typically 22pF, should be connected between the VFBP and VFBN pins of the ZSPM1025C.

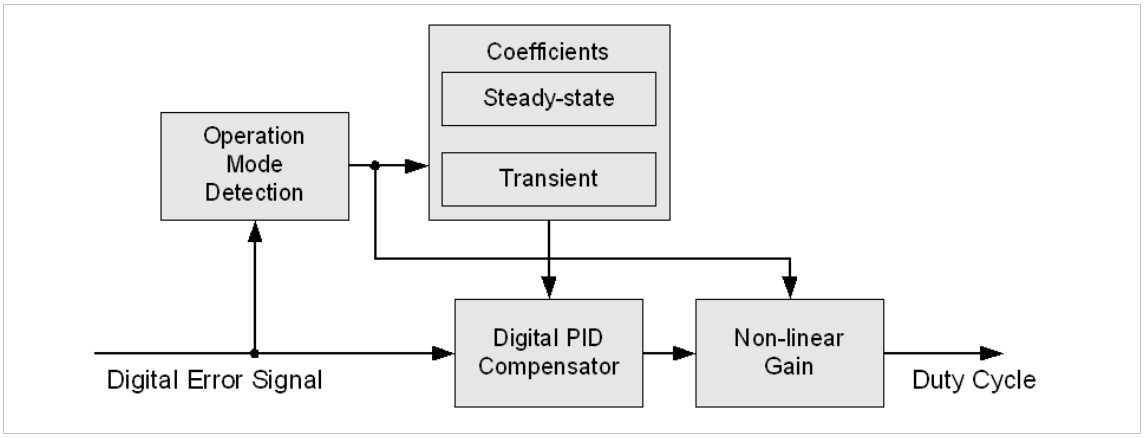
3.3.2.2. ZSPM1025D

The ZSPM1025D has been designed for an output voltage range from 1.25 to 3.40V. An external feedback divider is required for the ZSPM1025D. The VFBP pin should be connected to the converter output through a 1.75kΩ resistor, and a 1kΩ resistor should be connected between the VFBP and VFBN pin of the ZSPM1025D. A small filter capacitor, typically 22pF, should also be connected between the VFBP and VFBN pins of the ZSPM1025D.

3.3.3. Digital Compensator

The sampled output voltage is processed by a digital control loop in order to modulate the DPWM output signals controlling the power stage. This digital control loop works as a voltage-mode controller using a PID-type compensation. The basic structure of the controller is shown in Figure 3.1. The proprietary State-Law™ Control (SLC) concept features two parallel compensators, steady-state operation, and fast transient operation. The ZSPM1025C/D implements fast, reliable switching between the different compensation modes in order to ensure good transient performance and quiet steady state. This has been utilized to tune the compensators individually for the respective needs; i.e. quiet steady-state and fast transient performance.

Figure 3.1 Simplified Block Diagram for the Digital Compensation



Three different techniques are used to improve transient performance further:

- Tru-sample Technology™ is used to acquire fast, accurate, and continuous information about the output voltage so that the device can react quickly to any change in output voltage. Tru-sample Technology™ reduces phase-lag caused by sampling delays, reduces noise sensitivity, and improves transient performance.
- The Sub-cycle Response™ (SCR) technique, a method to drive the DPWM asynchronously during load transients, allows limiting the maximum deviation of the output voltage and recharging the output capacitors faster.
- A nonlinear gain adjustment is used during large load transients to boost the loop gain and reduce the settling time.

3.3.4. Power Sequencing and the CONTROL Pin

The ZSPM1025C/D has a set of pre-configured power-sequencing features. The typical sequence of events is shown in Figure 3.2. The individual values for the delay, ramp time, and post ramp time are listed in Table 3.1. Note that the device is slew-rate controlled for ramping. Hence, when pin-strapping options for the output voltage are used, the ramp time can change based on the configured slew-rate and the actual selected output voltage. The slew rate can be selected in the application circuit using the pin-strap options as explained in section 4.1.

The CONTROL pin is pre-configured for active high operation.

The ZSPM1025C/D features a power good (PGOOD) output, which can be used to indicate the state of the power rail. If the output voltage level is above the power good ON threshold, the pin is set to active, indicating a stable output voltage on the rail. The thresholds for the power good output turn-on and turn-off are listed in Table 3.2. Note that the power good thresholds are stored in the device as factors relative to the nominal output voltage. Hence, using the strapping options (see section 4.1) to change the output voltage level also changes the PGOOD thresholds.

Figure 3.2 Power Sequencing

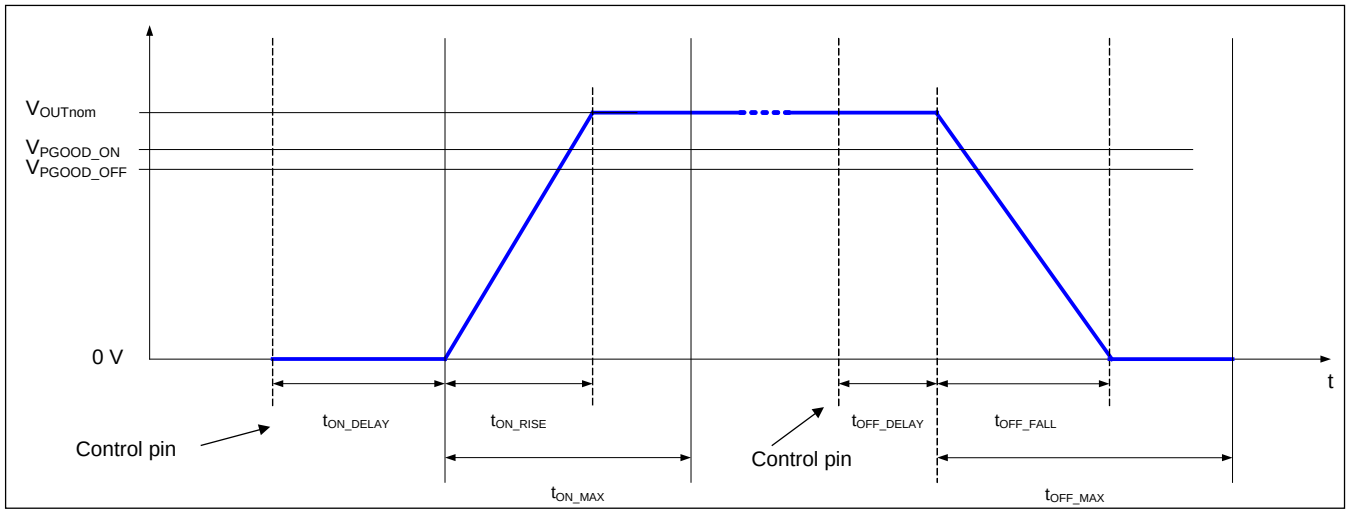


Table 3.1 Power Sequencing Timing

Parameter	ZSPM1025C	ZSPM1025D
t_{ON_DELAY}	10ms	10ms
t_{ON_RISE}	Pin Strap Selectable (see section 4.1)	Pin Strap Selectable (see section 4.1)
t_{ON_MAX}	188ms	188ms
t_{OFF_DELAY}	10ms	10ms
t_{OFF_FALL}*	50ms (VOUT = 1.20V) *Ramp down slew rate is 0.024V/ms*	50ms (VOUT = 1.80V) *Ramp down slew rate is 0.036V/ms*
t_{OFF_MAX}	188ms	188ms

* t_{OFF_FALL} is implemented as a slew rate by the ZSPM1025C/D. Use the device-specific slew rate and the selected nominal output voltage to calculate the actual t_{OFF_FALL} in milliseconds.

Table 3.2 Power Good (PGOOD) Output Thresholds

Parameter	Value
ON level	95% of VOUT Nominal VOUT nominal is pin-strap selectable (see section 4.1)
OFF level	90% of VOUT Nominal VOUT nominal is pin-strap selectable (see section 4.1)

3.3.5. Pre-biased Start-up and Soft-Off

Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this phase.

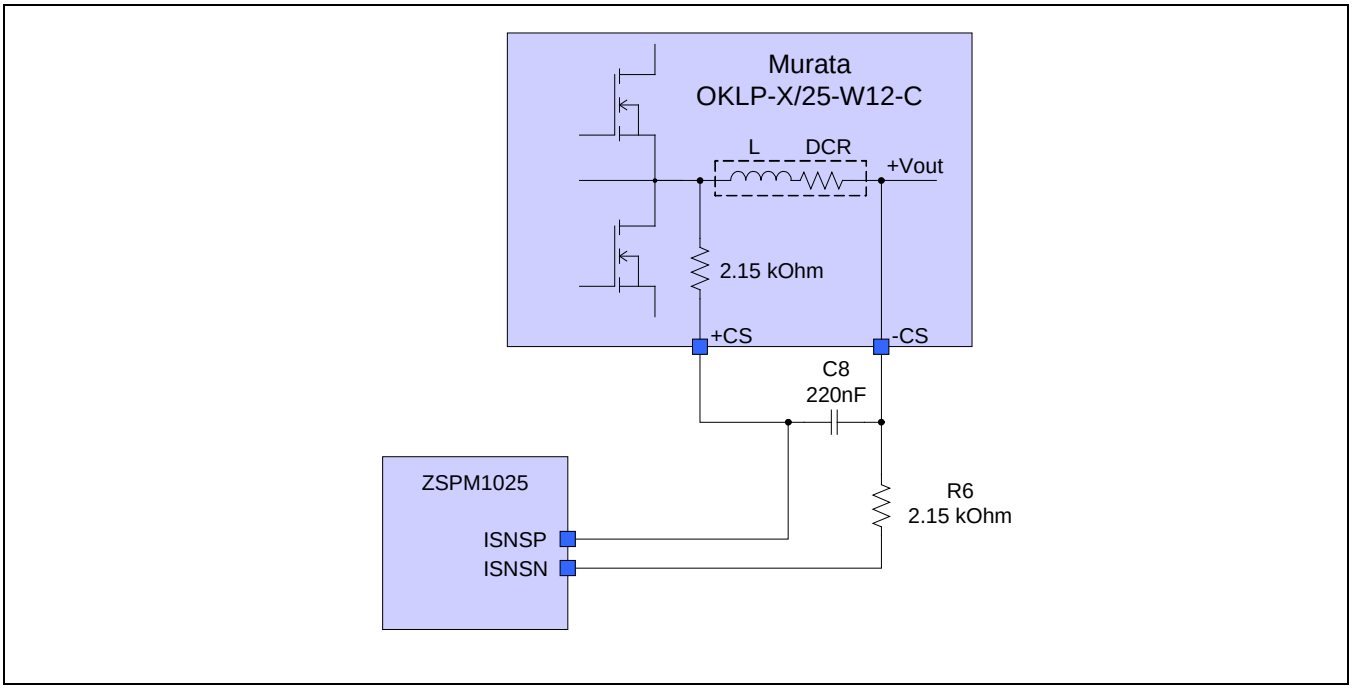
When the DC/DC converter output is disabled, i.e. when the CONTROL pin is set low, the ZSPM1025C/D will execute the soft-off sequence. The soft-off sequence will ramp down the output voltage to 0V and set the PWM output in a tri-state condition.

3.3.6. Current Sensing

The ZSPM1025C/D offers cycle-by-cycle average current sensing and over-current protection. A dedicated ADC is used to provide fast and accurate current information over the switching period. The acquired information is compared with the pre-configured over-current threshold to trigger an over-current fault event. DCR current sensing across the inductor on the Murata OKLP-X/25-W12-C is supported. Additionally, the device uses DCR temperature compensation via the external temperature sense element. This increases the accuracy of the current sense method by counteracting the significant change of the DCR over temperature.

The schematic of the required current sensing circuitry is shown in Figure 3.3 for the widely-used DCR current-sensing method, which uses the parasitic resistance of the inductor to acquire the current information. The principle is based on a matched time-constant between the inductor and the low-pass filter built from a 2.15kΩ resistor mounted on the Murata OKLP-X/25-W12-C Power Block and C8. Resistor R6 should be a precision 2.15kΩ resistor in order to provide good DC voltage rejection, .i.e. reduce the influence of the output voltage level on the current measurement.

Figure 3.3 Inductor Current Sensing Using the DCR Method



To improve the accuracy of the current measurement, which can be adversely affected by the temperature coefficient of the inductor's DCR, the ZSPM1025C/D features temperature compensation via the external temperature sensing. The temperature of the inductor can be measured with an external temperature sense element placed close to the inductor. This information is used to adapt the gain of the current sense path to compensate for the increase in actual DCR.

3.3.7. Temperature Measurement

The ZSPM1025C/D features two independent temperature measurement units. The internal temperature sensing measures the temperature inside the IC; the external temperature sensing element is placed on the Murata OKLP-X/25-W12-C Power Block. The ZSPM1025C/D drives 60µA into the external temperature sensing element and measures the voltage on the TEMP pin.

3.4. Fault Monitoring and Response Generation

The ZSPM1025C/D monitors various signals for possible fault conditions during operation. The fault thresholds of the ZSPM1025C/D controllers are given in Table 3.3.

Table 3.3 Fault Configuration Overview

Signal	Fault Threshold
Output Over-Voltage Fault	125% of Nominal VOUT*
Output Under-Voltage Fault	75% of Nominal VOUT*
Input Over-Voltage Fault	13.80V
Input Under-Voltage Fault	7.00V
Over-Current Fault	30.0A
External Over-Temperature Fault	105°C
Internal Over-Temperature Fault	100°C

*Nominal VOUT is selected by the pin-strap resistor on the CONFIG0 pin.

The controller fault handling will infinitely try to restart the converter on a fault condition. In analog controllers, this infinite re-try feature is also known as "hiccup mode."

3.4.1. Output Over/Under Voltage

To prevent damage to the load, the ZSPM1025C/D utilizes an output over-voltage protection circuit. The voltage at VFBP is continuously compared with a configurable threshold using a high-speed analog comparator. If the voltage exceeds the configured threshold, the fault response is generated and the PWM output is set to low.

The ZSPM1025C/D also monitors the output voltage with a lower threshold. If the output voltage falls below the under-voltage fault level, a fault event is generated and the PWM output is set to low.

Note that the fault thresholds are stored in the ZSPM1025C/D as factors relative to the nominal output voltage. Hence, using the strapping options (see section 4.1) to change the output voltage level, also changes the fault thresholds.

3.4.2. Output Current Protection

The ZSPM1025C/D continuously monitors the average inductor current and utilizes this information to protect the power supply against excessive output current.

3.4.3. Over-Temperature Protection

The ZSPM1025C/D monitors internal and external temperature. For the temperature fault conditions a soft-off sequence is started. The soft-off sequence will ramp down the output voltage to 0V and set the PWM output in a tri-state condition.

3.5. Monitoring and Debugging via I²C™

The Pink Power Designer™ GUI can be used to monitor the internal measurement signals of the ZSPM1025C/D during the development phase. The status of the internal fault handler can also be monitored within the Pink Power Designer™ GUI.

The Pink Power Designer™ GUI communicates with the ZSPM1025C/D via an I²C™* interface in which the SCL signal is connected to the GPIO3 pin and the SDA signal is connected to the GPIO2 pin.

* I²C™ is a trademark of NXP.

4 Application Information

The ZSPM1025C/D controllers have been designed and pre-configured to operate with the Murata OKLP-X/25-W12-C Power Block, which is a complete point-of-load solution for 25A output currents. This section includes information about the typical application circuits and recommended component values.

The pin-strap configuration options for the ZSPM1025C/D are also documented in this section.

4.1. Typical Application Circuit

Schematics for the typical application circuits for the ZSPM1025C and ZSPM1025D respectively are shown in Figure 4.1 and Figure 4.2. A list of recommended component values for the passive components can be found in Table 4.1.

Figure 4.1 ZSPM1025C – Application Circuit with a 5V Supply Voltage

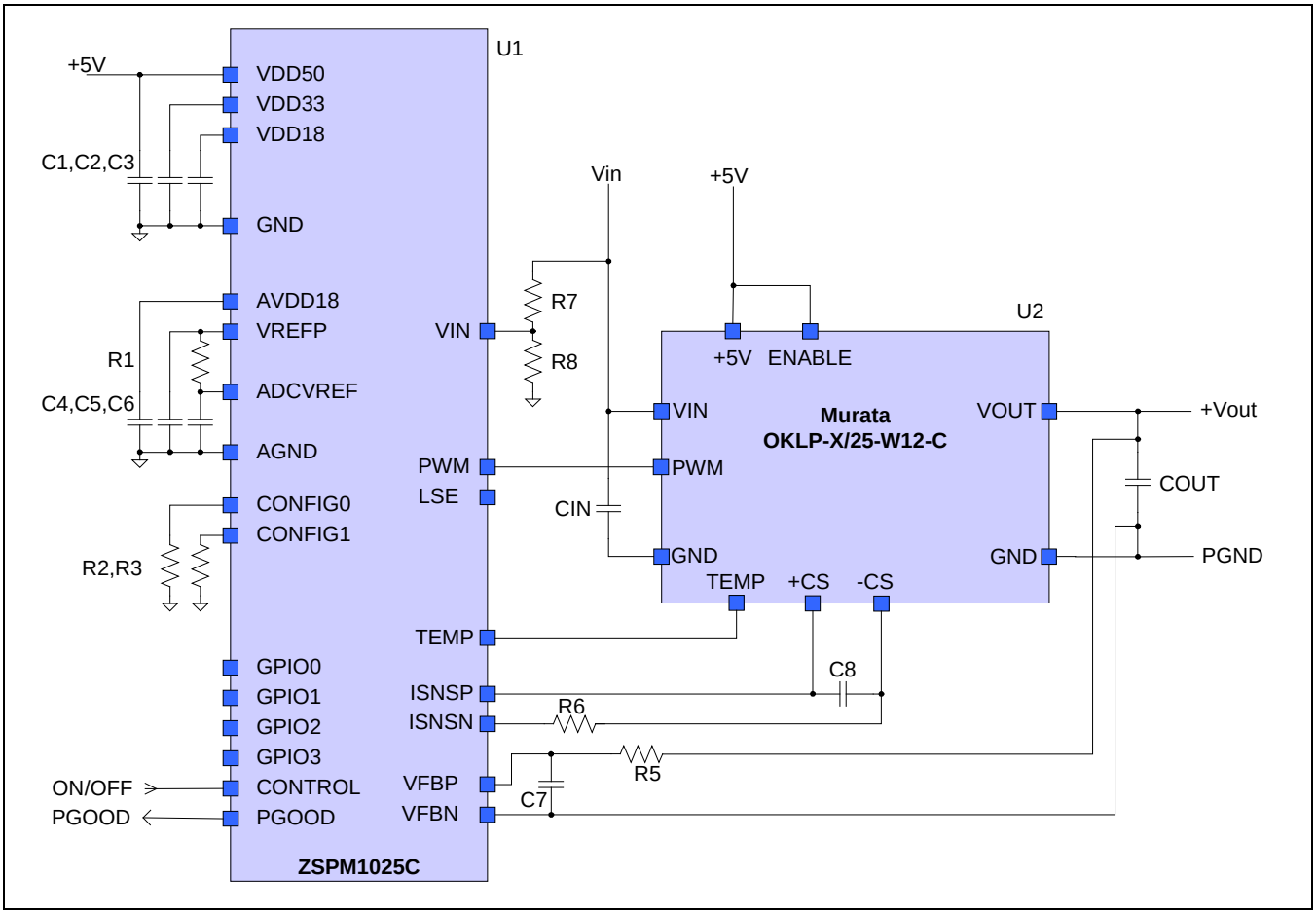


Figure 4.2 ZSPM1025D – Application Circuit with a 5V Supply Voltage

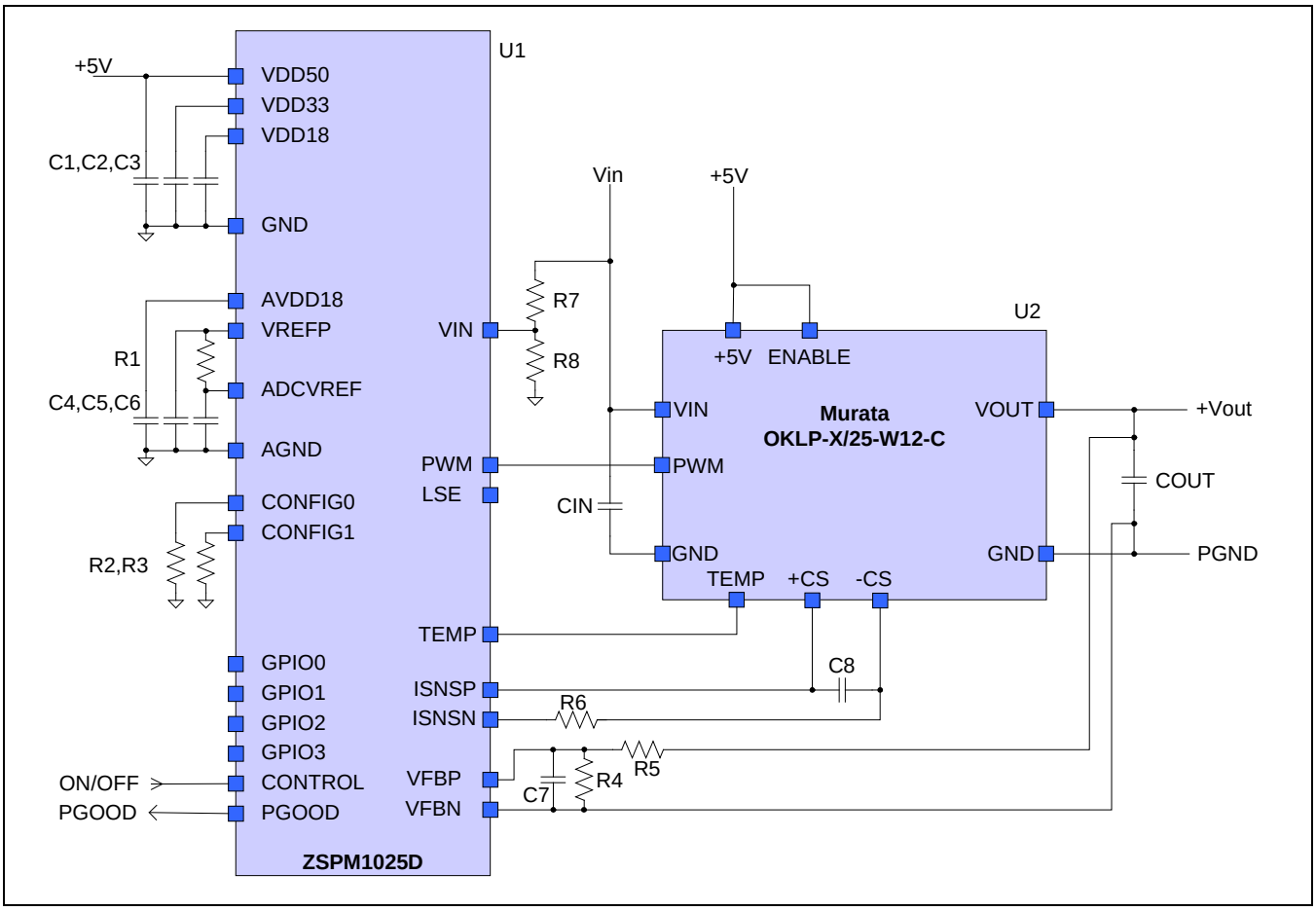


Table 4.1 Passive Component Values for the Application Circuits

Reference Designator	Component value	Description
C1	1.0µF	Ceramic capacitor.
C2	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C3	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C4	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C5	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C6	100nF	
C7	22pF	Output voltage sense filtering capacitor. Recommended 22pF; maximum 1nF.
C8	220nF*	DCR current-sense filter capacitor.
CIN		Input filter capacitors. Can be a combination of ceramic and electrolytic capacitors.
COUT		Output filter capacitors. See section 4.2.2 for more information on the output capacitor selection.
R1	51Ω*	
R2, R3		Pin-strap configuration resistors. See sections 4.2.1 and 4.2.2 for information on application-specific values.
R4	1.0kΩ*	Output voltage feedback divider bottom resistor. Connect between the VFBP and VFBN pins. *Important: R4 must not be used with the ZSPM1025C. If R4 is used with the ZSPM1025C, the output voltage will be much higher than the nominal output voltage.*
R5	1.75kΩ*	Output voltage feedback divider top resistor. Connect between the output terminal and the VFBP pin.
R6	2.15kΩ*	DCR current sense filter resistor.
R7	9.1kΩ*	Input voltage divider top resistor. Connect between the main power input and the VIN pin of the ZSPM1025C/D.
R8	1.0kΩ*	Input voltage divider bottom resistor. Connect between the VIN and AGND pins of the ZSPM1025C/D.

Notes:

** Fixed component values that must not be changed.*

4.2. Pin Strap Options of the ZSPM1025C/D

The ZSPM1025C/D provides two pin-strap configuration pins. The CONFIG0 pin is used to select the nominal output voltage of the non-isolated DC/DC converter. The CONFIG1 is used to select a set of compensation loop parameters in combination with the slew rate for the output voltage during the power-up sequence. There are four sets of compensation loop parameters that have been optimized for different ranges of output capacitance.

The CONFIG0 and CONFIG1 pins are used to determine the index of the selected values using the resistor values listed in Table 4.2. Each pin provides 30 configuration indexes based on resistor values from the E96 series. A resistor variation of ~2% is taken into account for initial tolerance and temperature dependency. The values are read during the initialization phase after a POR event and are then used to look up the selected index from the pre-configured look-up tables. Based on the index read by the ZSPM1025C/D, the controller will load the corresponding configuration from the OTP memory of the device.

Table 4.2 Pin Strap Resistor Values

Index	Resistor Value Using the E96 Series	Index	Resistor Value Using the E96 Series
0	0Ω	15	5.360kΩ
1	392Ω	16	6.040kΩ
2	576Ω	17	6.810kΩ
3	787Ω	18	7.680kΩ
4	1.000kΩ	19	8.660kΩ
5	1.240kΩ	20	9.530kΩ
6	1.500kΩ	21	10.50kΩ
7	1.780kΩ	22	11.80kΩ
8	2.100kΩ	23	13.00kΩ
9	2.430kΩ	24	14.30kΩ
10	2.800kΩ	25	15.80kΩ
11	3.240kΩ	26	17.40kΩ
12	3.740kΩ	27	19.10kΩ
13	4.220kΩ	28	21.00kΩ
14	4.750kΩ	29	23.20kΩ

4.2.1. CONFIG0 – Output Voltage

The nominal output voltage of the ZSPM1025C/D is set with a pin-strap resistor on the CONFIG0 pin. The selectable output voltages and the corresponding pin-strap resistor index are given in Table 4.3.

The nominal output voltage set points given for the ZSPM1025C are valid without an output voltage feedback divider. To achieve optimal performance the low pass filter consisting of resistor R5 and C7 (see Figure 4.1) should be included in the application circuit.

The nominal output voltage set points given for the ZSPM1025D are only valid if the resistors in the output voltage feedback divider, R4 and R5 (see Figure 4.2), have the resistances specified in Table 4.1.

Table 4.3 ZSPM1025C and ZSPM1025D - Nominal VOUT Pin-Strap Resistor Selection (CONFIG0 Pin)

Index	Resistor Value Using the E96 Series	Nominal VOUT – ZSPM1025C	Nominal VOUT – ZSPM1025D
0	0Ω	0.62 V	1.25 V
1	392Ω	0.64 V	1.30 V
2	576Ω	0.66 V	1.35 V
3	787Ω	0.68 V	1.40 V
4	1.000kΩ	0.70V	1.45 V
5	1.240kΩ	0.72V	1.50 V
6	1.500kΩ	0.74V	1.55 V
7	1.780kΩ	0.76 V	1.60 V
8	2.100kΩ	0.78 V	1.65 V
9	2.430kΩ	0.80 V	1.70 V
10	2.800kΩ	0.82V	1.75 V
11	3.240kΩ	0.84 V	1.80 V
12	3.740kΩ	0.86V	1.85 V
13	4.220kΩ	0.88 V	1.90 V
14	4.750kΩ	0.90 V	1.95 V
15	5.360kΩ	0.92 V	2.00 V
16	6.040kΩ	0.94 V	2.10 V
17	6.810kΩ	0.96 V	2.20 V
18	7.680kΩ	0.98 V	2.30 V
19	8.660kΩ	1.00 V	2.40 V
20	9.530kΩ	1.02 V	2.50 V
21	10.50kΩ	1.04 V	2.60 V
22	11.80kΩ	1.06 V	2.70 V
23	13.00kΩ	1.08 V	2.80 V
24	14.30kΩ	1.10 V	2.90 V
25	15.80kΩ	1.12 V	3.00 V
26	17.40kΩ	1.14V	3.10 V
27	19.10kΩ	1.16V	3.20 V
28	21.00kΩ	1.18 V	3.30 V
29	23.20kΩ	1.20 V	3.40 V

4.2.2. CONFIG1 – Compensation Loop and Output Voltage Slew Rate

The ZSPM1025C/D controllers can be configured to operate over a wide range of output capacitance. Four ranges of output capacitance have been specified to match typical customer requirements (see Table 4.4).

Typical performance measurements for both load transient performance and open-loop Bode plots can be found in section 4.3. Using less output capacitance than the minimum capacitance given in Table 4.4 is not recommended.

Table 4.4 Recommended Output Capacitor Ranges

Capacitor Range	Ceramic Capacitor	Bulk Electrolytic Capacitors
#1	Minimum 200µF Maximum 400µF	None
#2	Minimum 400µF Maximum 1000µF	None
#3	Minimum 100µF Maximum 600µF	Minimum 2 x 470µF, 7mΩ ESR Maximum 5 x 470µF, 7mΩ ESR
#4	Minimum 400µF Maximum 1000µF	Minimum 4 x 470µF, 7mΩ ESR Maximum 10 x 470µF, 7mΩ ESR

To get the optimal performance for a given output capacitor range, one of four sets of compensation loop parameters, Comp0 to Comp3, should be selected with a resistor between CONFIG1 and GND. The compensation loop parameters have been configured to ensure optimal transient performance and good control loop stability margins.

For each set of compensation loop parameters, there is a choice of seven slew rates for the output voltage during power-up. The selection of the slew rate can be used to limit the input current of the DC/DC converter while it is ramping up the output voltage. The current needed to charge the output capacitors increases in direct proportion to the slew rate.

Table 4.5 gives a complete list of the selectable compensation loop parameters and slew rates together with the equivalent pin-strap resistor values.

Table 4.5 ZSPM1025C and ZSPM1025D - Compensator and VOUT Slew Rate Pin Strap Resistor Selection

Index	Resistor Value Using the E96 Series	Compensator	VOUT Slew Rate
0	0Ω	Comp0 (Capacitor Range #1)	0.10 V/ms
1	392Ω		0.20 V/ms
2	576Ω		0.50 V/ms
3	787Ω		1.00 V/ms
4	1.000kΩ		2.00 V/ms
5	1.240kΩ		5.00 V/ms
6	1.500kΩ		10.00 V/ms
7	1.780kΩ	Comp1 (Capacitor Range #2)	0.10 V/ms
8	2.100kΩ		0.20 V/ms
9	2.430kΩ		0.50 V/ms
10	2.800kΩ		1.00 V/ms
11	3.240kΩ		2.00 V/ms
12	3.740kΩ		5.00 V/ms
13	4.220kΩ		10.00 V/ms
14	4.750kΩ	Comp2 (Capacitor Range #3)	0.10 V/ms
15	5.360kΩ		0.20 V/ms
16	6.040kΩ		0.50 V/ms
17	6.810kΩ		1.00 V/ms
18	7.680kΩ		2.00 V/ms
19	8.660kΩ		5.00 V/ms
20	9.530kΩ		10.00 V/ms
21	10.50kΩ	Comp3 (Capacitor Range #4)	0.10 V/ms
22	11.80kΩ		0.20 V/ms
23	13.00kΩ		0.50 V/ms
24	14.30kΩ		1.00 V/ms
25	15.80kΩ		2.00 V/ms
26	17.40kΩ		5.00 V/ms
27	19.10kΩ		10.00 V/ms
28	21.00kΩ	Comp0	0.10 V/ms
29	23.20kΩ		0.10 V/ms

4.3. Typical Performance Measurements for the ZSPM1025C and ZSPM1025D

The pre-programmed compensation loop parameters for the ZSPM1025C and ZSPM1025D have been designed to ensure stability and optimal transient performance for the OKLP-X/25-W12-C Power Block from Murata in combination with one of the four output capacitor ranges (see Table 4.4).

Load transient performance measurements and open-loop Bode plots for the ZSPM1025C can be found in sections 4.3.1 to 4.3.4. The transient load steps have been generated with a load resistor and a power MOSFET located on the same circuit board as the ZSPM1025C and the Murata OKLP-X/25-W12-C Power Block. The ZSPM8725-KIT evaluation kit can be used to further evaluate the performance of the ZSPM1025C for the four output capacitor ranges.

Load transient performance measurements and open-loop Bode plots for the ZSPM1025D are shown in sections 4.3.5 to 4.3.8. The transient load steps have been generated with a load resistor and a power MOSFET located on the same circuit board as the ZSPM1025D and the Murata OKLP-X/25-W12-C Power Block. The ZSPM8825-KIT evaluation kit can be used to further evaluate the performance of the ZSPM1025D for the four output capacitor ranges.

4.3.1. Typical Load Transient Response – ZSPM1025C – Capacitor Range #1 – Comp0

Test conditions: V_{IN} = 12.0V, V_{OUT} = 1.20V
Minimum output capacitance: 2 x 100µF/6.3V X5R
Maximum output capacitance: 3 x 100µF/6.3V X5R + 2 x 47µF/10V X7R

Figure 4-3 5 to 15A Load Step – Min. Capacitance

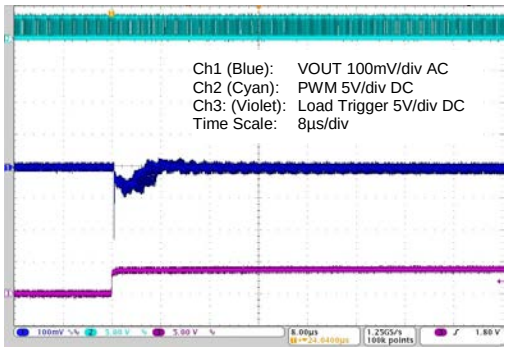


Figure 4-4 15 to 5A Load Step – Min. Capacitance

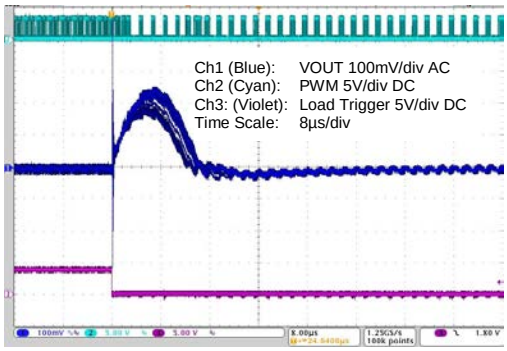


Figure 4-5 5 to 15A Load Step – Max. Capacitance

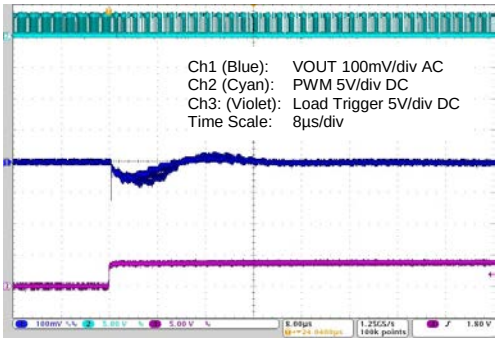


Figure 4-6 15 to 5A Load Step – Max. Capacitance

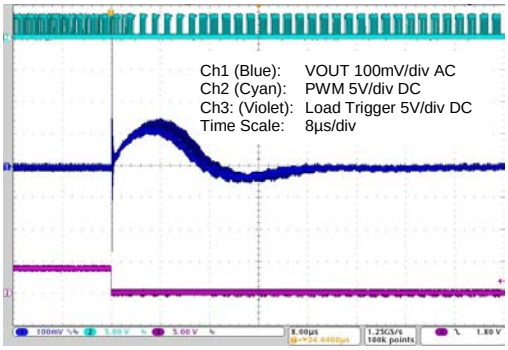
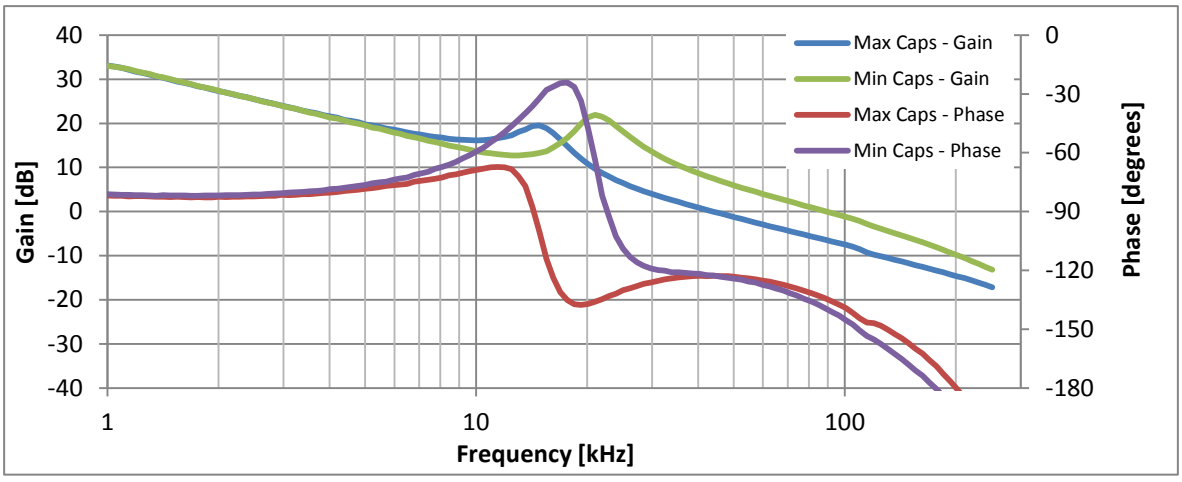


Figure 4-7 Open Loop Bode Plots



4.3.2. Typical Load Transient Response – ZSPM1025C – Capacitor Range #2 – Comp1

Test conditions: V_{IN} = 12.0V, V_{OUT} = 1.20V
Minimum output capacitance: 3 x 100µF/6.3V X5R + 2 x 47µF/10V X7R
Maximum output capacitance: 7 x 100µF/6.3V X5R + 4 x 47µF/10V X7R

Figure 4-8 5 to 15A Load Step – Min. Capacitance

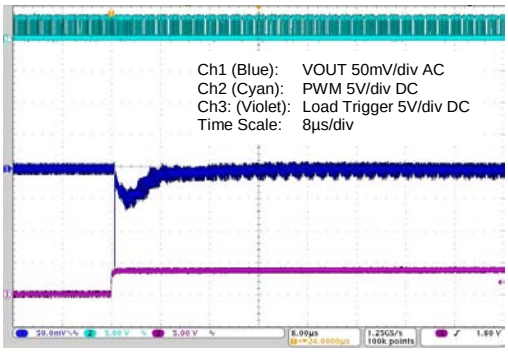


Figure 4-9 15 to 5A Load Step – Min. Capacitance

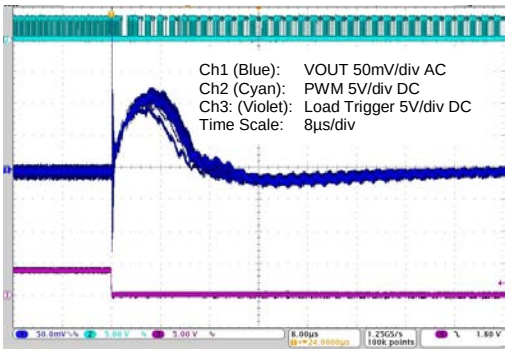


Figure 4-10 5 to 15A Load Step – Max. Capacitance

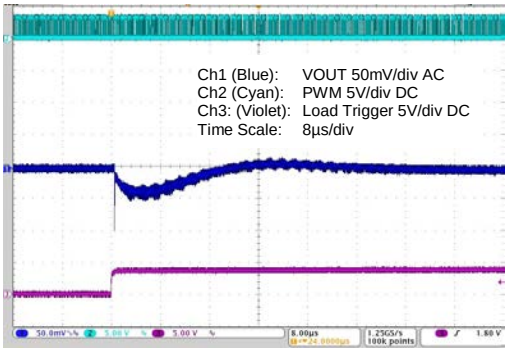


Figure 4-11 15 to 5A Load Step – Max. Capacitance

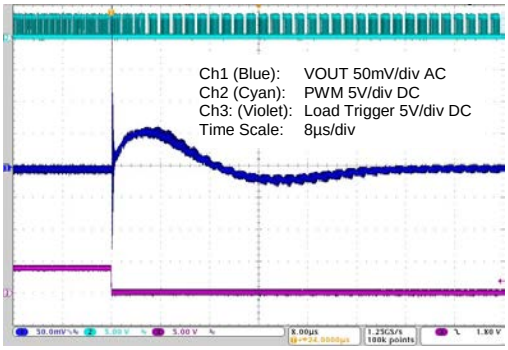
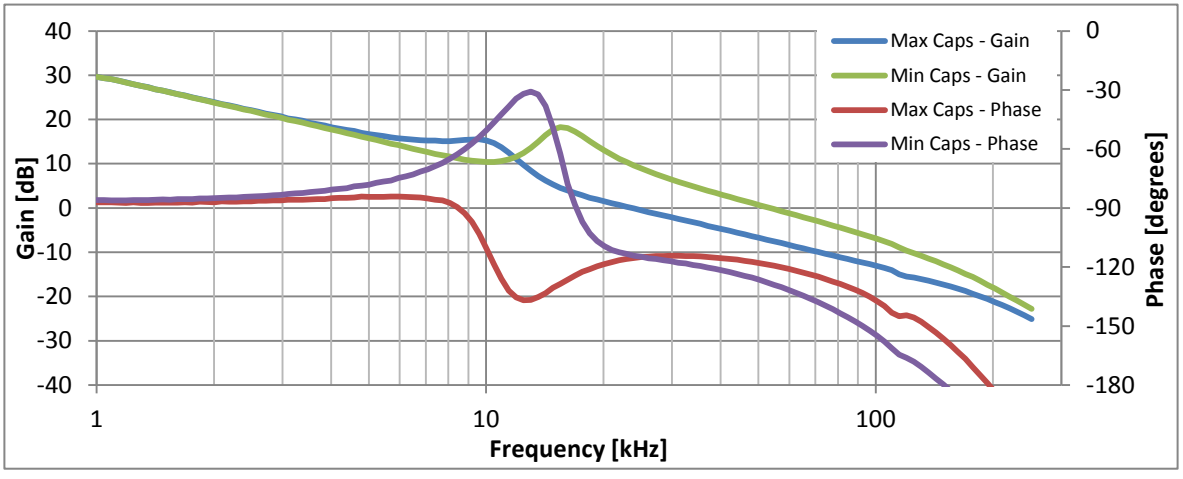


Figure 4-12 Open Loop Bode Plots



4.3.3. Typical Load Transient Response – ZSPM1025C – Capacitor Range #3 – Comp2

Test conditions: V_{IN} = 12.0V, V_{OUT} = 1.20V
Minimum output capacitance: 1 x 100µF/6.3V X5R + 2 x 470 µF/6.3V/7mΩ Aluminum Electrolytic Capacitor
Maximum output capacitance: 6 x 100 µF/6.3V X5R + 5 x 470 µF/6.3V/7mΩ Aluminum Electrolytic Capacitor

Figure 4-13 5 to 15A Load Step – Min. Capacitance

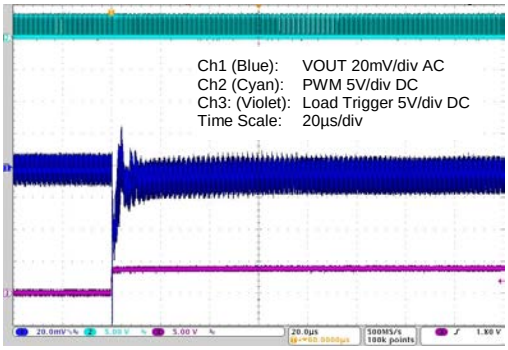


Figure 4-14 15 to 5A Load Step – Min. Capacitance

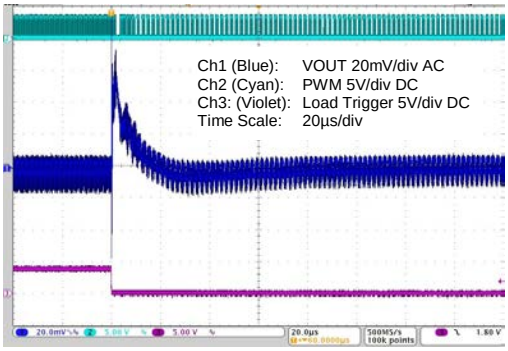


Figure 4-15 5 to 15A Load Step – Max. Capacitance

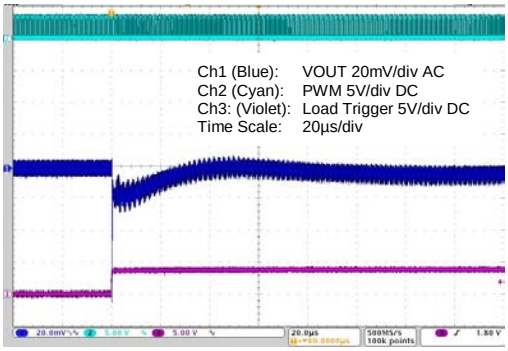


Figure 4-16 15 to 5A Load Step – Max. Capacitance

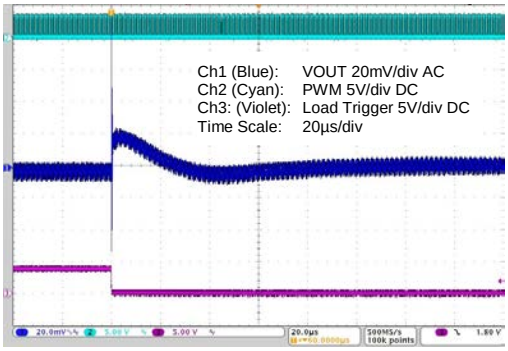
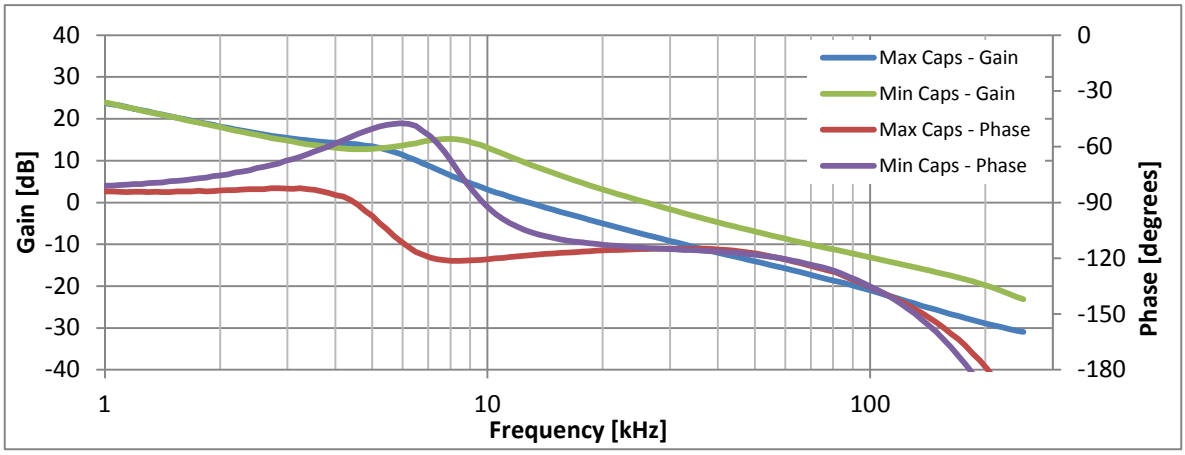


Figure 4-17 Open Loop Bode Plots



4.3.4. Typical Load Transient Response – ZSPM1025C – Capacitor Range #4 – Comp3

Test conditions: V_{IN} = 12.0V, V_{OUT} = 1.20V
Minimum output capacitance: 3 x 100µF/6.3V X5R + 2 x 47µF/10V X7R + 4 x 470 µF/6.3V/7mΩ Aluminum Electrolytic Capacitor
Maximum output capacitance: 7 x 100 µF/6.3V X5R + 4 x 47µF/10V X7R + 10 x 470 µF/6.3V/7mΩ Aluminum Electrolytic Capacitor

Figure 4-18 5 to 15A Load Step – Min. Capacitance

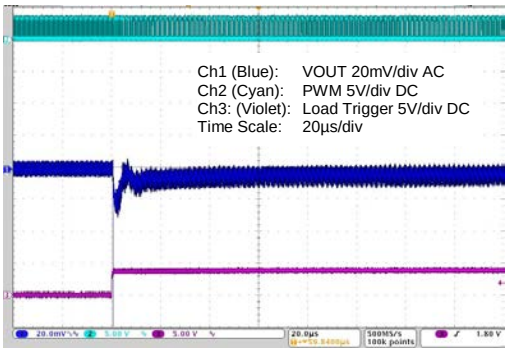


Figure 4-19 15 to 5A Load Step – Min. Capacitance

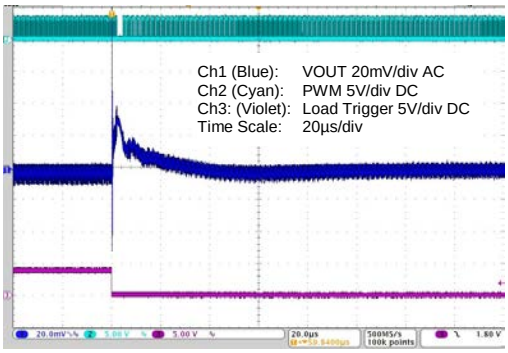


Figure 4-20 5 to 15A Load Step – Max. Capacitance

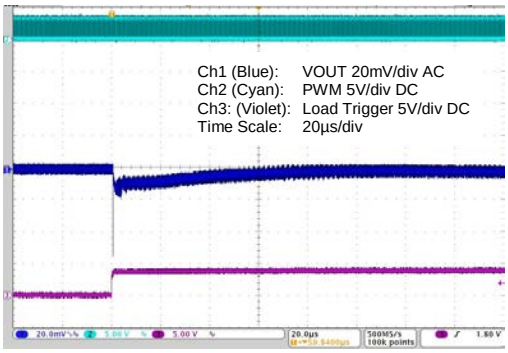


Figure 4-21 15 to 5A Load Step – Max. Capacitance

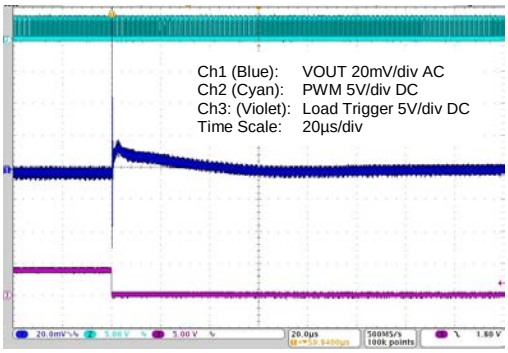
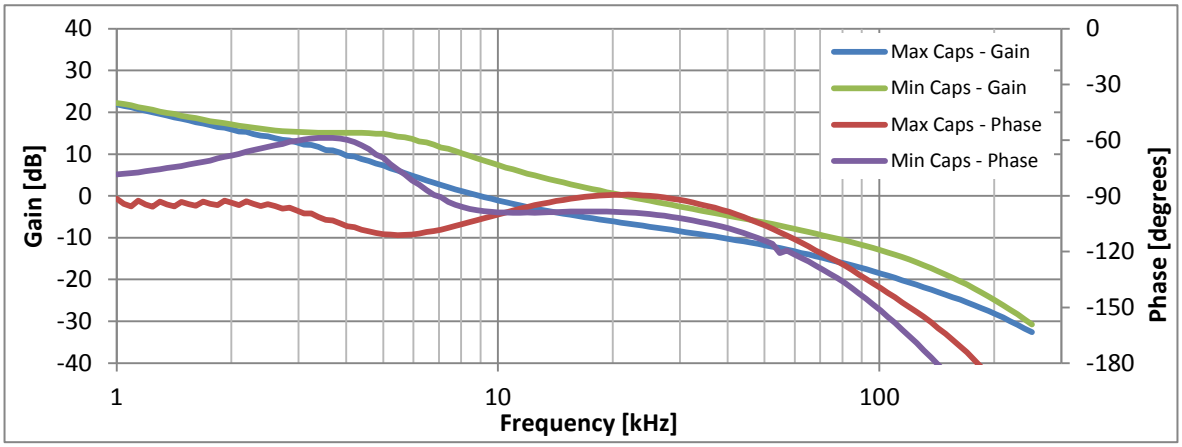


Figure 4-22 Open Loop Bode Plots



4.3.5. Typical Load Transient Response – ZSPM1025D – Capacitor Range #1 – Comp0

Test conditions: V_{IN} = 12.0V, V_{OUT} = 1.80V
Minimum output capacitance: 2 x 100µF/6.3V X5R
Maximum output capacitance: 3 x 100µF/6.3V X5R + 2 x 47µF/10V X7R

Figure 4-23 5 to 20A Load Step – Min. Capacitance

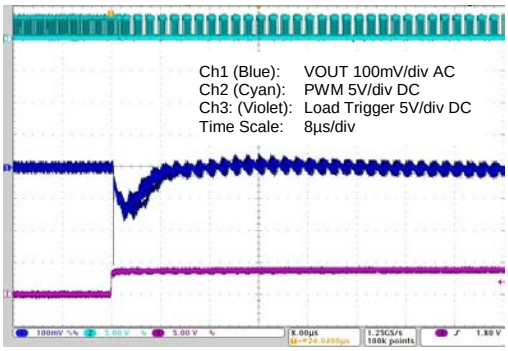


Figure 4-24 20 to 5A Load Step – Min. Capacitance

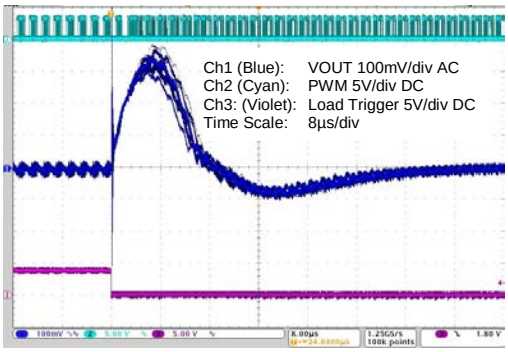


Figure 4-25 5 to 20A Load Step – Max. Capacitance

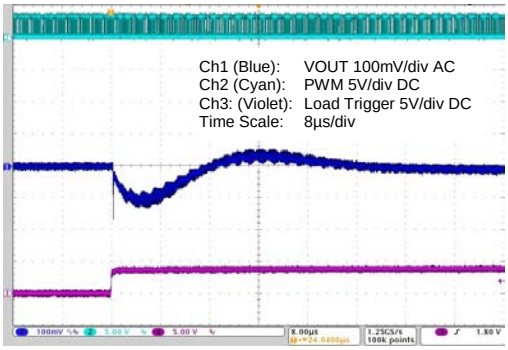


Figure 4-26 20 to 5A Load Step – Max. Capacitance

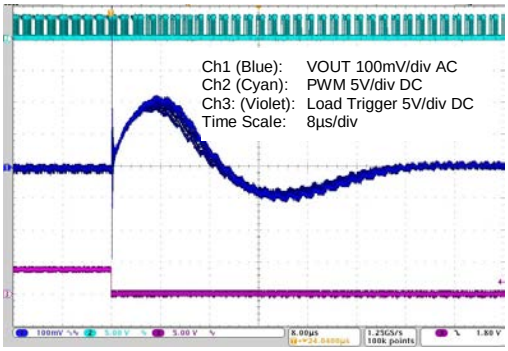
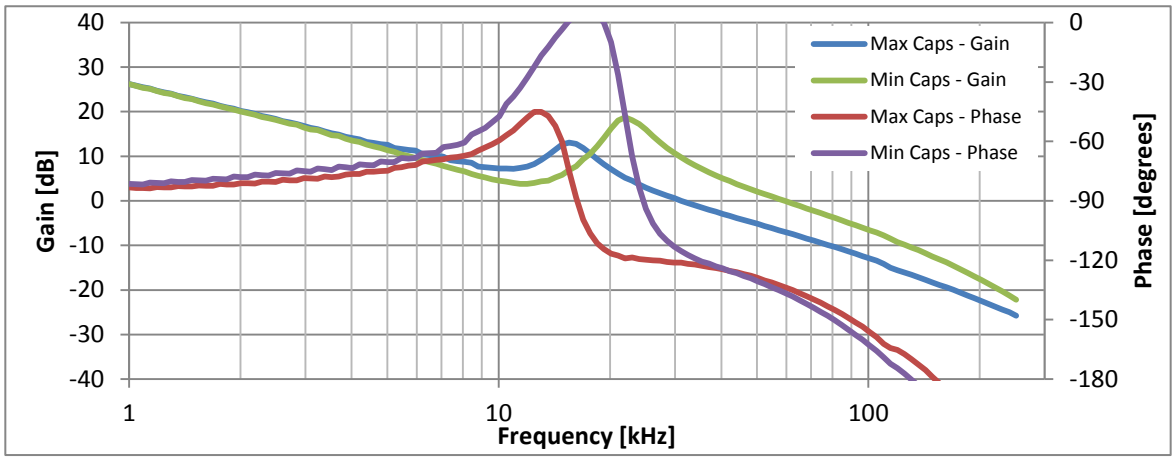


Figure 4-27 Open Loop Bode Plots



4.3.6. Typical Load Transient Response – ZSPM1025D – Capacitor Range #2 – Comp1

Test conditions: V_{IN} = 12.0V, V_{OUT} = 1.80V
Minimum output capacitance: 3 x 100µF/6.3V X5R + 2 x 47µF/10V X7R
Maximum output capacitance: 7 x 100µF/6.3V X5R + 4 x 47µF/10V X7R

Figure 4-28 5 to 20A Load Step – Min. Capacitance

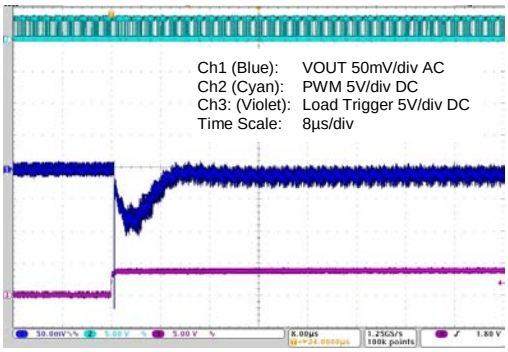


Figure 4-29 20 to 5A Load Step – Min. Capacitance

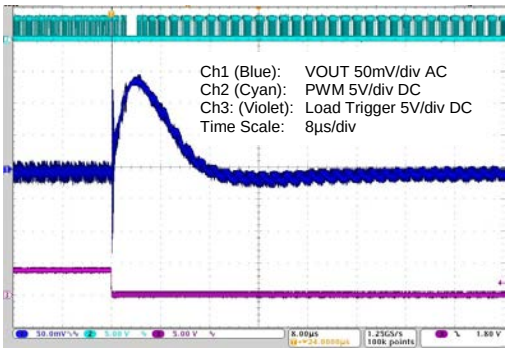


Figure 4-30 5 to 20A Load Step – Max. Capacitance

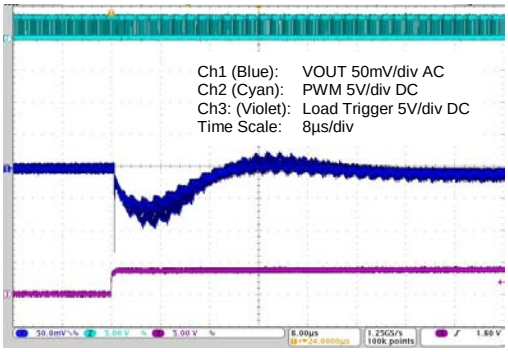


Figure 4-31 20 to 5A Load Step – Max. Capacitance

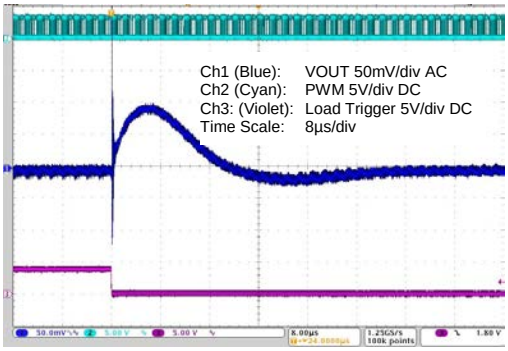
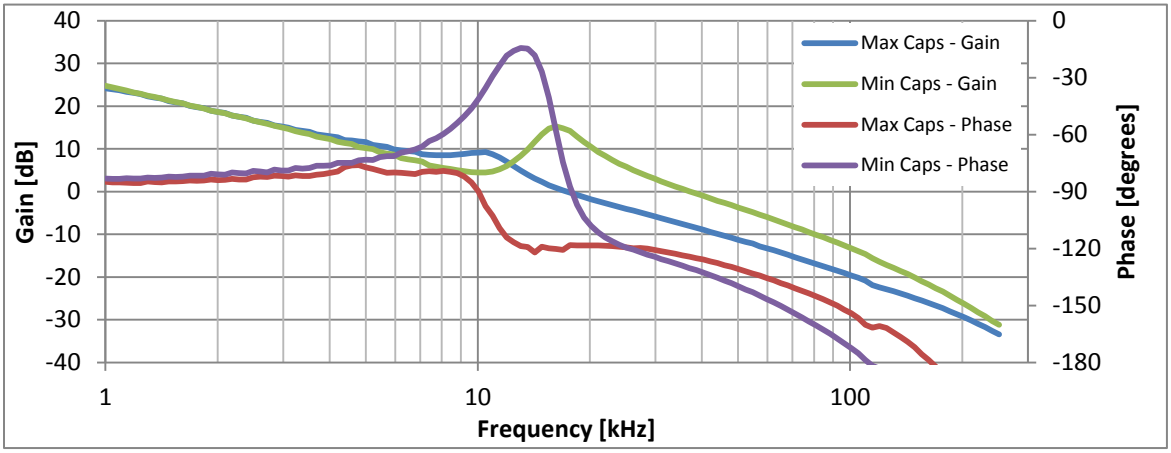


Figure 4-32 Open Loop Bode Plots



4.3.7. Typical Load Transient Response – ZSPM1025D – Capacitor Range #3 – Comp2

Test conditions: V_{IN} = 12.0V, V_{OUT} = 1.80V
Minimum output capacitance: 1 x 100µF/6.3V X5R + 2 x 470 µF/6.3V/7mΩ Aluminum Electrolytic Capacitor
Maximum output capacitance: 6 x 100 µF/6.3V X5R + 5 x 470 µF/6.3V/7mΩ Aluminum Electrolytic Capacitor

Figure 4-33 5 to 20A Load Step – Min. Capacitance

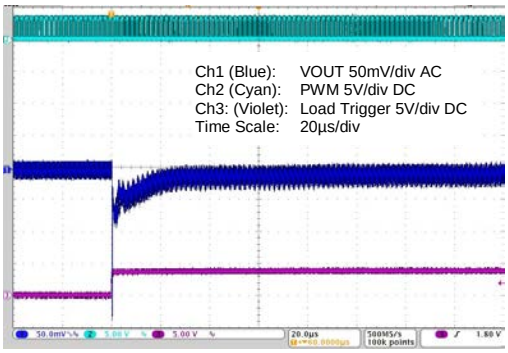


Figure 4-34 20 to 5A Load Step – Min. Capacitance

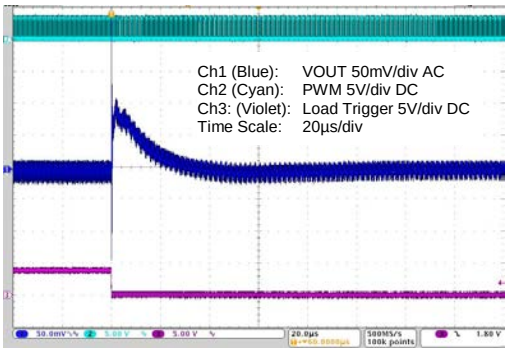


Figure 4-35 5 to 20A Load Step – Max. Capacitance

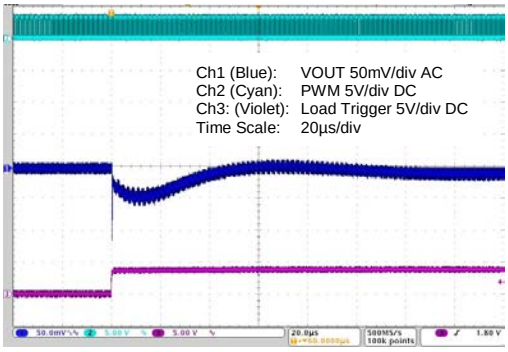


Figure 4-36 20 to 5A Load Step – Max. Capacitance

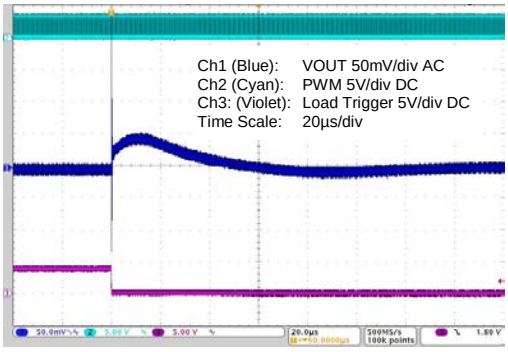
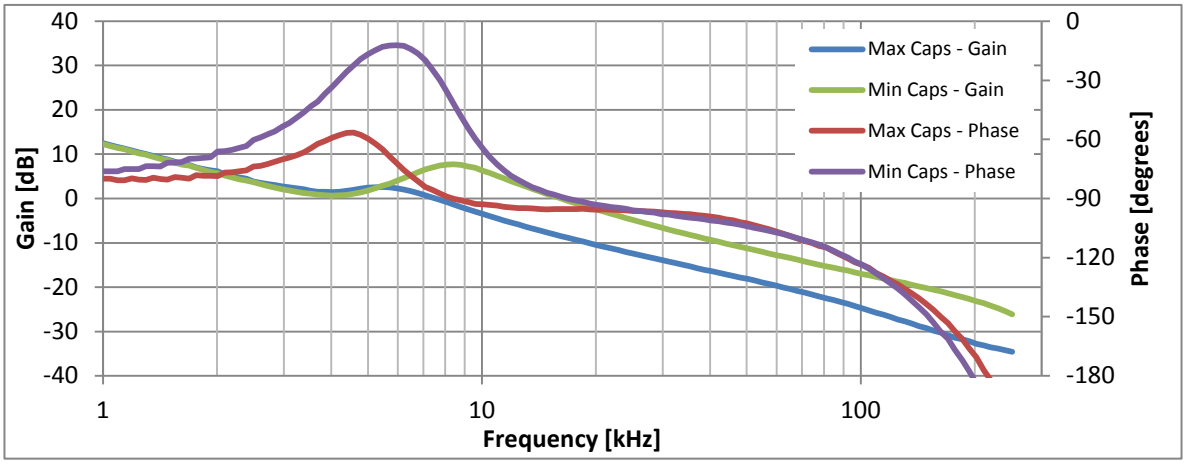


Figure 4-37 Open Loop Bode Plots



4.3.8. Typical Load Transient Response – ZSPM1025D – Capacitor Range #4 – Comp3

Test conditions: V_{IN} = 12.0V, V_{OUT} = 1.80V
Minimum output capacitance: 3 x 100µF/6.3V X5R + 2 x 47µF/10V X7R + 4 x 470 µF/6.3V/7mΩ Aluminum Electrolytic Capacitor
Maximum output capacitance: 7 x 100 µF/6.3V X5R + 4 x 47µF/10V X7R + 10 x 470 µF/6.3V/7mΩ Aluminum Electrolytic Capacitor

Figure 4-38 5 to 20A Load Step – Min. Capacitance

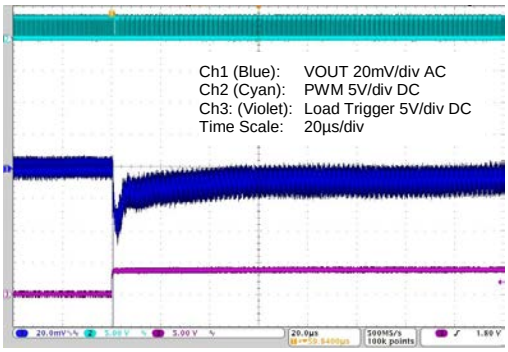


Figure 4-39 20 to 5A Load Step – Min. Capacitance

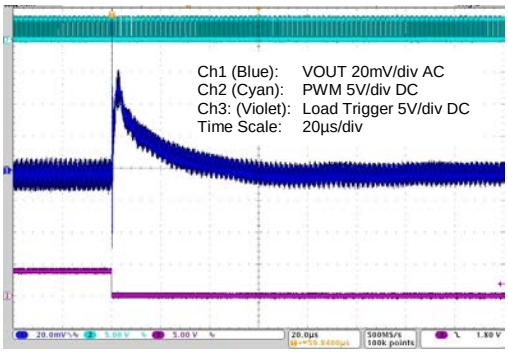


Figure 4-40 5 to 20A Load Step – Max. Capacitance

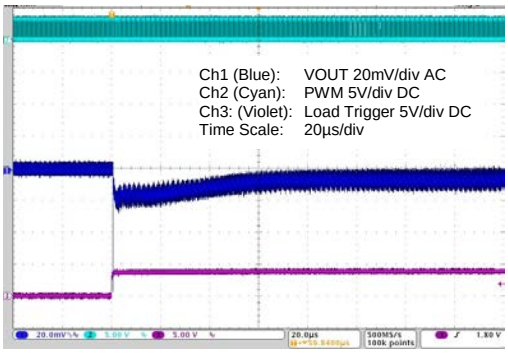


Figure 4-41 20 to 5A Load Step – Max. Capacitance

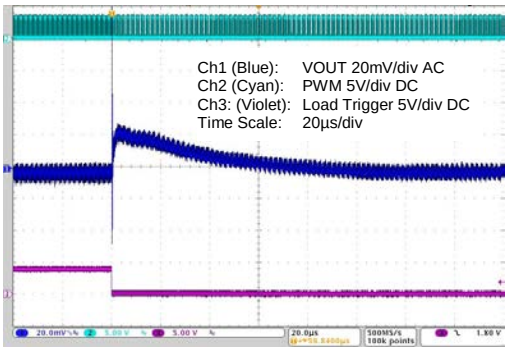
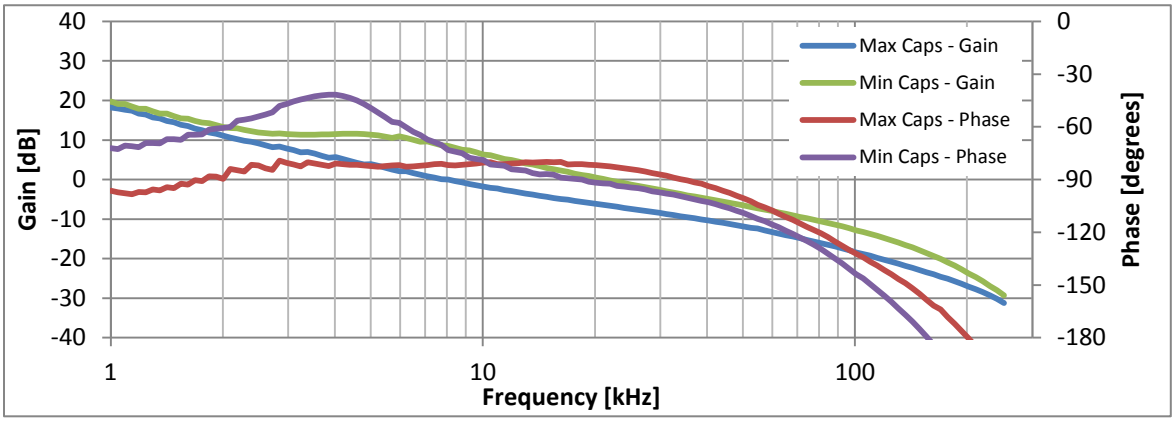


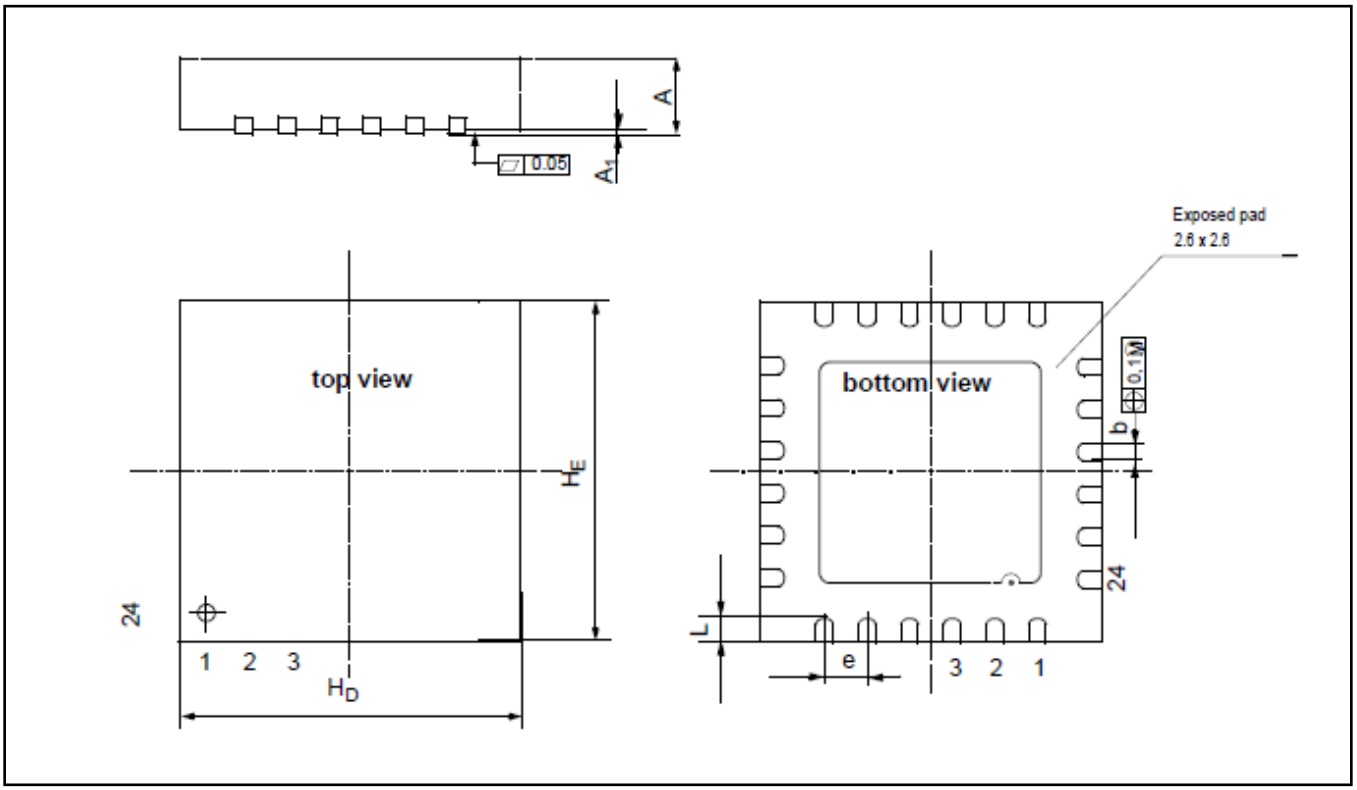
Figure 4-42 Open Loop Bode Plots



5 Mechanical Specifications

Based on JEDEC MO-220. All dimensions are in millimeters.

Figure 5.1 24-pin QFN Package Drawing



Dimension	Min (mm)	Max (mm)
A	0.8	0.90
A_1	0.00	0.05
b	0.18	0.30
e	0.5 nominal	
H_D	3.90	4.1
H_E	3.90	4.1
L	0.35	0.45

6 Glossary

Term	Description
DPWM	Digital Pulse-Width Modulator
DCR	DC Resistance
FET	Field-Effect Transistor
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
HKADC	Housekeeping Analog-To-Digital Converter
OT	Over-Temperature
OTP	One-Time Programmable Memory
OV	Over-Voltage
PID	Proportional/Integral/Derivative
POR	Power-On-Reset
SCR	Sub-cycle Response™
SLC	State-Law Control™
SPM	Smart Power Management

7 Ordering Information

Sales Code	Description	Package
ZSPM1025CA1W 0	ZSPM1025C Lead-free QFN24 — Temperature range: -40°C to +125°C	7” Reel
ZSPM1025DA1W 0	ZSPM1025D Lead-free QFN24 — Temperature range: -40°C to +125°C	7” Reel
ZSPM8725-KIT	Evaluation Kit for ZSPM1025C with PMBus™ Communication Interface *	Kit
ZSPM8825-KIT	Evaluation Kit for ZSPM1025D with PMBus™ Communication Interface *	Kit

* Pink Power Designer™ GUI for kit can be downloaded from the IDT web site at www.IDT.com/ZSPM1025C or www.IDT.com/ZSPM1025D.

8 Related Documents

Document
ZSPM1025C/D Feature Sheet
ZSPM1025 and ZSPM1035 Family Feature Sheet
ZSPM8725 Kit Description (for ZSPM1025C only)
ZSPM8825 Kit Description (for ZSPM1025D only)
ZSPM1025C/D Pink Power Designer™ GUI Guide

Visit the following product pages on IDT's website or contact your nearest sales office for the latest version of these documents.

Product pages:

www.IDT.com/ZSPM1025C

www.IDT.com/ZSPM1025D

9 Document Revision History

Revision	Date	Description
1.00	October 28, 2013	First release.
1.01	October 15, 2014	Update for cover/header imagery and contacts. Update for kit contents. Update for related documents in section 8.
	January 22, 2016	Changed to IDT branding.

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