

PROTECTION PRODUCTS - RailClamp®

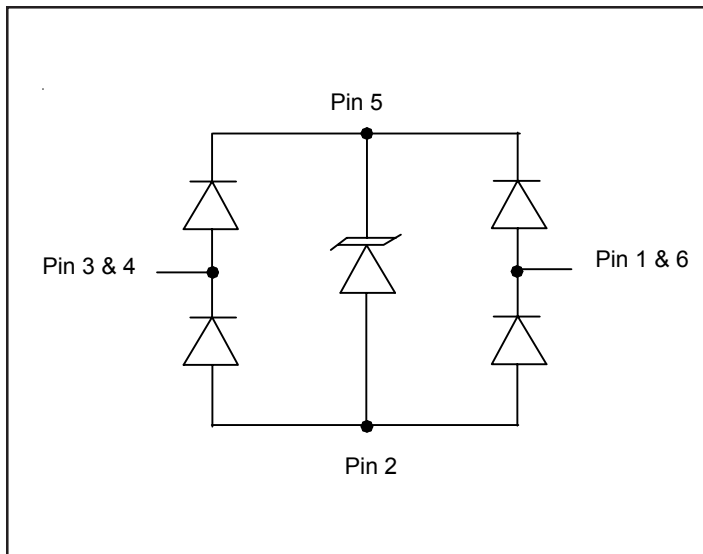
Description

The RailClamp® series consists of ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **CDE** (Cable Discharge Events), and **EFT** (electrical fast transients). They are designed for use in applications where board space is at a premium. Each device requires less than 2.9mm² of PCB area and will protect two high speed data lines.

The monolithic design incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. Each line has a typical capacitance of 0.9pF to ground and 0.3pF between lines. The capacitance of each line is well matched for constant signal balance. Signal integrity is further preserved with the flow through design. A connection to the TVS is provided for protection of external voltage busses, such as those found in USB applications. This device is optimized for ESD protection of portable electronics. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

The RClamp0502A is in a 6-pin, RoHS/WEEE compliant, SC-89 (SOT-666) package. It measures 1.6 x 1.6 x 0.6mm. The leads are finished with lead-free matte tin. The small package makes it ideal for use in portable electronics such as cell phones, laptops, and digital still cameras.

Circuit Diagram



Features

- ◆ Transient protection for high-speed data lines to **IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns)**
- ◆ Flow through design for ease of layout for high speed data line application
- ◆ Protects up to two I/O lines & power line
- ◆ Low capacitance (**<0.9pF**) for high-speed interfaces
- ◆ Ultra-small package requires less than 2.9mm² of PCB area
- ◆ Low leakage current and clamping voltage
- ◆ Low operating voltage: 5.0V
- ◆ Solid-state silicon-avalanche technology

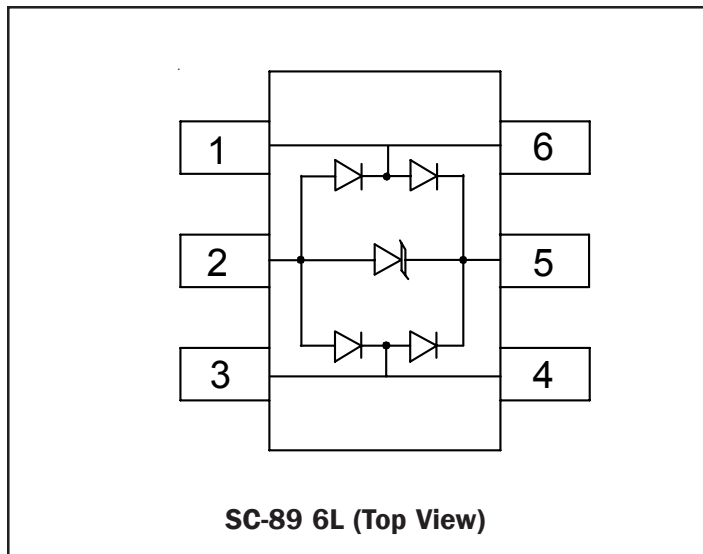
Mechanical Characteristics

- ◆ SC-89 (SOT-666) package
- ◆ RoHS/WEEE Compliant
- ◆ Lead Finish: Matte Tin
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking: A
- ◆ Packaging: Tape and Reel

Applications

- ◆ USB 2.0 High Speed
- ◆ 10/100/1000 Ethernet Ports
- ◆ High-Definition Multimedia Interface (HDMI)
- ◆ Digital Visual Interface (DVI)
- ◆ Monitors and Flat Panel Displays
- ◆ Video Graphics Cards
- ◆ IEEE 1394 Firewire Ports High Speed

Schematic & PIN Configuration



PROTECTION PRODUCTS
Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{pk}	50	Watts
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{pp}	3	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 15 ± 8	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

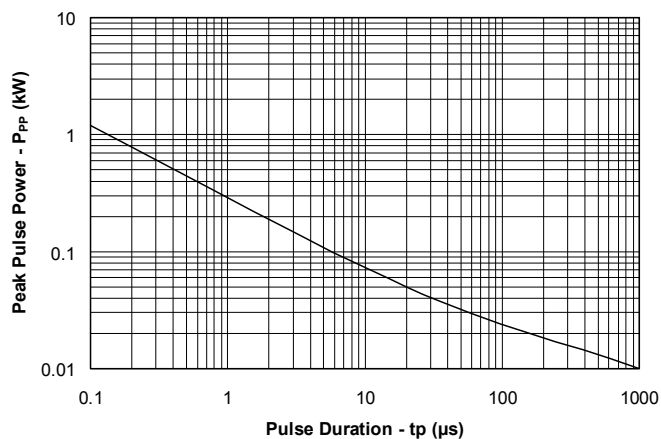
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Between I/O lines to Gnd or I/O to I/O			5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$ Between I/O lines to Gnd	6			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T = 25^\circ C$ Between I/O lines to Gnd or I/O to I/O			1	μA
Clamping Voltage	V_C	$I_{pp} = 1A, t_p = 8/20\mu s$ Between I/O lines to Gnd			14	V
Clamping Voltage	V_C	$I_{pp} = 3A, t_p = 8/20\mu s$ Between I/O to Gnd			16	V
Clamping Voltage	V_C	$I_{pp} = 3A, t_p = 8/20\mu s$ Between I/O to I/O			18	V
Junction Capacitance	C_j	$V_R = 0V, f = 1MHz$ Between I/O to Gnd			0.9	pF
Junction Capacitance	C_j	$V_R = 0V, f = 1MHz$ Between I/O to I/O		0.3	0.7	pF

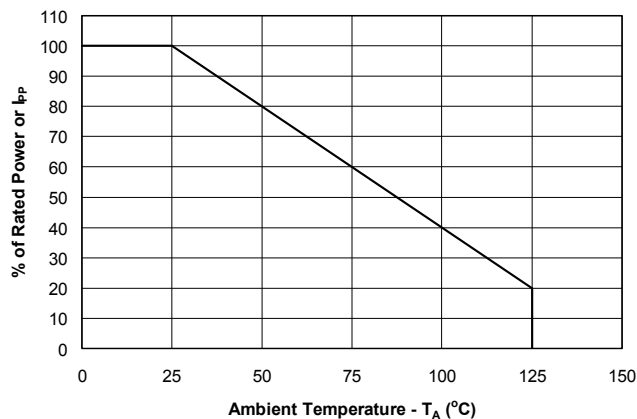
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Typical Characteristics

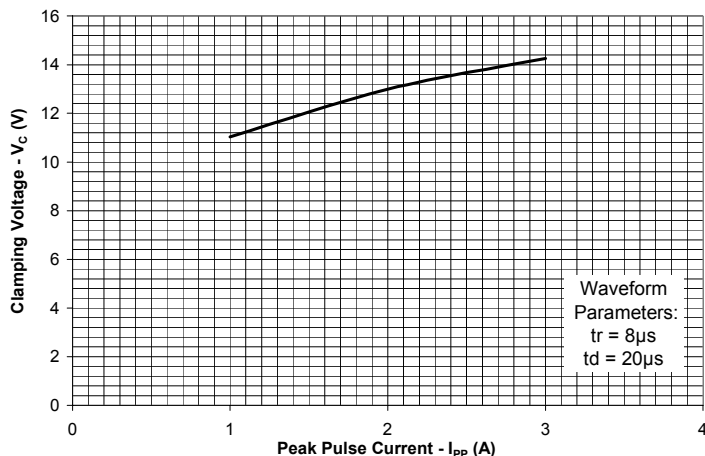
Non-Repetitive Peak Pulse Power vs. Pulse Time



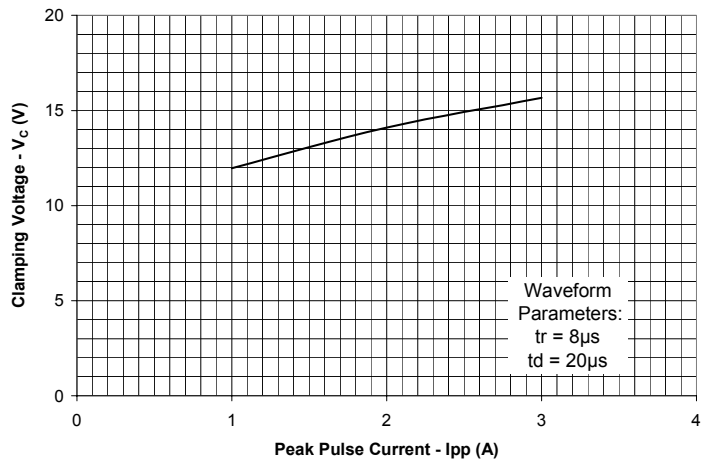
Power Derating Curve



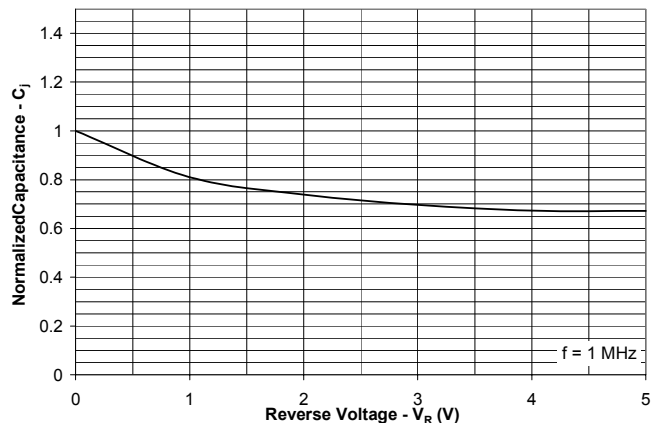
**Clamping Voltage vs. Peak Pulse Current
I/O to Gnd - Pin 1, 3, 4, 6 to Pin 2**



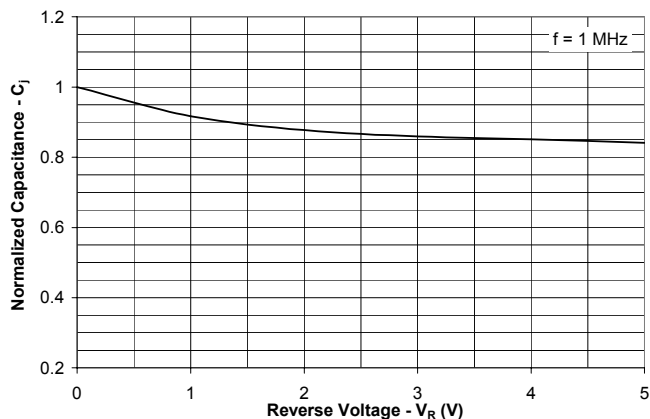
**Clamping Voltage vs. Peak Pulse Current
I/O to I/O**



**Normalized Capacitance vs. Reverse Voltage
I/O to Gnd - Pin 1, 3, 4, or 6 to Pin 2**



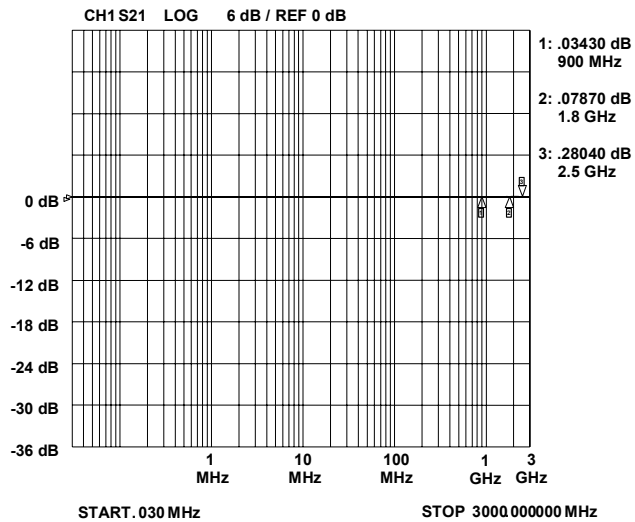
**Normalized Capacitance vs. Reverse Voltage
I/O to I/O**



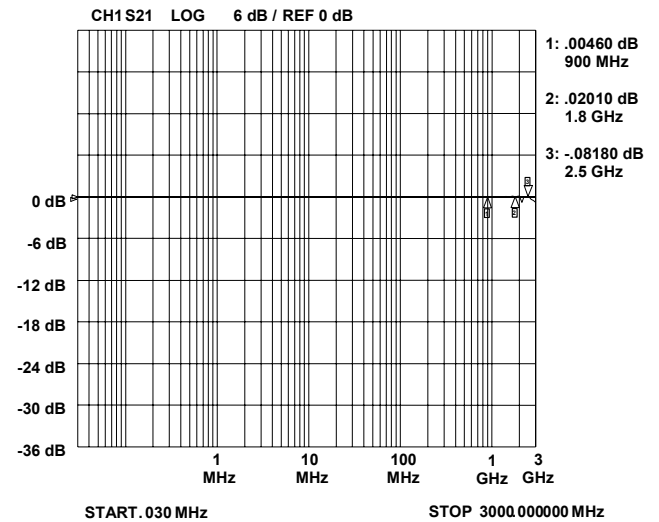
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Typical Characteristics

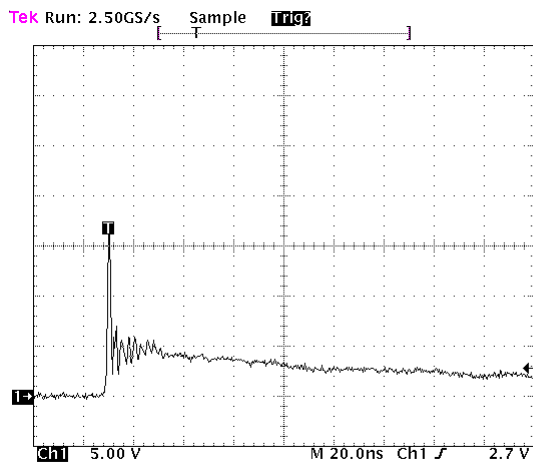
Insertion Loss S21 (I/O to I/O)



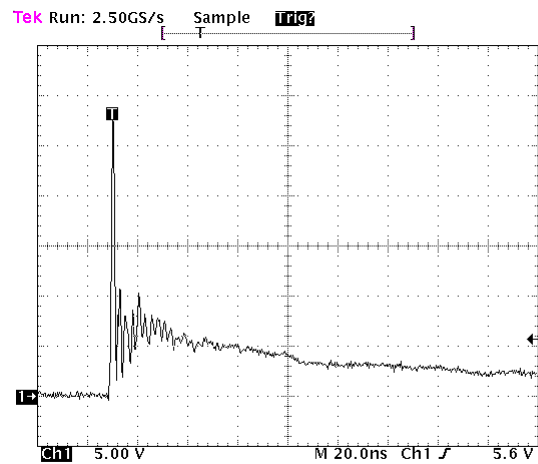
Insertion Loss S21 (I/O to Gnd)



ESD Response (4kV Contact per IEC 61000-4-2)



ESD Response (8kV Contact per IEC 61000-4-2)



PROTECTION PRODUCTS

Applications Information

Device Connection Options for Protection of Two High-Speed Data Lines

This device is designed to protect data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1 & 6 and pins 3 & 4. Pins 5 and 2 can be connected to ground or Vcc based on application and location of those connections. The connection to ground should be made directly to a ground plane. The path length should also be kept as short as possible to minimize parasitic inductance. Figure 1 shows the layout configuration to send data input at pins 6 and 4 and output at pins 1 and 3.

This device is designed for ease of PCB layout by allowing the traces run straight through the device. Figure 2 shows the proper way to design the PCB board trace in order to use the flow through layout for two line pairs. The solid line represents the PCB trace. Note the PCB traces are used to connect the pin pairs for each I/O (pin 1 to pin 6 and pins 3 to pin 4). For example, I/O 1 enters at pin 6 and exits at pin 1 and the PCB trace connects pins 6 and 1 together. This is also true for I/O 2. The negative reference (Gnd) is connected at pin 2. The positive reference is connected at pin 5.

Universal Serial Bus ESD Protection

The RClamp0502A may also be used to protect both upstream and downstream USB ports on monitors, computers, peripherals or portable systems. Each device will protect up to one USB port (Figure 3). When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.

Figure 1. Protection of Two Data Lines and One Power Supply Line

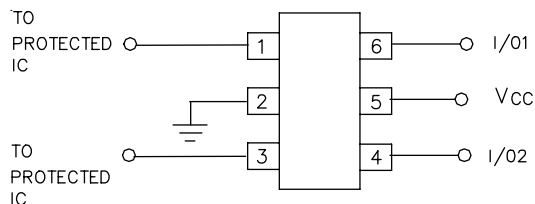


Figure 2. Flow Through Layout for Two Data Lines and one Power Line

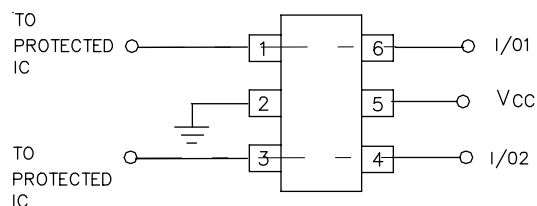
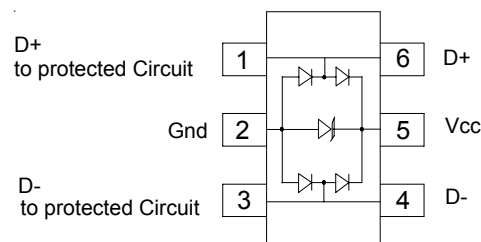


Figure 3. USB 2.0 (up to 480Mbps) Upstream or Downstream Port Protection



Matte Tin Lead Finish

Matte tin has become the industry standards lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

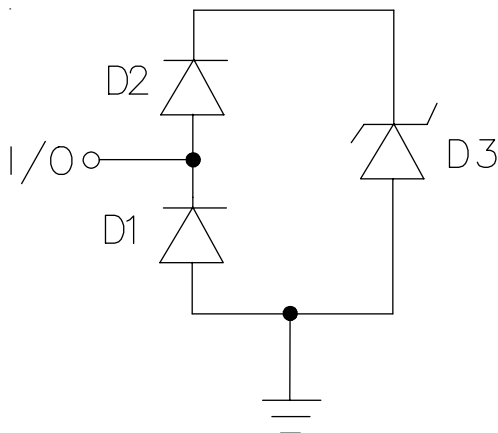
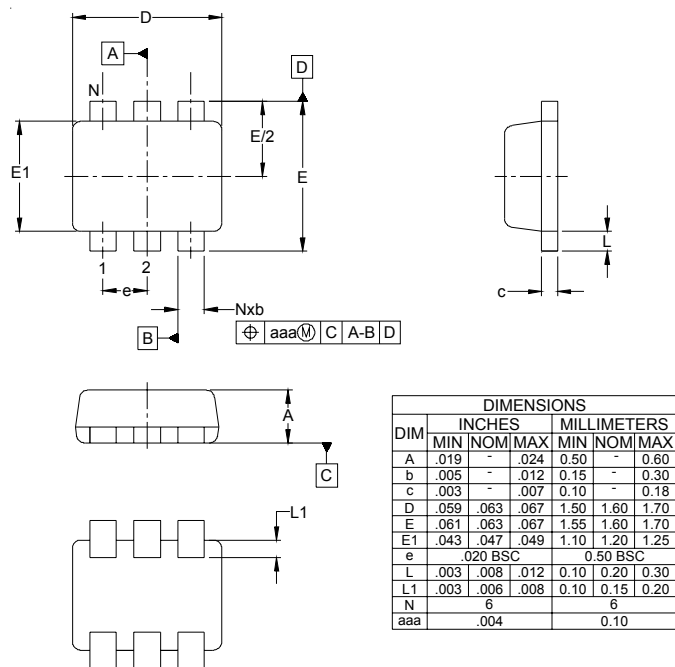
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Applications Information - Spice Model

Figure 1 - RClamp0502A Spice Model

Table 1 - RClamp0502A Spice Parameters				
Parameter	Unit	D1 (LCRD)	D2 (LCRD)	D3 (TVS)
IS	Amp	1E-20	1E-20	2.43E-13
BV	Volt	110	20	8
VJ	Volt	0.67	0.67	0.64
RS	Ohm	0.339	0.568	1.24
IBV	Amp	1E-3	1E-3	1E-3
CJO	Farad	0.7E-12	0.7E-12	83E-12
TT	sec	2.541E-9	2.541E-9	2.541E-9
M	--	0.01	0.01	0.222
N	--	1.1	1.1	1.1
EG	eV	1.11	1.11	1.11

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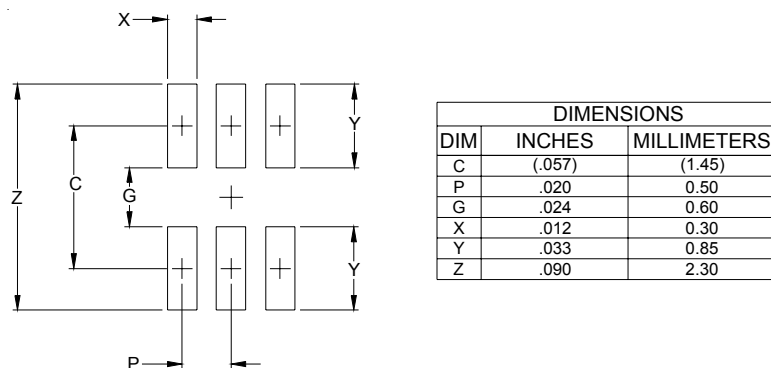
Outline Drawing - SC-89 (SOT-666)



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

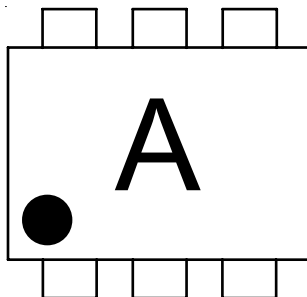
Land Pattern - SC-89 (SOT-666)



NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking

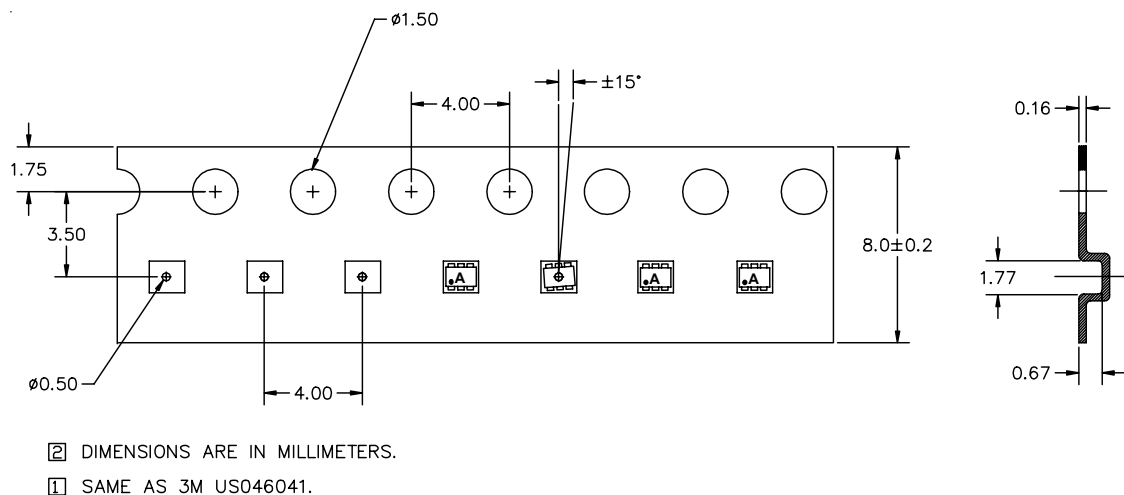


Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
RClamp0502A.TCT	Pb Free	3,000	7 Inch

RailClamp and RClamp are registered marks of Semtech Corporation

Tape and Reel Specification



Tape Specification and Device Orientation

Contact Information

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