

Features

- High-speed, low-noise, non-inverting split 1-10 buffer
- Maximum Frequency up to 250 MHz
- Low output skew < 60ps (Bank A, 2.5V)
- Low duty cycle distortion < 200ps
- Low propagation delay < 2.0ns (2.5V)
- Choice of 1.2V, 1.5V, 1.8V or 2.5V supply voltage on Bank A, Bank B, Bank C
- Industrial temperature range: -40°C to 85°C
- Packages (Pb-free & Green): 20-pin, TSSOP (L20)
20-pin, SSOP (H20)
20-pin, QSOP (Q20)

Description

The PI6C10810 is a 1.2V to 2.5V high-speed, low-noise 1-10 non-inverting clock buffer. The key goal in designing the PI6C10810 is to target networking applications that require low-skew, low-jitter, and high-frequency clock distribution.

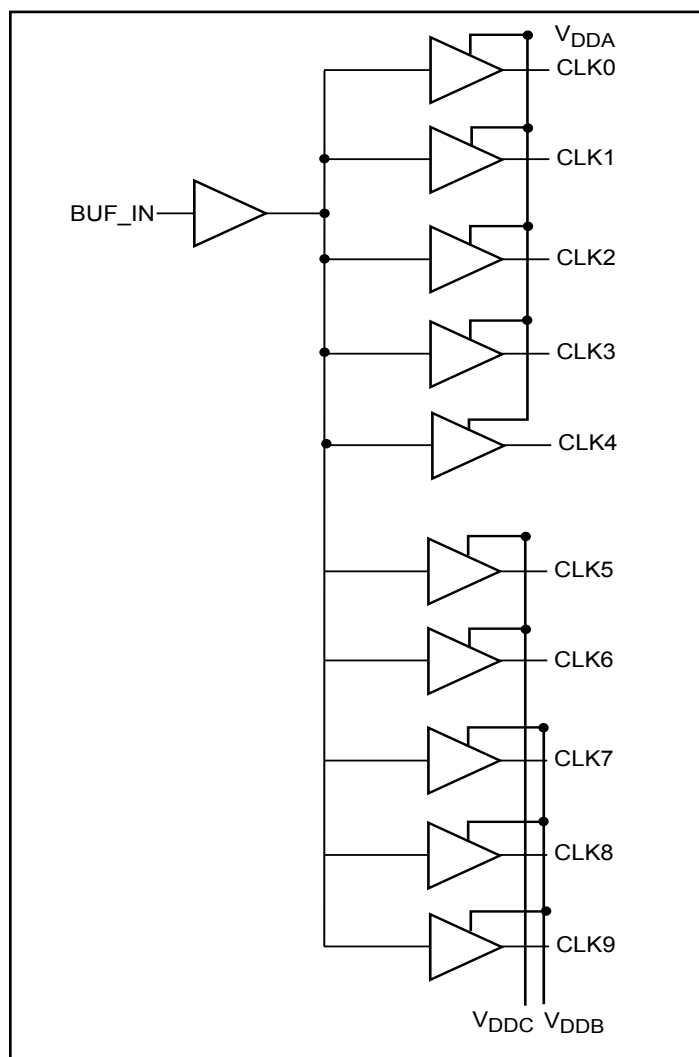
Providing output-to-output skew as low as 60ps, the PI6C10810 is an ideal clock distribution device for synchronous systems. Designing synchronous networking systems requires a tight level of skew from a large number of outputs.

CLK0-4 operate from V_{DDA} supply.

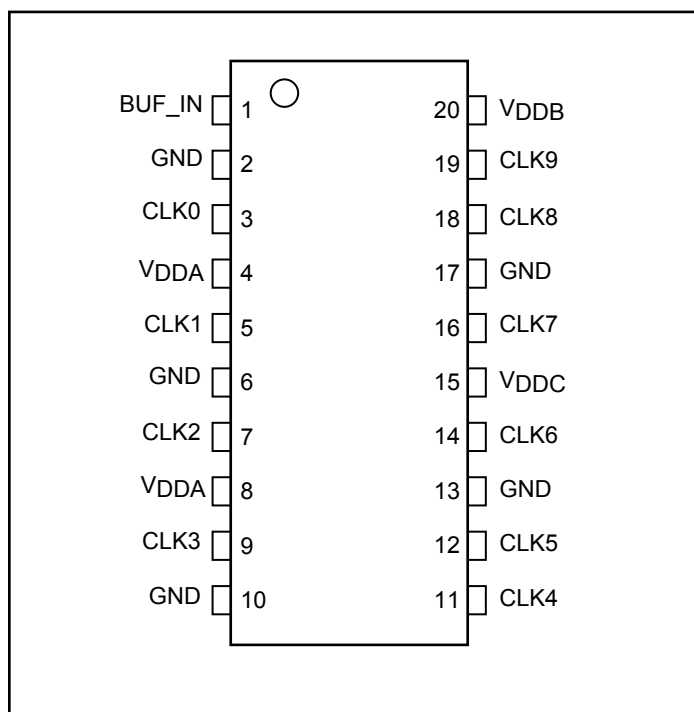
CLK5-6 operate from V_{DDC} supply.

CLK7-9 operate from V_{DDB} supply.

Block Diagram



Pin Configuration



Pin Description

Pin Name	Description
BUF_IN	Input
CLK [0:9]	Outputs
GND	Ground
V_{DDA} , V_{DDB} , V_{DDC}	Power (1.2V, 1.5V, 1.8V, 2.5V)

2.5V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C
V _{DD} Voltage	-0.5V to +3.6V
Output Voltage (max. 3.6V)	-0.5V to V _{DD} +0.5V
Input Voltage (max 3.6V).....	-0.5V to V _{DD} +0.5V

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.5V DC Characteristics (Over Operating Range: V_{DDA}, V_{DDB}, V_{DDC} = 2.5V ± 0.2V, T_A = -40° to 85°C)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
V _{DD}	Supply Voltage			2.3	2.5	2.7	
V _{IH}	Input HIGH Voltage	Logic HIGH level		1.7		3.6	V
V _{IL}	Input LOW Voltage	Logic LOW level		-0.3		0.7	
I _I	Input Current	V _{DD} = Max, V _{in} = V _{DD} or GND	I pin			15	μA
V _{OH}	Output High Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -1mA	2.0			V
			I _{OH} = -2mA	1.7			
			I _{OH} = -8mA	1.7			
V _{OL}	Output LOW Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 1mA			0.1	
			I _{OL} = 2mA			0.2	
			I _{OL} = 8mA			0.2	

Notes:

- For Max. or Min. conditions, use appropriate operating range values.
- Typical values are at V_{DD} = 2.5V, +25°C ambient and maximum loading.

2.5V AC Characteristics (Over Operating Range: V_{DDA}, V_{DDB}, V_{DDC} = 2.5V ± 0.2V, T_A = -40° to 85°C)

Parameters	Description		Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
F _{IN}	Input Frequency			0		250	MHz
t _{PLH} , t _{PHL} ⁽²⁾	Propagation Delay BUF_IN to CLKn		R _L = 500-Ohm, C _L = 3pF, 125 MHz Out-puts are measured @ V _{DD} /2	1.0	1.5	2.0	
t _{SK(O)} ⁽³⁾	Output to Output Skew between any two outputs of the same device @ same transition	Bank A (CLK0 - CLK4)		−60		60	ps
		Bank C (CLK5 - CLK6)		−30		30	
		Bank B (CLK7 - CLK9)		−150		150	
t _{SK(P)} ⁽³⁾	Pulse Skew between opposite transitions (t _{PHL} -t _{PLH}) of the same output				100	200	
t _{SK(T)} ⁽³⁾⁽⁵⁾	Part to Part Skew between two identical outputs of different parts on the same board ⁽⁴⁾					300	
t _{dc_in}	Duty Cycle In @ Ins edge rate			45		55	%
t _{dc_out}	Duty Cycle Out			40		57.5	
t _j ⁽⁵⁾	Additive Jitter					50	ps
t _{R(O)}	Output Rise Time 20%-80% CLKn		R _L = 500-Ohm, C _L = 3pF		0.5	0.7	ns
t _{F(O)}	Output Fall Time 80%-20% CLKn				0.5	0.7	

Notes:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew measured at worst case temperature (max. temp).
- Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
- Guaranteed by design

1.8V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C
V _{DD} Voltage	-0.5V to +2.5V
Output Voltage (max 2.5V)	-0.5V to V _{DD} +0.5V
Input Voltage (max 2.5V)	-0.5V to V _{DD} +0.5V

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1.8V DC Characteristics (Over Operating Range: V_{DDA}, V_{ddb}, V_{DDC} = 1.8V ± 0.15V, T_A = -40° to 85°C)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
V _{DD}	Supply Voltage			1.65	1.8	1.95	
V _{IH}	Input HIGH Voltage	Logic HIGH level		1.1		2.7	V
V _{IL}	Input LOW Voltage	Logic LOW level		-0.3		0.35*V _{DD}	
I _I	Input Current ⁽³⁾	V _{DD} = Max, V _{in} = V _{DD} or GND	I pin			15	μA
V _{OH}	Output High Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -2mA	1.35			V
			I _{OH} = -8mA	1.2			
V _{OL}	Output LOW Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 2mA			0.1	
			I _{OL} = 8mA			0.2	

Notes:

- For Max. or Min. conditions, use appropriate operating V_{DD} and T_A values.
- Typical values are at V_{DD} = 1.8V, +25°C ambient and maximum loading.
- This parameter is determined by device characterization but is not production tested.

1.8V AC Characteristics (Over Operating Range: V_{DDA}, V_{ddb}, V_{DDC} = 1.8V ± 0.15V, T_A = -40° to 85°C)

Parameters	Description		Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
F _{IN}	Input Frequency			0		200	MHz
t _{PLH} , t _{PHL} ⁽²⁾	Propagation Delay BUF_IN to CLKn		C _L = 3pF, R _L = 500-Ohm, 125 MHz Outputs are measured @ V _{DD} /2	1.0	2.3	2.8	
t _{SK(O)} ⁽³⁾	Output to Output Skew between any two outputs of the same device @ same transition	Bank A (CLK0 - CLK4)		−60		60	ps
		Bank C (CLK5 - CLK6)		30		30	
		Bank B (CLK7 - CLK9)		−200		200	
t _{SK(P)} ⁽³⁾	Pulse Skew between opposite transitions (t _{PHL} -t _{PLH}) of the same output				100	200	
t _{SK(T)} ⁽³⁾⁽⁵⁾	Part to Part Skew between two identical outputs of different parts on the same board ⁽⁴⁾					300	
t _{dc_in}	Duty Cycle In @ 1 ns edge rate			45		55	%
t _{dc_out}	Duty Cycle Out			40		57.5	
t _j ⁽⁵⁾	Additive Jitter					50	ps
t _{R(o)}	Output Rise Time 20% - 80% CLKn				0.5	0.8	ns
t _{F(o)}	Output Fall Time 80% - 20% CLKn				0.5	0.8	

Notes:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew measured at worst case temperature (max. temp).
- Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
- Guaranteed by design.

1.5V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C	Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
V _{DD} Voltage	-0.5V to +3.6V	
Output Voltage (max. 3.6V)	-0.5V to V _{DD} +0.5V	
Input Voltage (max 3.6V).....	-0.5V to V _{DD} +0.5V	

1.5V DC Characteristics (Over Operating Range: V_{DDA}, V_{DDB}, V_{DDC} = 1.5V ± 0.1V, T_A = -40° to 85°C)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
V _{DD}	Supply Voltage			1.4	1.5	1.6	
V _{IH}	Input HIGH Voltage	Logic HIGH level		0.65×V _{DD}		V _{DD}	V
V _{IL}	Input LOW Voltage	Logic LOW level		-0.3		0.35×V _{DD}	
I _I	Input Current	V _{DD} = Max, V _{in} = V _{DD} or GND	I pin			15	μA
V _{OH}	Output High Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -2mA	1.05			V
			I _{OH} = -8mA	1.75			
V _{OL}	Output LOW Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 2mA			0.35	
			I _{OL} = 8mA			0.65	

Notes:

- For Max. or Min. conditions, use appropriate operating range values.
- Typical values are at V_{DD} = 1.5V, +25°C ambient and maximum loading.

1.5V AC Characteristics (Over Operating Range: V_{DDA}, V_{DDB}, V_{DDC} = 1.5V ± 0.1V, T_A = -40° to 85°C)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ	Max.	Units
F _{IN}	Input Frequency			0		200	MHz
t _R /t _F	CLKn Rise/Fall Time	20% to 80%				1.0	ns
t _{PLH} , t _{PHL} ⁽²⁾	Propagation Delay BUF_IN to CLKn			2.0	2.8	3.5	ns
t _{SK(O)} ⁽³⁾	Output to Output Skew between any two outputs of the same device @ same transition	Bank A (CLK0 - CLK4)		-100		100	ps
		Bank C (CLK5 - CLK6)		-50		50	
		Bank B (CLK7 - CLK9)		-200		200	
t _{SK(P)} ⁽³⁾	Pulse Skew between opposite transitions (t _{PHL} -t _{PLH}) of the same output	C _L = 3pF, R _L = 500-Ohms, 125 MHz Outputs are measured @ V _{DD} /2			100	200	
t _{SK(T)} ⁽³⁾⁽⁵⁾	Part to Part Skew between two identical outputs of different parts on the same board ⁽⁴⁾					300	
t _{dc_in}	Duty Cycle In @ Ins edge rate			45		55	%
t _{dc_out} ⁽⁵⁾	Duty Cycle Out			40		60	
t _j	Additive Jitter					50	ps
t _{R(o)}	Output Rise Time 20% - 80% CLKn				0.6	0.9	ns
t _{F(o)}	Output Fall Time 80% - 20% CLKn				0.6	0.9	

Notes:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew measured at worst case temperature (max. temp).
- Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
- Guaranteed by design.

1.2V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C
V _{DD} Voltage	-0.5V to +3.6V
Output Voltage (max. 3.6V)	-0.5V to V _{DD} +0.5V
Input Voltage (max 3.6V).....	-0.5V to V _{DD} +0.5V

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1.2V DC Characteristics (Over Operating Range: V_{DDA}, V_{DDB}, V_{DDC} = 1.2V ± 0.1V, T_A = -40° to 85°C)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
V _{DD}	Supply Voltage			1.1	1.2	1.3	
V _{IH}	Input HIGH Voltage	Logic HIGH level		0.65×V _{DD}		V _{DD} +0.3	V
V _{IL}	Input LOW Voltage	Logic LOW level		-0.3		0.35×V _{DD}	
I _I	Input Current	V _{DD} = Max, V _{in} = V _{DD} or GND	I pin			15	μA
V _{OH}	Output High Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -2mA	1.05			V
			I _{OH} = -8mA	1.75			
V _{OL}	Output LOW Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 2mA			0.35	
			I _{OL} = 8mA			0.65	

Notes:

- For Max. or Min. conditions, use appropriate operating range values.
- Typical values are at V_{DD} = 1.2V, +25°C ambient and maximum loading.

1.2V AC Characteristics (Over Operating Range: V_{DDA}, V_{DDB}, V_{DDC} = 1.2V ± 0.1V, T_A = -40° to 85°C)

Parameters	Description		Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
F _{IN}	Input Frequency			0		150	MHz
t _{PLH} , t _{PHL} ⁽²⁾	Propagation Delay BUF_IN to CLK _n		C _L = 3pF, R _L = 500-Ohm, 125 MHz Outputs are measured @ V _{DD} /2	4	5	6	ns
t _{SK(O)} ⁽³⁾	Output to Output Skew between any two outputs of the same device @ same transition	Bank A (CLK0 - CLK4)		-150		150	ps
		Bank C (CLK5 - CLK6)		-50		50	
		Bank B (CLK7 - CLK9)		-300		300	
t _{SK(P)} ⁽³⁾	Pulse Skew between opposite transitions (t _{PHL} -t _{PLH}) of the same output				200	300	
t _{SK(T)} ⁽³⁾⁽⁵⁾	Part to Part Skew between two identical outputs of different parts on the same board ⁽⁴⁾					300	
t _{DC_IN}	Duty Cycle In @ 1ns edge rate			45		55	%
t _{DC_OUT}	Duty Cycle Out			40		60	
t _j ⁽⁵⁾	Additive Jitter					50	ps
t _{R(o)}	Output Rise Time 20% - 80% CLK _n				0.9	1	ns
t _{F(o)}	Output Fall Time 80% - 20% CLK _n				0.9	1	

Notes:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew measured at worst case temperature (max. temp).
- Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
- Guaranteed by design.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
I _{DDQ}	Quiescent Power Supply Current	V _{DDA} = V _{DDDB} = V _{DDC} = 2.7V	No Load. F _{IN} = 40MHz (Bank A, Bank B, Bank C included)		16		mA
		V _{DDA} = V _{DDDB} = V _{DDC} = 1.95V			12		
		V _{DDA} = V _{DDDB} = V _{DDC} = 1.6V			8		
		V _{DDA} = V _{DDDB} = V _{DDC} = 1.2V			8		
I _{OS}	Short Circuit Current	V _{DDA} = V _{DDDB} = V _{DDC}	2.7V 1.95V 1.6V 1.2V		±80 ±50 ±35 ±15		mA

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics.
- Typical values are at V_{DD} = 1.2V, 1.5V, 1.8V or 2.5V, and +25°C ambient.
- Per TTL driven input (V_{IN} = V_{DD} - 0.6V); all other inputs at V_{DD} or GND.

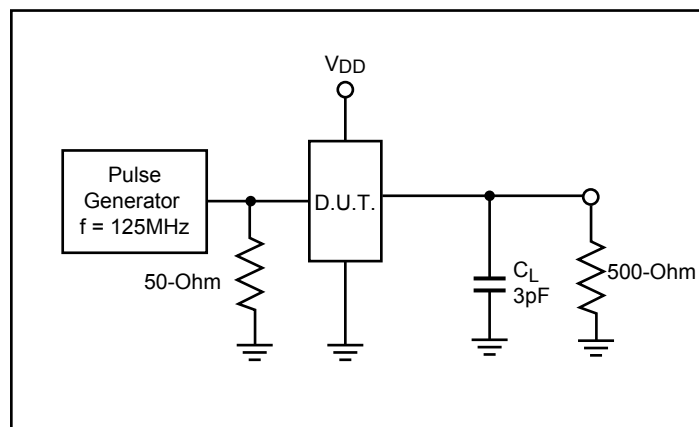
Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	3.0	4	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	6	

Note:

- This parameter is determined by device characterization but is not production tested.

Test Circuits for All Outputs

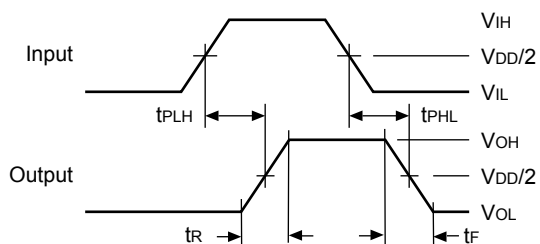


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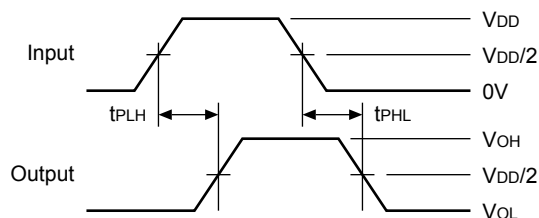
C_L = Load capacitance: includes jig and probe capacitance.

Switching Waveforms

Propagation Delay

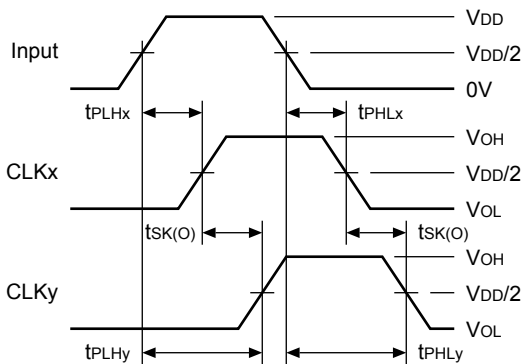


Pulse Skew – $t_{SK(P)}$



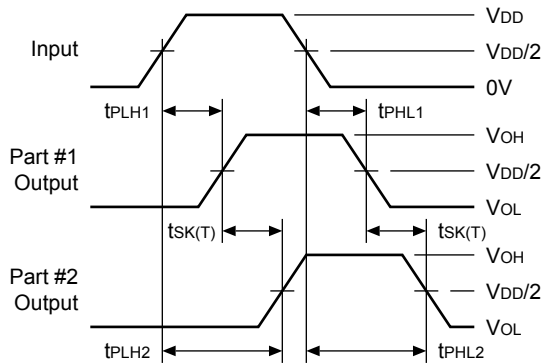
$$t_{SK(P)} = |t_{PLH} - t_{PHL}|$$

Output Skew – $t_{SK(O)}$



$$t_{SK(O)} = |t_{PLHy} - t_{PLHx}| \text{ or } |t_{PHLy} - t_{PHLx}|$$

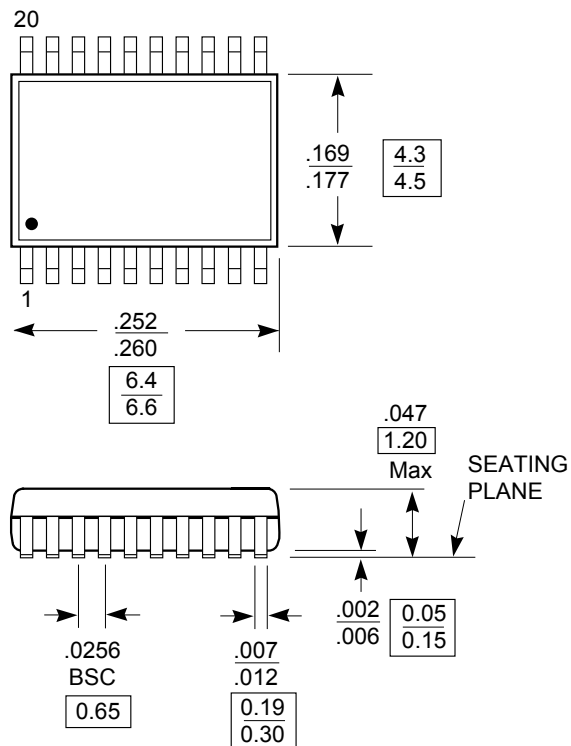
Package Skew – $t_{SK(T)}$



$$t_{SK(T)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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REVISION: E
DATE: 03/09/05



Note:

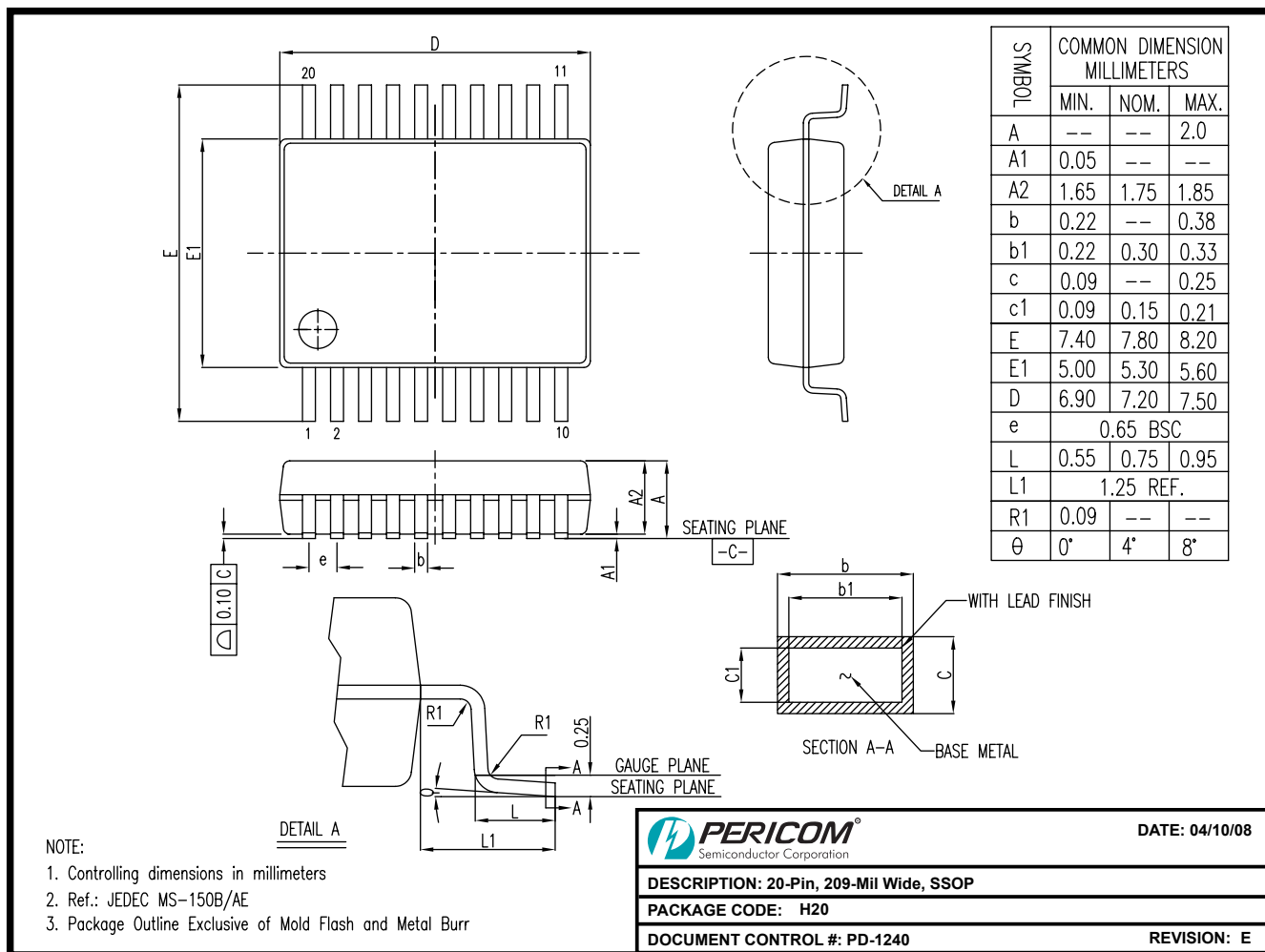
1. Package Outline Exclusive of Mold Flash and Metal Burr
2. Controlling dimensions in millimeters
3. Ref: JEDEC MO-153F/AC



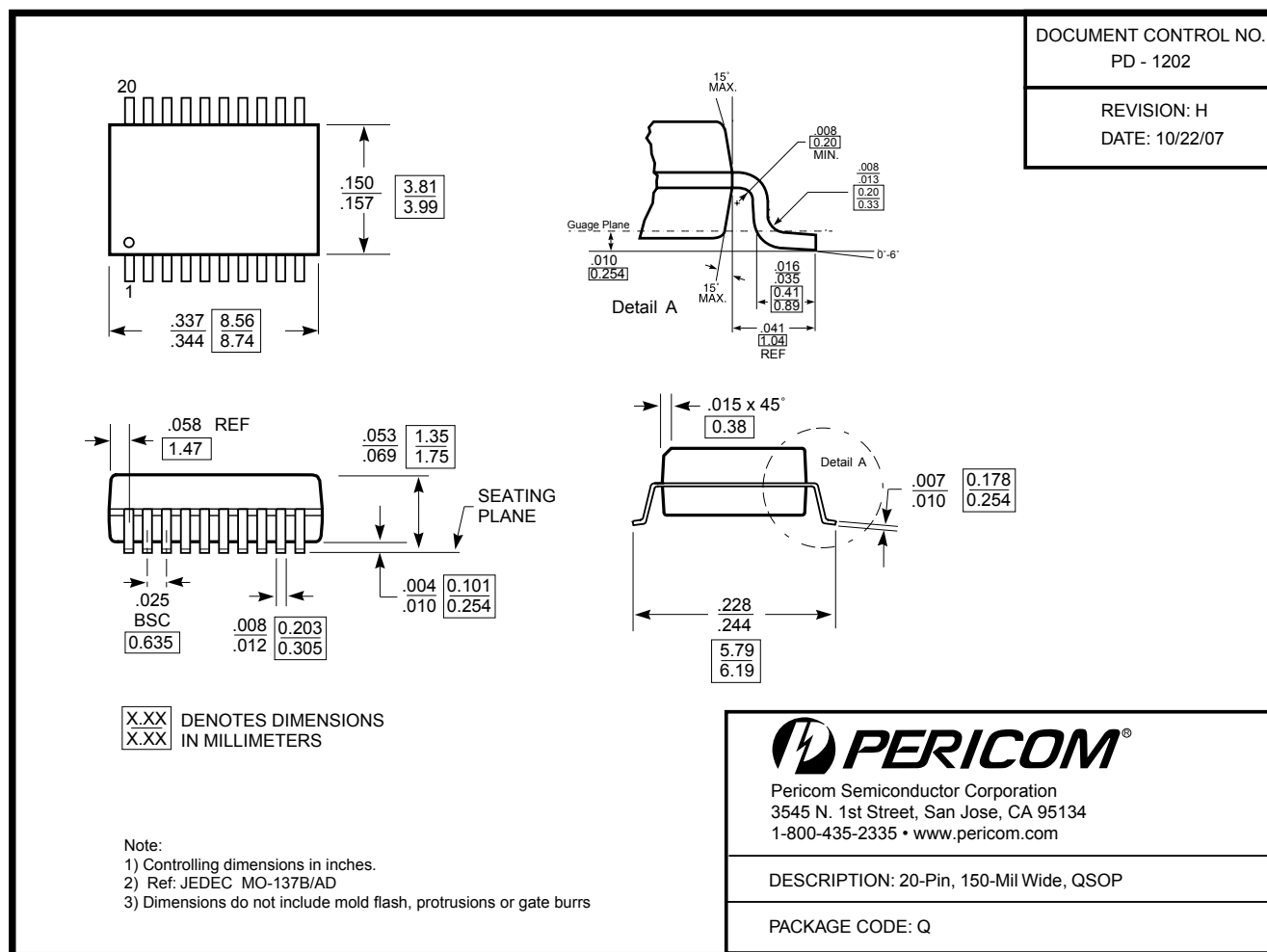
Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2336 • www.pericom.com

DESCRIPTION: 20-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L



08-0140



Ordering Information⁽¹⁻³⁾

Ordering Code	Package Code	Package Type
PI6C10810LE	L	Pb-free & Green, 20-pin 173-mil wide TSSOP
PI6C10810HE	H	Pb-free & Green, 20-pin 209-mil wide SSOP
PI6C10810QE	Q	Pb-free & Green, 20-pin 150-mil wide QSOP

Notes:

1. Thermal Characteristics can be found on the web at www.pericom.com/packaging/
2. E = Lead-free and Green
3. Adding an X suffix = Tape/Reel

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