4-bit I²C-bus and SMBus low power I/O port

Features

- ➔ Operation power supply voltage from 2.3V to 5.5V
- ➔ 4-bit I²C-bus GPIO with 5V tolerant I/Os
- ➔ Polarity inversion register
- ➔ Low current consumption
- ➔ 0Hz to 1MHz clock frequency
- ➔ Noise filter on SCL/SDA inputs
- ➔ Power-on reset
- ➔ 4 I/O pin which default to 4 inputs with 100kΩ pull-up resistor
- ➔ ESD protection (4KV HBM and 1KV CDM)
- ➔ Offered in three different packages:SOIC-8,MSOP-8 and TDFN2x3-8

Pin Configuration

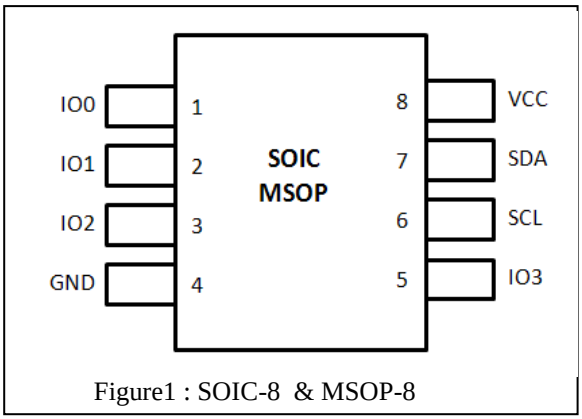


Figure1 : SOIC-8 & MSOP-8

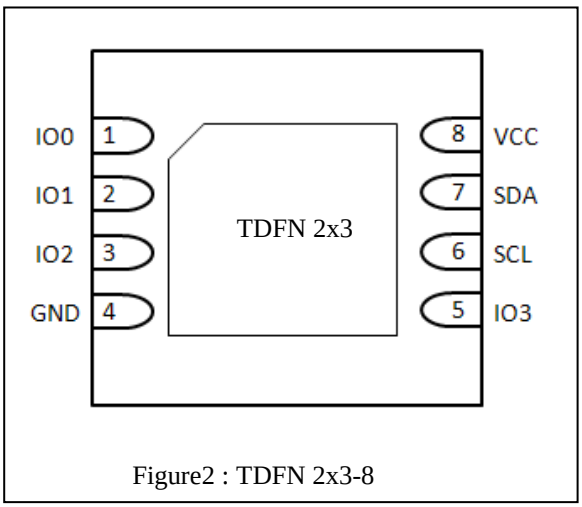


Figure2 : TDFN 2x3-8

Description

The PI4IOE5V9536 provides 4 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C-bus/ SMBus applications. It includes the features such as higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PI4IOE5V9536 consists of a 4-bit registers to configure the I/Os as either inputs or outputs, and a 4-bit polarity registers to change the polarity of the input port register data The data for each input or output is kept in the corresponding Input port or Output port register. All registers can be read by the system master.

Pin Description

* I = Input; O = Output; P = Power; G = Ground

Pin	Name	Type	Description
1	IO0	I/O	input/output 0
2	IO1	I/O	input/output 1
3	IO2	I/O	input/output 2
4	GND	G	Supply Ground
5	IO3	I/O	input/output 3
6	SCL	I	Serial clock line
7	SDA	I/O	Serial data line
8	VCC	P	Power supply

Maximum Ratings

Power supply	-0.5V to +6.0V
Voltage on an I/O pin	GND-0.5V to +6.0V
Input current	±20mA
Output current on an I/O pin	±50mA
Supply current	85mA
Ground supply current	100mA
Total power dissipation	200mW
Operation temperature	-40~85℃
Storage temperature	-65~150℃
Maximum Junction temperature ,T j(max)	125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb= -40 ℃ to +85 ℃; unless otherwise specified.

Table 2: Static characteristic

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
VCC	Supply voltage		2.3	-	5.5	V
I_{CC}	Supply current	Operating mode; VCC = 5.5 V; no load; f_{SCL}= 100 kHz	-	290	400	μA
I_{stb}	Standby current	Standby mode; VCC = 5.5 V; no load; V_I = GND; f_{SCL}= 0 kHz; I/O = inputs	-	225	350	uA
		Standby mode; VCC = 5.5 V; no load; V_I = VCC; f_{SCL}= 0 kHz; I/O = inputs	-	0.25	1	μA
V_{POR}	Power-on reset voltage[1]		-	1.16	1.41	V
Input SCL, input/output SDA						
V_{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V_{IH}	High level input voltage		0.7VCC	-	5.5	V
I_{OL}	Low level output current	V_{OL}=0.4V	3	6	-	mA
I_L	Leakage current	V_I=VCC=GND	-1	-	1	μA
C_i	Input capacitance	V_I =GND	-	6	10	pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/Os						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_{OL}	Low level output current	VCC = 2.3 V; V_{OL} = 0.5 V[2]	8	10	-	mA
		VCC = 2.3 V; V_{OL} = 0.7 V[2]	10	13	-	mA
		VCC = 3.0 V; V_{OL} = 0.5 V[2]	8	14	-	mA
		VCC = 3.0 V; V_{OL} = 0.7 V[2]	10	19	-	mA
		VCC = 4.5 V; V_{OL} = 0.5 V[2]	8	17	-	mA
		VCC =4.5 V; V_{OL} = 0.7 V[2]	10	24	-	mA
V_{OH}	High level output voltage	I_{OH}=-8mA;VCC=2.3V[3]	1.8	-	-	V
		I_{OH}=-10mA;VCC=2.3V[3]	1.7	-	-	V
		I_{OH}=-8mA;VCC=3.0V[3]	2.6	-	-	V
		I_{OH}=-10mA;VCC=3.0V[3]	2.5	-	-	V
		I_{OH}=-8mA;VCC=4.75V[3]	4.1	-	-	V
		I_{OH}=-10mA;VCC=4.75V[3]	4.0	-	-	V
I_{LIH}	High level input leakage current	VCC=3.6V; V_I=VCC	-	-	1	μA
I_{LIL}	Low level input leakage current	VCC=5.5V; V_I=GND	-	-	-100	μA
C_i	Input capacitance		-	3.7	10	pF
C_o	Output capacitance		-	3.7	10	pF

Note:
[1]: VCC must be lowered to 0.2 V for at least 5 us in order to reset part.
[2]: Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA
[3]: The total current sourced by all I/Os must be limited to 85mA.

Dynamic Characteristics

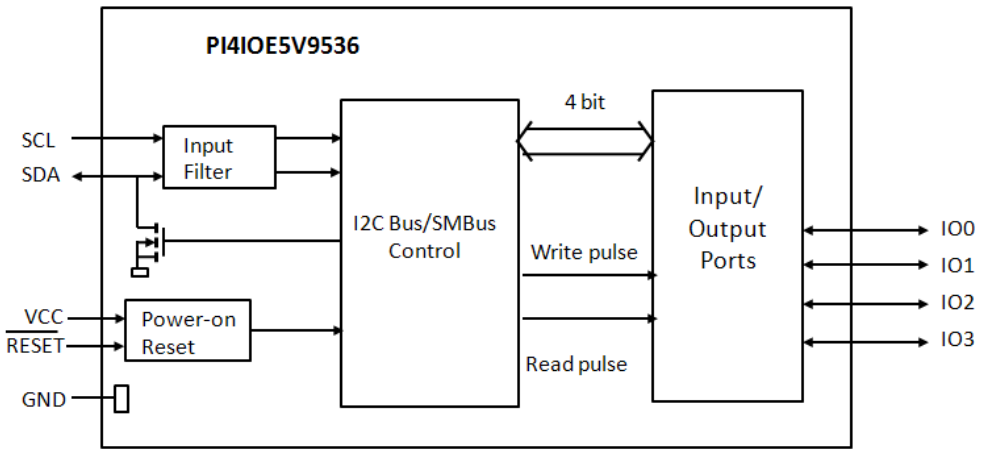
Table 3: Dynamic characteristics

Symbol	Parameter	Test Conditions	Standard mode I²C		Fast mode I²C		Fast mode Plus I²C		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{VD;ACK}$[1]	data valid acknowledge time		-	3.45	-	0.9	-	0.45	µs
$t_{HD;DAT}$[2]	data hold time		0	-	0	-	0	-	ns
$t_{VD;DAT}$	data valid time		-	3.45	-	0.9	-	0.45	us
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals		-	300	-	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	-	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50		50	ns
Port timing									
$t_{v(Q)}$	Data output valid time[3]		-	200	-	200	-	200	ns
$t_{su(D)}$	Data input set-up time		100	-	100	-	100	-	ns
$T_{h(D)}$	Data input hold time		1	-	1	-	1	-	µs

Note:
[1]: $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
[2]: $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3]: $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.

PI4IOE5V9536 Block Diagram

Fig3: Block diagram of PI4IOE5V9536



Note: All I/Os are set to inputs at reset.

Details Description

a. Device address

Table 4: Device address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	1	0	0	0	0	0	1	R/W

Note: Read "1", Write "0"

b. Registers

i. Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 5: Command byte

Command	Register
0	Input port register
1	Output port register
2	Polarity inversion register
3	Configuration register

ii. Register 0: input port registers

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 2. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 6: Input port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	1	1	1	1	X	X	X	X

iii. Register 1:Output port register

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 3. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 8: Output port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

iv. Register 2: Polarity inversion register

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 10: Polarity Inversion port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

v. Register 3: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to VCC

Table 12: Configuration port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

c. Power-on reset

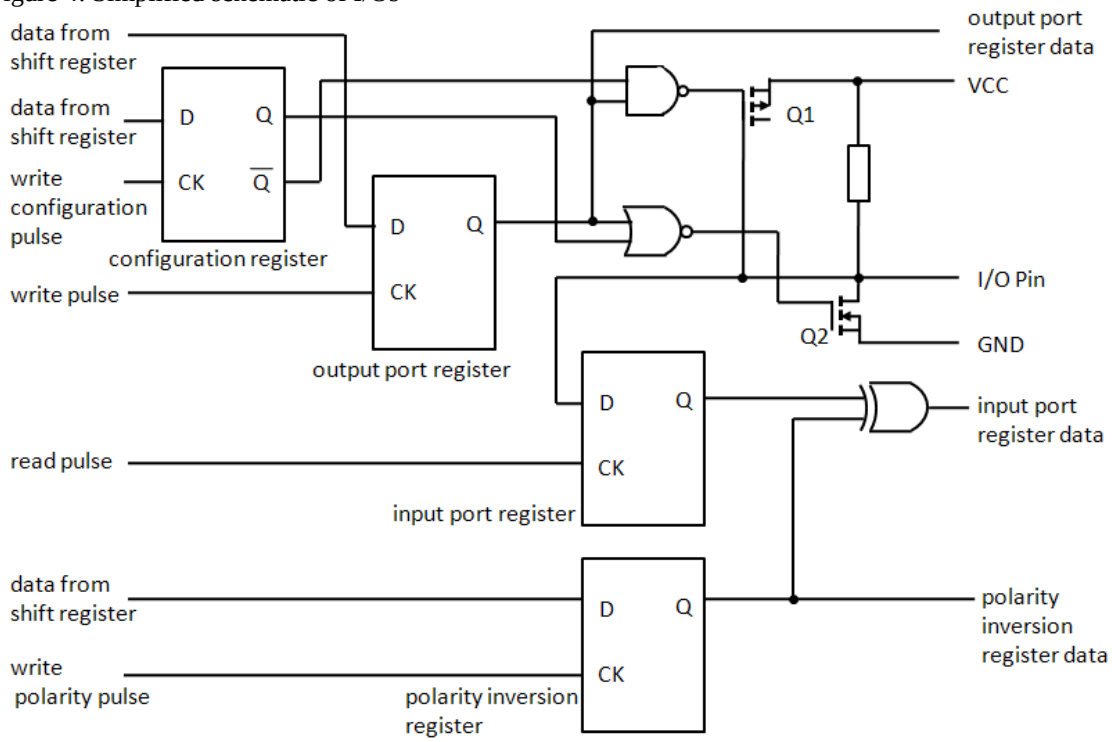
When power is applied to VCC, an internal power-on reset holds the PI4IOE5V9536 in a reset condition until VCC has reached V_{POR}. At that point, the reset condition is released and the PI4IOE5V9536 registers and SMBus state machine will initialize to their default states. Thereafter, VCC must be lowered below 0.2 V to reset the device. For a power reset cycle, VCC must be lowered below 0.2 V and then restored to the operating voltage.

d. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above VCC to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either VCC or GND.

Figure 4: Simplified schematic of I/Os



After power-on reset, all registers return to default values.

e. Bus Transaction

Data is transmitted to the PI4IOE5V9536 using the Write mode as shown in Figure 5.Data is read from the PI4IOE5V9536 using the read mode as shown in Figure 7.These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

Figure 5: Write to output registers

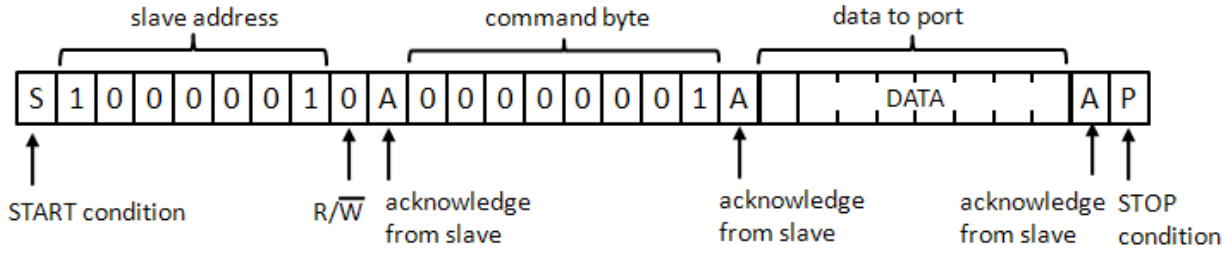


Figure 6: Write to polarity inversion registers

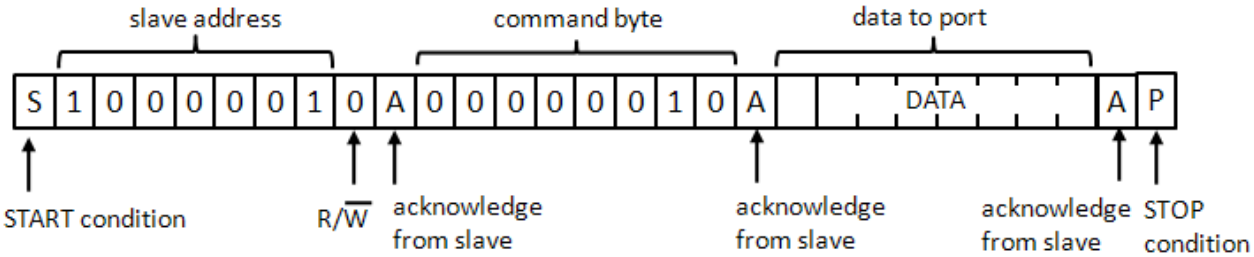
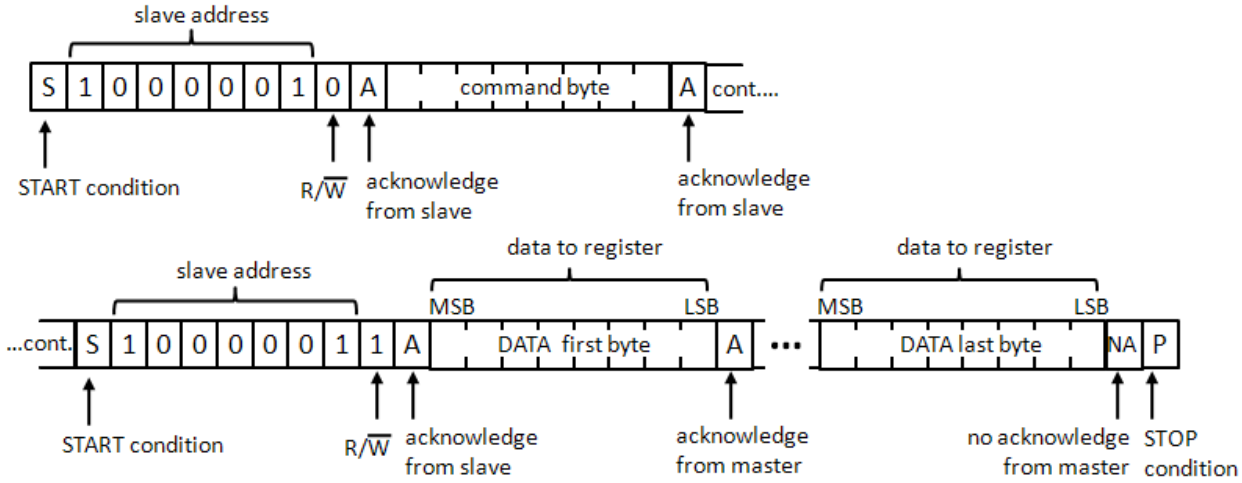
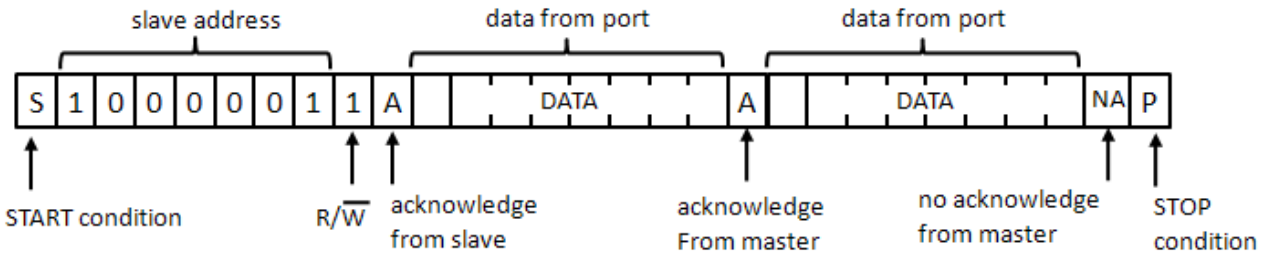


Figure 7: Read from registers



Note: Transfer can be stopped at any time by a STOP condition.

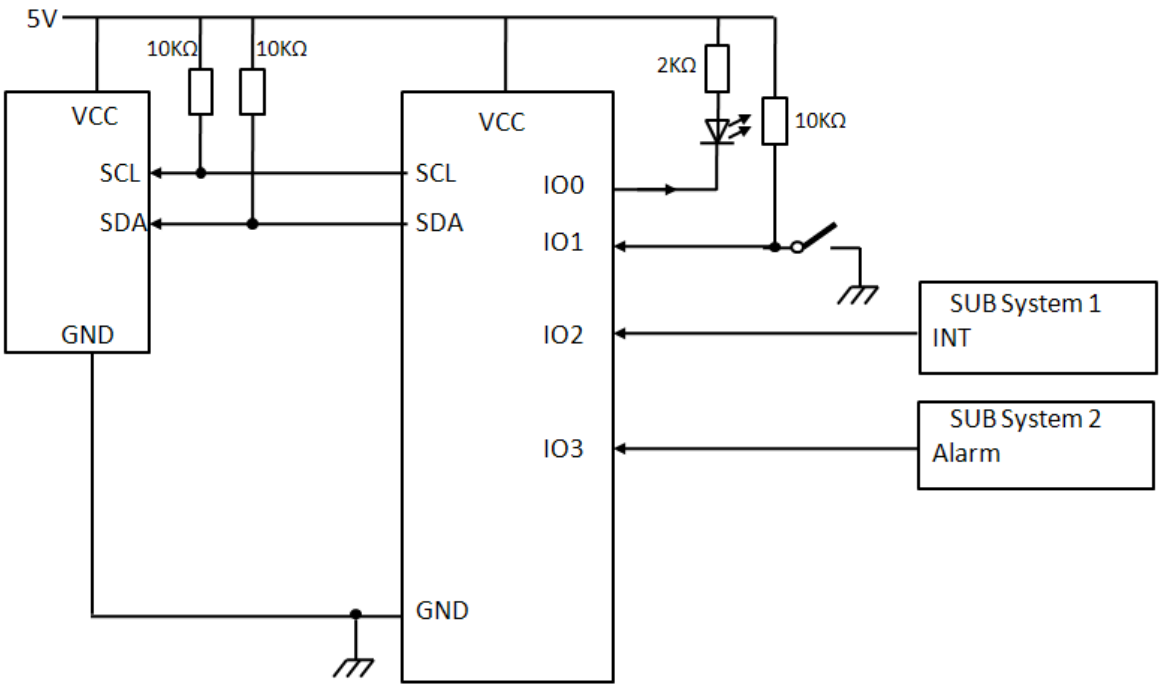
Figure 8: Read Input port register



Note: Transfer of data can be stopped at any moment by a STOP condition. It is assumed that the command byte has previously been set to '00' (read Input Port register).

Application design-in information

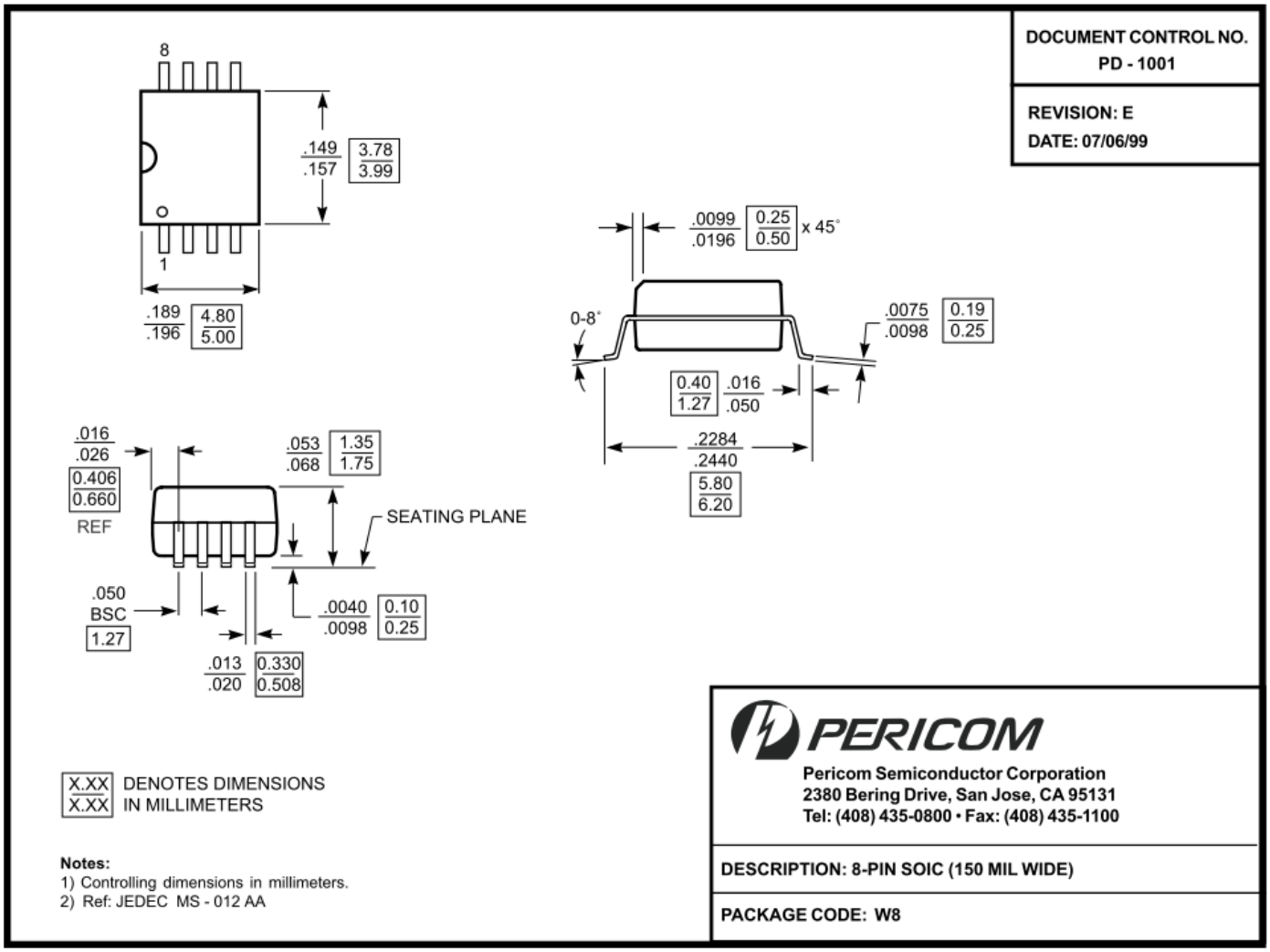
Figure 9: Typical application



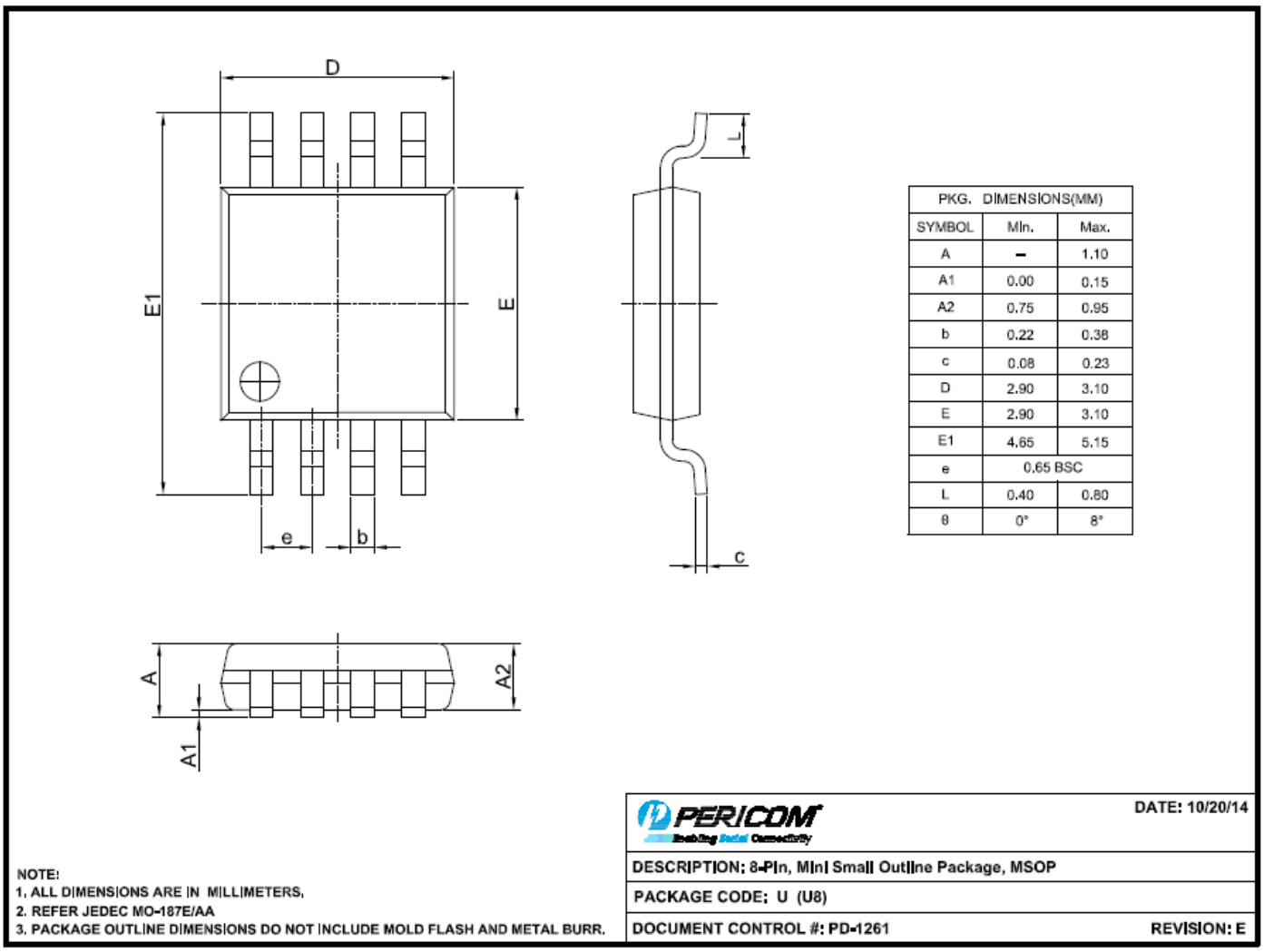
IO0 configured as outputs.
IO1, IO2, IO3 configured as inputs.

Mechanical Information

SOIC-8(W)



MSOP-8(U)



PKG. DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	–	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.65	5.15
e	0.65 BSC	
L	0.40	0.80
θ	0°	8°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. REFER JEDEC MO-187E/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

PERICOM Enabling Rapid Connectivity

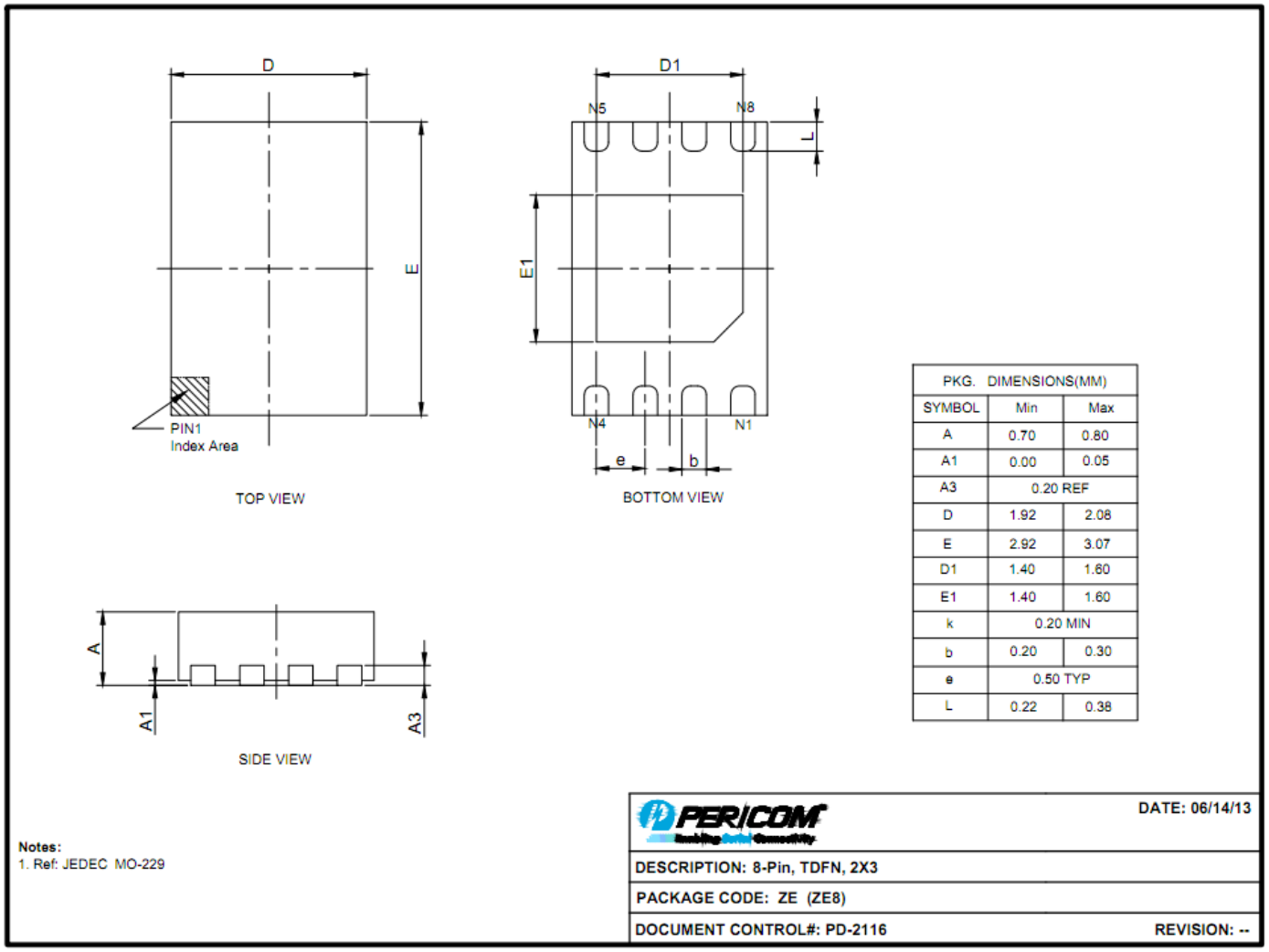
DATE: 10/20/14

DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP

PACKAGE CODE: U (U8)

DOCUMENT CONTROL #: PD-1261 REVISION: E

TDFN 2x3-8(ZE)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20 MIN	
b	0.20	0.30
e	0.50 TYP	
L	0.22	0.38

Ordering Information

Part No.	Package Code	Package
PI4IOE5V9536WE	W	8-Pin,150 mil Wide SOIC
PI4IOE5V9536WEX	W	8-Pin,150 mil Wide SOIC, Tape & Reel
PI4IOE5V9536UE	U	8-Pin, Mini Small Outline Package(MSOP)
PI4IOE5V9536UEX	U	8-Pin, Mini Small Outline Package(MSOP), Tape & Reel
PI4IOE5V9536ZEEX	ZE	8-Pin,TDFN2x3, Tape & Reel

Note:

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel