



PHT4NQ10LT

N-channel TrenchMOS logic level FET

Rev. 2 — 28 October 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Logic level compatible

1.3 Applications

- DC-to-DC converters
- High-speed line drivers
- General purpose switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	100	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1 ; see Figure 2	-	-	3.5	A
V_{GS}	gate-source voltage		-16	-	16	V
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 1.75\text{ A}$; $T_j = 25\text{ °C}$; see Figure 10 ; see Figure 11	-	200	250	mΩ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	<p>SOT223 (SC-73)</p>	<p>mbb076</p>
2	D	drain		
3	S	source		
4	D	drain		



3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHT4NQ10LT	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

4. Marking

Table 4. Marking codes

Type number	Marking code
PHT4NQ10LT	4NQ10L

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-16	16	V
I_D	drain current	$T_{sp} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$	-	2.2	A
		$T_{sp} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1 ; see Figure 2	-	3.5	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 1	-	14	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 3	-	6.9	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-65	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	3.5	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	14	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; $I_D = 3.5\text{ A}$; $R_{GS} = 50\text{ }\Omega$; $V_{sup} \leq 15\text{ V}$; unclamped; $t_p = 0.2\text{ ms}$; see Figure 4	-	45	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 15\text{ V}$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$; unclamped; see Figure 4	-	3.5	A

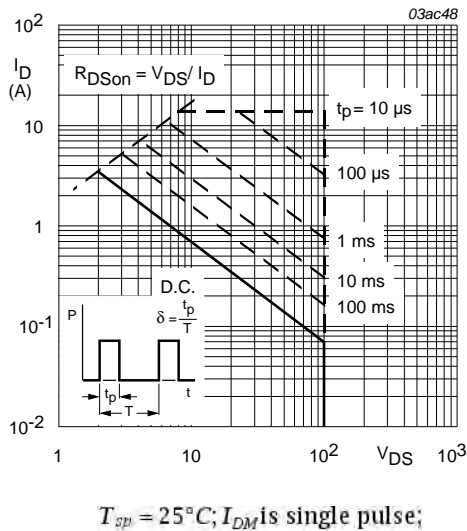


Fig 1. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

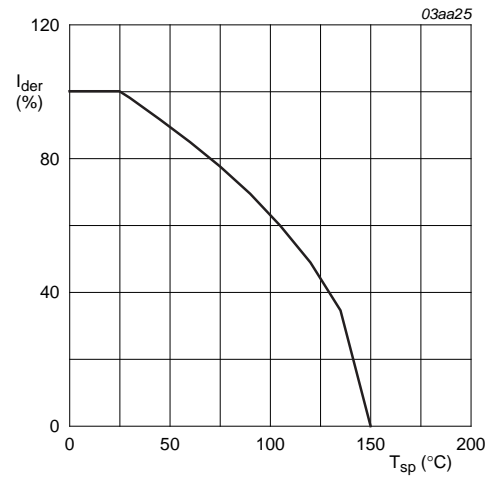


Fig 2. Normalized continuous drain current as a function of solder point temperature

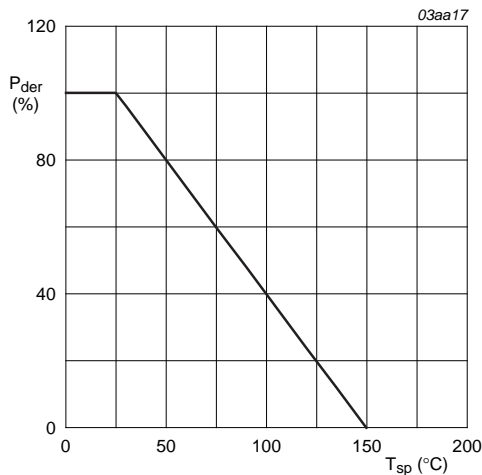


Fig 3. Normalized total power dissipation as a function of solder point temperature

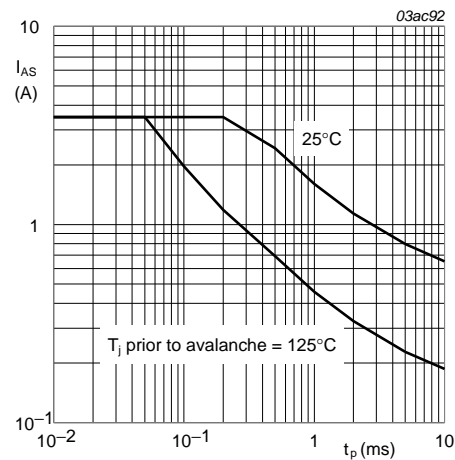


Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate	-	-	18	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board ; minimum footprint	-	-	150	K/W

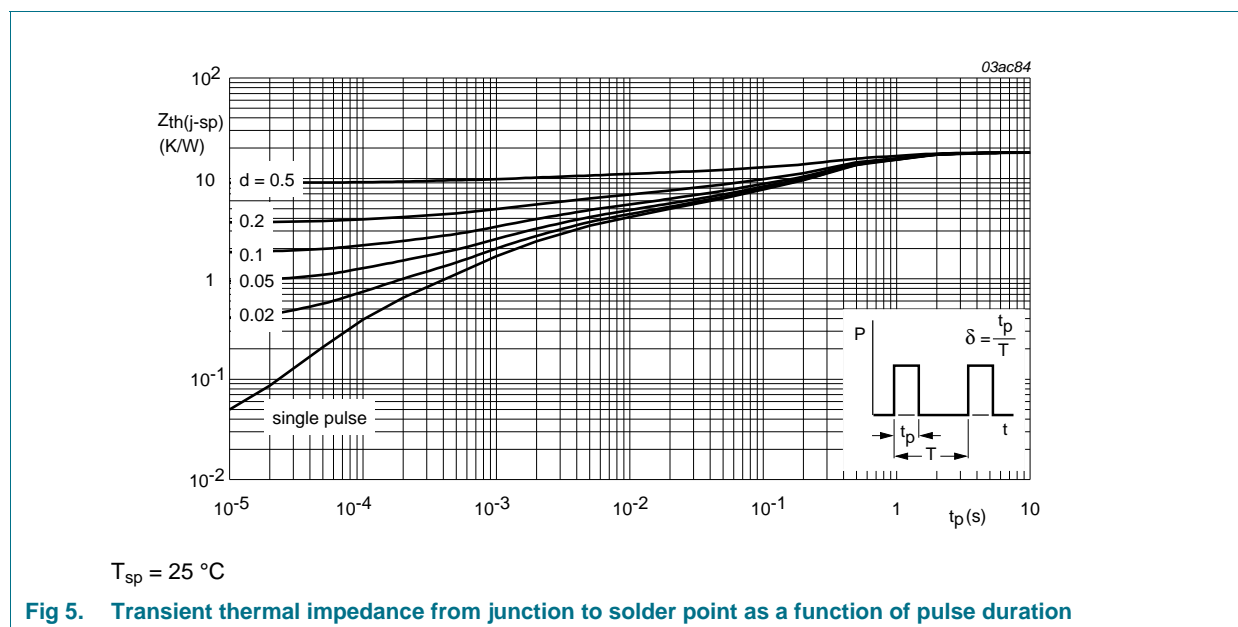


Fig 5. Transient thermal impedance from junction to solder point as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55\text{ }^{\circ}\text{C}$	89	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	100	130	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 150\text{ }^{\circ}\text{C}$; see Figure 9	0.6	-	-	V
		$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55\text{ }^{\circ}\text{C}$; see Figure 9	-	-	2.3	V
		$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 9	1	-	2	V
I_{GSS}	gate leakage current	$V_{GS} = -10\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	10	100	nA
		$V_{GS} = 10\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	10	100	nA

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 1.75 A; T _j = 150 °C; see Figure 10 ; see Figure 11	-	-	575	mΩ
		V _{GS} = 5 V; I _D = 1.75 A; T _j = 25 °C; see Figure 10 ; see Figure 11	-	200	250	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 3.5 A; V _{DS} = 80 V; V _{GS} = 5 V; T _j = 25 °C; see Figure 12	-	6.8	-	nC
Q _{GS}	gate-source charge		-	1.1	-	nC
Q _{GD}	gate-drain charge		-	3.6	-	nC
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 15 Ω; V _{GS} = 5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C	-	4	-	ns
t _r	rise time		-	10	-	ns
t _{d(off)}	turn-off delay time		-	52	-	ns
t _f	fall time		-	21	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 3.5 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 13	-	0.87	1.5	V
t _{rr}	reverse recovery time	I _S = 3.5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 30 V; T _j = 25 °C	-	50	-	ns
Q _r	recovered charge		-	100	-	nC

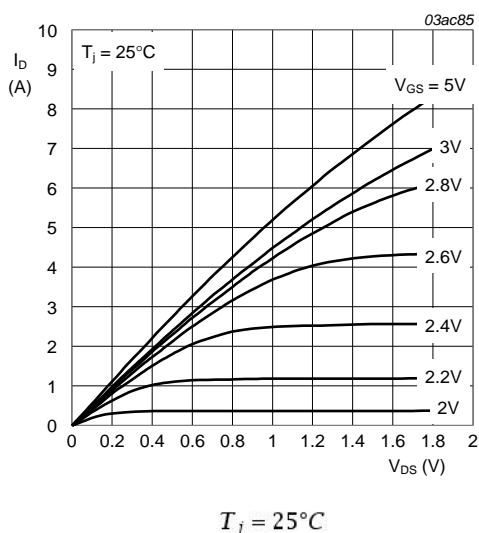


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

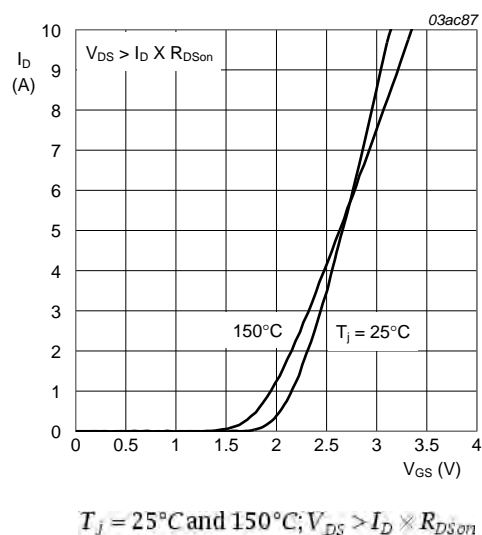


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

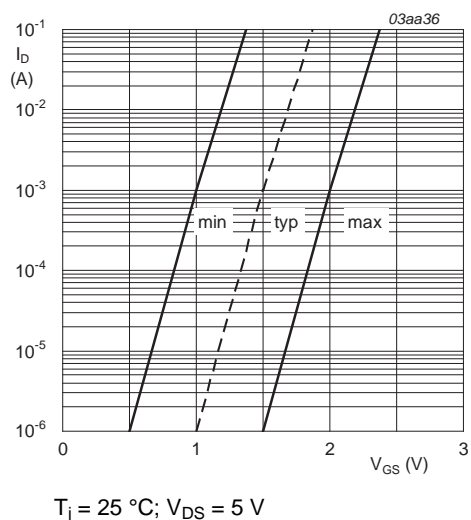


Fig 8. Sub-threshold drain current as a function of gate-source voltage

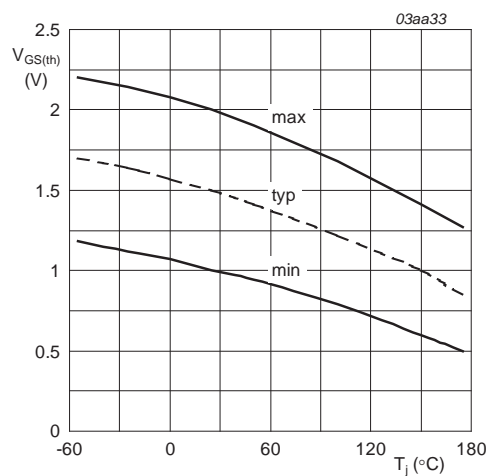


Fig 9. Gate-source threshold voltage as a function of junction temperature

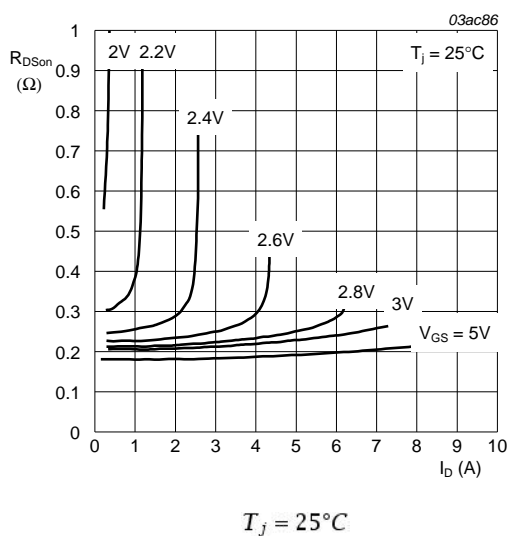


Fig 10. Drain-source on-state resistance as a function of drain current; typical values

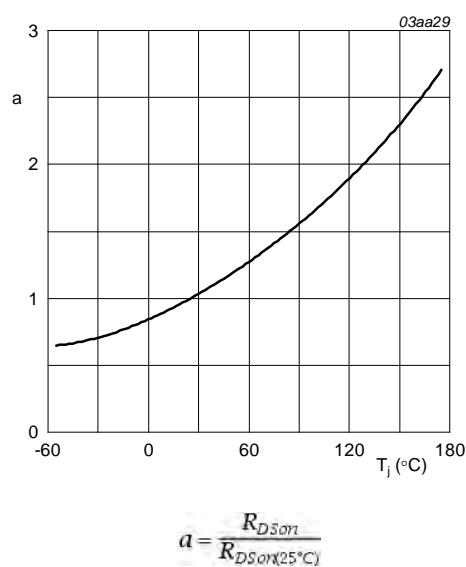
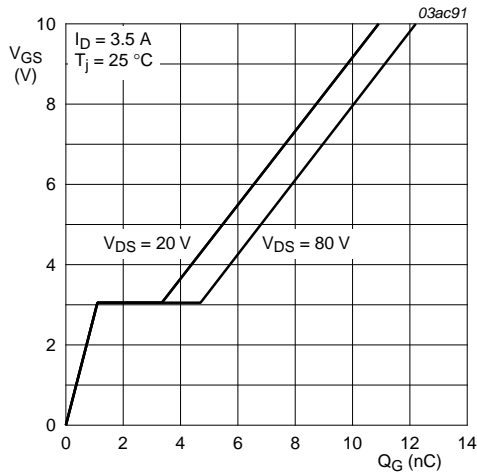
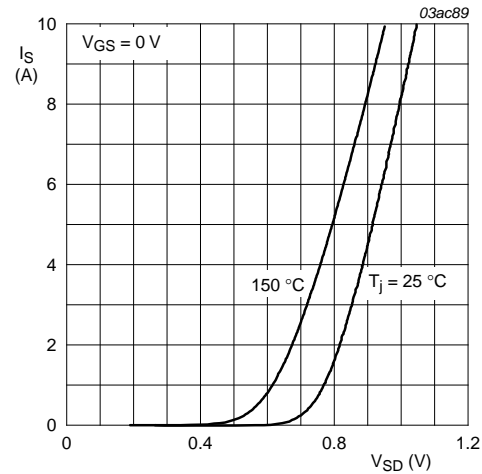


Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$$I_D = 3.5 \text{ A}; V_{DS} = 80 \text{ V}$$

Fig 12. Gate-source voltage as a function of gate charge; typical values



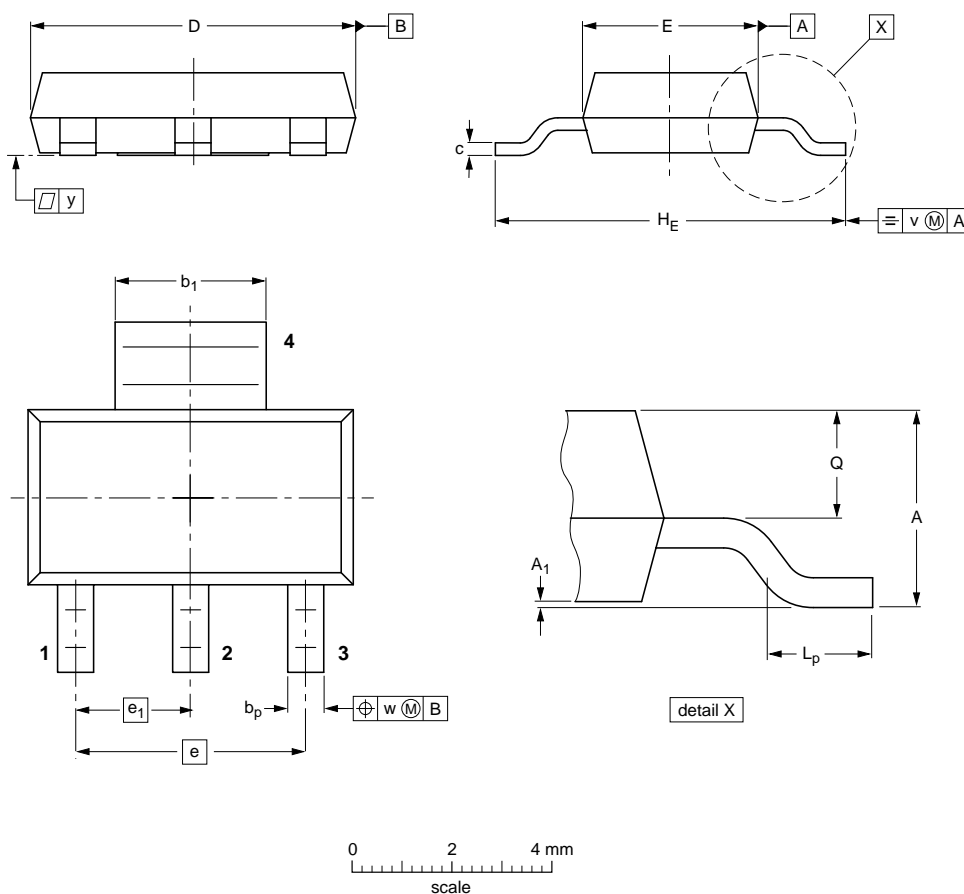
$$T_J = 25^\circ\text{C} \text{ and } 150^\circ\text{C}; V_{GS} = 0 \text{ V}$$

Fig 13. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

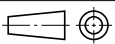
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			04-11-10 06-03-16

Fig 14. Package outline SOT223 (SC-73)

9. Soldering

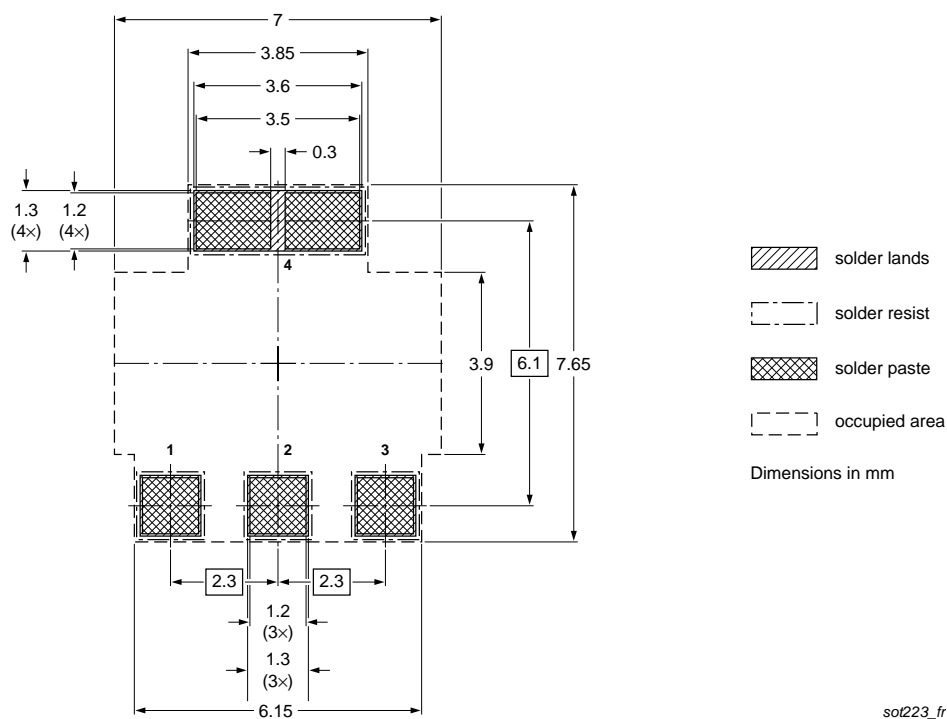


Fig 15. Reflow soldering footprint for SOT223 (SC-73)

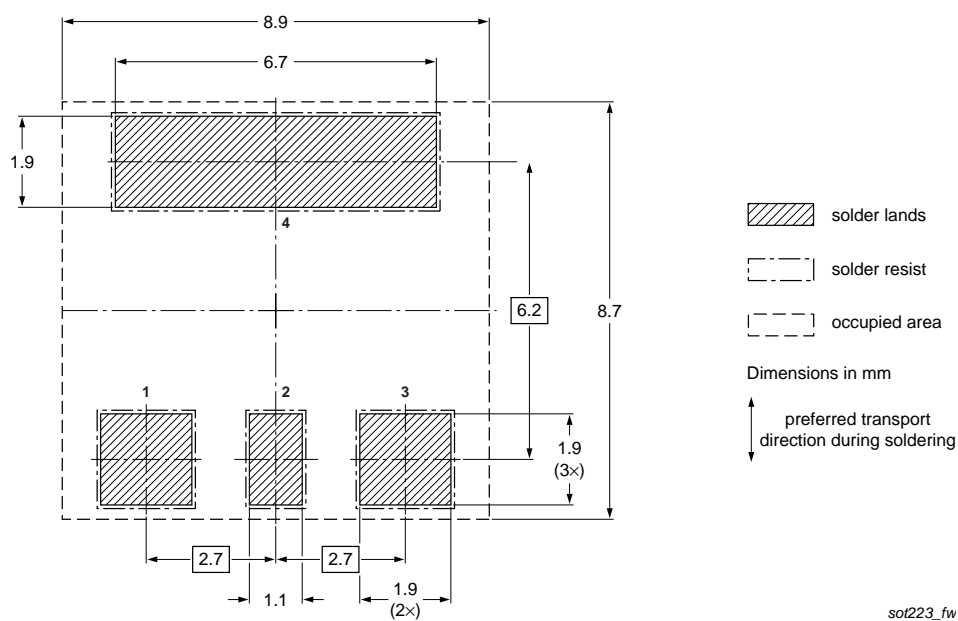


Fig 16. Wave soldering footprint for SOT223 (SC-73)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHT4NQ10LT v.2	20111028	Product data sheet	-	PHT4NQ10LT v.1
Modifications:	<ul style="list-style-type: none">• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• 1 "Product profile": updated• 7 "Characteristics": $Q_{G(tot)}$ value corrected• 11 "Legal information": updated			
PHT4NQ10LT v.1	20000911	Product specification	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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