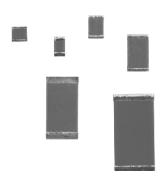
CHPHR

Vishay Sfernice



ESA High Stability Thick Film Resistor Chips



Vishay Sfernice thick film chip resistors CHPHR are specially designed to meet the requirements of the ESA 4001/026 specification. They have undergone the CNES evaluation (Space French National Agency). They are in level 1 of the ESA EPPL (European Preferred Part List) and ESA qualification is on-going.

FEATURES

HALOGEN FREE

- · SMD wraparound chip resistor
- Generic specification ESCC 4001
- Detailed specification ESCC 4001/026
- · Robust terminations
- Large ohmic value range 1 Ω to 10 M Ω
- HCHP option 0.55: for high frequency applications (up to 10 GHz)
- Halogen-free according to IEC 61249-2-21

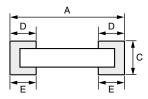
Evaluated to ESCC 4001/026.

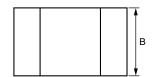
Sputtered Thin Film terminations, with nickel barrier, are very convenient for high operating conditions. They can withstand thousands of very severe thermal shocks.

B (W/A) type is for solder reflow assembly (variant 01 to 05)

G (W/A) type is for gluing (variant 06 to 10)

DIMENSIONS in millimeters





V4 DIANE		DIMENSIONS (mm)							
VARIANT NUMBER	STYLE	1	4	ı	В	(D,	, E
NOWBER		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
01, 06	0603	1.36	1.68	0.72	0.98	0.38	0.53	0.25	0.51
02, 07	0805	1.75	2.07	1.14	1.4	0.38	0.53	0.25	0.51
03, 08	1206	2.89	3.21	1.47	1.73	0.38	0.53	0.25	0.51
04, 09	2010	4.92	5.24	2.41	2.67	0.5	0.63	0.25	0.64
05, 10	2512	6.19	6.51	2.93	3.32	0.5	0.63	0.25	0.64

MECHANICAL SPECIFICATIONS

Substrate: Alumina

Technology: Thick film (Ruthenium oxyde)

Protection: **Epoxy** coating

B (W/A): SnPb over nickel barrier **Terminations:**

for solder reflow

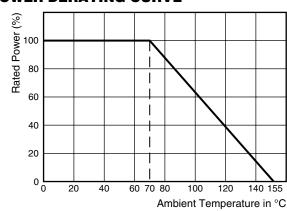
G (W/A) type: gold over nickel

barrier for gluing

CHIPS FOR HIGH FREQUENCY APPLICATIONS

High frequency option available up to 10 GHz 3 sizes: 0603, 0805, 1206

POWER DERATING CURVE



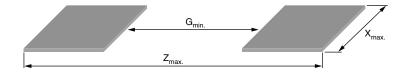




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SUGGESTED LAND PATTERN (please refer to IPC-7351A)



CHIP SIZE	Z _{max.}	G _{min.}	X _{max} .
0603	2.38	0.34	0.98
0805	2.77	0.73	1.40
1206	3.91	1.87	1.73
2010	5.94	3.64	2.67
2512	7.21	4.91	3.32

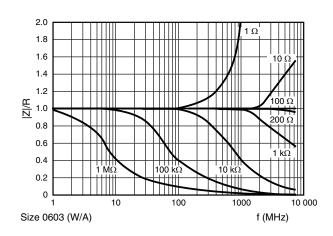
PACKAGING

Waffle-pack or tape and reel when specified

	NUMBER O				
SIZE	WAFFLE	TAPE ANI	TAPE WIDTH		
	PACK 2" × 2" MIN.		MAX.	WIDTH	
0603					
0805 0705	100		4000	8 mm	
1206	140	100			
2010	60		1000	8 mm ⁽²⁾	
2512	45		1000	O IIIIII (=)	

Notes

TYPICAL HF PERFORMANCE OF HCHP



ELECTR	ELECTRICAL SPECIFICATIONS							
VARIANT NUMBER STYLE		RESISTANCE RANGE R _n (2)		TOLEDANIOE	TEMPERATURE COEFFICIENT	CRITICAL	TERMINAL	WEIGHT
	STYLE (1)	MIN. (Ω)	MAX. (MΩ)	(± %) (2)	TC (± 10 ⁻⁶ /°C) ⁽²⁾	RESISTANCE ($k\Omega$)	MATERIAL AND FINISH	MAX. (g)
01	0603	1	10	1, 2, 5	100, 200	25	E4	0.002
02	0805	1	10	1, 2, 5	100, 200	50	E4	0.004
03	1206	1	10	1, 2, 5	100, 200	160	E4	0.008
04	2010	1	10	1, 2, 5	100, 200	180	E4	0.026
05	2512	1	10	1, 2, 5	100, 200	112.5	E4	0.042
06	0603	1	10	1, 2, 5	100, 200	25	E2	0.002
07	0805	1	10	1, 2, 5	100, 200	50	E2	0.004
08	1206	1	10	1, 2, 5	100, 200	160	E2	0.008
09	2010	1	10	1, 2, 5	100, 200	180	E2	0.026
10	2512	1	10	1, 2, 5	100, 200	112.5	E2	0.042

Notes

⁽¹⁾ MOQ for tape and reel: 50 pieces

^{(2) 12} mm on request

⁽¹⁾ See physical dimensions

⁽²⁾ Restrictions might apply depending on ohmic value please refer to Table 1

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Table 1

RESISTANCE (Ω)	VALUE SERIES	AVAILABLE TOLERANCE (± %)	AVAILABLE TEMPERATURE COEFFICIENT (± 10 ⁻⁶ /°C)	
1 ≤ R _n < 10		2, 5	200	
10 ≤ R _n < 1 M	Any value in the resistance range to 3 significant figures	1, 2, 5	100, 200	
R _n ≥ 1 M	to o digrimodrit ligares	2, 5	200	

MAXIMUM RATINGS						
CHARACTERISTICS	VARIANT NUMBER	STYLE	SYMBOLS	LIMITS	UNITS	REMARKS
	01, 06	0603		100		
	02, 07	0805		200		
Rated dissipation	03, 08	1206	P _n	250	mW	(1)
	04, 09	2010		500		
	05, 10	2512		800		
	01, 06	0603		50		
	02, 07	0805		100		
Limiting element voltage	03, 08	1206	U_L	250	V	-
	04, 09	2010		300		
	05, 10	2512		300		
Rated voltage	All	All	U _R	$\sqrt{(P_n x R_n)}$	V	(2)
	01, 06	0603		100		
	02, 07	0805		200		
Isolation voltage	03, 08	1206	U _I	300	V	-
	04, 09	2010		300		
	05, 10	2512		300		
Operating temperature range	All	All	T _{op}	- 55 to + 155	°C	T _{amb}
Storage temperature range	All	All	T _{stg}	- 55 to + 155	°C	-
Soldering temperature	All	All	T _{sol}	+ 260	°C	(3)

Notes

- $^{(1)}$ At T_{amb} \leq + 70 °C. For T_{amb} > + 70 °C derate linearly to 0 W at T_{amb} = + 155 °C
- $^{(2)}$ Shall never exceed limiting element voltage. R_{n} = Rated resistance
- (3) Duration 10 s maximum

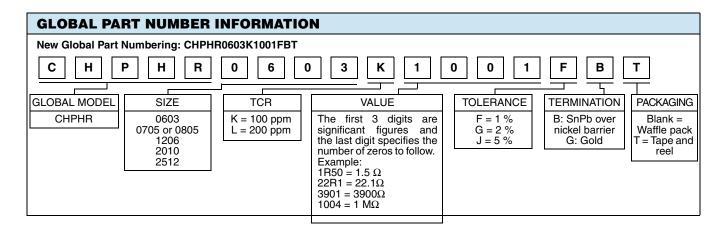
PERFORMANCE					
TEST	CONDITIONS	LIMITS REQUIRED BY THE ESCC4001/026 SPECIFICATION			
Insulation resistance	ESCC4001 § 8.3.1.2 V = 100 V	1000 MΩ			
Low temperature electrical measurement	ESCC4001 § 8.3.1.1 TC = 100 ppm/°C TC = 200 ppm/°C	± 0.8 % ± 1.6 %			
High temperature electrical measurement	ESCC4001 § 8.3.3 TC = 100 ppm/°C TC = 200 ppm/°C	± 1.36 % ± 2.72 %			
Rapid change of temperature	ESCC4001 § 8.8	± 0.25 + (0.05 Ω x 100/R _n) %			
Robustness of terminations	ESCC4001 § 8.11.2	± 0.25 + (0.05 Ω x 100/R _n) %			
Resistance to solder heat	ESCC4001 § 8.12	± 0.5 + (0.05 Ω x 100/R _n) %			
Climatic sequence	ESCC4001 § 8.10	± 1 + (0.05 Ω x 100/R _n) %			
Load life	ESCC4001 § 8.13 1000 h 2000 h	$\pm 1 + (0.05 \Omega \times 100/R_n) \%$ $\pm 1.5 + (0.05 \Omega \times 100/R_n) \%$			

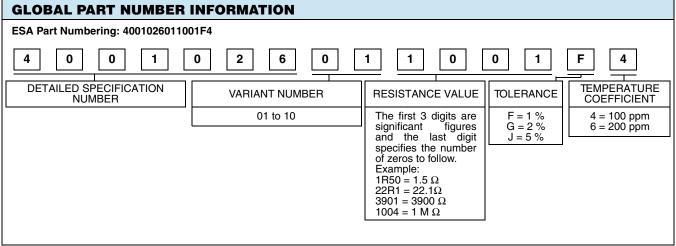




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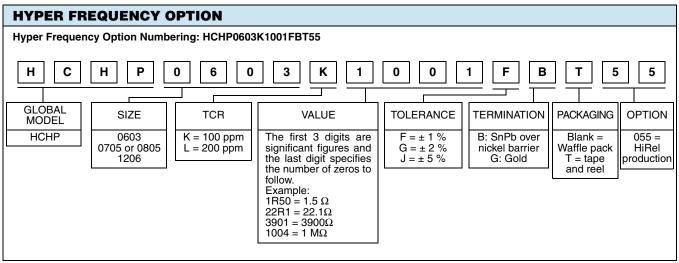
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Note

• MOQ for tape and reel: 50 pieces



Note

• MOQ for taping: 50 pieces

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NOTION OF SINGLE LOT

The homogeneity of lots is given by the front end lot numbers (primary process lot) and not by the date code.

The date code is applied after completion of end of production testing. Parts coming from different lots might have same date code.

A customer who needs lot homogeneity should mention on his order: SINGLE PRODUCTION LOT

OPTIONS

LOT VALIDATION TESTING

For procurement of qualified components, lot validation testing is not required and shall only be performed if specifically stipulated in the purchase order.

For procurement of unqualified components, lot validation testing shall be performed as stipulated in the purchase order. The need for lot validation testing shall be determined by the orderer.

When lot validation testing is required, it shall consist of the performance of one or more of the tests or subgroup test sequences of chart F4 indicated in the ESA generic Specification ESCC 4001. The testing to be performed and the sample size shall be as stipulated in the purchase order. When procurement of more than one component type is involved from a family, range or series, the selection of representative samples shall also be stipulated in the purchase order.

Lot validation testing will be composed of one LVT charges and LVT samples:

Lot validation test charges has to be ordered separately on purchase order.

Lot validation samples have to be ordered separately on purchase order.

FINAL INSPECTION

If requested by the orderer a final inspection can be performed on site.

Final inspection has to be stipulated separately on purchase order.

www.vishay.com

For technical questions, contact: sfer@vishay.com



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