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1. Product profile

1.1 General description

Dual logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Suitable for high frequency applications due to fast switching characteristics
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery applications

1.4 Quick reference data

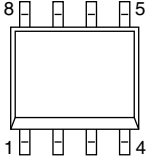
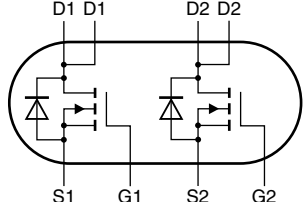
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	30	V
I_D	drain current	$T_{amb} = 25\text{ °C}$; pulsed; see Figure 1 ; see Figure 3	[1]	-	6.3	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$; pulsed; see Figure 2	[1]	-	2	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 7\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 ; see Figure 10	-	24	30	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 7\text{ A}$; $V_{DS} = 15\text{ V}$; $T_j = 25\text{ °C}$; see Figure 11	-	3	-	nC

[1] Single device conducting.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 SOT96-1 (SO8)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHN203	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	30	V
V_{DGR}	drain-gate voltage	$T_j \leq 150\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	-	30	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$T_{amb} = 70\text{ °C}$; pulsed; see Figure 1	[1]	-	5	A
		$T_{amb} = 25\text{ °C}$; pulsed; see Figure 1 ; see Figure 3	[1]	-	6.3	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{amb} = 25\text{ °C}$; see Figure 3	[1]	-	18	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$; pulsed; see Figure 2	[1]	-	2	W
T_{stg}	storage temperature		-55	-	150	°C
T_j	junction temperature		-55	-	150	°C

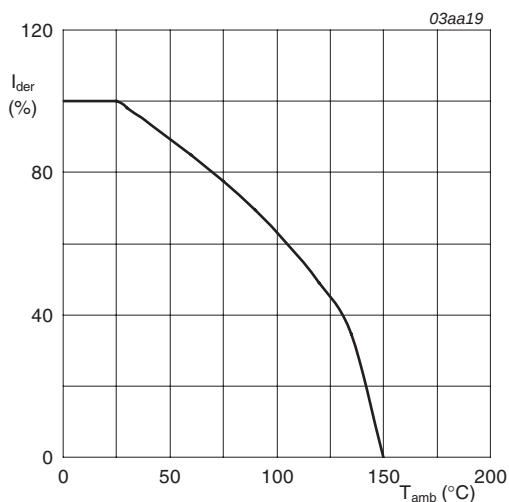
Source-drain diode

I_S	source current	$T_{amb} = 25\text{ °C}$; pulsed	[1]	-	2	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{amb} = 25\text{ °C}$	[1]	-	4.1	A

Avalanche ruggedness

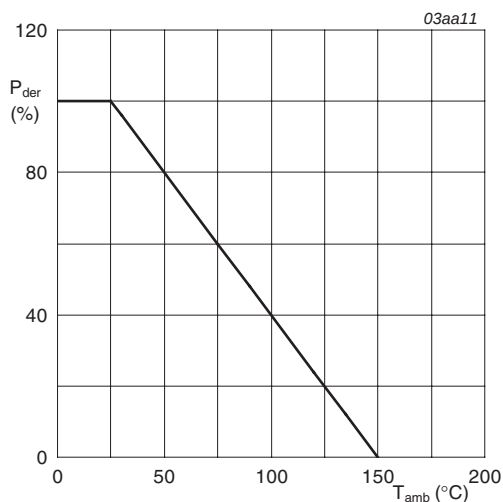
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 8.7\text{ A}$; $V_{sup} \leq 30\text{ V}$; unclamped; $t_p = 0.2\text{ ms}$; $R_{GS} = 50\text{ }\Omega$	-	-	37.8	mJ
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[1] Single device conducting.



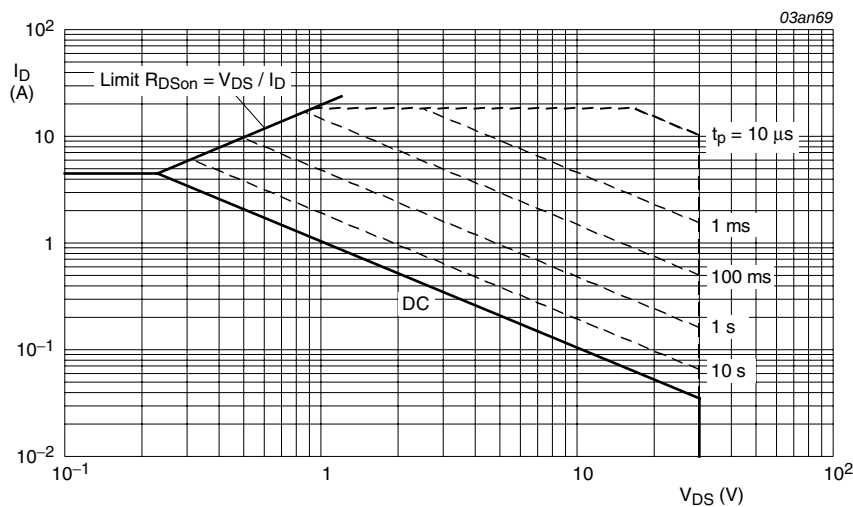
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of ambient temperature



$$P_{der} = \frac{P(tot)}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of ambient temperature



$$T_{amb} = 25^{\circ}C; I_{DM} \text{ is single pulse}; V_{GS} = 10V$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	-	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; see Figure 4	-	-	62.5	K/W

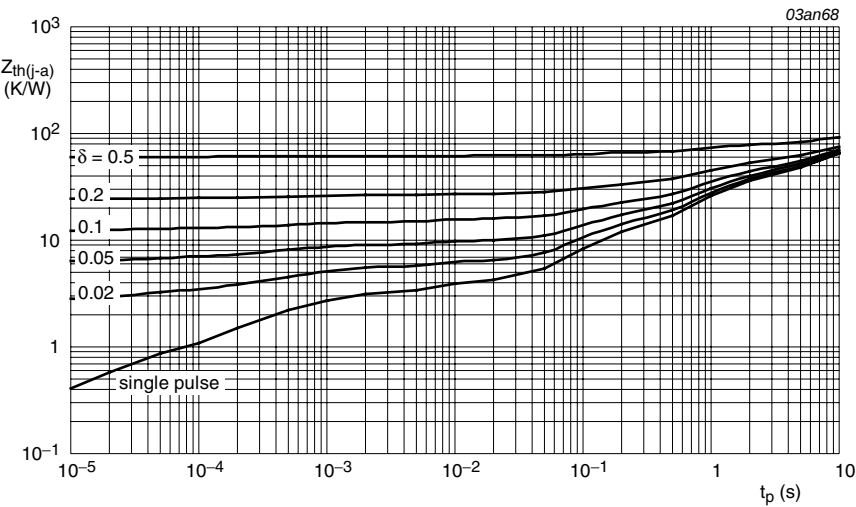


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	27	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 8	-	-	2.2	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 150 °C; see Figure 8	0.6	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 8	1	1.5	2	V
I _{DSS}	drain leakage current	V _{DS} = 24 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μA
		V _{DS} = 24 V; V _{GS} = 0 V; T _j = 150 °C	-	-	10	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 7 A; T _j = 25 °C; see Figure 9 ; see Figure 10	-	24	30	mΩ
		V _{GS} = 4.5 V; I _D = 3.5 A; T _j = 25 °C; see Figure 9 ; see Figure 10	-	30	55	mΩ
		V _{GS} = 10 V; I _D = 7 A; T _j = 150 °C; see Figure 9 ; see Figure 10	-	40.8	51	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 7 A; V _{DS} = 15 V; V _{GS} = 10 V; T _j = 25 °C; see Figure 11	-	14.6	-	nC
Q _{GS}	gate-source charge		-	2	-	nC
Q _{GD}	gate-drain charge		-	3	-	nC
C _{iss}	input capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 12	-	560	-	pF
C _{oss}	output capacitance		-	125	-	pF
C _{rss}	reverse transfer capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 12	-	85	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 25 V; R _L = 25 Ω; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C	-	5	-	ns
t _r	rise time		-	6	-	ns
t _{d(off)}	turn-off delay time		-	21	-	ns
t _f	fall time		-	11	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 1.25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 13	-	0.75	1	V
t _{rr}	reverse recovery time	I _S = 2 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _j = 25 °C	-	30	-	ns

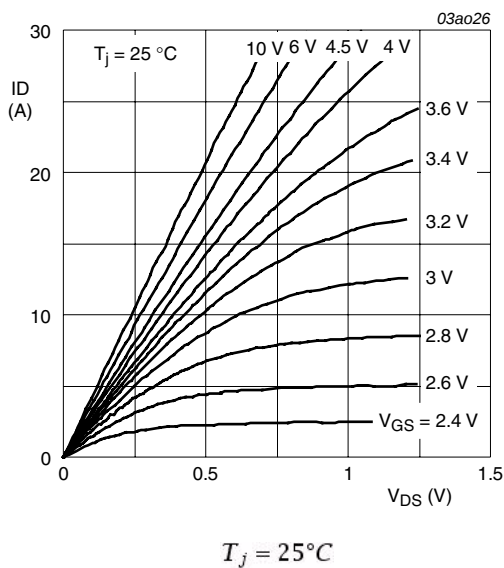


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical value

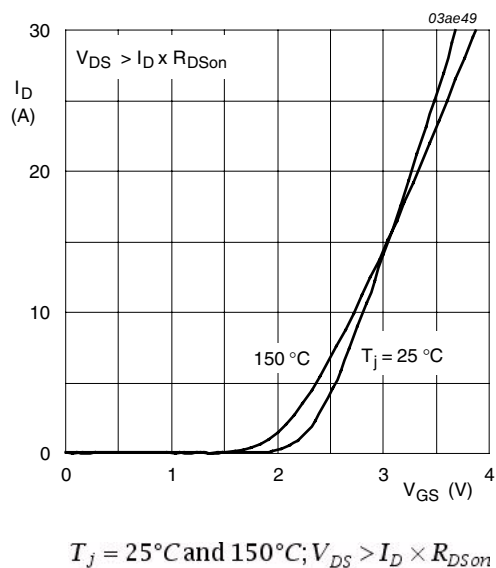


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

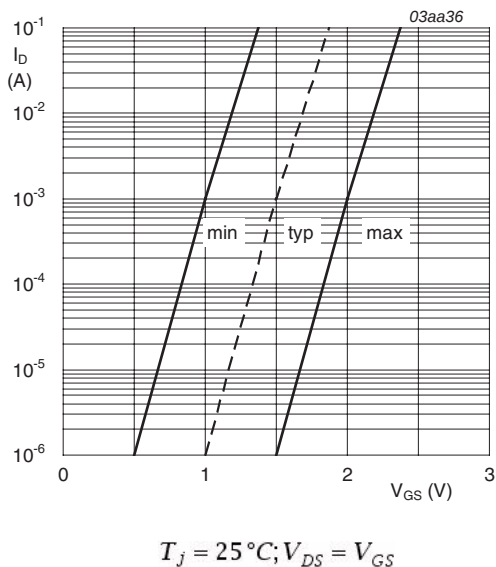


Fig 7. Sub-threshold drain current as a function of gate-source voltage

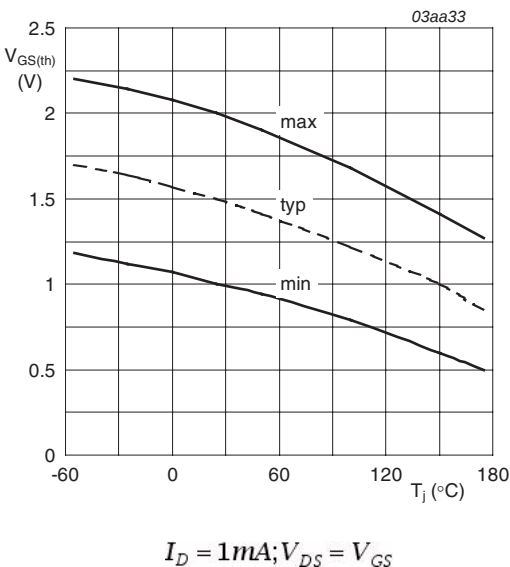


Fig 8. Gate-source threshold voltage as a function of junction temperature

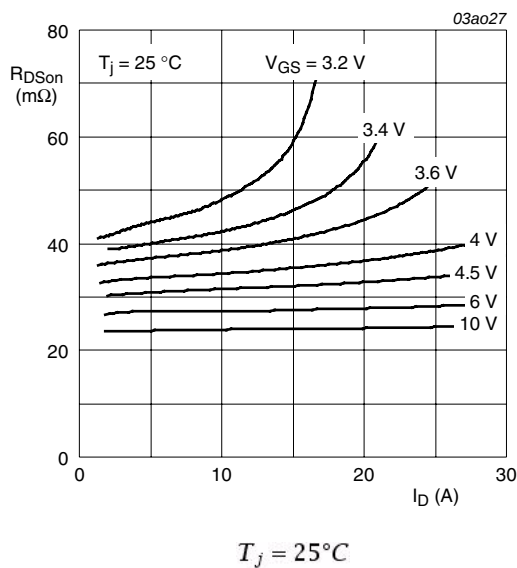


Fig 9. Drain-source on-state resistance as a function of drain current; typical values

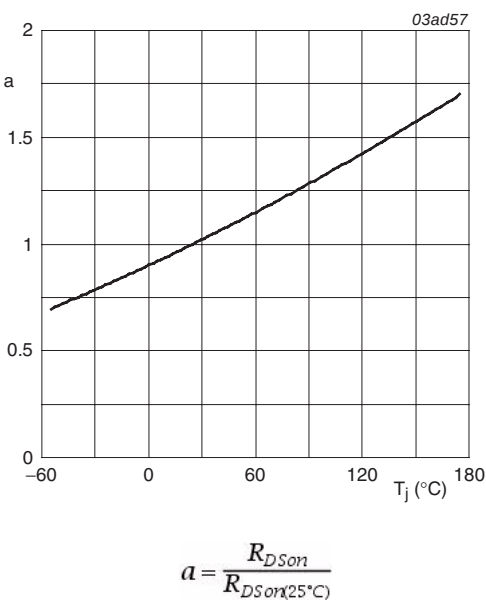


Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature

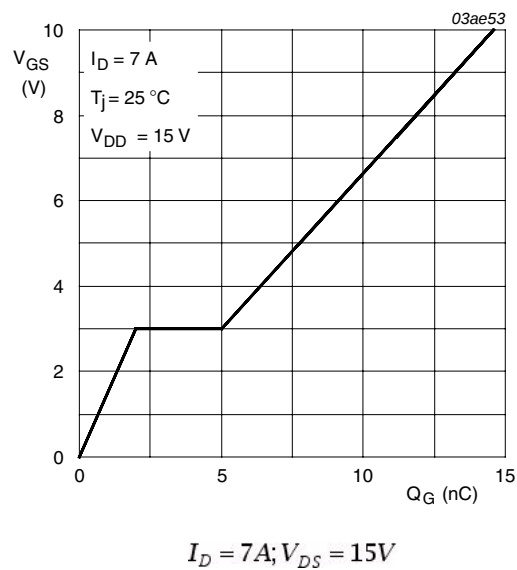


Fig 11. Gate-source voltage as a function of gate charge; typical values

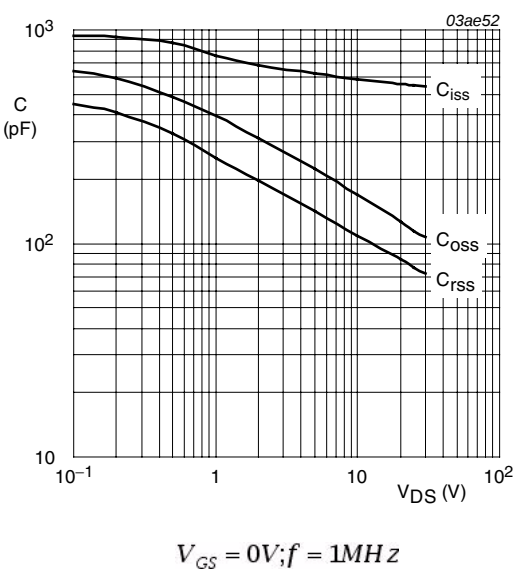


Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

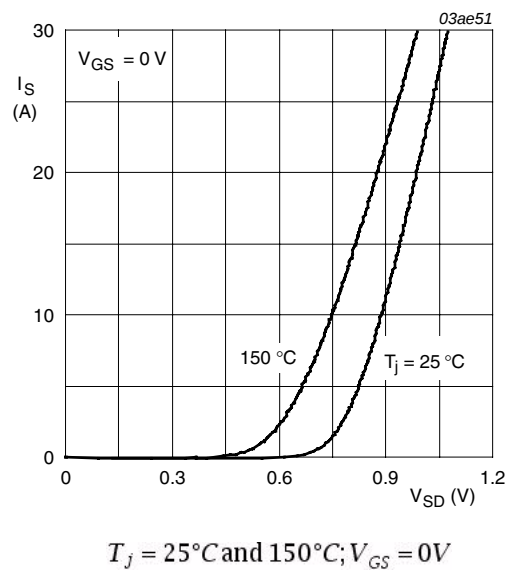


Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

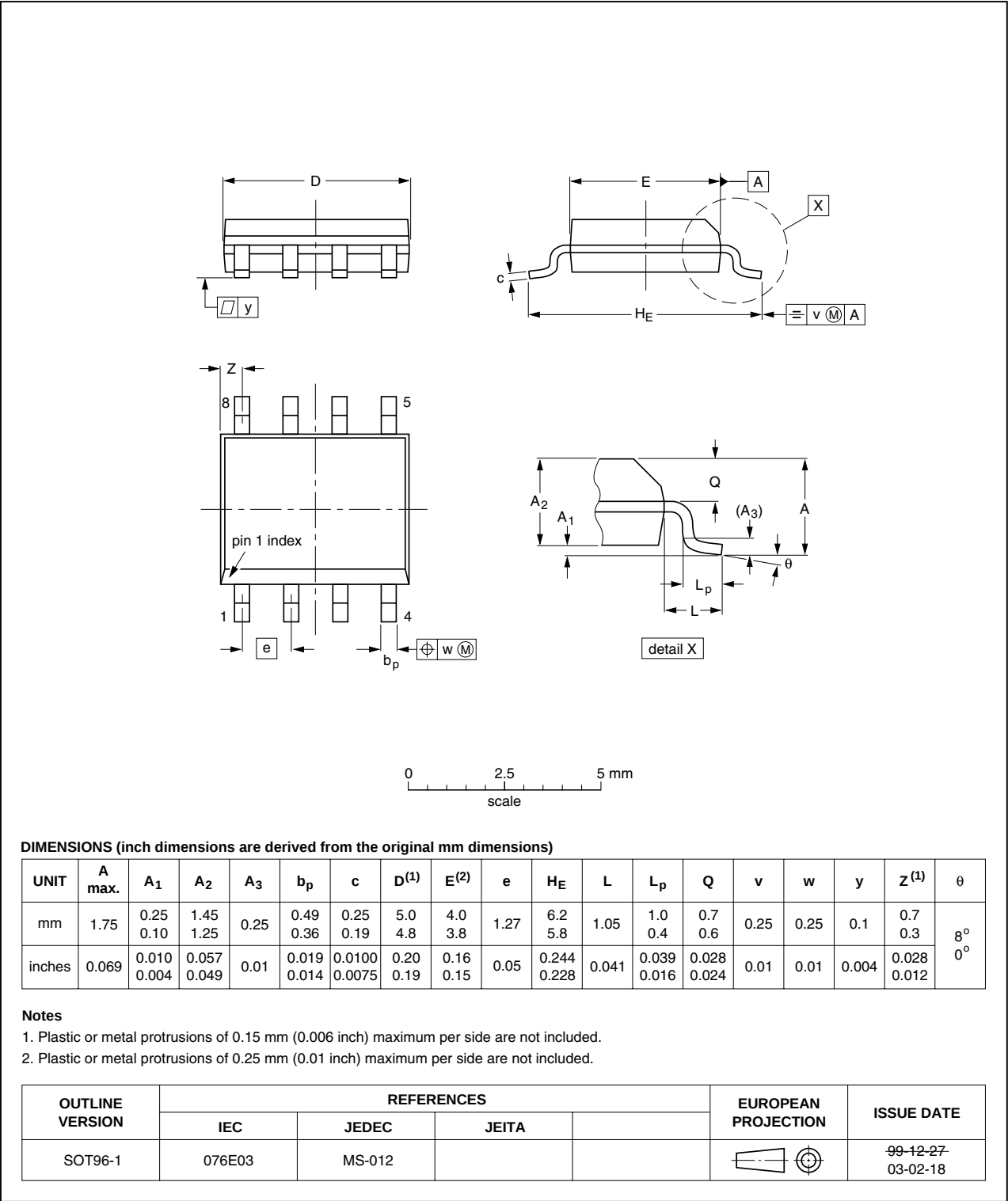


Fig 14. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHN203 _5	20100427	Product data sheet	-	PHN203 _4
Modifications:	• Various changes to content.			
PHN203 _4	20091208	Product data sheet	-	PHN203-03
PHN203 -03	20040126	Product data	-	PHN203 _2
PHN203 _2	19990101	Product specification	-	PHN203 _1
PHN203 _1	19980204	Objective specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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