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Kind regards,

Team Nexperia

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC convertors
- Notebook computers
- Portable equipment
- Switched-mode power supplies

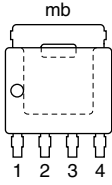
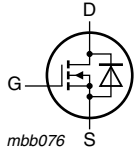
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	62.5	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 50\text{ A}$ ; $V_{DS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 11</a>	-	12.8	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	2.25	2.65	mΩ

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>SOT669 (LFAK)</b></p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

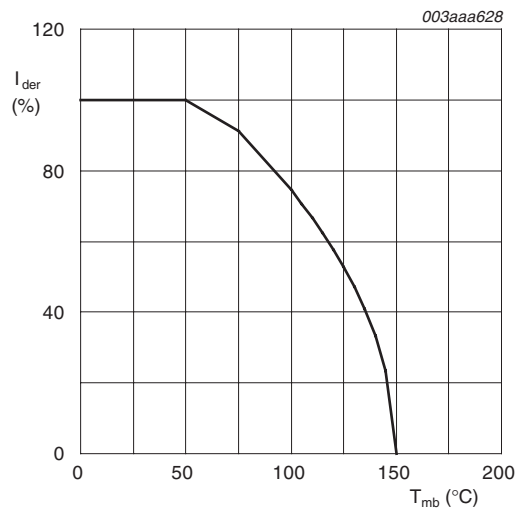
Type number	Package		Version
	Name	Description	
PH3120L	LFAK	plastic single-ended surface-mounted package (LFAK); 4 leads	SOT669

## 4. Limiting values

**Table 4. Limiting values**

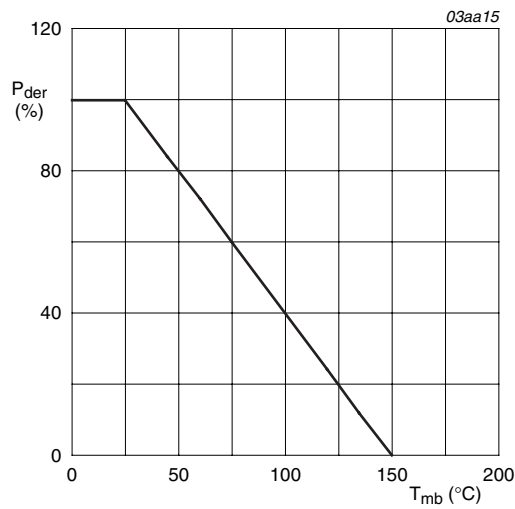
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	20	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	100	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	76	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	300	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	62.5	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	52	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	152	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 46.2\text{ A}$ ; $V_{sup} \leq 20\text{ V}$ ; unclamped; $t_p = 0.32\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	210	mJ



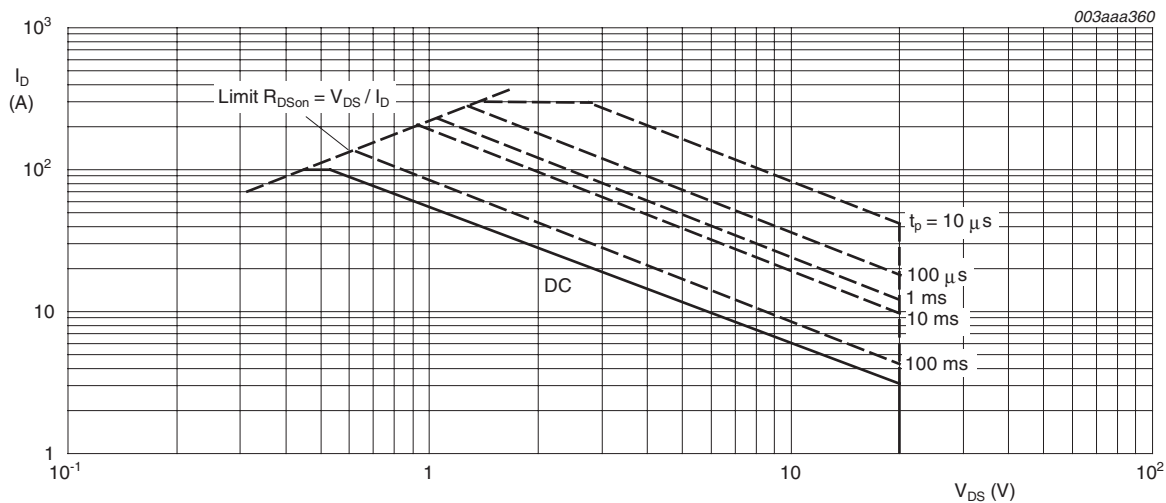
$$V_{GS} \geq 10\text{ V}; I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25^\circ\text{C}; I_{DM} \text{ is single pulse}; V_{GS} = 10\text{ V}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W

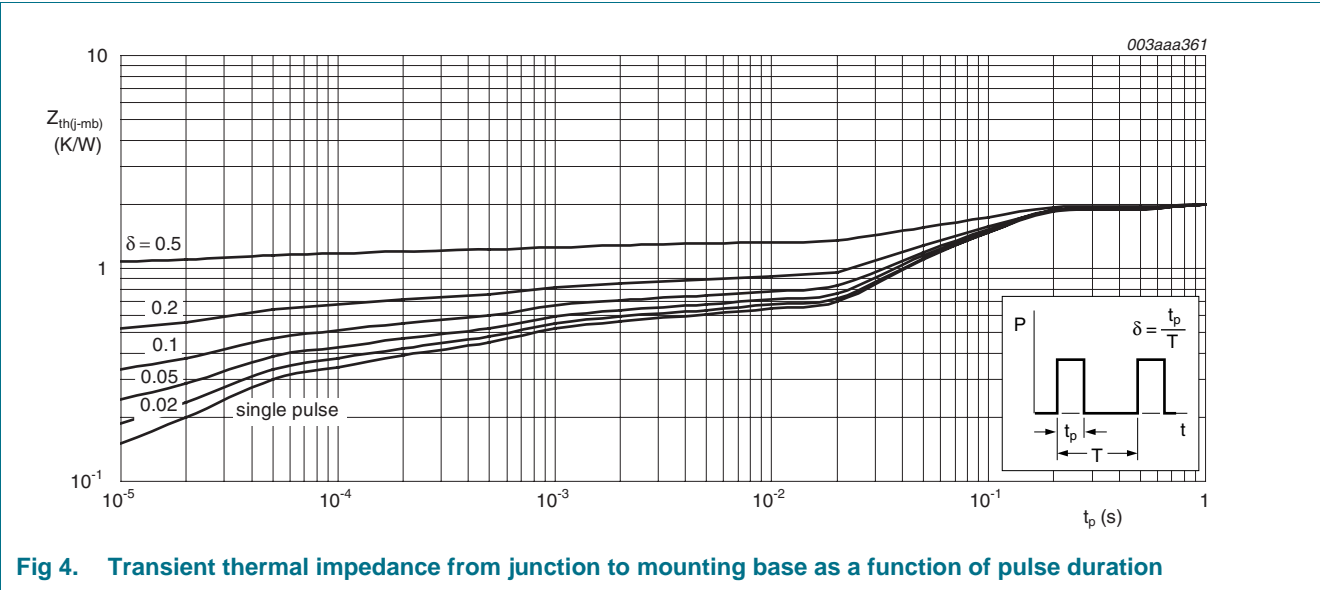
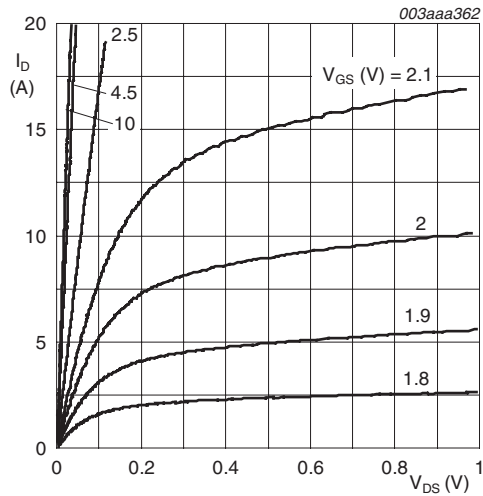


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

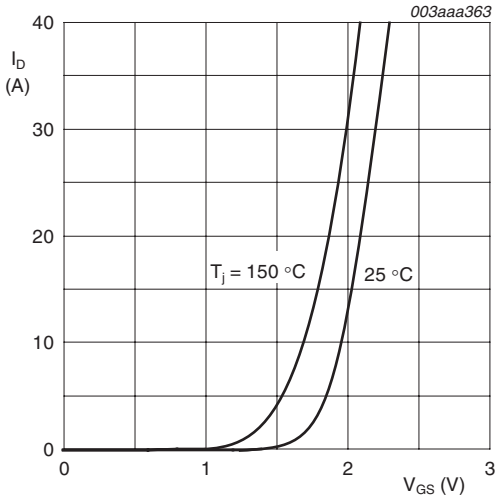
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 10 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	20	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 150 °C; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	0.65	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	1	1.5	2	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C	-	-	500	μA
		V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.06	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 15 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -15 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	2.25	2.65	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 150 °C; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	5.1	6.3	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	3	3.7	mΩ
Dynamic characteristics						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 50 A; V <sub>DS</sub> = 10 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a>	-	48.5	-	nC
Q <sub>GS</sub>	gate-source charge		-	12.7	-	nC
Q <sub>GD</sub>	gate-drain charge		-	12.8	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 10 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	4457	-	pF
C <sub>oss</sub>	output capacitance		-	1480	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	940	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 10 V; R <sub>L</sub> = 0.4 Ω; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 4.7 Ω; T <sub>j</sub> = 25 °C; I <sub>D</sub> = 25 A	-	34	-	ns
t <sub>r</sub>	rise time		-	90	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	114	-	ns
t <sub>f</sub>	fall time		-	88	-	ns
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 13</a>	-	0.77	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C	-	63	-	ns



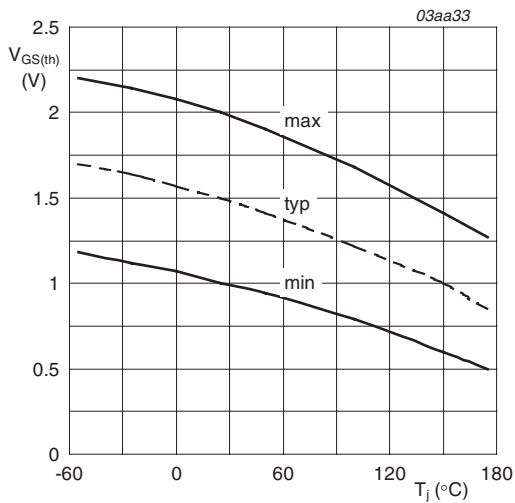
$T_j = 25^{\circ}\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



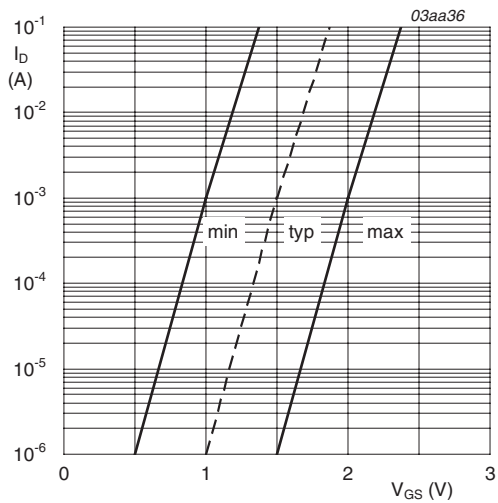
$T_j = 25^{\circ}\text{C}$  and  $150^{\circ}\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



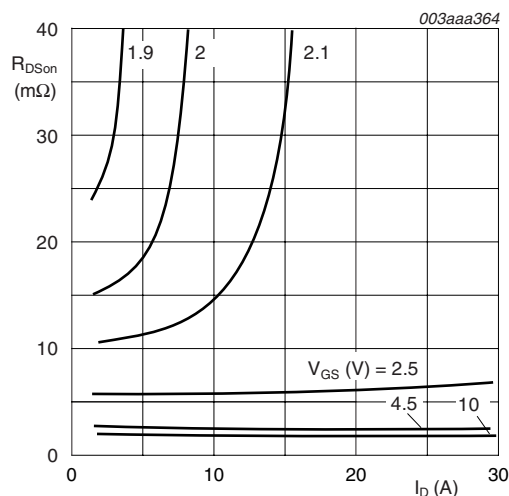
$I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature

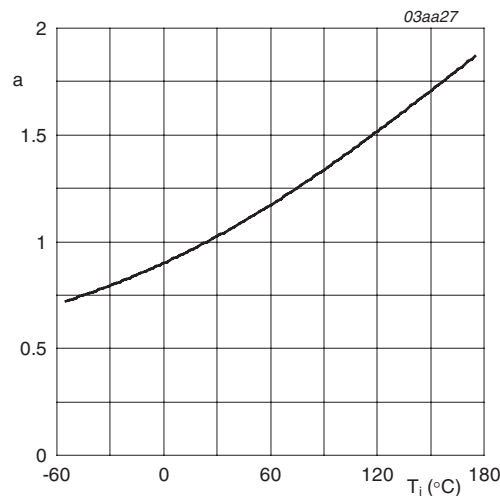


$T_j = 25^{\circ}\text{C}$ ;  $V_{DS} = V_{GS}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage

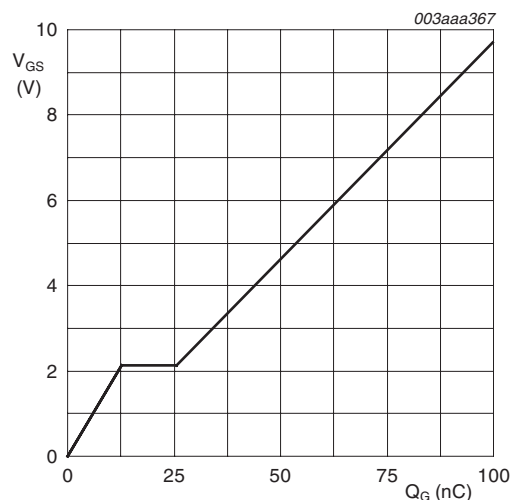

 $T_j = 25^\circ\text{C}$ 

**Fig 9.** Drain-source on-state resistance as a function of drain current; typical values

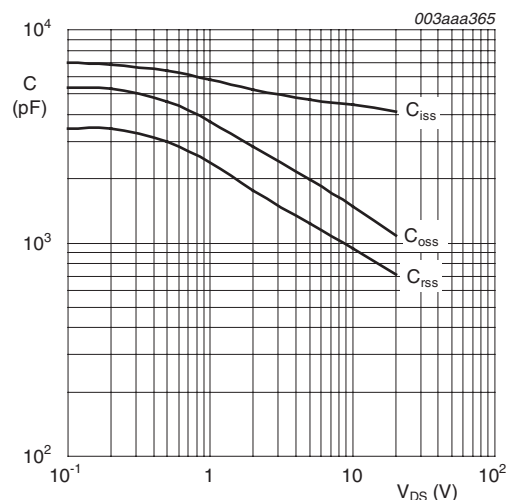


$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

**Fig 10.** Normalized drain-source on-state resistance factor as a function of junction temperature

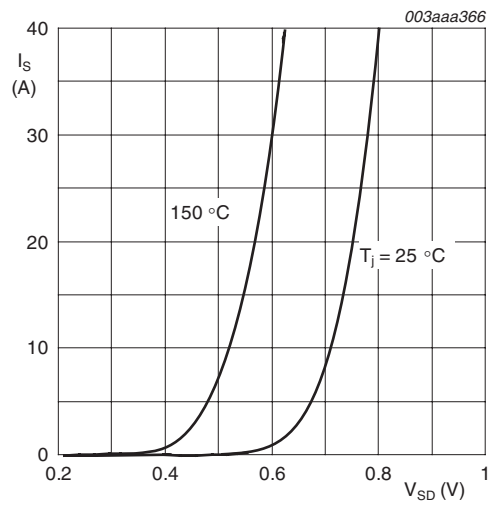

 $I_D = 50\text{A}; V_{DS} = 10\text{V}$ 

**Fig 11.** Gate-source voltage as a function of gate charge; typical values


 $V_{GS} = 0\text{V}; f = 1\text{MHz}$ 

**Fig 12.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{GS} = 0\text{V}$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFAK); 4 leads

SOT669

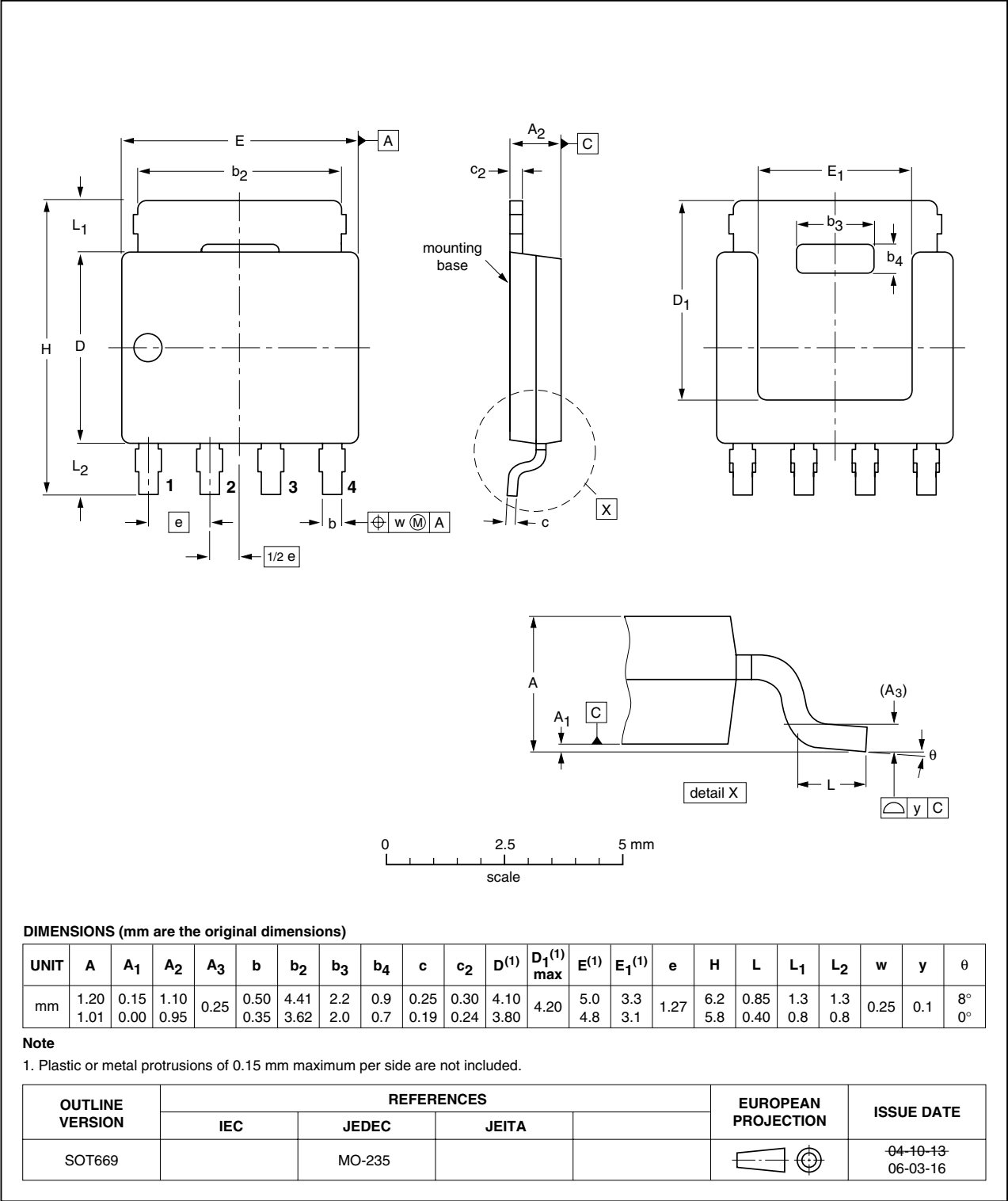


Fig 14. Package outline SOT669 (LFAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH3120L_3	20090330	Product data sheet	-	PH3120L_2
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>			
PH3120L_2 (9397 750 14089)	20050120	Product data sheet	-	PH3120L-01
PH3120L-01 (9397 750 12812)	20040304	Preliminary data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

1 Product profile .....1

1.1 General description .....1

1.2 Features and benefits .....1

1.3 Applications .....1

1.4 Quick reference data .....1

2 Pinning information .....2

3 Ordering information .....2

4 Limiting values .....2

5 Thermal characteristics .....4

6 Characteristics .....5

7 Package outline .....9

8 Revision history .....10

9 Legal information .....11

9.1 Data sheet status .....11

9.2 Definitions .....11

9.3 Disclaimers .....11

9.4 Trademarks .....11

10 Contact information .....11



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