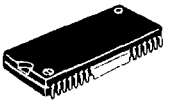
HA13601S — Advance Information

Three Phase Motor Driver with Speed Discriminator

Description

The HA13601S is hall sensorless three-phase brushless DC motor driver for HDD and has the following functions and features.

HA13601S



(MP-26DT)

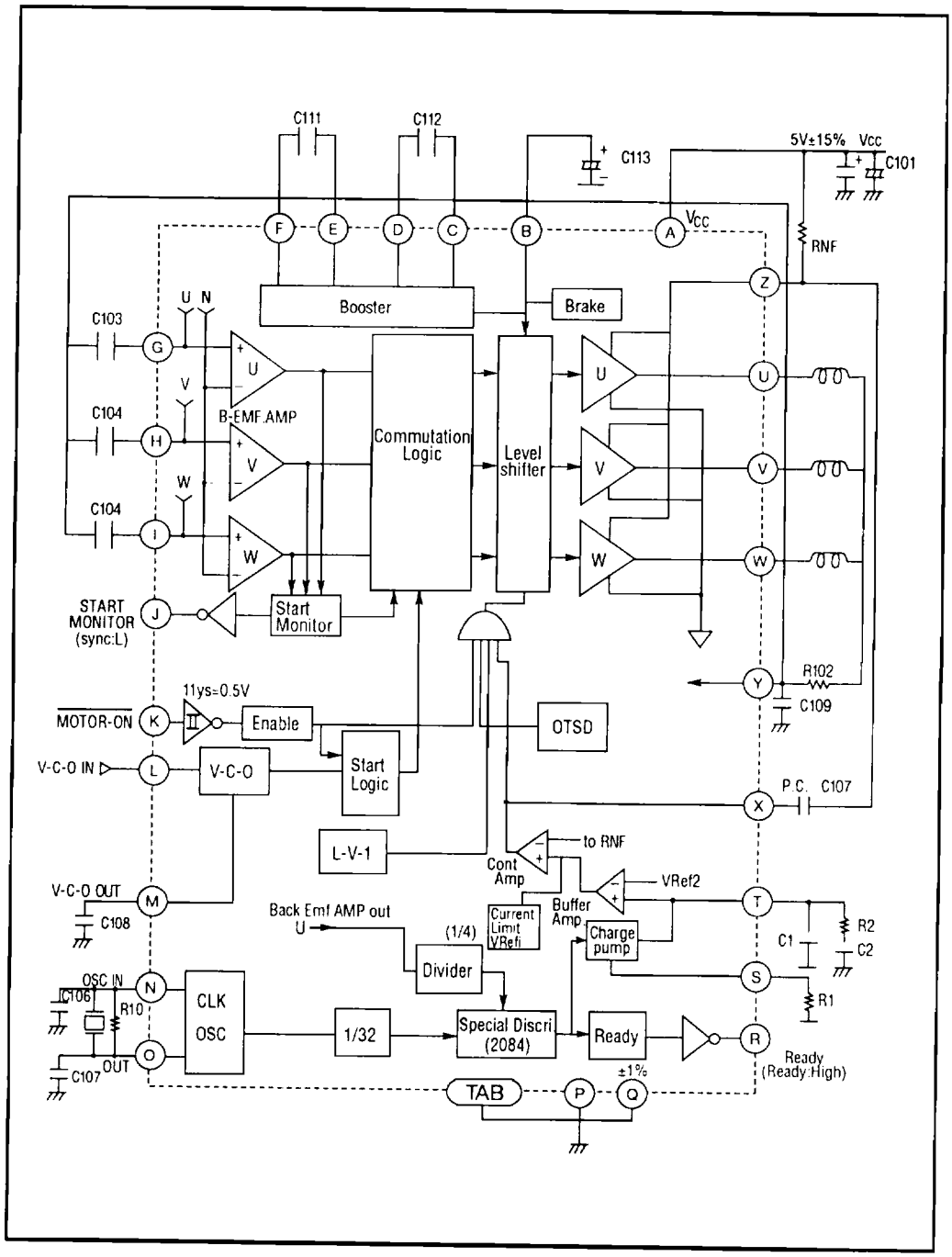
Functions

- 3-phase motor drive circuit (2.0 A/phase)
- Start up circuit
- Digital servo system
- Digital ready circuit
- Power off brake circuit
- Booster circuit
- Current limit circuit
- Start monitor circuit
- Motor on/off (Included chip enable)
- Internal protector (OTSD, LVI)

Features

- Hall sensorless motor driving system
- Low on voltage; 1.0 V max. ($@I_O$ = 1.0 A)
- Applicable for 4.0 MHz clock
- Small surface mount package ($\theta_j - c \leq 7°C/W$)

Block Diagram



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External Components

Parts No.	Recommended Value	Purpose	Notes
R_{101}	1 MΩ	Oscillation	
R_{102}	—	Neutral filter	
R_{NF}	—	Current sensing	5
R_1	≤ 10 kΩ	Integral constants	4
R_2	—		
C_{101}	10 μF and 0.1 μF	Power supply by-passing	
C_{102}	0.1 μF	Control amp phase compensation	
C_{103}, C_{104}, C_{105}	0.01 μF	Output filter	
C_{106}, C_{107},	10 pF	Oscillation	
C_{108}	—	VCO time constants	1, 2
C_{109}	—	Neutral filter	
C_{111}, C_{112}	0.01 μF	Booster	
C_{113}	0.47 μ	Booster & Brake set up time	
C_1	—	Integral constants	4
C_2	—		
X'tal	—	Oscillation	3

Notes: 1. The VCO frequency f_{VCO} should be satisfied with the following equation.

$$f_{VCO} = 5 \bullet \sqrt{\frac{P \bullet J}{K_T \bullet I_O}} \quad \text{.....(1)}$$

where,
J : moment of inertia (kg • cm • s²)
P : number of poles in the motor
K_T : Torque constant (kg = cm/A)
I_O : Output maximum current (A)

2. The OSC frequency f_{OSC} is determined by the following equation.

$$f_{OSC} = 555.6\, N_o \bullet P \bullet D \quad \text{.....(2)}$$

where,
N_o : Standard rotation speed (rpm)
D : Dividing ratio on divider (D = 1/4)

3. The integral constant can be designed as follows:

$$\omega_o \leq \frac{2\pi}{10 \bullet 4} \times \frac{N_o}{60} \times \frac{P}{2} \quad \text{.....(3)}$$

$$\frac{R_2}{R_1} = \frac{4}{9.55} \times \frac{R_{NF} \bullet J \bullet \omega_o \bullet N_o}{V_{R1} \bullet k_T \bullet G_{CTL}} \quad \text{.....(4)}$$

$$R_1 \leq 25\ k\Omega \quad \text{.....(5)}$$

$$C_1 = 1 / (\sqrt{10} \bullet \omega_o \bullet R_2)\ [F] \quad \text{.....(6)}$$

$$C_2 = 10 \bullet C_1\ [F] \quad \text{.....(7)}$$

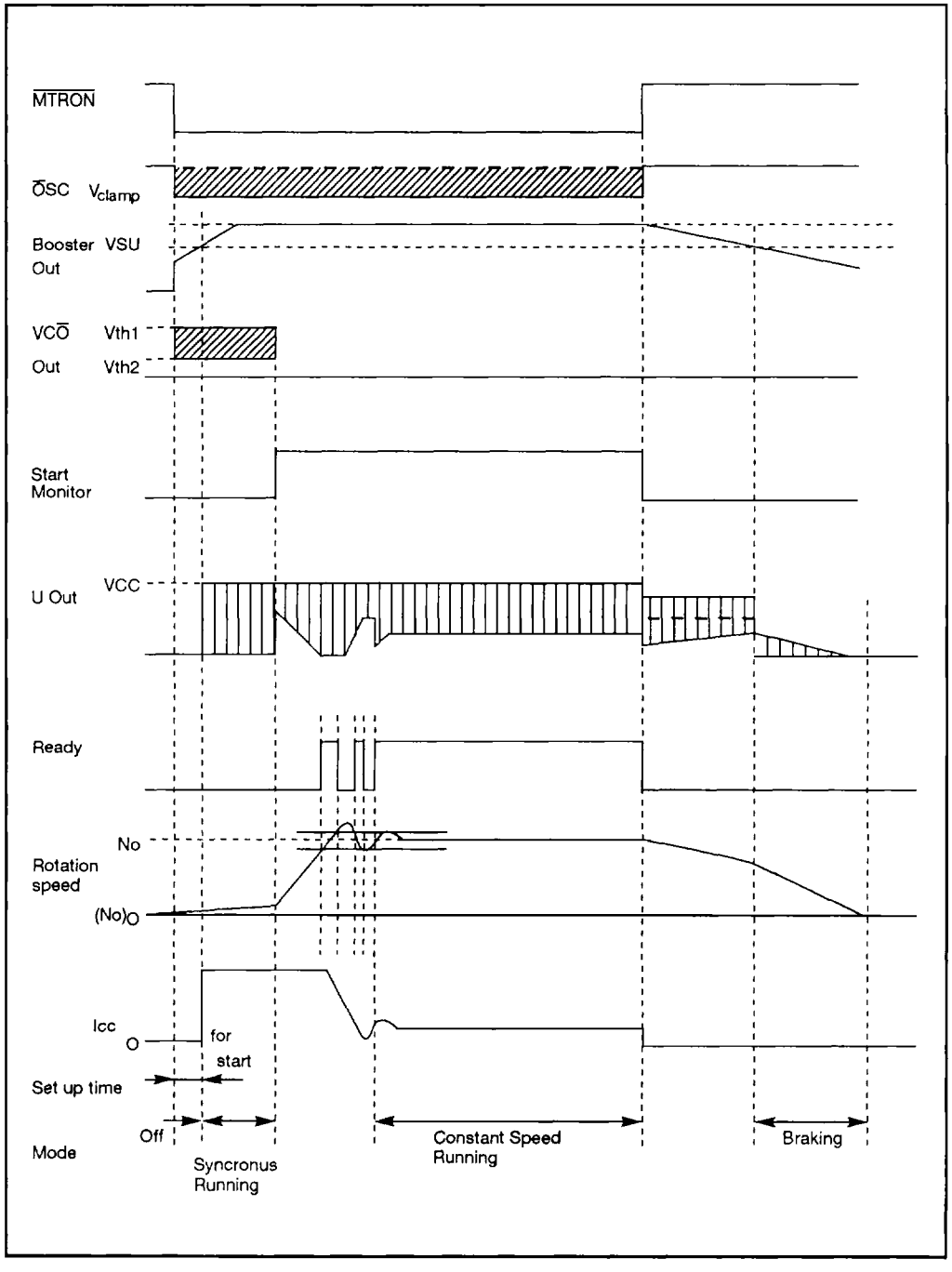
where,
G_{CTL}: gain from pin T to pin Z (see electrical characteristics)

4. Some motors require these components.
5. Output maximum current t_{OMAX} is determined by the following equation.

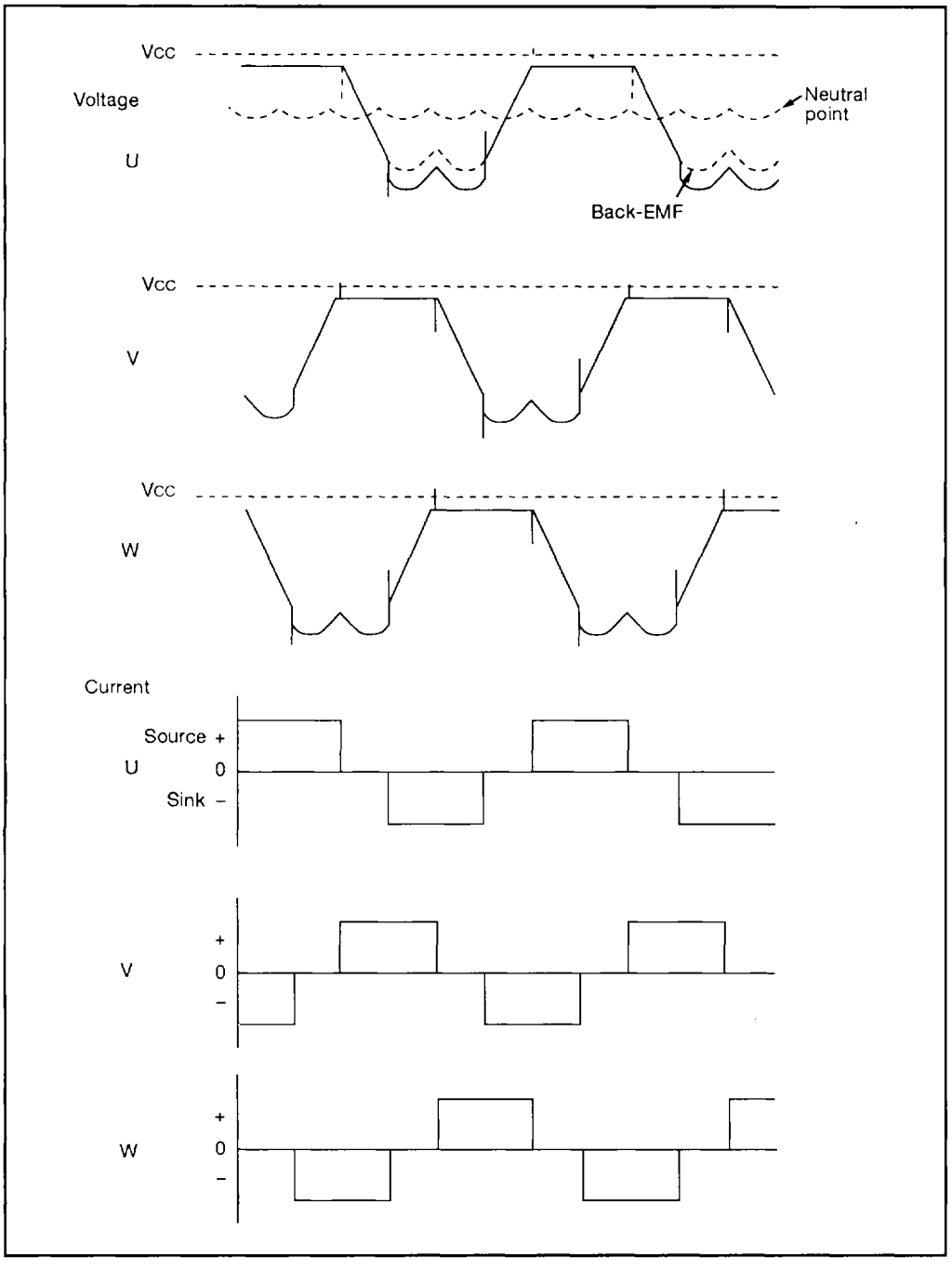
$$I_{OMAX} = V_{ref1}/R_{NF} \quad \text{.....(8)}$$

where,
V_{ref1} : Current limiter reference voltage

Timing Chart



Running


Vcc
Voltage
U
Neutral point
Back-EMF
Vcc
V
Vcc
W
Current
Source +
U
0
Sink –
V
+
0
–
W
+
0
–

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Notes
Power supply voltage	V_{CC}	7.0	V	1
Input voltage	V_{IN}	V_{CC}	V	2
Output current	I_O	2.0	A	3
Power dissipation	P_T	5	W	4
Junction temperature	T_j	+150	°C	5
Storage temperature	T_{stg}	−55 to +125	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Notes: 1. Operating voltage range is 4.25 V to 6.5 V.
2. Applied to $\overline{\text{MTRON}}$ and VCOIN inputs.
3. Operating locus must be within the ASO.
ASO of upper and lower power transistors are shown in figure 1 in references.
4. Value at T_C = 136°C
Thermal resistance is shown below.
$\theta_{j-c} \leq 7$°C/W, $\theta_{j-a1} \leq 15$°C/W (using Fe board), $\theta_{j-a2} \leq 62$°C/W (Using epoxy board)
5. Operating junction temperature is T_{jop} = 0°C to +125°C

Electrical Characteristics (Ta = 25°C, V_{CC} = 5.0 V)

Block	Item	Symbol	Min	Typ	Max	Unit	Test conditions	Applicable Terminal	Notes
Total	Quiescent current	I_{CC1}	—	8	12	mA	Pin K = 0.0 V	A	
		I_{CC2}	—	0.1	1.0		Pin K = 5.0 V		
MITRON	Input low voltage	V_{IL}	—	—	1.5	V		K	
	Input high voltage	V_{IH}	3.5	—	—				
	Input low current	I_{IL}	—	—	±10	μA			
	Input high current	I_{IH}	—	—	±10				
Output amp.	Leak current	I_{CER1}	—	—	1.0	mA	V_{CE} = 7 V	U,V,W	
	On voltage	$V_{DS(ON)}$	—	—	1.0	V	I_O = 1.0 A		1
	On Resistance	$R_{DS(ON)}$	—	0.6	1.0	Ω	I_O = 1.0 A		
	Current reference voltage limiter	V_{ref1}	225	250	275	mV	R_{NF} = 1.0 Ω	Z	2
VCO	Threshold voltage	V_{th1}	—	3.0	—	V		M	3
	Threshold voltage	V_{th2}	—	1.0	—				
	Sink current	I_{ts1}	40	50	60	μA	R_1 = 6.2 kΩ	M	
	Source current	I_{tf1}	40	50	60		Pin L = 5.0 V		
	Leak voltage	I_{CER2}	—	—	±5	μA	Pin J = 5.0 V	M	
B.EMF Amp	Min. input sensitivity	V_{min}	30	—	—	mV_{P-P}		G,H,I	
Control amp	Gain	G_{ctl}	–7	–9	–11	dB		T,Z	
	Internal reference	V_{ref2}	2.1	2.3	2.5	V			
Oscillator	Frequency error	f_{err}	—	—	±0.1	%	X'tal = 4 MHz	N,O	
Speed discri	Operating frequency	f_{osc}	—	—	8	MHz		N,O	
	Count number	N	—	2084	—	—			5
Charge pump	R_1 set-up voltage	V	1.15	1.25	1.35	V	R_1 = 6.2 kΩ	S	
	Charge current	I_{CH}	42	50	58	μA	R_1 = 6.2 kΩ Pin T - 1.0 V	T	
	Discharge current	I_{DIS}	–42	–50	–58				
	Leak current	I_{CER3}	—	—	±50	nA			
	Current ratio	I_{rat}	0.9	1.0	1.1	—	$t_{rat} = I_{CH}/I_{DIS}$		
Start monitor	Output high voltage	V_{OH1}	V_{CC} – 0.4	—	—	V	I_O = –1.0 mA	J	
	Output low voltage	V_{OL1}	—	—	0.4		I_O = 1.0 mA		
Ready	Output high voltage	V_{OH2}	V_{CC} – 0.4	—	—	V	I_O = –1.0 mA	R	4
	Output low voltage	V_{OL2}	—	—	0.4		I_O = 1.0 mA		
LVI	Recovery voltage	V_{LVI}	—	3.5	4.0	V			
Booster	Clamp voltage		Vclamp	V_{CC} + 7	V_{CC} + 9	V_{CC} + 11	V		B
	Set up voltage	V_{su}	V_{CC} + 3	—	V_{CC} + 4				
Brake	Start time	T_{br}	TBD	500	TBD	ms	C_{113} = 0.47μF	U,V,W	
OTSD	Operating temperature	T_{TSD}	125	150	—	°C			5
	Hysteresis temperature	T_{hys}	—	25	—				

Notes: 1. Sum of upper and lower TRS.
2. The reference voltage V_{ref2} is measured from pin A to pin Z.
3. See timing chart.
4. Ready output becomes high while the rotation speed error is smaller than 1%.
5. Design guide only

References

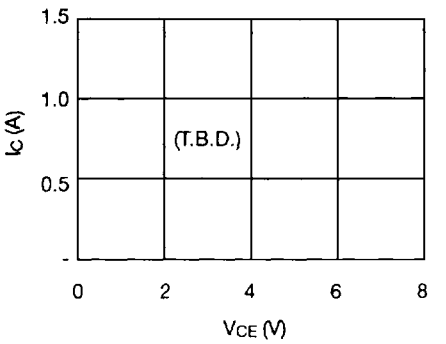


Figure 1 ASO of Output Stages