MINDSPEED®

Product Brief

PC333 Public Access Small Cell SoC: 32-User, LABS

PC333 Features

- Implements a complete 3GPP Release 6/7 HSPA+ Femto Access Point (FAP) supporting
  - Up to 32 simultaneous users or channels
  - 3GPP Local Area Basestation Compliant
  - Up to 21Mbps HSDPA, 5.5 Mbps HSUPA
  - RX diversity support
  - Soft handover support
  - Enhanced cell-FACH
- Support for up to 400 smart phones using smartSignaling™ (Enhanced cell-FACH)
- Pin Compatible with PC302/PC312 and PC323
- Glueless RF interface
- High performance 700MHz ARM11 subsystem suitable for running protocol stacks
  - ARM1176JZ-S processing core
- Advanced security features including:
  - ARM TrustZone®
  - Hardware accelerator IPsec and Kasumi
  - True Random Number Generator
  - User defined secure boot
  - One Time Programmable (OTP) keys provide for encrypted boot
- Energy saving modes to enable low power operation.
- Network monitoring functions extends zero-touch femtocell provisioning to picocells

Description

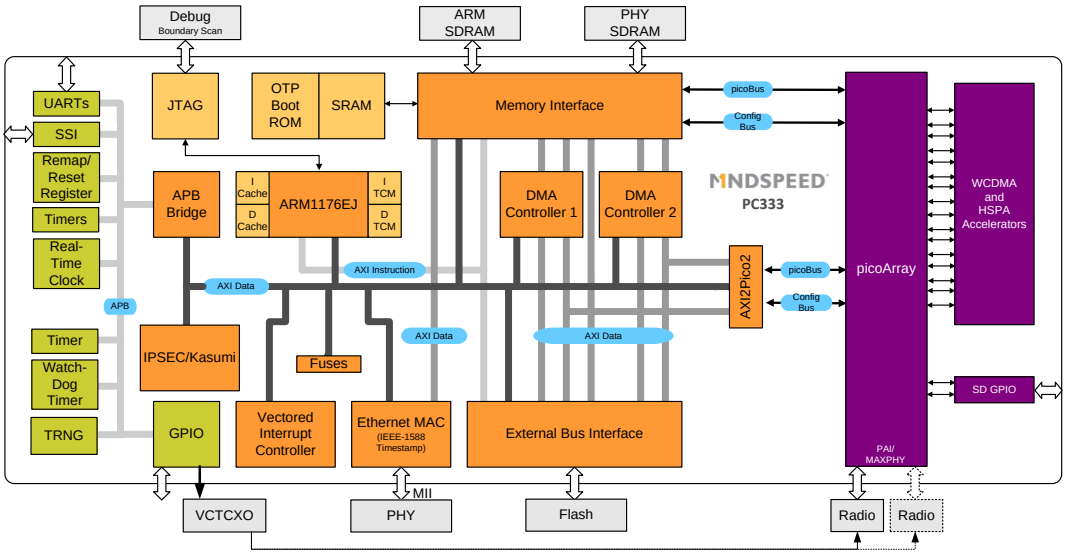
The Mindspeed PC333 is a single chip 3GPP Local Area Basestation Femtocell baseband and host processor SoC solution. It is part of Mindspeed's complete baseband platform family of chips that drives femtocell cost models from residential through to enterprise, metro and picocells.

The PC333 supports 32 channels of voice and data for uplink and downlink. The 32 channels may be configured as user voice/data, RACH, DCH, E-DCH, or common E-DCH. For instance 30 users with full UL/DL capability and 2 channels of RACH could be configured.

The PC333 consists of 3GPP NodeB Local Area Basestation baseband, ARM11 processor, cryptographic engine, high-speed accelerators, and peripherals to support HSPA+ requirements. All baseband processing from digital samples to/from RF through to network interfacing are integrated enabling an extremely low BOM cost.

Pin compatibility with PC302, PC312 and PC323 allows the creation of a single design suitable for residential, indoor enterprise and outdoor metrocell applications.

Enhanced security features are supported for authentication, location detection, encryption and the code protection.



SoC Architecture

The PC333 SoC consists of a ARM11 processor 3GPP NodeB PHY, cryptographic engine, high-speed accelerators, and peripherals to support Enterprise HSPA+ FAP requirements. The ARM processor supports customer or partner FAP stack, and communicates to the PHY via the standard layer 1 interface. The picoArray processors and accelerator logic supports the Physical Layer software. The picoArray is used to implement scheduling and a management algorithms in Node-B mode and can be reconfigured to implement network monitoring functions when needed for provisioning and interference mitigation. The picoArray's flexibility allows software upgrades to be applied as necessary in line with product releases, localizations, standardization updates, bug fixes, and performance enhancements.

To minimize cost and power the PC333 has dedicated hardware support for sample, chip and symbol rate PHY processing including turbo decoders, rake receivers, equalizers etc.

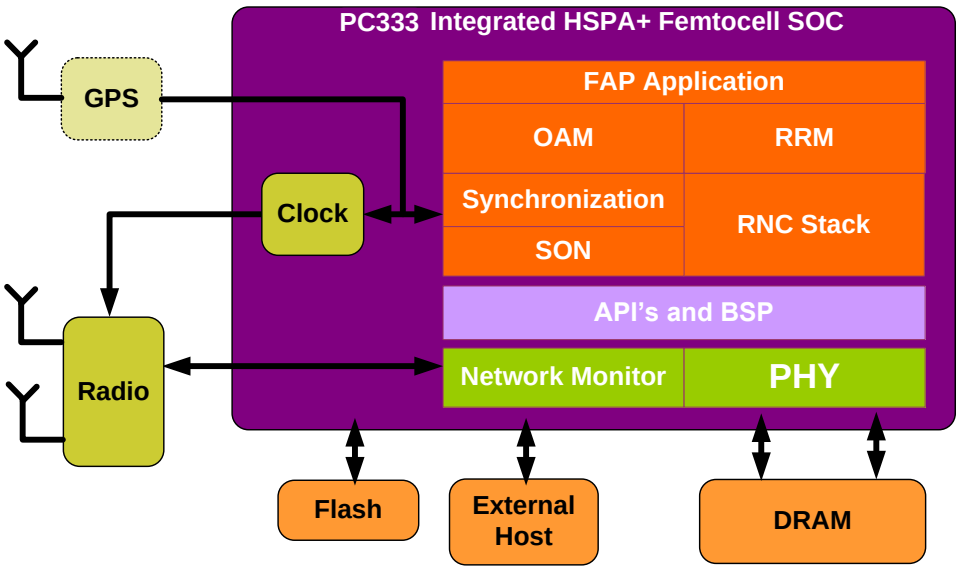


Figure 1 PC333 Femtocell System on Chip Architecture

ARM Sub-System

The ARM sub-system is based around the ARM1176JZ-S core from ARM Ltd. This powerful 32-bit RISC processor is highly optimized for low power, high performance, computing needed for RNC stack and Trusted Platform Module (TPM) processing. The PC333 ARM11 sub-system has been architected to aid RNC stack processing, security and the synchronization functions needed for operation.

ARM Memory Architecture

The memory architecture supports a full range of memory types, allowing flexible memory map allocation depending upon the particular application requirements. The cache and tightly coupled memory deliver maximum processor performance. The memory types are summarized as follows

- On-chip memory for maximum performance
  - 32kB instruction, 32kB data cache, 32-bits wide
  - 16kB instruction, 16kB data TCM (Tightly Coupled Memory), 32-bits wide single cycle access
  - 128kB SRAM, 32-bits wide
- NAND or NOR Flash interface
- DDR2 SDRAM Interfaces

ARM Peripherals

The PC333 integrates a number of peripheral blocks allowing both a reduction in total system BOM cost, as well as providing flexible interfaces to application specific sub-systems. The principle ARM1176JZ-S peripheral blocks are summarized as follows:

- Ethernet MAC with Reduced MII and IEEE-1588 support
  - Reverse MII interface allowing direct connection to MII interfaces of router/WiFi chipsets
- 2 8-channel DMA controllers
- 8 GPIOs with interrupts
- Up to another 48 GPIOs (dependent upon system usage/muxing)
- Vectored Interrupt Controller
- IPsec Encryption/decryption engine
- Kasumi ciphering
- SHA1/2 authentication

Security

The PC333 includes a number of security features:

- Secure boot is provided over conventional flash, SPI flash or the MII interface.
- On-chip customer-programmed One Time Programmable (OTP) keys provide for encrypted boot and other authentication functions. Additional 16k bytes of OTP non-volatile storage that serves as the boot code for the device is sufficient to accommodate a customer's own secure boot function. This allows choices about how the device behaves at boot in terms of self-generated keys for authentication to the network, storage of multiple long keys (2048 bits and longer).
- A True Random Number Generator (TRNG) enhances the ability to create asymmetric keys.
- On-chip IPsec and Kasumi encryption secures the flow of data from the network and wireless interfaces. A cryptographic engine provides support for SHA1, SHA2, AES, DES & 3DES algorithms. Support is also provided for the 3GPP Kasumi security algorithm. An IPsec offload engine implements crypto and hashing functions for IPsec (as specified in RFCs 4301-4309)
- The PC333 implements the TrustZone® from ARM to allow creation of hypervisors in an OS for secure key transactions, certificate transactions, and authentication of software processes.

PC333 Performance capability

The PC333 offers the following HSPA+ performance features. A summary of capability using the PC8229-333 PHY is given in Table 1.

Parameter	PC8229-333
Specification Version (Features)	3GPP FDD Release 6-7
Basestation Specification	Local Area Basestation
Cell Capabilities	
Number of carriers	1
Number of cells	1
Number of Tx antennas	1
Number of Rx antennas	2
Maximum cell radius	2000 m
Maximum UE speed	120 km/h
Soft handover	YES
Common Channels	
P-SCH and S-SCH	1
P-CPICH	1
P-CCPCH	1
S-CCPCH	2
PICH	1
PRACH signatures	4
Enhanced CELL_FACH	YES
Dedicated Channels	
Max channels	32
Max simultaneous R99 dedicated channel users	32[1] (Soft PRACH)
F-DPCH	YES
HSDPA Channels	
Maximum number of OVSF codes	15
Maximum number of served users	32
Maximum number of HS-SCCH	2
HS-PDSCH modulation	QPSK, 16QAM, 64 QAM
UE categories	1-20
Peak HSDPA Data rate	21 Mbps
HSUPA Channels	
Maximum number of served users	32
Peak HSUPA Data rate	5.5Mbps
TTIs supported	10ms, 2ms
HSUPA minimum SFs supported	SF2
UE categories	1-6
HSUPA modulation	QPSK

Table 1 Summary of PC8229-323 PHY capabilities

[1] 32 users supported with Soft PRACH on PC8229-3x3, some roadmap features not supported in this mode.

RX Diversity

RX diversity is essential in basestations that support greater than 8 users, such as Enterprise and Metrocell applications. Uplink pole capacity becomes severely restricted with higher UE count as noise rise increases. Using RX diversity allows the baseband to overcome inevitable nulls in the RX paths, as at least one antenna is likely to have an un-faded uplink for a given UE. Maximal ratio combining of the two antennas maximizes received signal to noise ratio, and subsequently maximizes pole capacity. RX diversity results in higher uplink performance, capacity, and lower UE TX power thus saving UE battery life.

Soft handover

Soft handover within the network improves the UE experience by increased cell edge coverage and smoother transitioning between adjacent cells on the same frequency. Soft handover baseband processing is supported in Enterprise and Metrocell Femtocells applications, with the benefit of PC8229 flexibility of channel resource availability. PHY support includes extended rake receiver window, increased frequency offset support and inner loop power control support (DL TPC pattern). By selection combining within the RNC functionality in the uplink results in lower target SIR, lower UE power and reduced uplink interference, and hence improving coverage and capacity performance.

smartSignaling™ Push Email and Smartphone Capacity Extension

smartSignaling™ is a set of features to reduce the operator's network signaling load, improve service to smartphones, and improve smartphone UE battery life. smartSignaling™ is Mindspeed's support for enhanced cell_FACH capability which allows the use of common channels and allows smartphones to maintain a connected state eliminating repetitive data session setup and tear-down, therefore reducing signaling load. Where the full dedicated user count is not required then redundant user channels can be allocated to RACH or common E-DCH functions to support enhanced cell-FACH, supporting smartphones in the exchange of small amounts of data in push-email or similar applications. Simulation analysis has shown that up to 400 smartphone connections can be supported using the smartSignaling™ feature.

PC333 Supported Software

Mindspeed supplies the following software targeted for PC333 based developments:

- PC8229-323 24 user HSPA+ Physical layer software PHY incl APIs and diagnostics
- PC8210-3x3 3G Network Monitor Physical layer software PHY
- PC8211-3x3 2G Network Monitor Physical layer software PHY
- systemTest Application software supporting TS25.141 test cases
- Libradio radio control library
- Board Support Package (BSP 4 or later)
- PC5100 picoTools development tool

PC333 Supported Hardware/Systems

Mindspeed supplies the following hardware targeted for PC333 based developments:

- PC7333 Enterprise/Metro development platform
- PC5300 picoICE JTAG Debugger

Package

The PC333 package is Plastic Ball Grid Array PBGA 396. The pin and package compatible with PC302, PC312 and PC323.

Power Dissipation

The PC333 has many energy saving features to enable the lowest power FAP implementations in line with the EEC Code of Conduct on Energy Consumption of Broadband Equipment. The nominal power consumption in typical conditions with 8 users is 1.89W (further information found in the PC3x3 datasheet).

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