Advance Product Information

VSC880

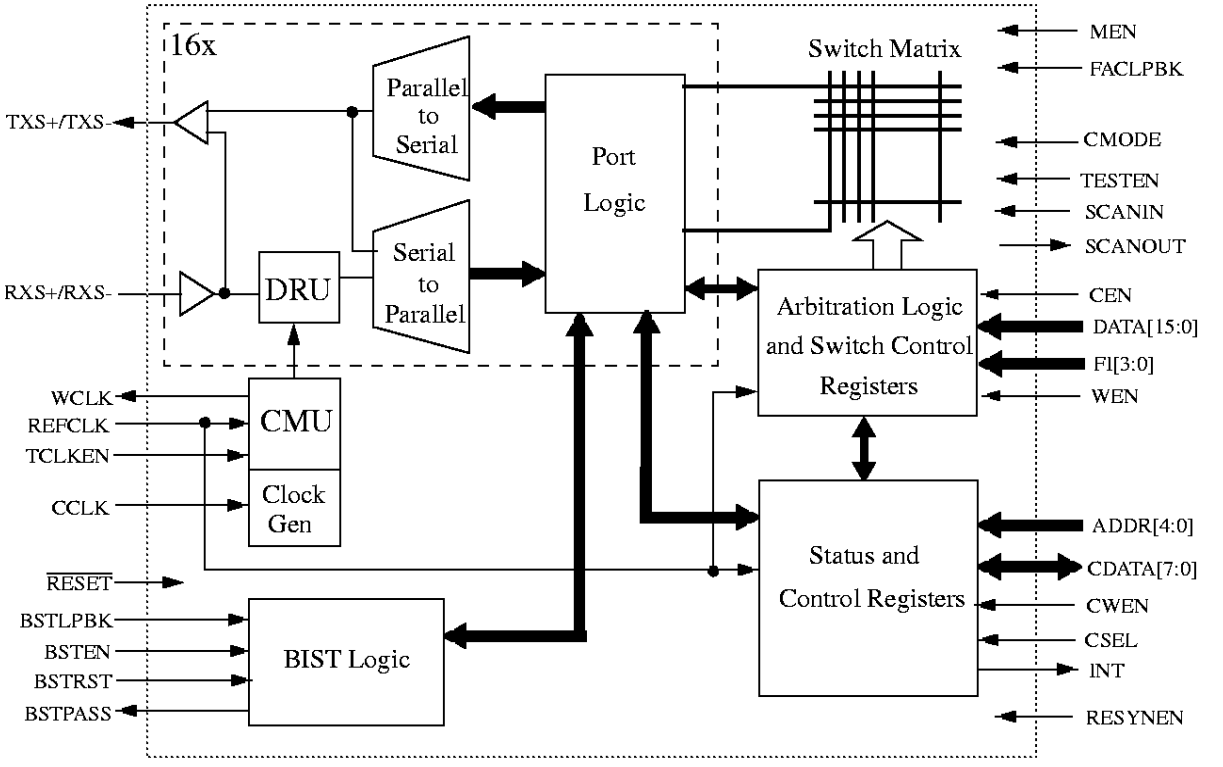
High Performance 16 x16 Serial Crosspoint Switch

CONDENSED

Features

- 16 X 16 Synchronous Serial Cross Point Switch
- Serial Data Rates are 2.0Gb/s
- 32Gb/s Aggregate Data Bandwidth
- Parallel Switches Can Increase Data Bandwidth in Multiples of 32Gb/s
- Designed in Conjunction with the VSC870 Backplane Transceiver
- Automatic Word and Cell Synchronization to the Transceiver
- Two Modes of Operation: Distributed Control Self-routing *Packet Mode* and Central Control *Cell Mode*
- Multicast is Supported in all Modes
- Supports Variable Length Packets in Packet Mode
- Built-in Flow Control Channel in Packet Mode
- Supports Cell Synchronization in Cell Mode
- Parallel CPU Interface and Parallel Switch Configuration Interface
- Loopback, Built-in Self Test and Scan Functions
- 5V Tolerant TTL Inputs
- Single 3.3V Power Supply or Dual 2.0V/3.3V Power Supply to Reduce Power Dissipation
- Comes in a 304 BGA Package

Switch Block Diagram



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General Description

The VSC880 is a 16 x 16 serial cross point switch with serial data rates at 2.125Gb/s. The VSC880 has been designed to operate with the VSC870 backplane transceiver to establish a synchronous high performance switching system with an aggregate bandwidth of 32Gb/s. The switch chip transmits the master word clock (62.5Mb/s), and master cell clock (if used) to all port cards through the serial data channels. The transceivers automatically perform bit alignment, word alignment and cell alignment to the switch chip. The transceiver and switch chip have been optimized for both self-routing and cell based systems and include special commands for connection requests (self-routing) and cell synchronous operation (cell based). In addition, a parallel CPU interface can be used to control internal modes and read status information from the switch. A 20 bit interface can also be used to program the switch matrix in 4 clock cycles. The switch chip runs off of a 3.3V or 3.3V/2.0V power supplies.

Pin Descriptions

Pin	*Name*	*I/O*	*Freq Type*	*Description*
TXS[15:0]+/ TXS[15:0]-	Transmit Serial Outputs	O	2.125Gb/s CML	16 high speed serial differential transmit channels
RXS[15:0]+/ RXS[15:0]-	Receive Serial Inputs	I	2.125Gb/s CML	16 high speed serial differential receive channels
DATA[15:0]	Configuration Data Input	I	62.5Mb/s TTL	Parallel input signals used to program the switch matrix in 4 clock cycles when the signal CEN is HIGH.
FI[3:0]	Force IDLE Input	I	62.5Mb/s TTL	Parallel input signals used to program force IDLE words at the switch matrix output in 4 clock cycles when the signal CEN is HIGH.
CEN	Configure Enable	I	62.5Mb/s TTL	When CEN is held HIGH, the inputs DATA[15:0] and FI[3:0] can be used to program the switch matrix in 4 word clock cycles timed to the WEN signal.
WEN	Write Enable	I	62.5Mb/s TTL	If CEN is HIGH, this signal provides a synchronization pulse for loading switch configuration data into DATA[15:0] and FI[3:0].
ADDR[4:0]	Data Address	I	62.5Mb/s TTL	The address to read and write data through parallel interface CDATA[7:0].
CSEL	Chip Select	I	62.5Mb/s TTL	This signal allows several switch chips to share an 8 bit data bus connected to CDATA[7:0]. If CSEL is HIGH, data will be output from CDATA[8:0]. If CSEL is LOW, the outputs will be high impedance and the inputs disabled.
CDATA[7:0]	Status Data Output	B	62.5Mb/s TTL	Bidirectional CPU interface for the status and control registers. If CSEL is HIGH, the data will be output on the rising edge of REFCLK. If CSEL is LOW, the outputs will be high impedance and the inputs will be disabled.
CWEN	Control Write Enable	I	62.5Mb/s TTL	This signal is set HIGH to read the internal status registers through the parallel interface CDATA[7:0]. It is set LOW to write into this interface.

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Pin	Name	I/O	Freq Type	Description
RESYNEN	Resynch Enable	I	<1MHz TTL	If RESYNEN is HIGH, all links that have a link error condition will be reinitialized. This will override the internal control register settings.
INT	Interrupt	O	<1MHz TTL	If INT is HIGH, a receive error has occurred in one of the links that has it's output enable (OE) bit set HIGH and interrupt control register bit set HIGH.
MEN	Message Enable	I	<1MHz TTL	This signal is reserved for future use and should be set LOW during normal operation.
FACLPBK	Facility Loop Back	I	<1MHz TTL	If this signal is set HIGH, all serial inputs are looped back to their serial outputs.
CMODE	Cell Mode	I	<1MHz TTL	CMODE is set HIGH for Cell Mode operation.
TESTEN	Scan Test Enable	I	<1MHz TTL	When TESTEN is HIGH, the chip is placed in scan test mode. In this mode, REFCLK is used to shift the scan data.
SCANIN	Scan Data In	I	62.5Mb/s TTL	The scan test input signal.
SCANOUT	Scan Data Out	O	62.5Mb/s TTL	The scan test output signal.
WCLK	Word Clock	O	62.5MHz TTL	This is the word clock output.
REFCLK	Reference Clock	I	62.5MHz TTL	This is the reference clock and the source of the system wide word clock period.
TCLKEN	Test Clock Enable	I	<1MHz TTL	This input is set HIGH in test mode, so that the CMU is bypassed and the REFCLK becomes the bit clock.
CCLK	Cell Clock	I	62.5MHz TTL	This is the source of the system wide cell clock. It is internally synchronized to the REFCLK.
$\overline{\text{RESET}}$	Reset	I	<1MHz TTL	Global chip reset (active LOW)
BSTLPBK	Built-in Self Test Loop Back	I	<1MHz TTL	When BSTLPBK is set HIGH, all serial data output signals are looped back to their serial data inputs.
BSTEN	Built-in Self Test Enable	I	<1MHz TTL	When BSTEN is HIGH, at-speed built-in self testing is enabled.
BSTRST	Built-in Self Test Reset	I	<1MHz TTL	The BSTRST signal is set HIGH to reset the PRBS generator and comparator.
BSTPASS	Built-in Self Test Pass	O	<1MHz TTL	The BSTPASS signal is HIGH if BTSEN is HIGH and the PRBS comparator detects the correct pattern in built-in self test mode.

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AC Characteristics

Table 12.2: CML and TTL Outputs

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$T_{R,TTL}$	TTL Output Rise Time			TBD	ns	10-90%
$T_{F,TTL}$	TTL Output Fall Time			TBD	ns	10-90%
$T_{R,CML}$	CML Output Rise Time			TBD	ps	20-80%
$T_{F,CML}$	CML Output Fall Time			TBD	ps	20-80%

Figure 1: Transmit Data Input Timing Diagram

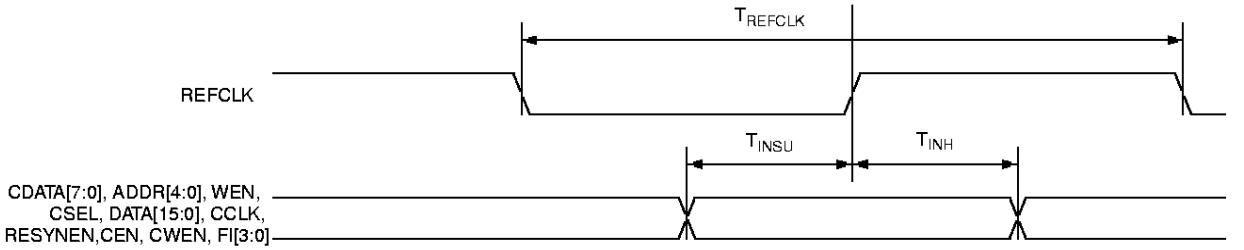

Table 12.2: Transmit Data Input Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{REFCLK}	Word clock period		16		ns
T_{INSU}	Parallel data setup time with respect to REFCLK			TBD	ns
T_{INH}	Parallel data hold time with respect to REFCLK			TBD	ns
T_{SKEW}	REFCLK to REFCLK skew using parallel switch chips			TBD	ns

Note: Duty cycle for T_{REFCLK} is 50% +/- 10% worst case

Figure 2: Receive Data Output Timing Diagram

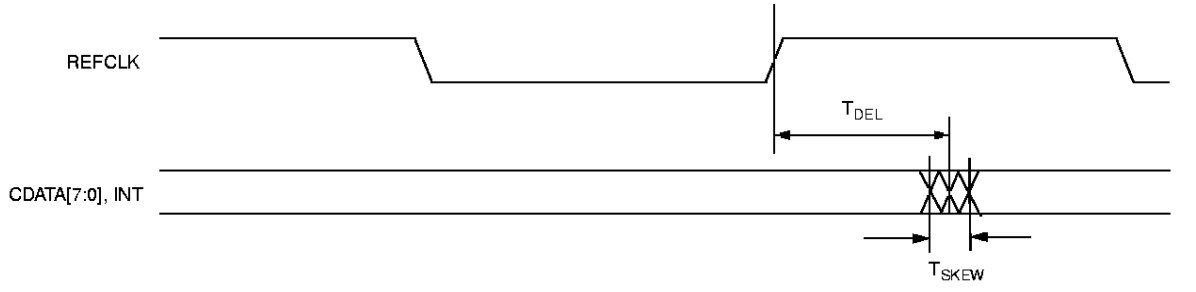

Table 12.2: Receive Data Output Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{DEL}	REFCLK to output delay	TBD		TBD	ns

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Table 12.2: CML and TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -6.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.4	V	I_{OL} = +6.0 mA
V_{OCM}	O/P Common Mode Range (CML)	TBD	—	TBD	V	At Min ΔV_{OUT}
ΔV_{OUT}	Differential Output Voltage (CML)	400	—	1300	mV	100Ω across input
V_{ICM}	I/P Common Mode Range (CML)	TBD	—	TBD	V	At Min ΔV_{IN}
ΔV_{IN}	Differential Input Voltage (CML)	200	—	1600	mV	—
V_{IH}	Input HIGH voltage (TTL)	2.0	—	V_{DD}+1.0	V	—
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	300	µA	V_{IN} =2.4V
I_{IL}	Input LOW current (TTL)	- 50	—	—	µA	V_{IN} = 0.4V

Hot Swap

The CML input and output buffers are subject to hot swap events while being connected and disconnected from the passive backplane. If the input is powered down but still receiving a signal from an output, the input must tolerate extra input current and power. If the input is powered up but has no input connection, it must go to a valid logic state. The table below lists the CML I/O parameters that relate to hot swap condition.

Table 12.3: Hot Swap CML I/O Parameters

Parameters	Description	Value	Units	Conditions
I_{CO}	CML maximum current delivered per output pin	TBD	mA	Normal Operation
I_{CI}	CML maximum current allowed per input pin	TBD	mA	V_{DD} = 0V
P_{CI}	CML maximum added power per input pin	TBD	mW	V_{DD} = 0V
V_{CDL}	CML input default logic state	HIGH	—	Input Open

Power Dissipation

Table 12.2: Power Supply Currents

Parameter	Description	(Max)	Units
I_{DD}	Power supply current from V_{DD}	3200	mA
I_{MM}	Power supply current from V_{MM}	5200	mA
P_{DS}	Single supply power dissipation (V_{DD})	29.0	W
P_{DD}	Dual supply power dissipation (V_{DD} and V_{MM})	22.0	W

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Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND ..... -0.5V to +4V
Power Supply Voltage (V_{MM}) Potential to GND ..... -0.5V to +4V
DC Input Voltage (CML inputs) ..... -0.5V to V_{DD} + 1.0V
DC Input Voltage (TTL inputs) ..... -0.5V to V_{DD} + 1.0V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 1.0V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (CML Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55° to +125°C
Storage Temperature ..... -65°C to +150°C
Maximum Input ESD (Human Body Model) ..... 1500 V

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) ..... +3.3V ±5 %
Power Supply Voltage (V_{MM}) ..... +2.0V ±5 % or +3.3V ±5 %
Commercial Operating Temperature Range* (T) ..... 0° to 70°C
Extended Operating Temperature Range* (T) ..... 0° to 110°C

* Lower limit of specification is ambient temperature and upper limit is case temperature.

Notice

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Warning

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