NEC

MOS INTEGRATED CIRCUIT

μPD16650

120-/128-OUTPUT TFT-LCD GATE DRIVER

The μPD16650 is a TFT-LCD gate driver. Provided with a level shift circuit at the logic input, this chip can output a high gate scan voltage for a CMOS-level input. The μPD16650 has an output change-over function for switching from the 120-output mode to the 128-output mode, and vice versa, thereby supporting the VGA, SVGA, and XGA panels. Its output enable function ($\overline{OE}$) enables installing the driver on either side.

FEATURES

- Output with high dielectric strength (on/off range: V_{DD} - V_{EE1} = 40 V_{MAX}.)
- Built-in shift direction change-over function
- Shiftable negative supply voltage (V_{EE1}) level (shift range: |V_{EE1} - V_{EE2}| = 10 V)
- Two acceptable CMOS input levels (3.3 and 5 V)
- Output enable function
- MC-selectable output count (MC = high: 120-output mode)
  (MC = low : 128-output mode)
- Slim TCP

ORDERING INFORMATION

Part number	Package
μPD16650N-×××	TCP (TAB package)
μPD16650N-×××	Standard TCP (OL pitch = 220 μm)

Remark When ordering, the customer can specify the external form of the TCP. Call one of our sales representatives for more information.

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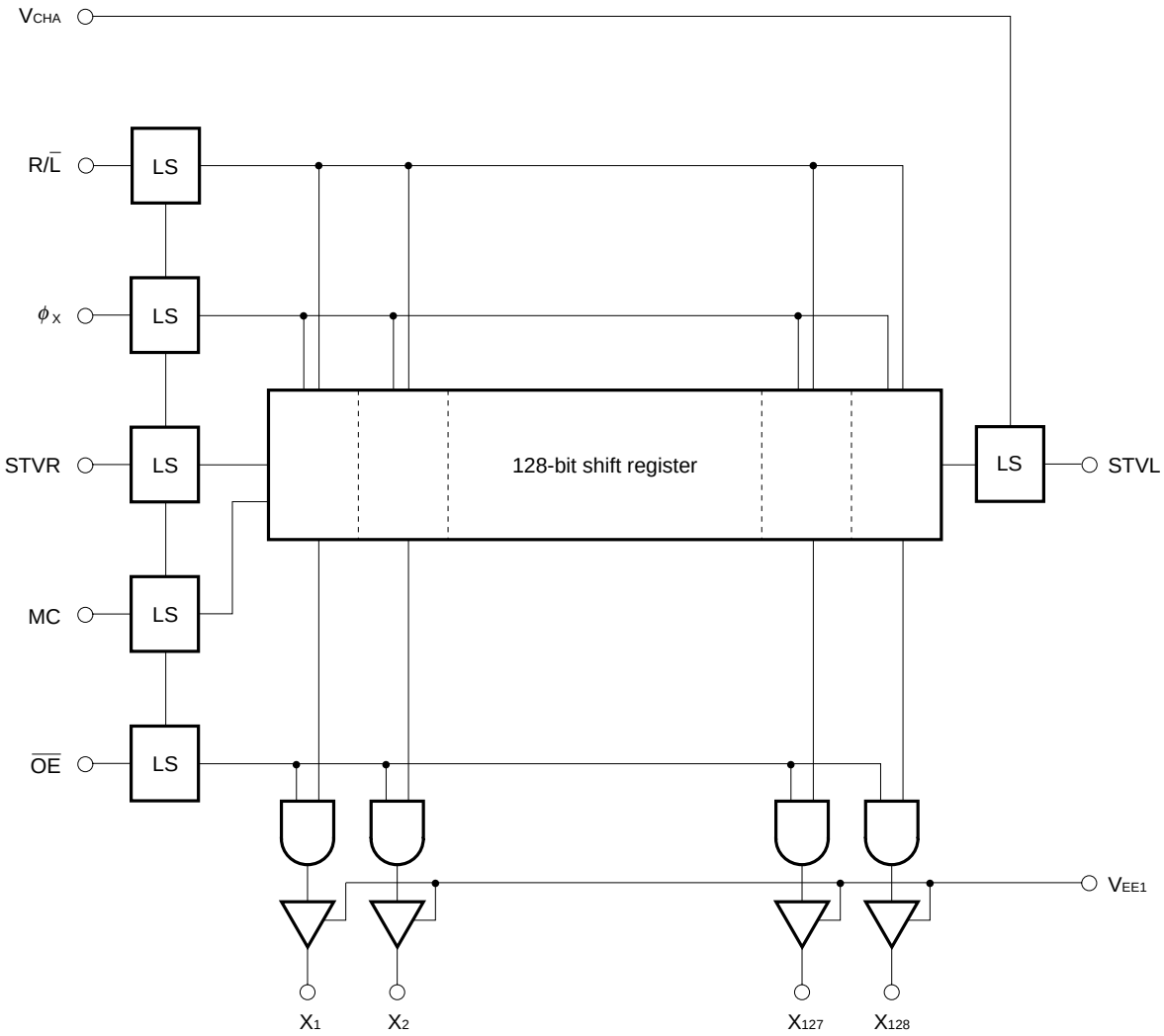
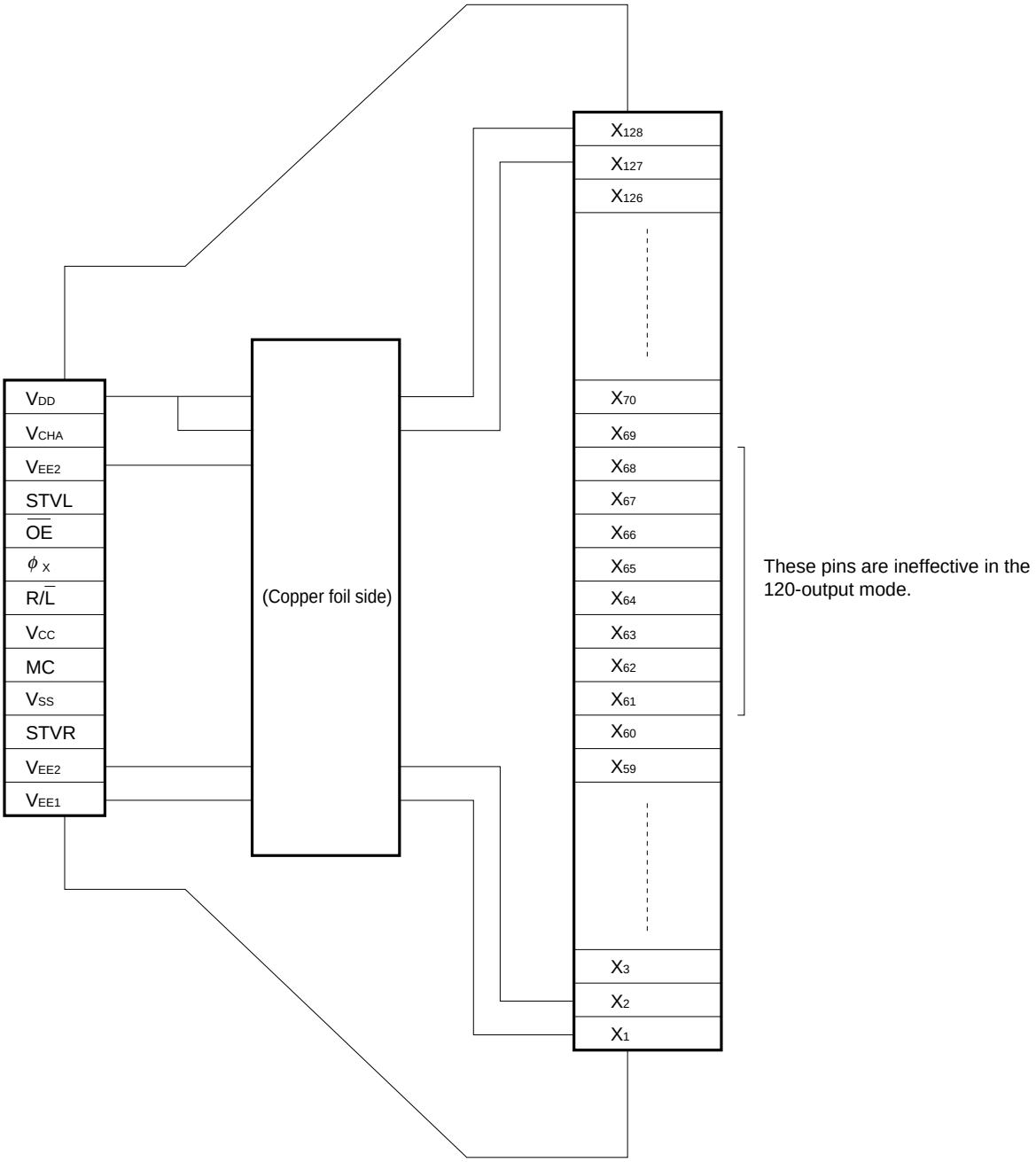
BLOCK DIAGRAM



Remark LS (level shifter): Interfaces the 5 V CMOS level with the V_{DD}-V_{EE2} level.

PIN CONNECTION DIAGRAM (μPD16650N-×××)



Caution The V_{CHA} pin should be connected to the V_{DD} or V_{EE2} pin on the TCP. (This method eliminates the necessity to provide the V_{CHA} input pin on the TCP, resulting in a reduction in the number of required input pins.)

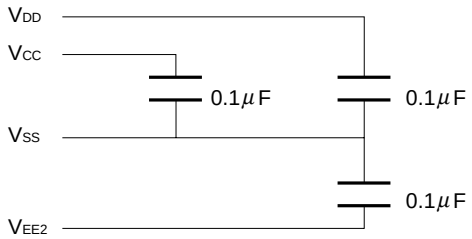
PIN DESCRIPTION

Pin symbol	Pin name	Description of function
X_1 to X_{128}	Driver output	Output scan signals to drive the TFT-LCD gate electrodes. The output changes when the shift clock ϕ_X rises. The amplitude of the driver output is V_{DD} - V_{EE1}. See the timing charts shown later for details of how to switch between the 120-output mode and 128-output mode.
MC	Output count change-over input	Receives a signal that changes the number of outputs. For the 120-output mode, this pin must be supplied with a high level (V_{CC}). For the 128-output mode, it must be supplied with a low level (V_{SS} or V_{EE2}).
V_{CHA}	Logic voltage change-over input	Must be supplied with the V_{EE2} level when the logic supply voltage is 3.3 V, and with the V_{DD} level when the logic supply voltage is 5.0 V.
STVR STVL	Start pulse input/output	Receives an input to the internal shift register. The input data is loaded on the shift register at the positive-going edge of the shift clock ϕ_X. The scan signals are output from X_1 to X_{128}. The input/output level is the CMOS level.
		Outputs a start pulse to the next stage if a cascade connection is used. In the 120-output mode, the start pulse is output at the negative-going edge of the 120th shift clock ϕ_X pulse, and cleared at the negative-going edge of the 121st pulse. In the 128-output mode, the start pulse is output at the negative-going edge of the 128th shift clock ϕ_X pulse, and cleared at the negative-going edge of the 129th pulse.
R/$\overline{L}$	Shift direction change-over input	R/L = high (for shift right): STVR → X_1 → X_{128} → STVL R/L = low (for shift left) : STVL → X_{128} → X_1 → STVR
ϕ_X	Shift clock input	Receives a shift clock pulse for the internal shift register. A shift occurs at the positive-going edge of the shift clock pulse.
$\overline{OE}$	Output enable input	When this pin is at a high level, the driver output is fixed at a low level. The shift register is not cleared, however. The internal logic circuit operates even when the pin is at a high level. The signal supplied to this pin is not synchronized with the clock.
V_{DD}	Driver positive supply voltage	Receives the supply voltage for both the logic circuit and driver.
V_{CC}	Reference voltage	5 ±0.5 V/3.3 ±0.3 V Reference voltage for the LS1 and LS2 level shifters.
V_{SS}	Ground	Must be connected to the system ground.
V_{EE1}	Driver negative supply voltage	V_{EE1} (for the driver)
V_{EE2}	Driver negative supply voltage	V_{EE2} (for the logic circuit)

CAUTIONS FOR USE

1) Power-on sequence
To prevent latch-up disruption, the power must be switched on in the order:
$V_{CC} \rightarrow V_{EE1} \rightarrow V_{EE2} \rightarrow V_{DD} \rightarrow$ Logic input
When witching off, reverse the order. This order must be observed also during transition.

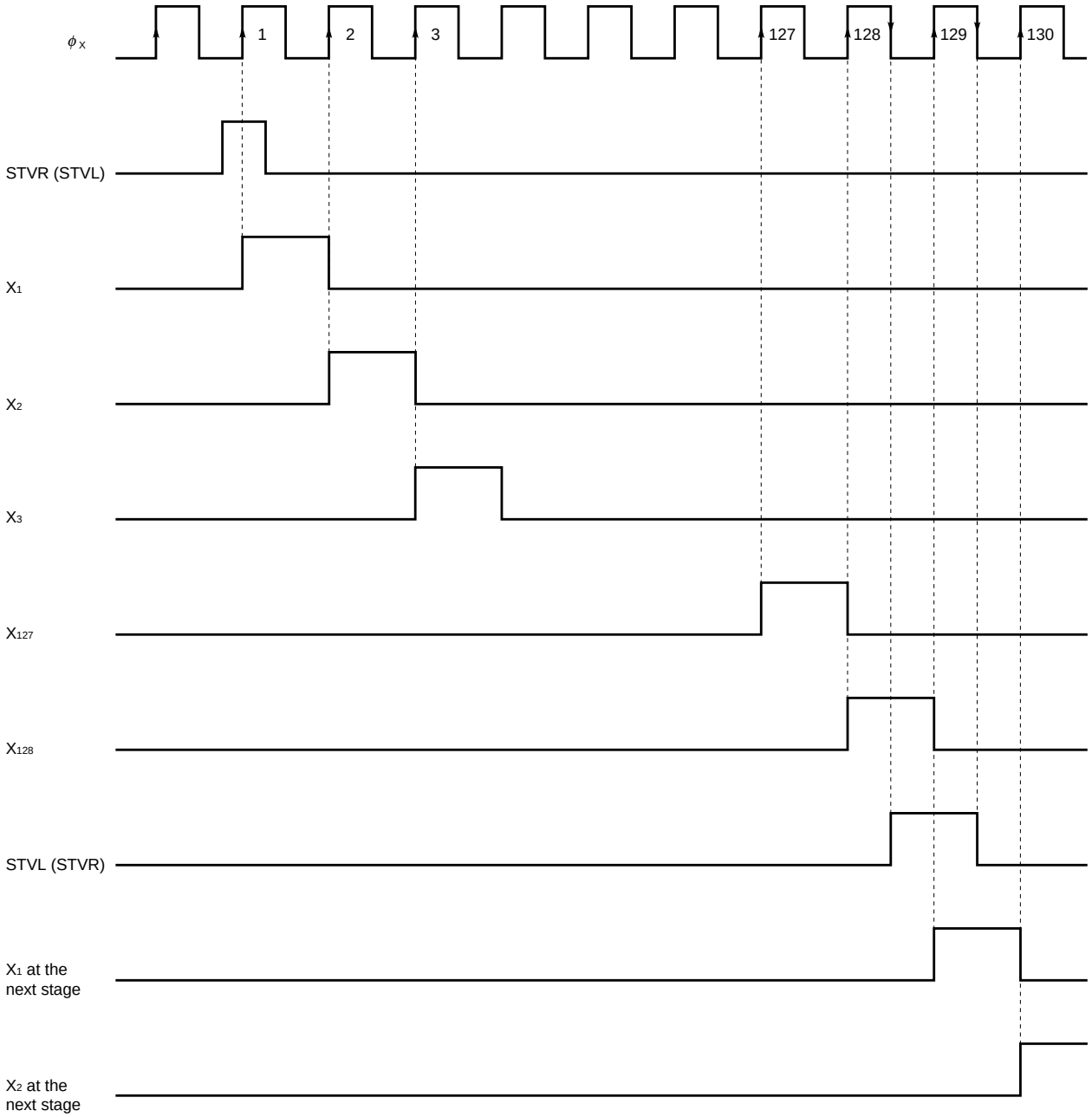
2) Insertion of bypass capacitors
The internal logic circuit operates at a high voltage. To make V_{IH} and V_{IL} immune to noise, use capacitors of 0.1 μF or so between supply voltages as shown below.



3) Negative voltage level shift
If it is necessary to shift the level of a negative supply voltage, shift the V_{EE1} (driver supply voltage) level. The shift should be limited to within: $V_{EE2} \leq V_{EE1} \leq V_{EE2} + 10$ V
Note that shifting the V_{EE1} level results in the ON-state output resistance and output fall time ratings being changed.

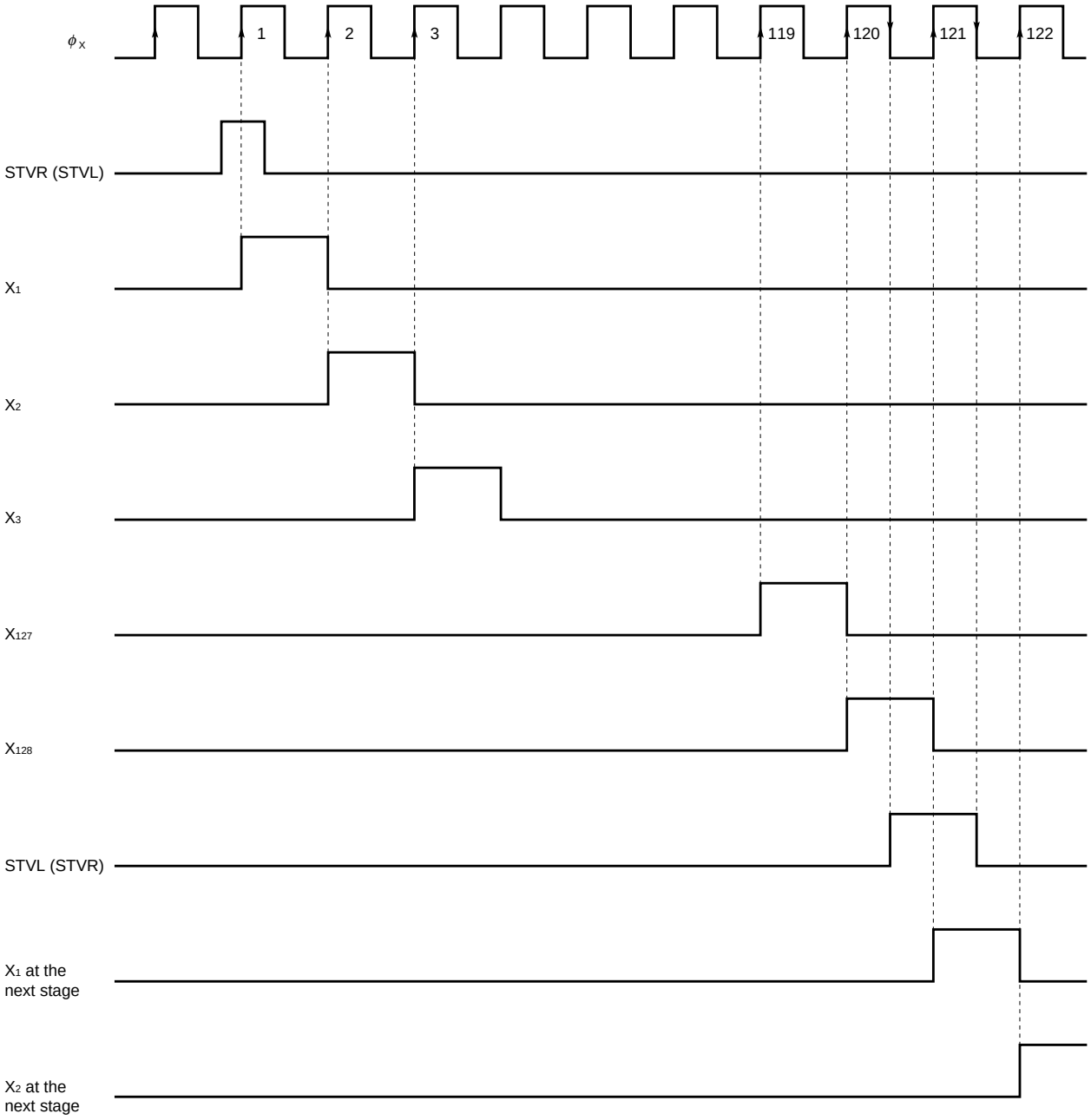
4) Handling the V_{EE1} and V_{EE2} driver negative supply voltage pins
For applications in which a negative supply voltage level is not shifted, connect the V_{EE1} pin (driver supply voltage) to the V_{EE2} pin (logic supply voltage) outside the TCP. Fix all unused input pins to the V_{EE2} level.

TIMING CHART (MC = Vss, 128-OUTPUT MODE, AND R/$\overline{L}$ = Vcc)



Caution Do not change all outputs simultaneously, because such a sequence may result in malfunction.

TIMING CHART (MC = Vcc, 120-OUTPUT MODE, AND R/$\overline{L}$ = Vcc)



Cautions 1. Do not change all outputs simultaneously, because such a sequence may result in malfunction.

2. The output sequence in the 120-output mode is as follows:
STVR (STVL) → X_1 → X_2 ... X_{60} → X_{69} ... X_{127} → X_{128} → STVL (STVR)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Rated value	Unit
Supply voltage	V_{DD}		–0.5 to +28	V
Supply voltage	V_{CC}		–0.5 to +7	V
Supply voltage	V_{DD}-V_{EE1} V_{DD}-V_{EE2}		–0.5 to +42	V
Supply voltage	V_{EE1}, V_{EE2}		–22 to +0.5	V
Input voltage	V_I		V_{EE2} – 0.5 to V_{DD2} + 0.5	V
Input current	I_I		±10	mA
Output current	I_O		±10	mA
Operating temperature range	T_A		–20 to +85	°C
Storage temperature range	$T_{stg.}$		–55 to +125	°C

RECOMMENDED OPERATING RANGES (T_A = –20 °C to +70 °C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		16		25	V
Supply voltage	V_{EE1}		V_{EE2}		V_{EE2} + 10	V
Supply voltage	V_{EE2}		–20		0	V
Supply voltage	V_{DD}-V_{EE1} V_{DD}-V_{EE2}		20		40	V
Supply voltage	V_{CC}	For the 3.3 V logic input	3.0	3.3	3.6	V
Supply voltage	V_{CC}	For the 5.0 V logic input	4.5	5.0	5.5	V

Remark When shifting the level of V_{EE1} (driver supply voltage), satisfy the condition:
$V_{EE2} \leq V_{EE1} \leq V_{EE2}$ + 10 V
Note that shifting the V_{EE1} level results in the ON-state output resistance and output fall time ratings being changed.

ELECTRICAL CHARACTERISTICS
(T_A = –20 °C to +70 °C, V_{DD} = 20 V, V_{EE1} = V_{EE2} = –20 V, V_{CC} = 3.3 ±0.3 V or 5.0 ±0.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	Other than V_{CHA}	0.7V_{CC}		V_{CC}	V
Input low voltage	V_{IL}	Other than V_{CHA}	V_{EE2}		0.3V_{CC}	V
Output high voltage	V_{OH}	STVR(STVL), I_{OH} = –40 μA	V_{CC} – 0.4		V_{CC}	V
Output low voltage	V_{OL}	STVR(STVL), I_{OL} = 40 μA	V_{SS}		V_{SS} + 0.4	V
Output high current	I_{XOH}	X_n, V_X = V_{DD} – 1 V			–1.5	mA
Output low current	I_{XOL}	X_n, V_X = V_{EE1} + 1 V	1.5			mA
ON-state output resistance	R_{ON1}	V_X = V_{EE1} + 1 V or V_{DD} – 1 V			660	Ω
Input leakage current	I_{IL}	V_I = 0 V, 5.0 V, or 3.3 V			±1.0	μA
Dynamic drain current	I_{DD}	V_{DD}, fϕ_X = 31.5 kHz		0.5	1.0	mA
	I_{EE}	$V_{EE1/2}$, fϕ_X = 31.5 kHz		–0.5	–1.0	mA
	I_{CC}	V_{CC}, fϕ_X = 31.5 kHz		50	100	μA

SWITCHING CHARACTERISTICS

(T_A = –20 °C to +70 °C, V_{DD} = 20 V, V_{EE1} = V_{EE2} = –20 V, V_{SS} = 0 V, V_{CC} = 3.3 ±0.3 V or 5.0 ±0.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
STVR and STVL output delay	t_{PHL1}	C_L = 20 pF			600	ns
	t_{PLH1}	CLK → STVR(STVL)			600	ns
Driver output delay	t_{PHL2}	C_L = 220 pF			700	ns
	t_{PLH2}	CLK → X_n			700	ns
	t_{d1}	C_L = 220 pF, $\overline{OE}$: L → H			700	ns
	t_{d2}	C_L = 220 pF, $\overline{OE}$: H → L			700	ns
Output rise time	t_{THL}	C_L = 220 pF			300	ns
Output fall time	t_{TLH}	C_L = 220 pF			300	ns
Input capacitance	C_I	T_A = 25 °C			15	pF
Maximum clock frequency	$f\phi_X$	For cascade connection	100			kHz

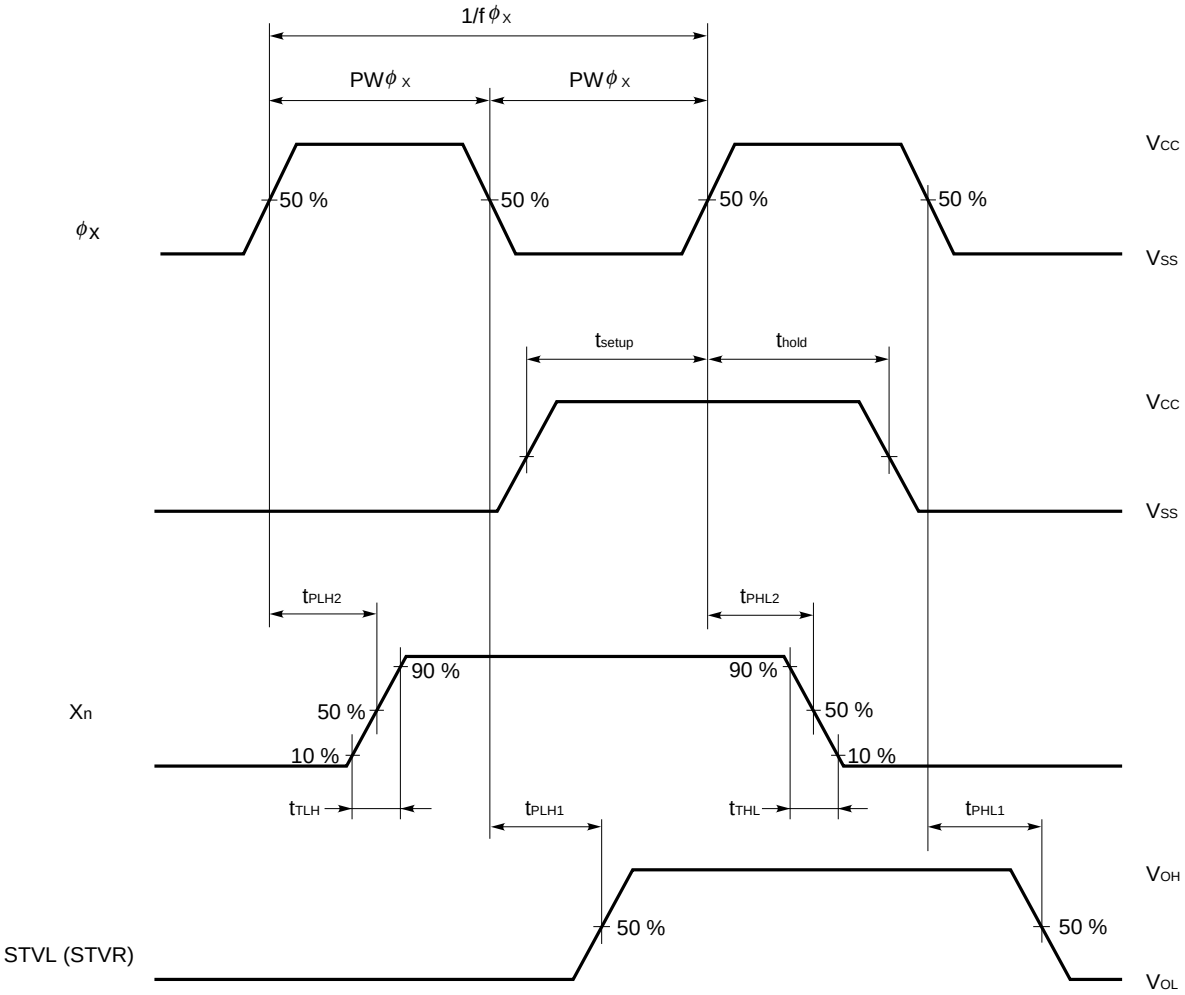
TIMING REQUIREMENTS

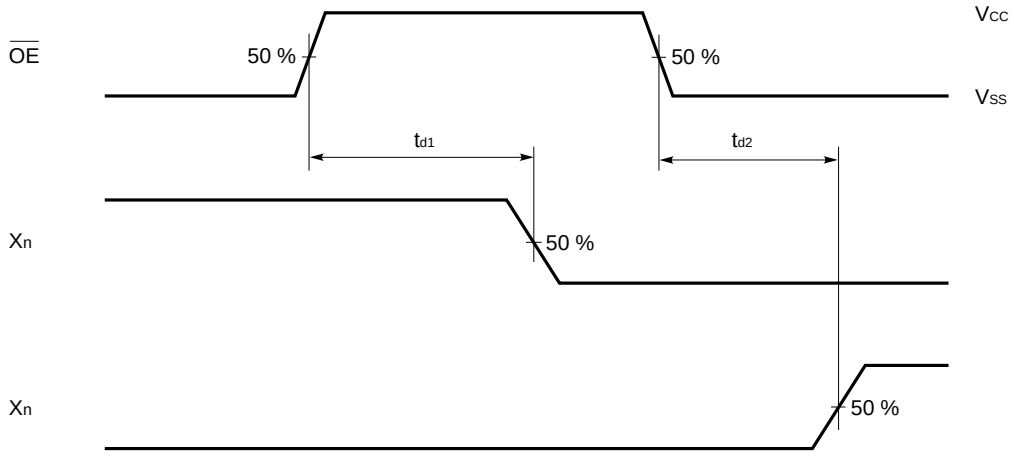
(T_A = –20 °C to +70 °C, V_{DD} = 20 V, V_{EE1} = V_{EE2} = –20 V, V_{SS} = 0 V, V_{CC} = 3.3 ±0.3 V or 5.0 ±0.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse high width	$PW\phi_X(H)$	Duty = 50 %	500			ns
Clock pulse low width	$PW\phi_X(L)$	Duty = 50 %	500			ns
Data setup time	t_{setup}	STVR(STVL) ↑ → CLK ↑	100			ns
Data hold time	t_{hold}	CLK ↑ → STVR(STVL) ↓	100			ns

Remark The logic input rise time (t_r) and fall time (t_f) must be within 20 ns (between 10 % and 90 % of the peak amplitude of the input).

SWITCHING CHARACTERISTIC WAVEFORM (R/$\overline{L}$ = HIGH)





RECOMMENDED MOUNTING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

μPD16650N-×××

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C; heating for 2 to 3 seconds; pressure 100 g (per solder)
	ACF (Sheet-shape bonding agent)	Temporary bonding 70 to 100 °C; pressure 3 to 8 kg/cm^2; time 3 to 5 secs. Real bonding 165 to 180 °C; pressure 25 to 45 kg/cm^2; time 30 to 40 secs. (when using the anisotropic conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

Reference

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)

Quality Grades to NEC's Semiconductor Devices (IEI-1209)

[MEMO]

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