⚡ PERICOM®

6 GHz 1:4 LVPECL Fanout Buffer with Internal Termination

Features

➜ Input Clock Frequency up to 6 GHz Typical

➜ 4 pairs of differential LVPECL outputs

➜ Low additive jitter, < 0.05ps (max)

➜ Input CLK accepts: LVPECL, LVDS, CML, SSTL input level

➜ Output to Output skew: <20ps

➜ Operating Temperature: -40°C to 85°C

➜ Power supply: 3.3V ±10% or 2.5V ±5%

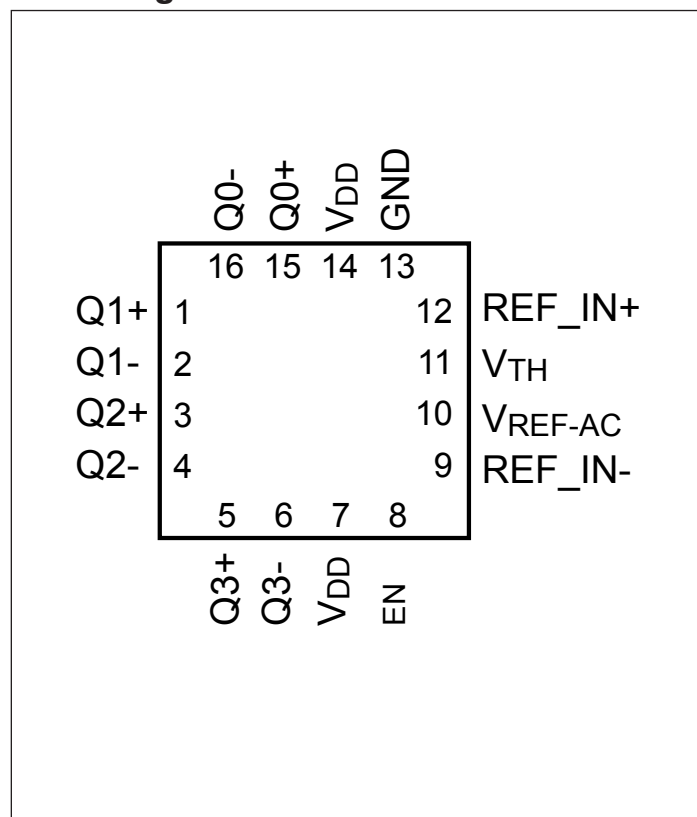➜ Packaging (Pb-free & Green)

➜ 16-pin TQFN available

Description

The PI6C5916004 is a high-performance low-skew 1-to-4 LVPECL fanout buffer. The CLK inputs accept LVPECL, LVDS, CML and SSTL signals. PI6C5916004 is ideal for clock distribution applications such as providing fanout for low noise Pericom oscillators.

Block Diagram
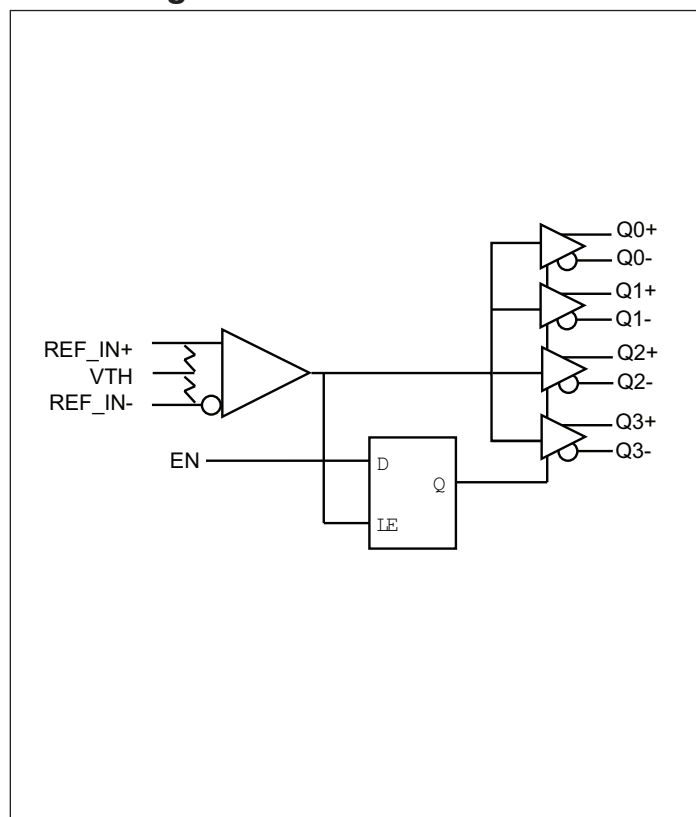
Pin Configuration

Pin Description[1]

Pin #	Name	Type	Description
1, 2	Q1+, Q1-	Output	Differential output pair, LVPECL interface level.
3, 4	Q2+, Q2-	Output	Differential output pair, LVPECL interface level.
5, 6	Q3+, Q3-	Output	Differential output pair, LVPECL interface level.
7	V_{DD}	Power	Core Power Supply
8	EN	Input	Synchronous Output Enable, with internal 25k-ohm pull-up resistor. Logic high selects enable, and logic low selects disable.
9	REF_IN-	Input	Differential IN negative input, AC and DC coupled
10	V_{REF-AC}	Output	Reference Voltage: Biased to VDD-1.4V. Used when AC coupling inputs
11	V_{TH}	Input	Differential pair IN center-tap node. Tie to VREF-AC for AC coupled inputs.
12	REF_IN+	Input	Differential IN positive input, AC and DC coupled
13	GND	Power	Ground
14	V_{DD}	Power	Core Power Supply
15, 16	Q0+, Q0-	Output	Differential output pair, LVPECL interface level.

Functional Description

REF_IN+	REF_IN-	EN	Q+	Q-
0	1	1	0	1
1	0	1	1	0
X	X	0	0	1

Maximum Ratings (Over operating free-air temperature range)

Storage Temperature.. -65°C to+155°C
Ambient Temperature with Power Applied.........-40°C to+85°C
3.3V Analog Supply Voltage .... -0.5 to +4.6V
ESD Protection (HBM) 2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Core Power Supply Voltage		3.0		3.6	V
			2.375		2.625	V
T_A	Ambient Temperature		-40		85	^{o}C
I_{DD}	Core Power Supply Current	No load, max V_{DD}			150	mA
R_{DIFF_IN}	Differential Input Resistance (REF_IN+ to REF_IN-)		90	100	110	Ω
V_{IH}	Input High Voltage		1.2		V_{DD} -0.9	V
V_{IL}	Input Low Voltage		0.4		V_{IH}-0.1	V
V_{IN}	Input Voltage Swing		0.1		1.7	V
V_{DIFF_IN}	Differential Input Swing		0.2			V
V_{REF-AC}	Output Reference Voltage		V_{DD} -1.5	V_{DD} -1.3	V_{DD} -1.15	V

LVCMOS/LVTTL DC Characteristics (TA = -40°C to +85°C, V_{DD} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{IL}	Input Low Voltage		0		0.8	
I_{IH}	Input High Current		-125		20	µA
I_{IL}	Input Low Current		-300			µA

LVPECL DC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, 2.5V ±5%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{DD} = 3.3V ± 10%	V_{DD}-1.4	V_{DD} -1.145	V_{DD}-0.76	V
		V_{DD} = 2.5V ± 5%	V_{DD}- 1.1	V_{DD} -0.95	V_{DD}-0.8	V
V_{OL}	Output Low Voltage	V_{DD} = 3.3V ± 10%	V_{DD}-2.1	V_{DD}-1.945	V_{DD}-1.6	V
		V_{DD} = 2.5V ± 5%	V_{DD}-1.75	V_{DD}-1.6	V_{DD}-1.4	V
V_{OUT}	Output Voltage Swing		550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing		1100	1600		mV

AC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, 2.5V ±5%)

| Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{max}	Output Frequency			6		GHz
t_{pd}	Propagation Delay[1]				500	ps
T_{sk}	Output-to-output Skew[2]				30	ps
	Device to Device skew				200	ps
T_s	Setup time			240		ps
T_h	Hold time			240		ps
t_r/t_f	Output Rise/Fall time	20% - 80%	20		80	ps
t_{odc}	Output duty cycle	f ≤ 2 GHz	48		52	%
		2 GHz ≤ f < 6 GHz	45		55	%
t_j	Buffer additive jitter RMS	156.25MHz with 12KHz to 20MHz integration range		10		fs

Notes:

1. Measured from the differential input to the differential output crossing point

2. Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point
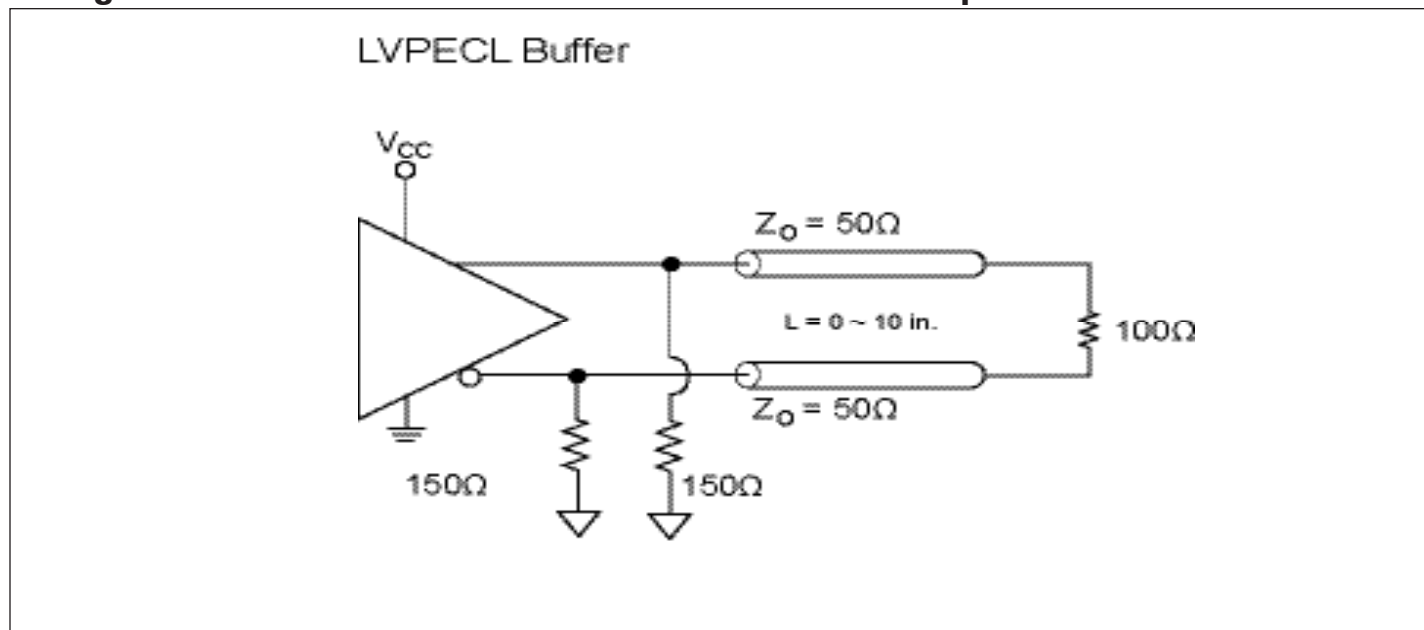
Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	57.7 °C/W
Θ_{JC}	Junction-to-case thermal resistance		32.2 °C/W

Phase Noise Plots
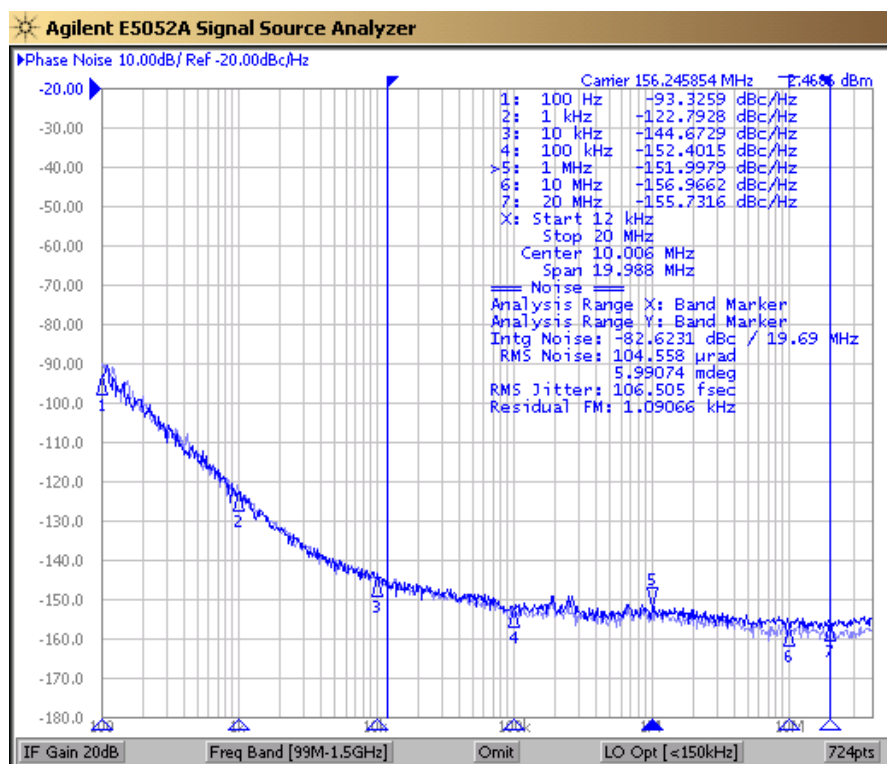
Configuration Test Load Board Termination for LVPECL Outputs

Output Swing vs Frequency

PI6C5916004 Differential Output Swing vs Frequency
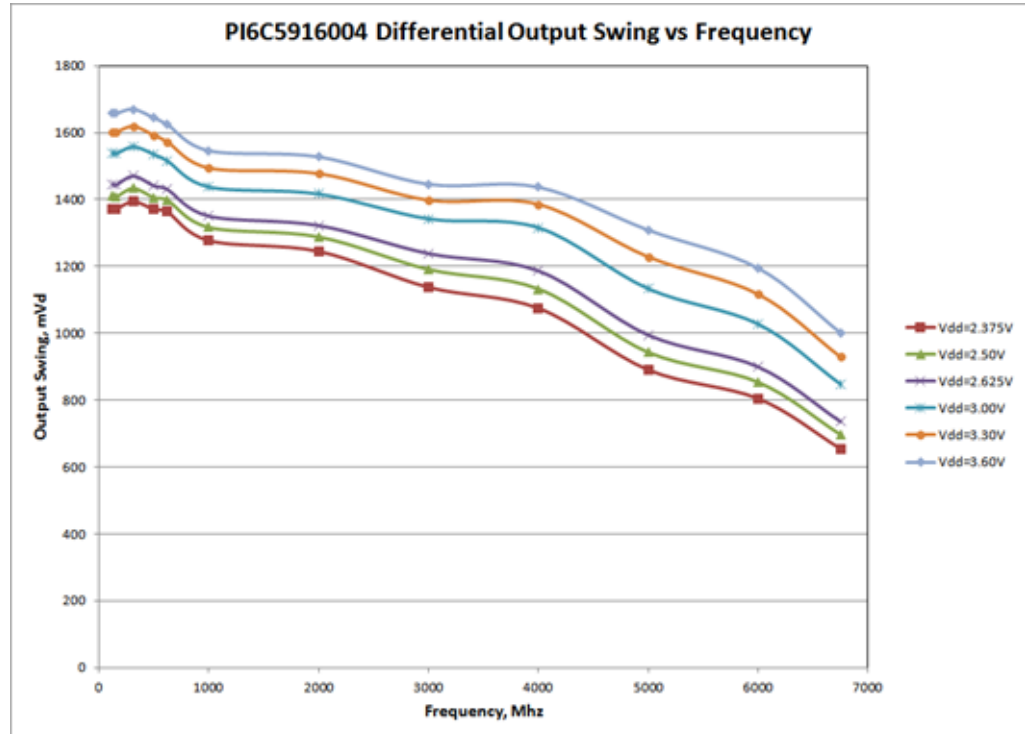
Propagation Delay vs Temperature

PI6C5916004 Propagation Delay versus Temperature
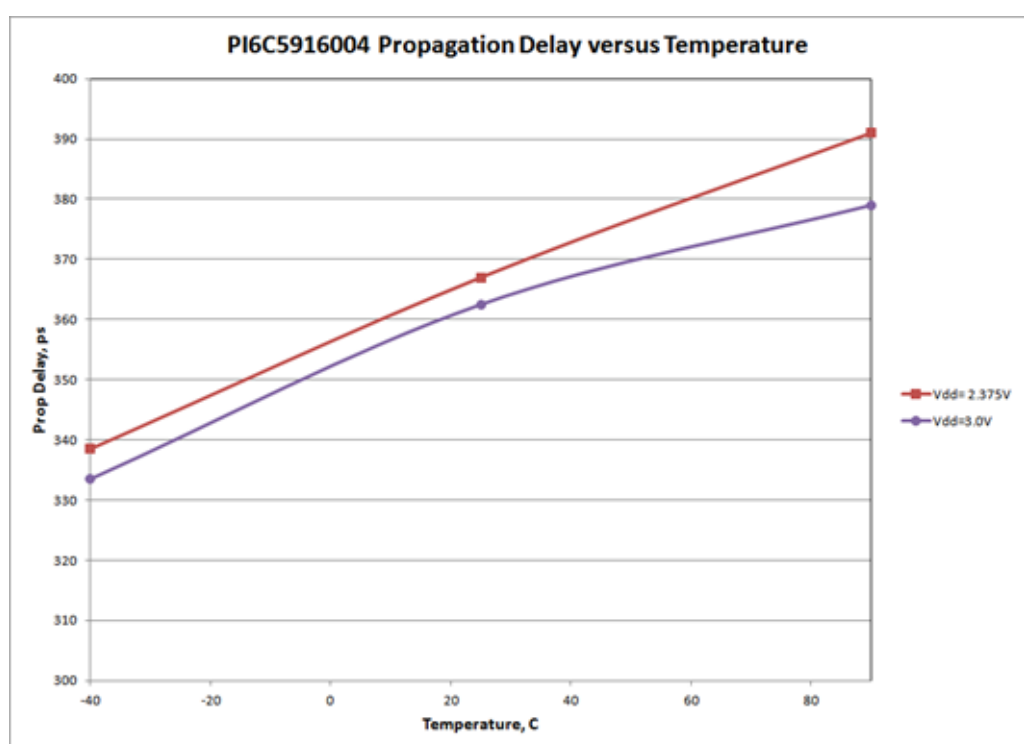
Application information

Suggest for Unused Inputs and Outputs

LVCMOS Input Control Pins

It is suggested to add pull-up=4.7k and pull-down=1k for LVC-MOS pins even though they have internal pull-up/down but with much higher value (>=50k) for higher design reliability.

REF_IN=/ REF_IN- Input Pins

They can be left floating if unused. For added reliability, connect $1k\Omega$ to GND.

Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power supply power.

Power Decoupling & Routing

VDD Pin Decoupling

As general design rule, each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as shown in Fig. 1.
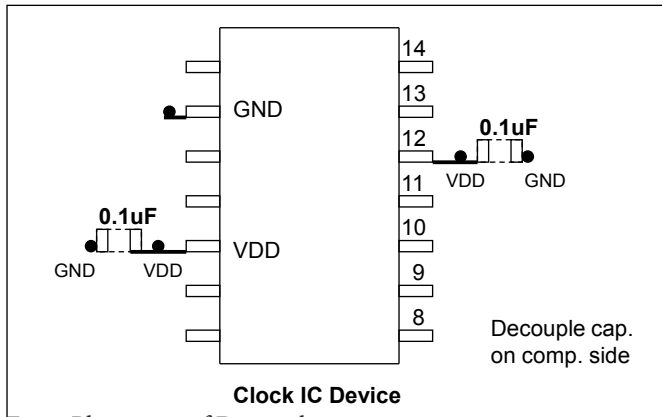

Fig 1: Placement of Decoupling caps

Differential Clock Trace Routing

Always route differential signals symmetrically, make sure there is enough keep-out space to the adjacent trace (>20mil.). In 156.25MHz XO drives IC example, it is better routing differential trace on component side as the following Fig. 2.
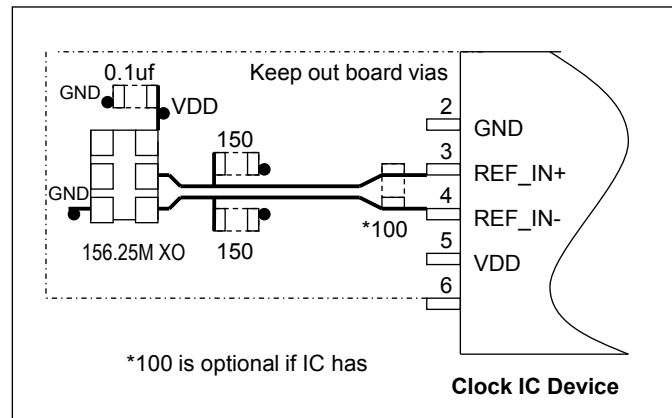

Fig 2: IC routing for XO drive

Clock timing is the most important component in PCB design, so its trace routing must be planned and routed as a first priority in manual routing. Some good practices are to use minimum vias (total trace vias count <4), use independent layers with good reference plane and keep other signal traces away from clock traces (>20mil.) etc.

LVPECL and LVDS Input Interface

LVPECL and LVDS DC Input

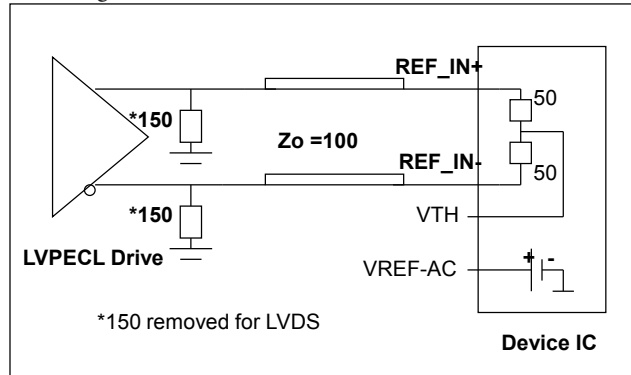LVPECL and LVDS clock input to this IC is connected as shown in the Fig. 3.

Fig 3: LVPECL/ LVDS Input

LVPECL and LVDS AC Input

LVPECL and LVDS AC drive to this clock IC requires the use of the VREF-AC output to recover the DC bias for the IC input as shown in Fig. 4
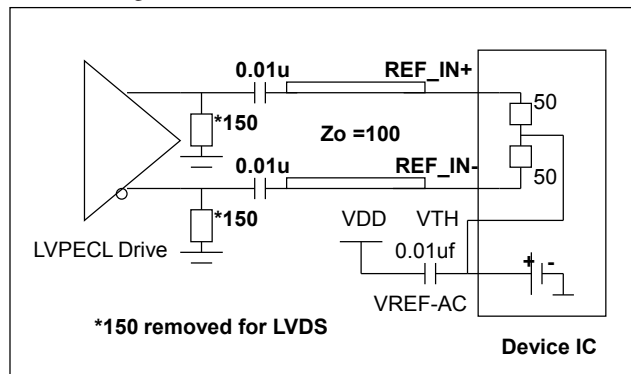

Fig 4: LVPECL/ LVDS AC Coupled Input

CML AC-Coupled Input

CML AC-coupled drive requires a connection to VREF-AC as shown in Fig. 5. The CML DC drive is not recommended as different vendors have different CML DC voltage level. CML is mostly used in AC coupled drive configuration for data and clock signals.
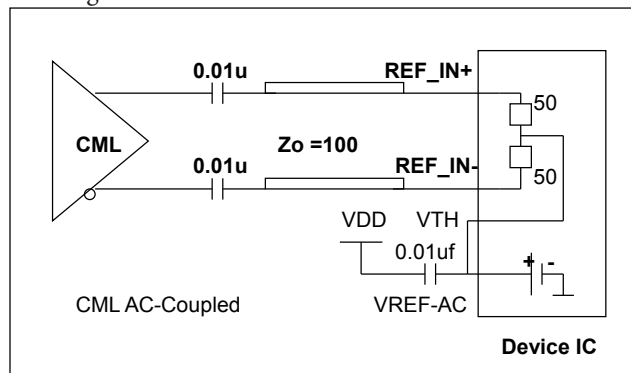

Fig 5: CML AC-Coupled Input Interface

HCSL AC-Coupled Input

It is suggested to use AC coupling to buffer PCIe HCSL 100MHz clock since its V_cm is relatively low at about 0.4V, as shown in Fig. 6.
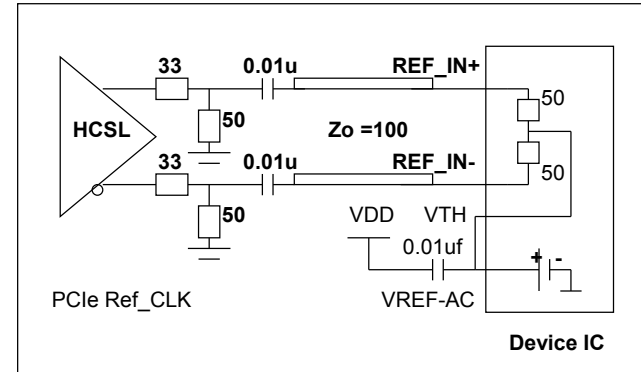

Fig 6: HCSL AC-Coupled Input Interface

CMOS Clock DC Drive Input

LVCMOS clock has voltage Voh levels such as 3.3V, 2.5V, 1.8V. CMOS drive requires a Vcm design at the input: Vcm= ½ (CMOS V) as shown in Fig. 7. Rs =22 ~33ohm typically.

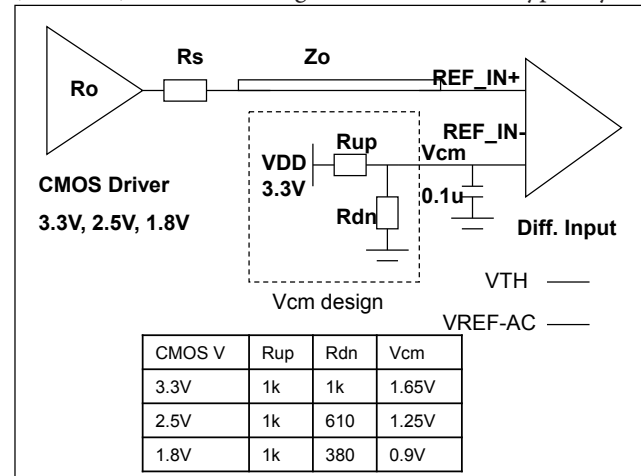| CMOS V	Rup	Rdn	Vcm
3.3V	1k	1k	1.65V
2.5V	1k	610	1.25V
1.8V	1k	380	0.9V

Fig 7: CMOS DC Input Vcm Design

Device LVPECL Output Terminations

LVPECL Output Popular Termination

The most popular LVPECL termination is 150ohm pull-down bias and 100ohm across at RX side. Please consult ASIC data-sheet if it already has 100ohm or equivalent internal termination. If so, do not connect external 100ohm across as shown in Fig. 8. This popular termination's advantage is that it does not allow any bias through from V_{DD}. This prevents V_{DD} system noise coupling onto clock trace.
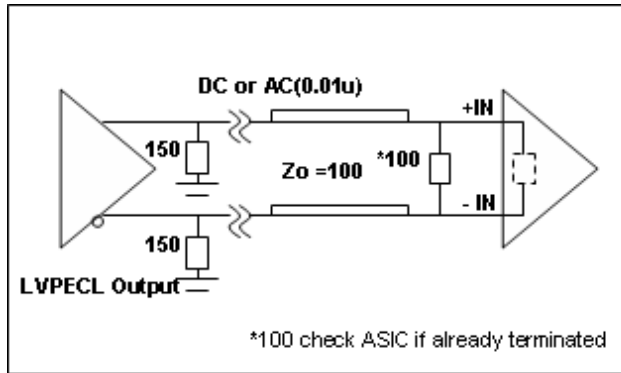
Fig. 8 LVPECL Output Popular Termination

LVPECL Output Thevenin Termination

Fig. 9 shows LVPECL output Thevenin termination which is used for shorter trace drive (<5in.), but it takes V_{DD} bias current and V_{DD} noise can get onto clock trace. It also requires more component count. So it is seldom used today.
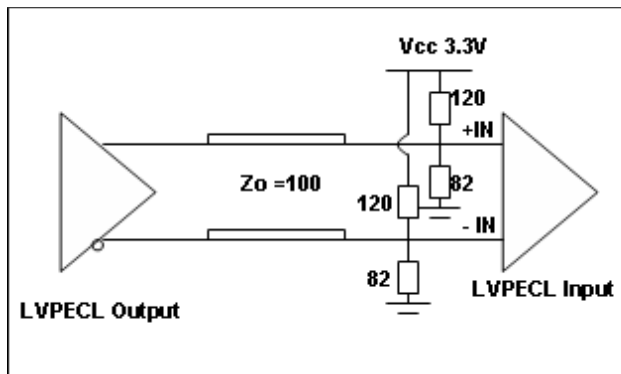
Fig. 9 LVPECL Thevenin Output Termination

LVPECL Output AC Thevenin Termination

LVPECL AC Thevenin terminations require a 150ohm pull-down before the AC coupling capacitor at the source as shown in Fig. 10. Note that pull-up/down resistor value is swapped compared to Fig. 9. This circuit is good for short trace (<5in.) application only.

Fig. 10 LVPECL Output AC Thenvenin Termination
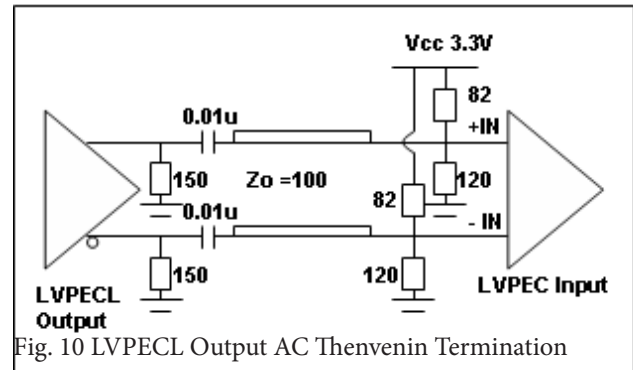
LVPECL Output Drive HCSL Input

Using the LVPECL output to drive a HCSL input can be done using a typical LVPECL AC Thenvenin termination scheme. Use pull-up/down 450/60ohm to generate Vcm=0.4V for the HCSL input clock. This termination is equivalent to 50Ohm load as shown in Fig. 11.

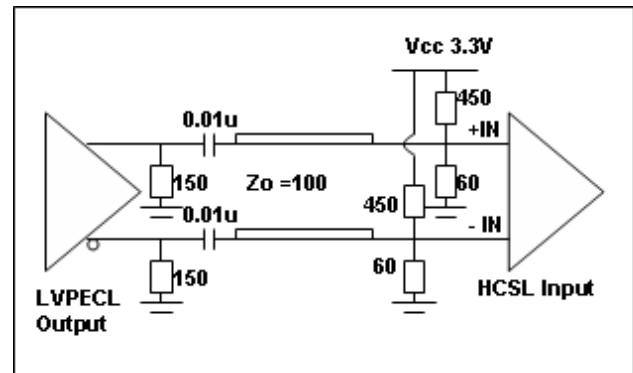Fig. 11 LVPECL Output Drive HCSL Termination

LVPECL Output V_swing Adjustment

It is suggested to add another cross 100ohm at TX side to tune the LVPECL output V_swing without changing the optimal 150ohm pull-down bias in Fig. 12. This form of double termination can reduce the V_swing in ½ of the original at the RX side. By fine tuning the 100ohm resistor at the TX side with larger values like 150 to 200ohm, one can increase the V_swing by > 1/2 ratio.
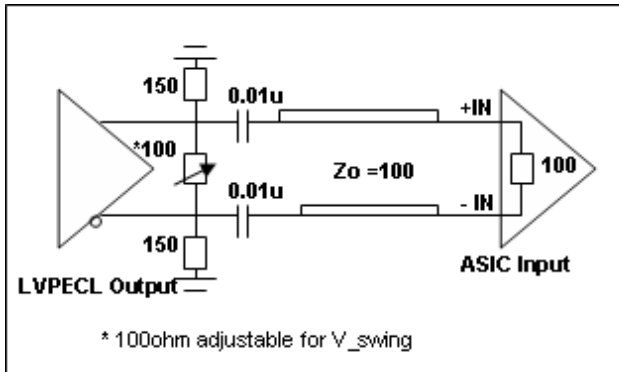

Fig. 12 LVPECL Output V_swing Adjustment

Clock Jitter Definitions

Total jitter= RJ + DJ

Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter: , where is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

Phase Jitter

Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz@10kHz which is phase noise power in 1-Hz normalized bandwidth vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter <=1ps at 12k to 20MHz offset band as SONET standard specification.

PCIe Ref_CLK Jitter

PCIe reference clock jitter specification requires testing via the PCI-SIG jitter tool, which is regulated by US PCI-SIG organization. The jitter tool has PCIe Serdes embedded filter to calculate the equivalent jitter that relates to data link eye closure. Direct peak-peak jitter or phase jitter test data, normally is higher than jitter measure using PCI-SIG jitter tool. It has high-frequency jitter and low-frequency jitter spec. limit. For more information, please refer to the PCI-SIG website: http://www.pcisig.com/specifications/pciexpress/

Device Thermal Calculation

Fig. 13 shows the JEDEC thermal model in a 4-layer PCB.
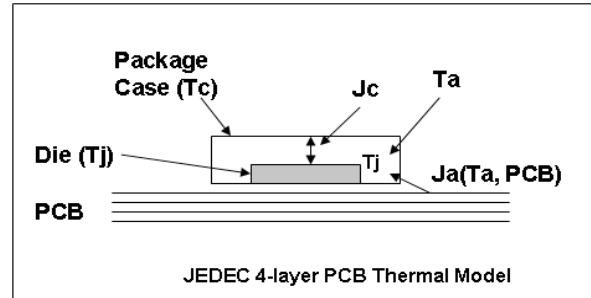

Fig. 13 JEDEC IC Thermal Model

Important factors to influence device operating temperature are:

1) The power dissipation from the chip (P_chip) is after subtracting power dissipation from external loads. Generally it can be the no-load device Idd

2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker has better heat dissipation

3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature Tj

The individual device thermal calculation formula:

Tj =Ta + Pchip x Ja

Tc = Tj - Pchip x Jc

Ja ____ Package thermal resistance from die to the ambient air in C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce Ja (still air) by 20~30%

Jc ____ Package thermal resistance from die to the package case in C/W unit

Tj ____ Die junction temperature in C (industry limit <125C max.)

Ta ____ Ambiant air température in C

Tc ____ Package case temperature in C

Pchip____ IC actually consumes power through Iee/GND current

Thermal calculation example

To calculate Tj and Tc of PI6CV304 in an SOIC-8 package:

Step 1: Go to Pericom web to find Ja=157 C/W, Jc=42 C/W

http://www.pericom.com/support/packaging/packaging-me-chanicals-and-thermal-characteristics/

Step 2: Go to device datasheet to find Idd=40mA max.

I_{DD}	Supply Current	$C_L = 33pF/33MHz$		20	mA
		$C_L = 33pF/66MHz$		40	
		$C_L = 22pF/80MHz$		35	
		$C_L = 15pF/100MHz$		32	
		$C_L = 10pF/125MHz$		28	
		$C_L = 10pF/155MHz$		41	

Step 3: P_total= 3.3Vx40mA=0.132W

Step 4: If Ta=85C

      Tj= 85 + Ja xP_total= 85+25.9 = 105.7C

      Tc= Tj + Jc xP_total= 105.7- 5.54 = 100.1C

Note:

The above calculation is directly using Idd current without sub-tracting the load power, so it is a conservative estimation. For more precise thermal calculation, use P_unload or P_chip from device Iee or GND current to calculate Tj, especially for LVPECL buffer ICs that have a 150ohm pull-down and equivalent 100ohm differential RX load.

Packaging Mechanical: 16-pin TQFN (ZH)

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220

DATE: 12/07/11

DESCRIPTION: 16-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH16)

DOCUMENT CONTROL #: PD-2047

REVISION: C
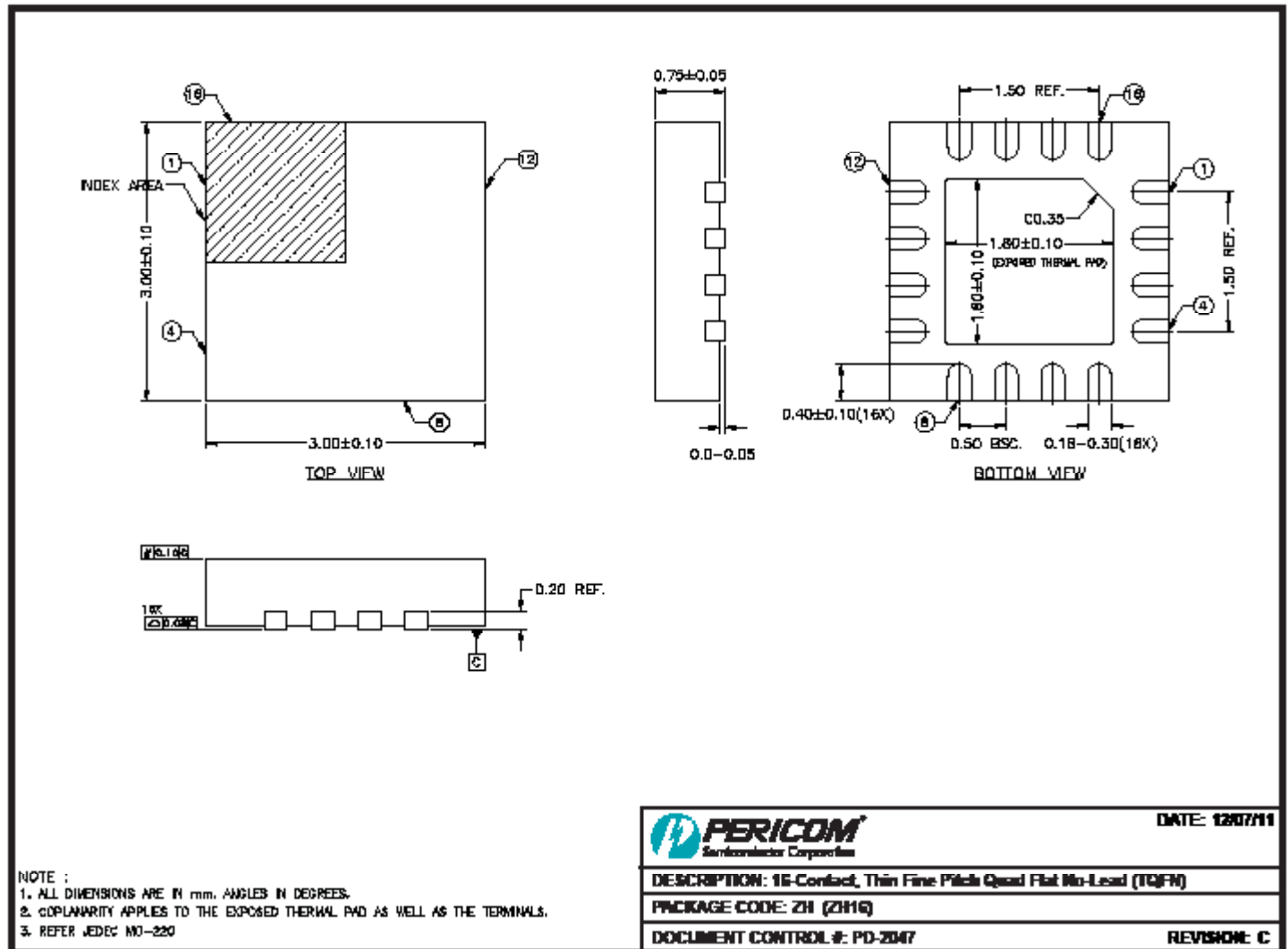
Ordering Information[1,2,3]

Ordering Code	Package Code	Package Description
PI6C5916004ZHIE	ZH	Pb-free & Green, 16-pin QFN

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

2. E = Pb-free & Green

3. X suffix = Tape/Reel