Power MOSFET 95 Amps, 24 Volts

N-Channel DPAK

Features

- High Power and Current Handling Capability
- Fast Switching Performance
- Low R_{DS(on)} to Minimize Conduction Loss
- Low Gate Charge to Minimize Switching Losses
- Pb-Free Packages are Available

Applications

- CPU Motherboard Vcore Applications
- High Frequency DC–DC Converters
- Motor Drives
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	24	V
Gate-to-Source Voltage	V_{GS}	±20	V
Thermal Resistance, Junction-to-Case Total Power Dissipation @ T _A = 25°C Drain Current -	R _{θJC} P _D	1.45 86	°C/W W
 Continuous @ T_A= 25°C, Limited by Package Continuous @ T_A= 25°C, Limited by Wires 	I _D I _D	95 32	A A
Thermal Resistance, Junction–to– Ambient (Note 1)	$R_{\theta JA}$	52	°C/W
- Total Power Dissipation @ T _A = 25°C - Drain Current - Continuous @ T _A = 25°C	P _D I _D	2.4 15.8	W A
Thermal Resistance, Junction–to–Ambient (Note 2)	$R_{\theta JA}$	100	°C/W
- Total Power Dissipation @ T _A = 25°C - Drain Current - Continuous @ T _A = 25°C	P _D I _D	1.25 12	W A
Operating Junction and Storage Temperature	T _J , T _{STG}	–55 to 150	°C
Continuous Source Current (Body Diode)	I _S	45	Α
Single Pulse Drain-to-Source Avalanche Energy – (V_{DD} = 25 V, V_{G} = 10, I_{PK} = 13 A, L = 1 mH, R_{G} = 25 Ω)	E _{AS}	84	mJ
Lead Temperature for Soldering Purposes (1/8 in from case for 10 seconds)	TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq

- [1 oz] including traces).
- 2. Surface mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq).

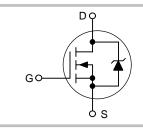


ON Semiconductor®

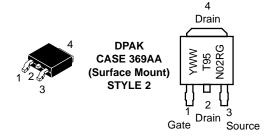
http://onsemi.com

V _{(BR)DSS}	R _{DS(ON)} TYP	I _D MAX*
24 V	4.5 mΩ @ 10 V	95 A
24 V	5.9 mΩ @ 4.5 V	95 A

*ID MAX in the product summary table is continuous and steady at 25°C.

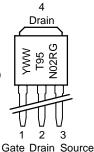


MARKING DIAGRAMS & PIN ASSIGNMENTS





DPAK CASE 369D (Straight Lead) STYLE 2



= Year WW = Work Week T95N02R = Device Code = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.45	°C/W
Junction-to-Ambient - Steady State (Note 3)	$R_{ heta JA}$	52	
Junction-to-Ambient - Steady State (Note 4)	$R_{\theta JA}$	100	

^{3.} Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
4. Surface mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•				•	•	•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		24	29		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T				15		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 20 V	$T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$			1.5 10	μΑ
Gate-to-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} =				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 2$	250 μΑ	1.0		2.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.0		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D =$: 10 A		5.9	8.0	mΩ
		V _{GS} = 10 V, I _D =	20 A		4.5	5.0	1
Forward Transconductance	gFS	$V_{GS} = 10 \text{ V}, I_{D} =$	10 A		30		S
CHARGES, CAPACITANCES AND GATE	RESISTANCE						
Input Capacitance	C _{ISS}				2400		pF
Output Capacitance	C _{OSS}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz, } V_{DS} = 20 \text{ V}$			1020		
Reverse Transfer Capacitance	C _{RSS}				390		1
Total Gate Charge	Q _T				21		nC
	Q_{GS} $V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}; I_D = 10 \text{ A}$		V; I _D = 10 A		4.4		
	Q_{GD}				9.1		
SWITCHING CHARACTERISTICS							
Turn-on Delay Time	t _{d(on)}				10		ns
Rise Time	t _r	$V_{GS} = 10 \text{ V}, V_{DD} = 10 \text{ V},$ $I_{D} = 30 \text{ A}, R_{G} = 3 \Omega$			82		
Turn-off Time	t _{d(off)}				26		
Fall Time	t _f				70		
DRAIN-SOURCE DIODE CHARACTERIS	STICS						
Forward Diode Voltage	V_{SD}	$V_{GS} = 0 \text{ V}, I_{S} = 20 \text{ A}$	$T_J = 25^{\circ}C$		0.83	1.2	V
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } d_{ISD}/dt = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 20 \text{ A}$			45		ns
Charge Time	Ta				20		
Discharge Time	T _b				30]

^{5.} Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

TYPICAL CHARACTERISTICS

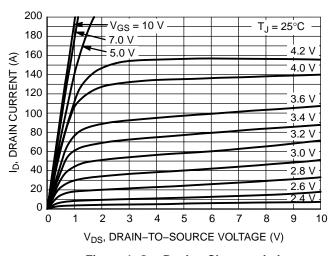


Figure 1. On-Region Characteristics

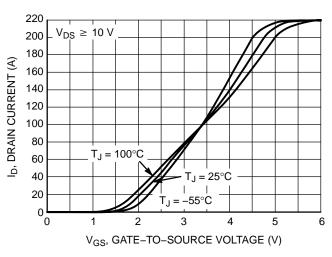


Figure 2. Transfer Characteristics

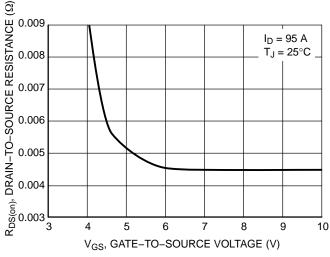


Figure 3. On–Resistance versus Gate–to–Source Voltage

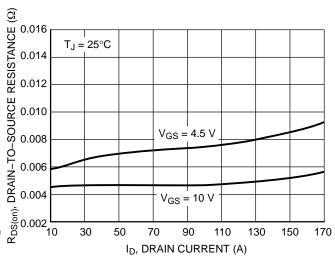


Figure 4. On-Resistance versus Drain Current and Gate Voltage

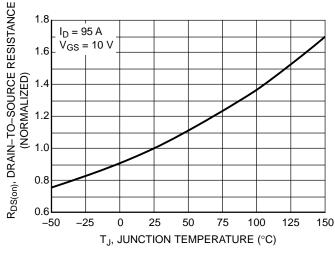


Figure 5. On–Resistance Variation with Temperature

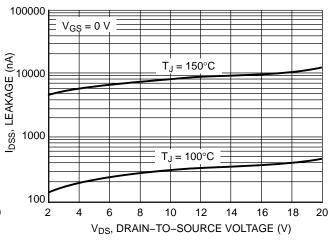


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL CHARACTERISTICS

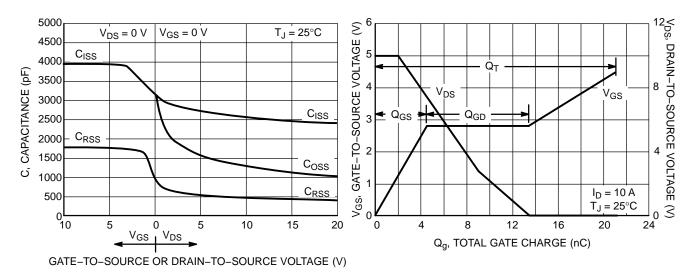


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

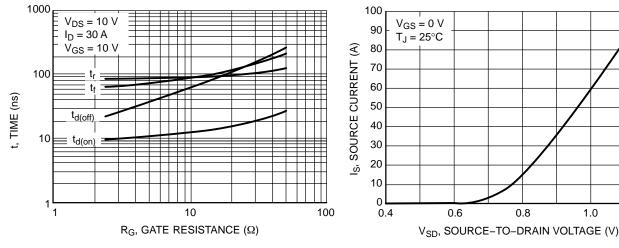


Figure 9. Resistive Switching Time Variation versus Gate Resistance

Figure 10. Diode Forward Voltage versus

Current

1.2

ORDERING INFORMATION

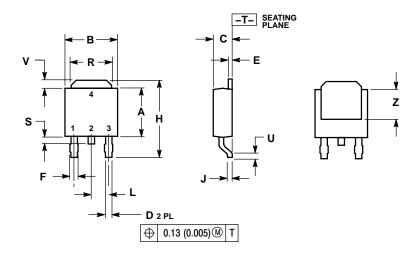
Device	Package	Shipping [†]
NTD95N02R	DPAK	75 Units / Rail
NTD95N02RG	DPAK (Pb-Free)	75 Units / Rail
NTD95N02R-001	DPAK	75 Units / Rail
NTD95N02R-001G	DPAK (Pb-Free)	75 Units / Rail
NTD95N02RT4	DPAK	2500 Units / Tape & Reel
NTD95N02RT4G	DPAK (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE)

CASE 369AA-01 ISSUE A

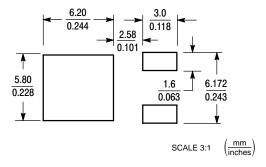


- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.22
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
Н	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090	BSC	2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020		0.51	
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

SOLDERING FOOTPRINT*

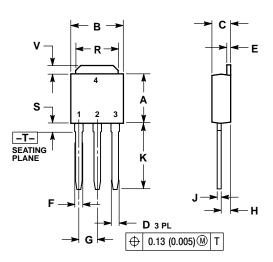


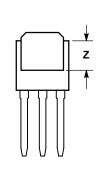
^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK

CASE 369D-01 ISSUE B





NOTES:

- DIMENSIONING AND TOLERANCING PER
 ANSI V14 5M 1982
- ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETER	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	0.090 BSC 2.29 BS0		BSC
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

STYLE 2:

- PIN 1. GATE
 - 2. DRAIN
 - 3. SOURCE
 - 4. DRAIN

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