MIC4607

85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection

General Description

The MIC4607 is an 85V, three-phase MOSFET driver. The MIC4607 features a fast (35ns) propagation delay time and 20ns driver rise/fall times for a 1nF capacitive load. TTL inputs can be separate high- and low-side signals or a single PWM input with high and low drive generated internally. High- and low-side outputs are guaranteed to not overlap in either mode. The MIC4607 includes overcurrent protection as well as a high-voltage internal diode that charges the high-side gate drive bootstrap capacitor.

A robust, high-speed, and low-power level shifter provides clean level transitions to the high-side output. The robust operation of the MIC4607 ensures that the outputs are not affected by supply glitches, HS ringing below ground, or HS slewing with high-speed voltage transitions. Undervoltage protection is provided on both the low-side and high-side drivers.

The MIC4607 is available in a both a 28-pin 4mm × 5mm QFN and 28-pin TSSOP package with an operating junction temperature range of –40°C to +125°C.

Datasheets and support documentation are available on Micrel's website at: www.micrel.com.

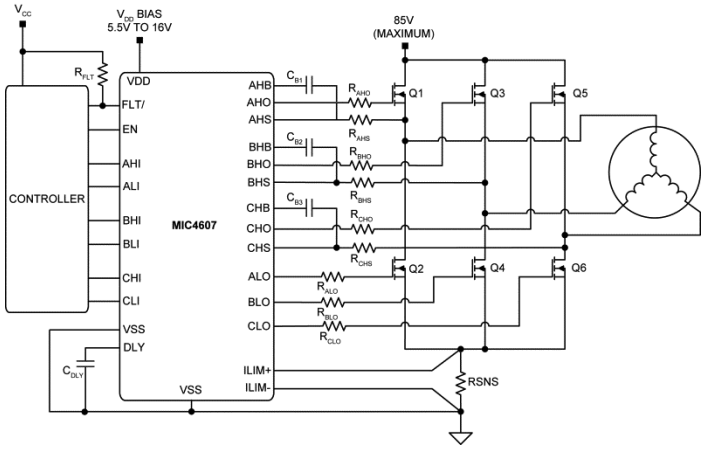
Features

- Gate drive supply voltage up to 16V
- Overcurrent protection
- Drives high-side and low-side N-Channel MOSFETs with independent inputs or with a single PWM signal
- TTL input thresholds
- On-chip bootstrap diodes
- Fast 35ns propagation times
- Shoot-through protection
- Drives 1000pF load with 20ns rise and fall times
- Low power consumption
- Supply undervoltage protection
- –40°C to +125°C junction temperature range

Applications

- Three-phase and BLDC motor drives
- Three-phase inverters

Typical Application

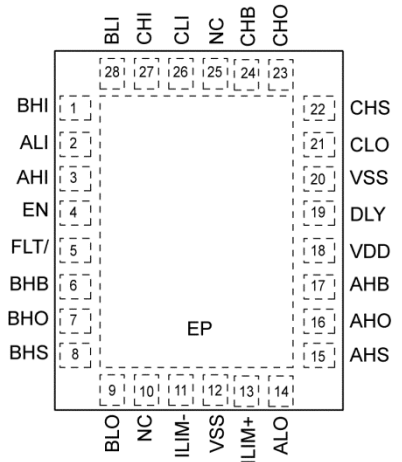


Three-Phase Motor Driver

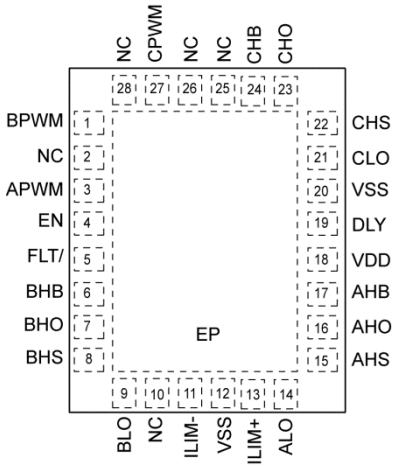
Ordering Information

Part Number	Input	Version	Junction Temperature Range	Package
MIC4607-1YML	TTL	Dual Inputs	–40°C to +125°C	28-Pin 4mm × 5mm QFN
MIC4607-2YML	TTL	Single PWM Input	–40°C to +125°C	28-Pin 4mm × 5mm QFN
MIC4607-1YTS	TTL	Dual Inputs	–40°C to +125°C	28-Pin TSSOP
MIC4607-2YTS	TTL	Single PWM Input	–40°C to +125°C	28-Pin TSSOP

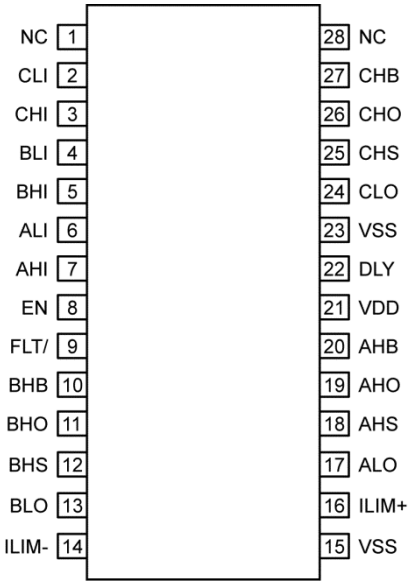
Pin Configurations



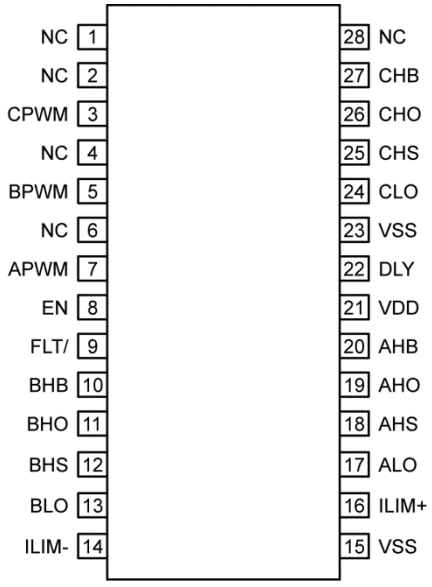
MIC4607-1
28-Pin 4mm × 5mm (ML)
(Top View)



MIC4607-2
28-Pin 4mm × 5mm (ML)
(Top View)



MIC4607-1
28-Pin TSSOP (TS)
(Top View)



MIC4607-2
28-Pin TSSOP (TS)
(Top View)

Pin Description

Pin Number QFN	Pin Number TSSOP	Pin Name		Pin Function
		"-1"	"-2"	
1	5	BHI	BPWM	High-side input (-1) or PWM input (-2) for Phase B.
2	6	ALI	NC	Low-side input (-1) or no connect (-2) for Phase A.
3	7	AHI	APWM	High-side input (-1) or PWM input (-2) for Phase A.
4	8	EN		Active high enable input. High input enables all outputs and initiates normal operation. Low input shuts down device into a low LQ mode.
5	9	FLT/		Open Drain. FLT/ pin goes low when outputs are latched off due to an overcurrent event. Must be pulled-up to an external voltage with a resistor.
6	10	BHB		Phase B High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and BHS. An on-board bootstrap diode is connected from VDD to BHB.
7	11	BHO		Phase B High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
8	12	BHS		Phase B High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the *Applications* section for additional information on the resistor.
9	13	BLO		Phase B Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
10	---	NC		No Connect.
11	14	ILIM-		Differential Current-Limit Input. Connect to most negative end of the external current-sense resistor.
12	15	VSS		Power Ground for Phase A and Phase B.
13	16	ILIM+		Differential Current-Limit Input. Connect to most positive end of the external current-sense resistor.
14	17	ALO		Phase A Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
15	18	AHS		Phase C High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the *Applications* section for additional information on the resistor.
16	19	AHO		Phase A High Side Drive Output. Connect to the gate of the external high-side power MOSFET.
17	20	AHB		Phase A High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and AHS. An on-board bootstrap diode is connected from VDD to AHB.
18	21	VDD		Input Supply for Gate Drivers and Internal Logic/Control Circuitry. Decouple this pin to VSS with a minimum 2.2µF ceramic capacitor.
19	22	DLY		Fault Delay. Connect an external capacitor from this pin to ground to increase the current-limit reset delay. Leave open for minimum delay. Do not externally drive this pin.
20	23	VSS		Phase C Power and Control Circuitry Ground.
21	24	CLO		Phase C Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.

Pin Description (Continued)

Pin Number QFN	Pin Number TSSOP	Pin Name		Pin Function
		"-1"	"-2"	
22	25	CHS		Phase C High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the *Applications* section for additional information on the resistor.
23	26	CHO		Phase C High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
24	27	CHB		Phase C High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and CHS. An on-board bootstrap diode is connected from VDD to CHB.
25	28	NC		No Connect.
---	1	NC		No Connect.
26	2	CLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase C.
27	3	CHI	CPWM	High-Side Input (-1) or PWM Input (-2) for Phase C.
28	4	BLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase B.
EP		ePad		Exposed Heatsink Pad: Connect to GND for best thermal performance.

Absolute Maximum Ratings[1, 2]

Supply Voltage (V_{DD}, V_{xHB} – V_{xHS}) ..... –0.3V to 18V
Input Voltages (V_{xLI}, V_{xHI}, V_{xPWM}, V_{EN})..... –0.3V to V_{DD} + 0.3V
FLT/ Pin..... –0.3V to V_{DD} + 0.3V
DLY Pin ..... –0.3V to 18V
Voltage on xLO (V_{xLO}) ..... –0.3V to V_{DD} + 0.3V
Voltage on xHO (V_{xHO}) .....V_{HS} – 0.3V to V_{HB} + 0.3V
Voltage on xHS (Continuous)..... –1V to 90V
Voltage on xHB 108V
ILIM+ ..... –0.3V to +5V
ILIM– ..... –0.3V to +2V
Average Current in VDD to HB Diode.....100mA
Lead Temperature (soldering, 10s).....260°C
Storage Temperature (T_S) .....–60°C to +150°C
ESD Rating[4]
HBM.....1kV
MM.....200V
CDM.....200V

Operating Ratings[2, 3]

Supply Voltage (V_{DD}) [decreasing V_{DD}] ..... 5.25V to 16V
Supply Voltage (V_{DD}) [increasing V_{DD}] ..... 5.5V to 16V
Voltage on xHS ..... –1V to 85V
Voltage on xHS (repetitive transient <100ns) .... –5V to 90V
HS Slew Rate.....50V/ns
Voltage on xHB .....V_{HS} + 5.5V to V_{HS} + 16V
and/or.....V_{DD} – 1V to V_{DD} + 85V
Ambient Temperature (T_A) .....–40°C to +125°C
Junction Temperature (T_J) .....–40°C to +125°C
Junction Thermal Resistance
4mm × 5mm QFN-28L (θ_{JA}).....43°C/W
4mm × 5mm QFN-28L (θ_{JC}).....3.4°C/W
TSSOP-28L (θ_{JA}) .....70°C/W
TSSOP-28L (θ_{JC}) .....20°C/W

Electrical Characteristics[2, 5]

V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C; unless noted.
Bold values indicate –40°C< T_J < +125°C.

Symbol	Parameter	Condition[2]	Min.	Typ.	Max.	Units
Supply Current						
I_{DD}	V_{DD} Quiescent Current	xLI = xHI = 0V		390	**750**	µA
I_{DDSH}	V_{DD} Shutdown Current	xLI = xHI = 0V; EN = 0V with HS = floating		2.2	**10**	µA
		xLI = xHI = 0V ; EN = 0V; HS = 0V		58	**150**	
I_{DDO}	V_{DD} Operating Current	f = 20kHz		0.6	**1.5**	mA
I_{HB}	Per Channel xHB Quiescent Current	xLI = xHI = 0V or xLI = 0V and xHI = 5V		20	**75**	µA
I_{HBO}	Per Channel xHB Operating Current	f = 20kHz		30	**400**	µA
I_{HBS}	xHB to V_{SS} Current, Quiescent	V_{xHS} = V_{xHB} = 90V		0.05	5	µA
I_{HBSO}	xHB to V_{SS} Current, Operating	f = 20kHz		30	**300**	µA

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. “x” in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).
3. The device is not guaranteed to function outside its operating ratings.
4. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
5. Specification for packaged product only.

Electrical Characteristics[2, 5] (Continued)

V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C; unless noted.
Bold values indicate –40°C< T_J < +125°C.

Symbol	Parameter	Condition[2]	Min.	Typ.	Max.	Units
Input (TTL: xLI, xHI, xPWM, EN)[6]						
V_{IL}	Low-Level Input Voltage				**0.8**	V
V_{IH}	High-Level Input Voltage		**2.2**			V
V_{HYS}	Input Voltage Hysteresis			0.1		V
R_I	Input Pull-Down Resistance	xLI and xHI Inputs (-1 Version)	**100**	300	**500**	kΩ
		xPWM Input (-2 Version)	**50**	130	**250**	
Undervoltage Protection						
V_{DDR}	V_{DD} Falling Threshold		**3.8**	4.4	**4.9**	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.25		V
V_{HBR}	xHB Falling Threshold		**4.0**	4.4	**4.9**	V
V_{HBH}	xHB Threshold Hysteresis			0.25		V
Overcurrent Protection						
V_{ILIM+}	Rising Overcurrent Threshold	(V_{ILIM+} – $V_{ILIM–}$)	175	200	225	mV
t_{ILIM_PROP}	ILIM to Gate Propagation Delay	V_{ILIM+} = 0.5V peak		70		ns
Fault Circuit						
V_{OLF}	FLT/ Output Low Voltage	V_{ILIM} = 1V; $I_{FLT/}$ = 1mA		0.2	0.5	V
V_{DLY+}	Rising DLY Threshold			1.5		V
I_{DLY}	DLY Current Source	V_{DLY} = 0V	0.3	0.44	0.6	µA
t_{FCL}	Fault Clear Time	C_{DLY} = 1nF		670		µs
Bootstrap Diode						
V_{DL}	Low-Current Forward Voltage	$I_{VDD-xHB}$ = 100µA		0.4	**0.70**	V
V_{DH}	High-Current Forward Voltage	$I_{VDD-xHB}$ = 50mA		0.8	**1**	V
R_D	Dynamic Resistance	$I_{VDD-xHB}$ = 50mA		4	**6**	Ω
xLO Gate Driver						
V_{OLL}	Low-Level Output Voltage	I_{xLO} = 50mA		0.3	**0.6**	V
V_{OHL}	High-Level Output Voltage	I_{xLO} = –50mA, V_{OHL} = V_{DD} - V_{xLO}		0.5	**1**	V
I_{OHL}	Peak Sink Current	V_{xLO} = 0V		1		A
I_{OLL}	Peak Source Current	V_{xLO} = 12V		1		A

Note:

6. $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

Electrical Characteristics[2, 5] (Continued)

V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C; unless noted.
Bold values indicate –40°C< T_J < +125°C.

Symbol	Parameter	Condition[2]	Min.	Typ.	Max.	Units
xHO Gate Driver						
V_{OLH}	Low-Level Output Voltage	I_{xHO} = 50mA		0.3	**0.6**	V
V_{OHH}	High-Level Output Voltage	I_{xHO} = –50mA, V_{OHH} = V_{xHB} – V_{xHO}		0.5	**1**	V
I_{OHH}	Peak Sink Current	V_{xHO} = 0V		1		A
I_{OLH}	Peak Source Current	V_{xHO} = 12V		1		A
Switching Specifications (LI/HI mode with inputs non-overlapping, assumes HS low before LI goes high and LO low before HI goes high).						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			35	**75**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			35	**75**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			35	**75**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			35	**75**	ns
$t_{R/F}$	Output Rise/Fall Time	C_L = 1000pF		20		ns
$t_{R/F}$	Output Rise/Fall Time (3V to 9V)	CL = 0.1µF		0.8		µs
t_{PW}	Minimum Input Pulse Width that Changes the Output	Note 7		50		ns
Switching Specifications PWM Mode (MIC4607-2) or LI/HI mode (MIC4607-1) with Overlapping LI/HI Inputs						
t_{LOOFF}	Delay from PWM Going High / LI Low, to LO Going Low			35	**75**	ns
V_{LOOFF}	LO Output Voltage Threshold for LO FET to be Considered Off			1.9		V
t_{HOON}	Delay from LO Off to HO Going High			35	**75**	ns
t_{HOOFF}	Delay from PWM or HI Going Low to HO Going Low			35	**75**	ns
V_{SWTH}	Switch Node Voltage Threshold Signaling HO is Off		1	2.2	**4**	V
t_{LOON}	Delay between HO FET Being Considered Off to LO Turning On			35	**75**	ns
t_{SWTO}	Forced xLO On if V_{SWTH} is Not Detected		**100**	250	**500**	ns

Note:

7. Guaranteed by design. Not production tested.

Timing Diagrams

Non-Overlapping LI/HI Input Mode (MIC4607-1)

In non-overlapping LI/HI input mode, enough delay is added between the xLI and xHI inputs to allow xHS to be low before xLI is pulled high and similarly xLO is low before xHI goes high.

xHO goes high with a high signal on xHI after a typical delay of 35ns (t_{HPLH}). xHI going low drives xHO low also with typical delay of 35ns (t_{HPHL}).

Likewise, xLI going high forces xLO high after typical delay of 35ns (t_{LPLH}) and xLO follows low transition of xLI after typical delay of 35ns (t_{LPHL}).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20ns driving 1000pF capacitive loads

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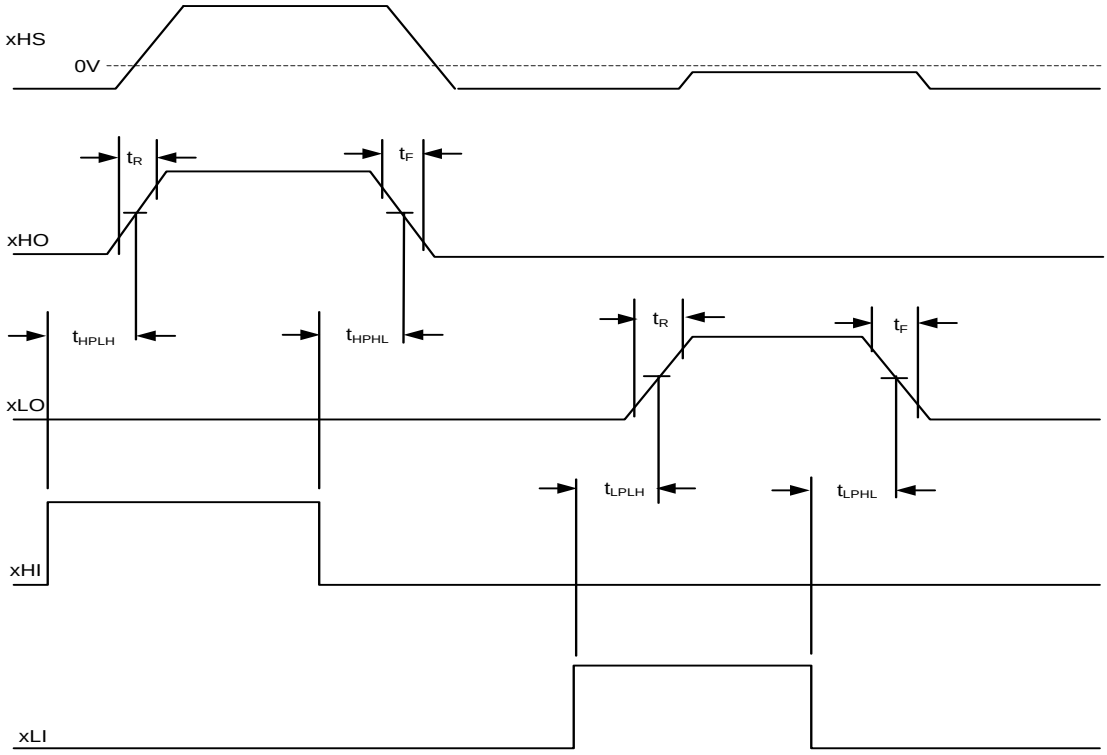


Figure 1. Separate Non-Overlapping LI/HI Input Mode (MIC4607-1)

Notes:

All propagation delays are measured from the 50% voltage level and rise/fall times are measured 10% to 90%.

"x" in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

Timing Diagrams (Continued)

Overlapping LI/HI Input Mode (MIC4607-1)

When xLI/xHI input high signals overlap, xLO/xHO output states are determined by the first output to be turned on. That is, if xLI goes high (ON), while xHO is high, xHO stays high until xHI goes low at which point, after a delay of t_{HOOFF} and when xHS < 2.2V, xLO goes high with a delay of t_{LOON}. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xHI edge delayed by a typical 250ns will set “HS latch” allowing xLO to go high.

If xHS falls very fast, xLO will be held low by a 35ns delay gated by HI going low. Conversely, xHI going high (ON) when xLO is high has no effect on outputs until xLI is pulled low (off) and xLO falls to < 1.9V. Delay from xLI going low to xLO falling is t_{LOOFF} and delay from xLO < 1.9V to xHO being on is t_{HOON}.

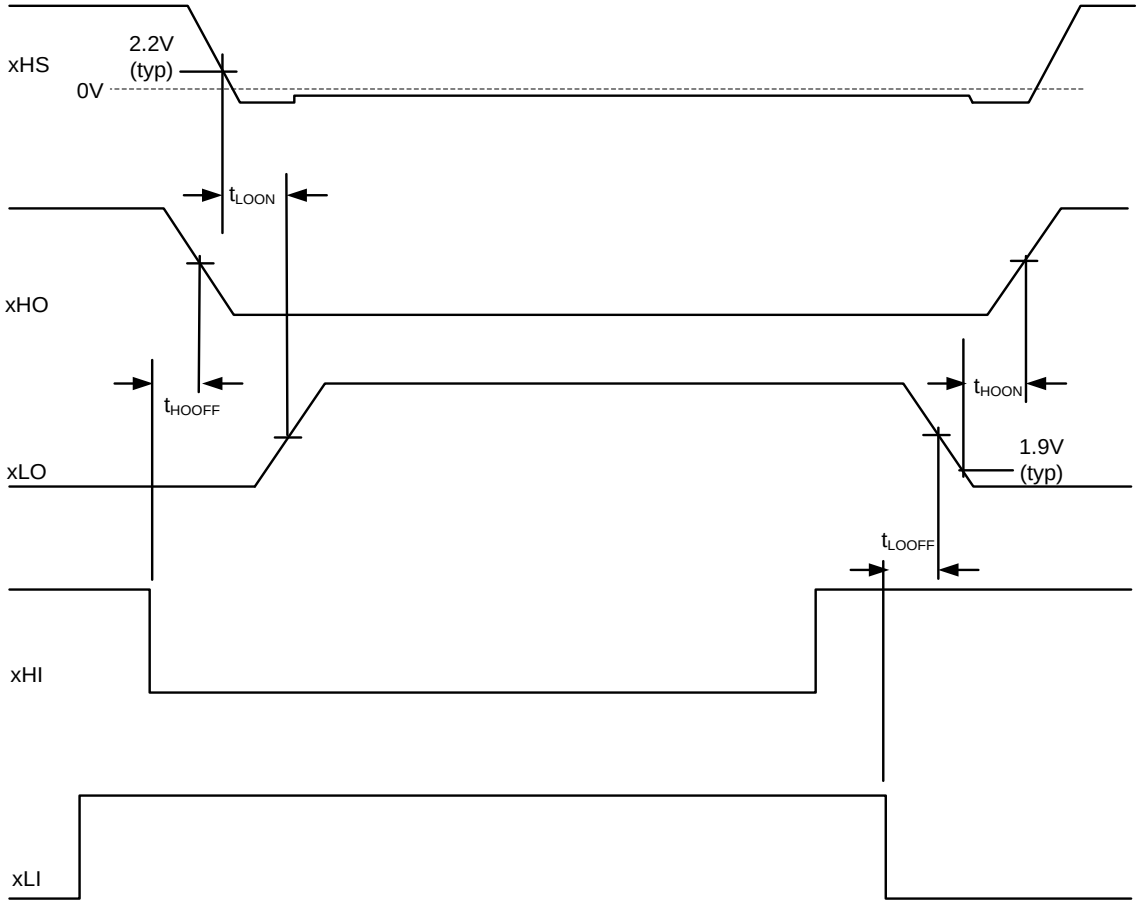


Figure 2. Separate Overlapping LI/HI Input Mode (MIC4607-1)

Timing Diagrams (Continued)

PWM Input Mode (MIC4607-2)

A low going xPWM signal applied to the MIC4607-2 causes xHO to go low, typically 35ns (t_{HOOFF}) after the xPWM input goes low, at which point the switch node, xHS, falls (1 – 2).

When xHS reaches 2.2V (V_{SWTH}), the external high-side MOSFET is deemed off and xLO goes high, typically within 35ns (t_{LOON}) (3-4). xHS falling below 2.2V sets a latch that can only be reset by xPWM going high. This design prevents ringing on xHS from causing an indeterminate xLO state. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xPWM edge delayed by 250ns will set “HS latch” allowing xLO to go high.

A 35ns delay gated by xPWM going low can determine the time to xLO going high for fast falling HS designs. xPWM going high forces xLO low in typically 35ns (t_{LOOFF}) (5 – 6).

When xLO reaches 1.9V (V_{LOOFF}), the low-side MOSFET is deemed off and xHO is allowed to go high. The delay between these two points is typically 35ns (t_{HOON}) (7 – 8).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20ns driving 1000pF capacitive loads.

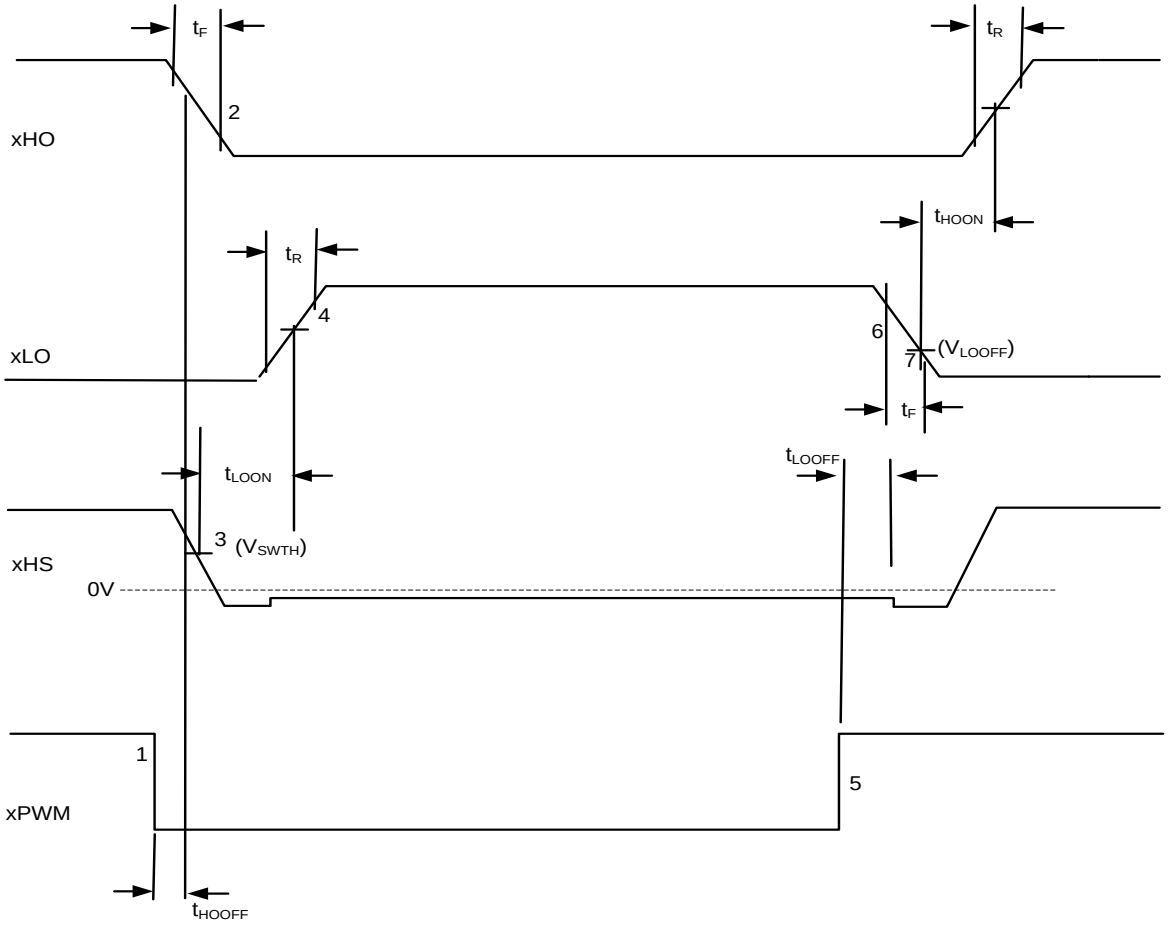


Figure 3. PWM Mode (MIC4607-2)

Overcurrent Timing Diagram

The motor current is sensed in an external resistor that is connected between the low-side MOSFET's source pins and ground. If the sense resistor voltage exceeds the rising overcurrent threshold (typically 0.2V), all LO and HO outputs are latched off and the FLT/ pin is pulled low. Once the outputs are latched off, an internal current source (typically 0.44uA) begins to charge up the external C_{DELAY} capacitor. The outputs remain latched off and all xLI/xHI (or xPWM) input signals are ignored until the voltage on the C_{DELAY} capacitor rises above the V_{DLY+} threshold (typically 1.5V), which resets the latch on the first rising edge of any LI input of the MIC4607-1 (or falling edge on any PWM input for the MIC4607-2).

Once this occurs, the C_{DLY} capacitor is discharged, the FLT/ pin returns to a high impedance state and all outputs will respond to their respective input signals.

On startup, the current limit latch is reset during a rising V_{DD} or a rising EN pin voltage to assure normal operation.

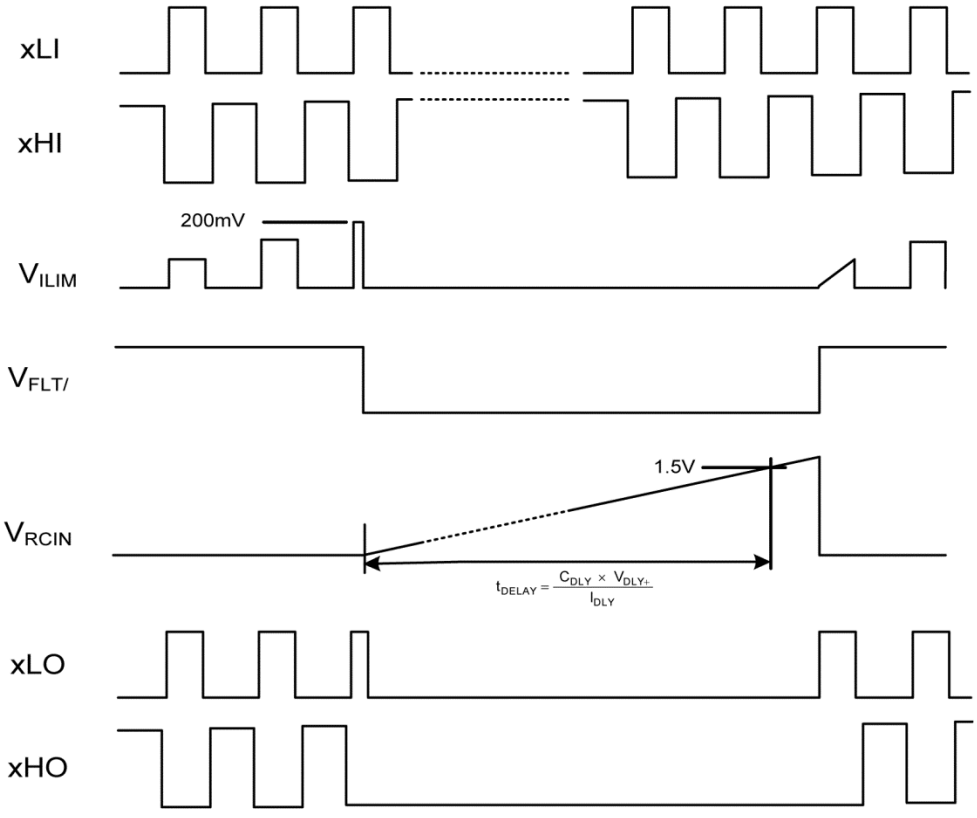
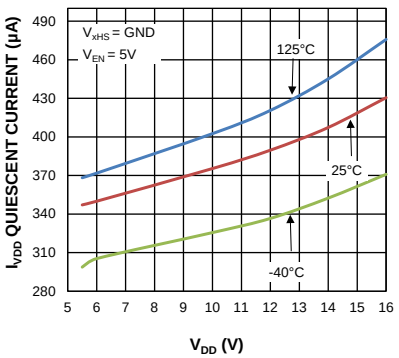


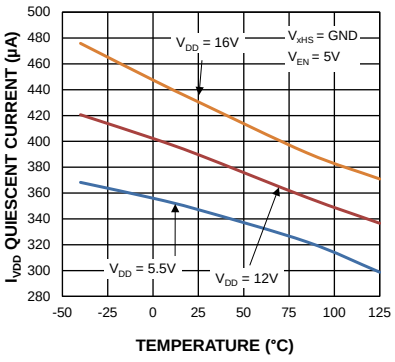
Figure 4. Overcurrent Timing Diagram

Typical Characteristics

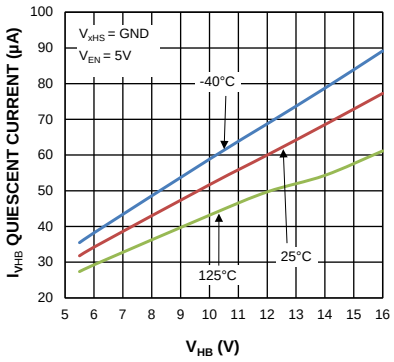
V_{DD} Quiescent Current vs. V_{DD} Voltage



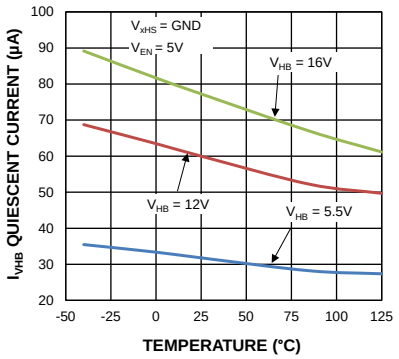
V_{DD} Quiescent Current vs. Temperature



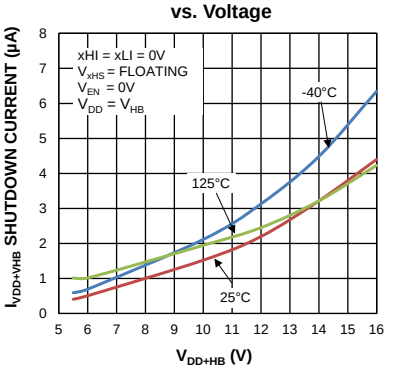
V_{HB} Quiescent Current (All Channels) vs. V_{HB} Voltage



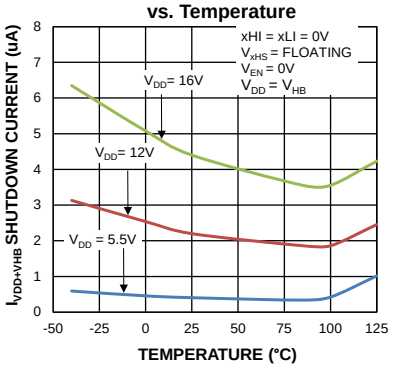
V_{HB} Quiescent Current (All Channels) vs. Temperature



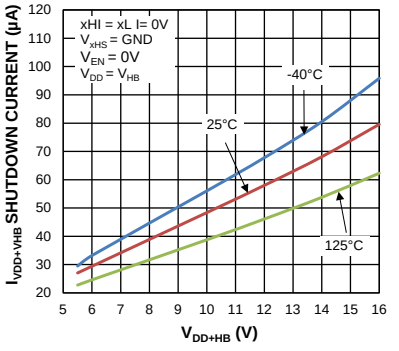
V_{DD+HB} Shutdown Current (Floating Switch Node) vs. Voltage



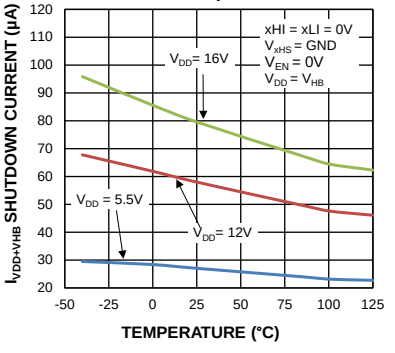
V_{DD+HB} Shutdown Current (Floating Switch Node) vs. Temperature



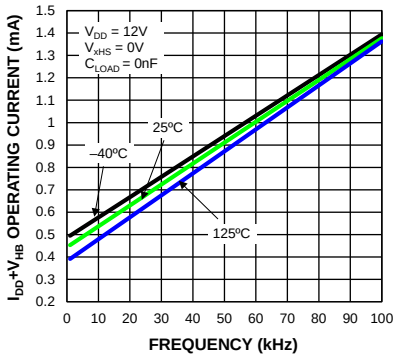
V_{DD+HB} Shutdown Current (Grounded Switch Node) vs. Voltage



V_{DD+HB} Shutdown Current (Grounded Switch Node) vs. Temperature

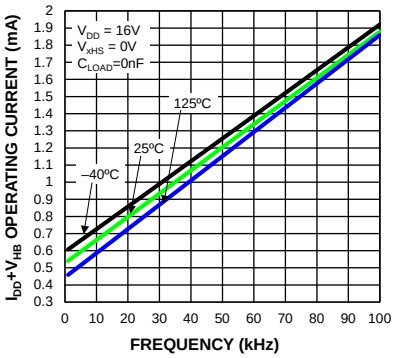


V_{DD+HB} Operating Current vs. Switching Frequency

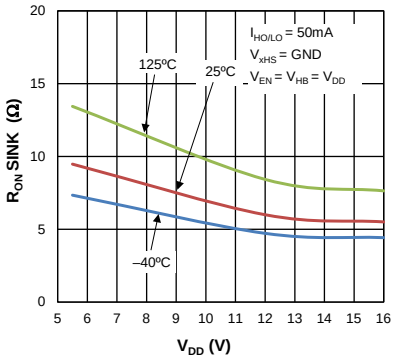


Typical Characteristics (Continued)

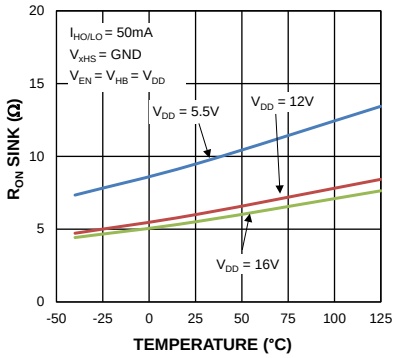
V_{DD+HB} Operating Current vs. Switching Frequency



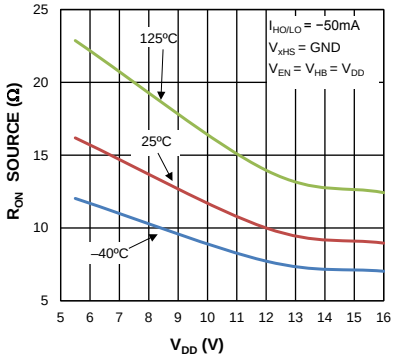
HO/LO Sink On-Resistance vs. V_{DD}



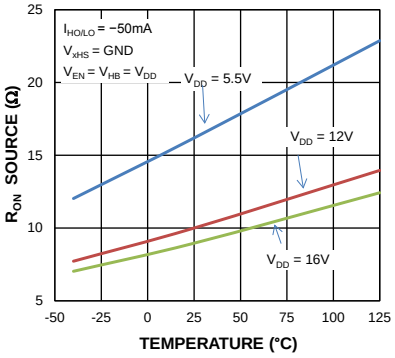
HO/LO Sink On-Resistance vs. Temperature



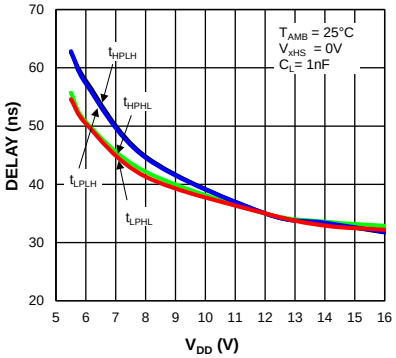
HO/LO Source On-Resistance vs. V_{DD}



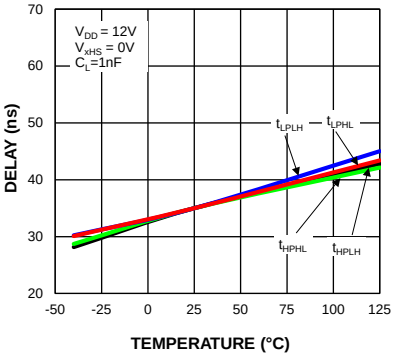
HO/LO Source On-Resistance vs. Temperature



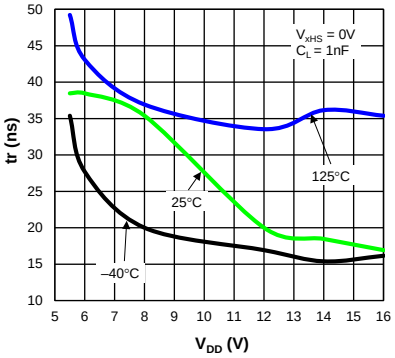
Propagation Delay (HI/LI Input) vs. V_{DD} Voltage



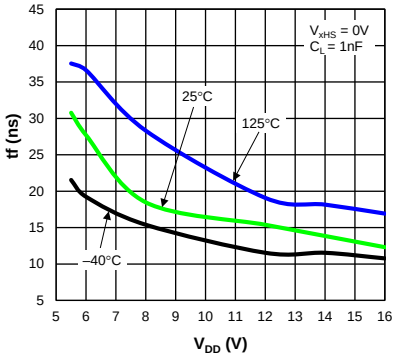
Propagation Delay (HI/LI Input) vs. Temperature



Output Rise Time vs. V_{DD} Voltage

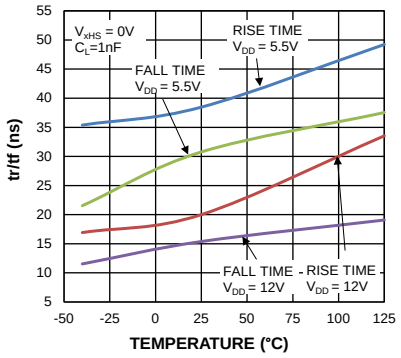


Output Fall Time vs. V_{DD} Voltage

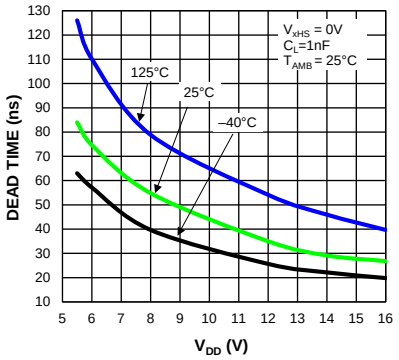


Typical Characteristics (Continued)

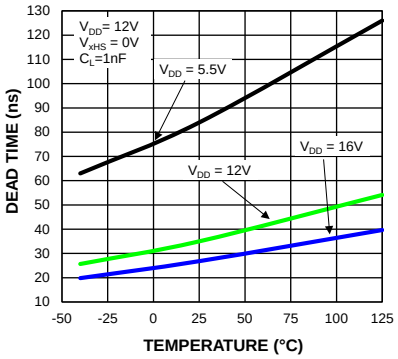
Rise/Fall Time vs. Temperature



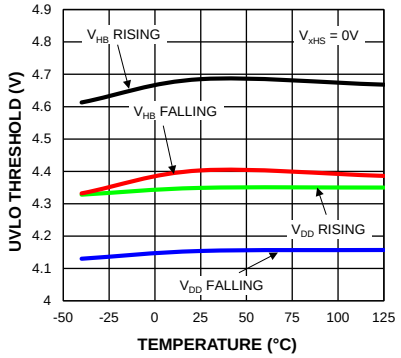
Dead Time vs. V_{DD} Voltage



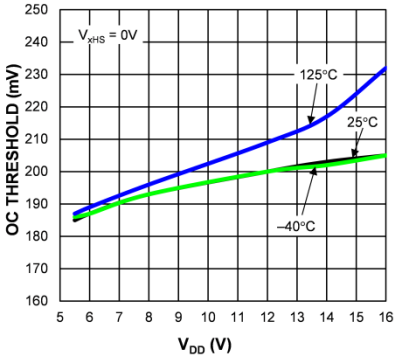
Dead Time vs. Temperature



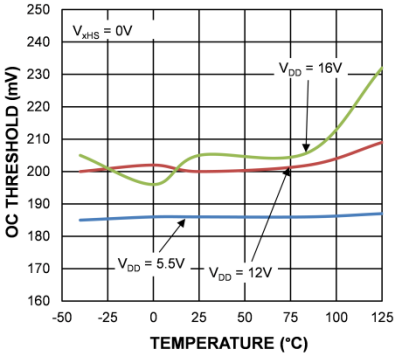
V_{DD}/V_{HB} UVLO vs. Temperature



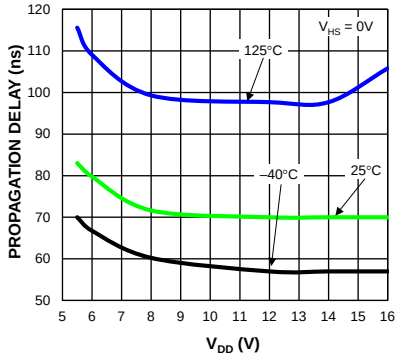
Overcurrent Threshold vs. V_{DD} Voltage



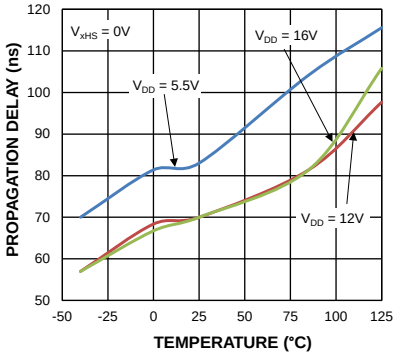
Overcurrent Threshold vs. Temperature



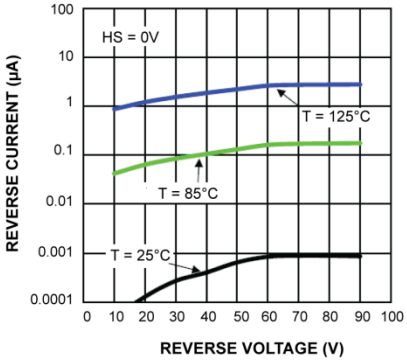
Overcurrent Propagation Delay vs. V_{DD} Voltage



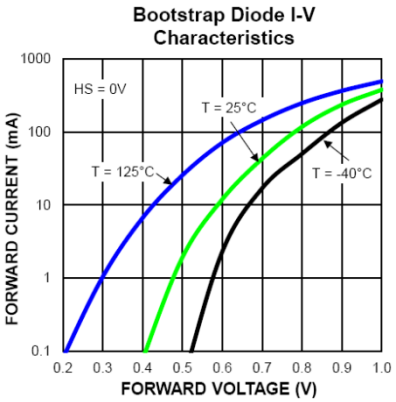
Overcurrent Propagation Delay vs. Temperature



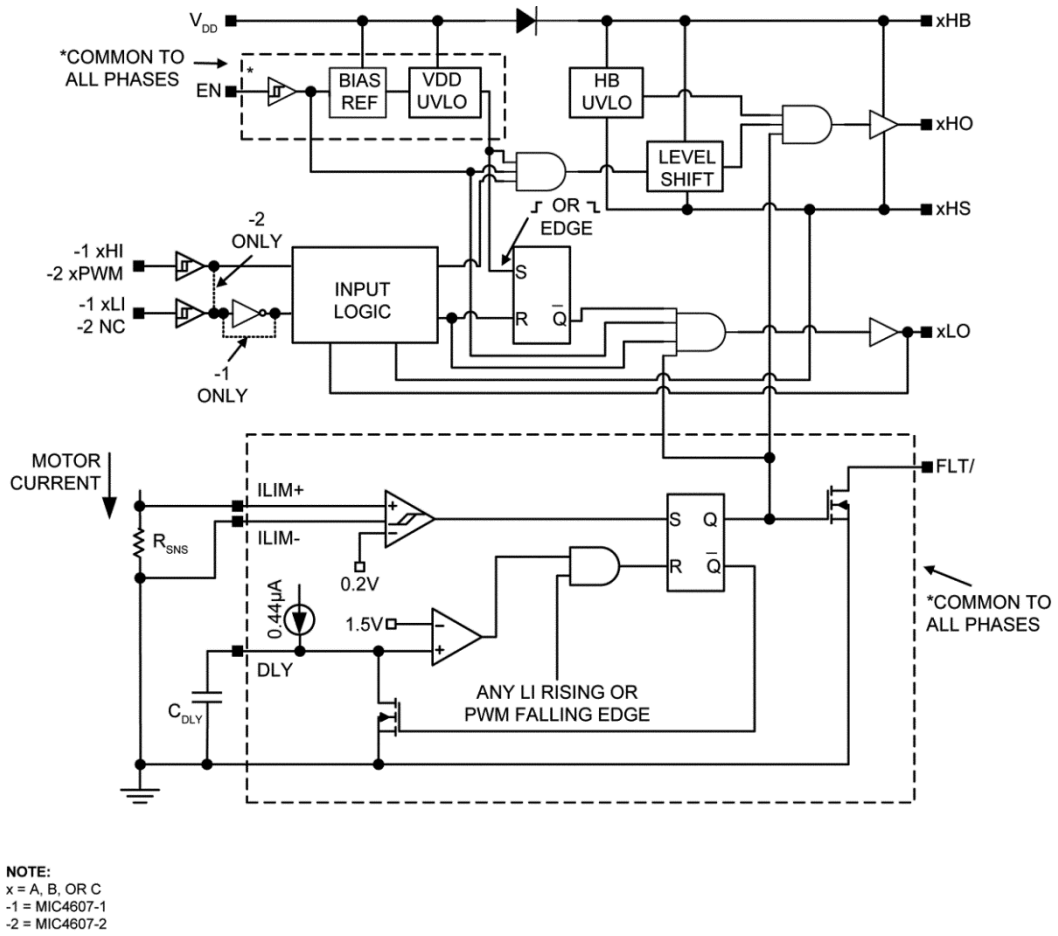
Bootstrap Diode Reverse Current



Typical Characteristics (Continued)



Functional Diagram



NOTE:
x = A, B, OR C
-1 = MIC4607-1
-2 = MIC4607-2

Figure 5. MIC4607 xPhase Top-Level Functional Diagram

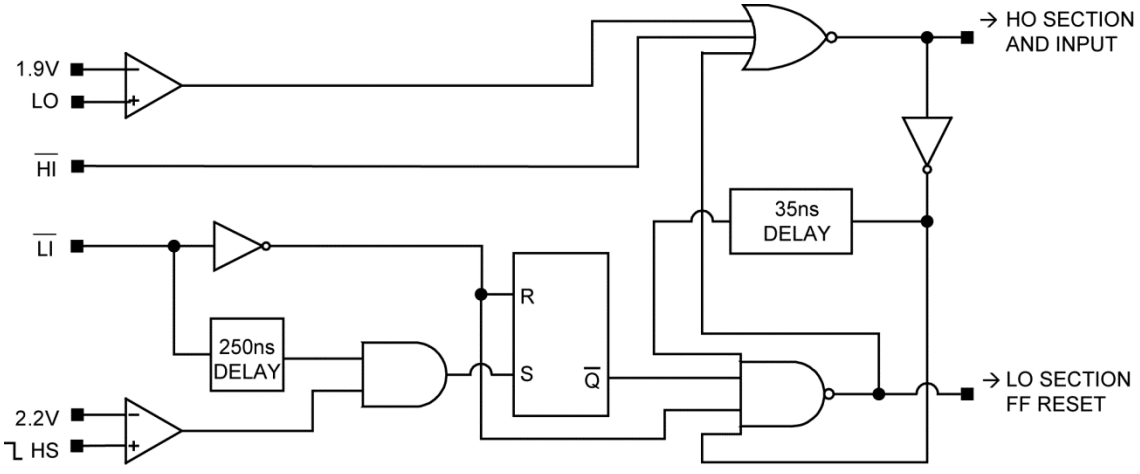


Figure 6. Input Logic Block

Functional Description

The MIC4607 is a non-inverting, 85V three-phase MOSFET driver designed to independently drive all six N-Channel MOSFETs in a three-phase bridge. The MIC4607 offers a wide 5.5V to 16V V_{DD} operating supply range with either six independent TTL inputs (MIC4607-1) or three PWM inputs, one for each phase (MIC4607-2). Refer to the *Functional Diagram* section.

The drivers contain input buffers with hysteresis, four independent UVLO circuits (three high-side and one low-side), and six output drivers. The high-side output drivers utilize a high-speed level-shifting circuit that is referenced to its HS pin. Each phase has an internal diode that is used by the bootstrap circuits to provide the drive voltages for each of the three high-side outputs. A programmable overcurrent protection circuit turns off all outputs during an overcurrent fault.

Startup and UVLO

The UVLO circuits force the driver's outputs low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuits monitor the voltage between the xHB and xHS pins. Hysteresis in the UVLO circuits prevent system noise and finite circuit impedance from causing chatter during turn-on.

Enable Inputs

There is one external enable pin that controls all three phases. A logic high on the enable pin (EN) allows for startup of all phases and normal operation. Conversely, when a logic low is applied on the enable pin, all phases turn-off and the device enters a low current shutdown mode. All outputs (xHO and xLO) are pulled low when EN is low. Do not leave the EN pin floating.

Input Stage

All input pins (xLI and xHI) are referenced to the VSS pin. The MIC4607 has a TTL-compatible input range and can be used with input signals with amplitude less than the supply voltage. The threshold level is independent of the VDD supply voltage and there is no dependence between IVDD and the input signal amplitude. This feature makes the MIC4607 an excellent level translator that will drive high level gate threshold MOSFETs from a low-voltage PWM IC.

Low-Side Driver

The low-side driver is designed to drive a ground (VSS pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low R_{DSON} from the external power device. Refer to Figure 7.

A high level applied to the xLI pin causes V_{DD} to be applied to the gate of the external MOSFET. A low level on the xLI pin grounds the gate of the external MOSFET.

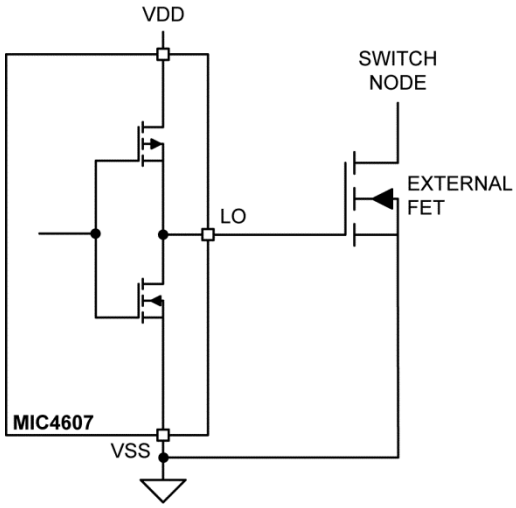


Figure 7. Low-Side Driver Block Diagram

High-Side Driver and Bootstrap Circuit

Figure 8 illustrates a block diagram of the high-side driver and bootstrap circuit. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.

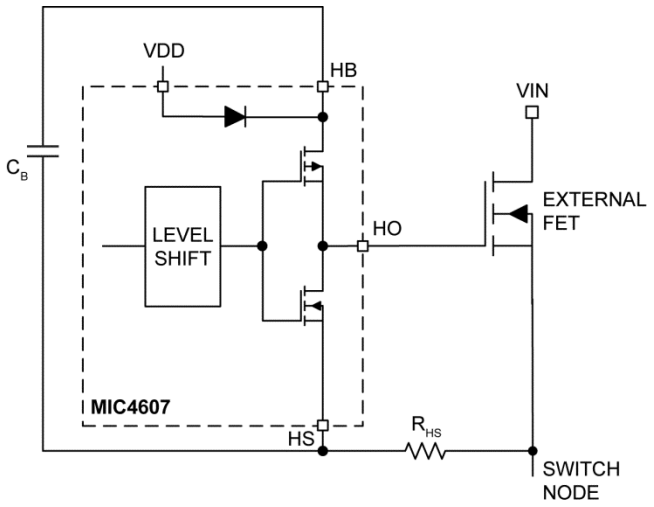


Figure 8. High-Side Driver and Bootstrap-Circuit Block Diagram

A low-power, high-speed, level-shifting circuit isolates the low side (VSS pin) referenced circuitry from the high-side (xHS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap capacitor (C_B) while the voltage level of the xHS pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor, C_B. In a typical application, such as the motor driver shown in Figure 9 (only Phase A illustrated), the AHS pin is at ground potential while the low-side MOSFET is on. The internal diode charges capacitor C_B to V_{DD}-V_F during this time (where V_F is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the AHO pin turns on, the voltage across capacitor C_B is applied to the gate of the high-side external MOSFET. As the high-side MOSFET turns on, voltage on the AHS pin rises with the source of the high-side MOSFET until it reaches V_{IN}. As the AHS and AHB pins rise, the internal diode is reverse biased, preventing capacitor C_B from discharging. During this time, the high-side MOSFET is kept ON by the voltage across capacitor C_B.

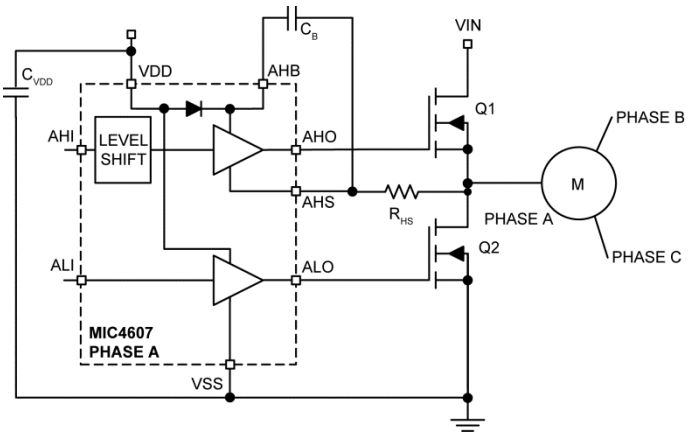


Figure 9. MIC4607 Motor Driver Example

Programmable Gate Drive

The MIC4607 offers programmable gate drive, meaning the MOSFET gate drive (gate-to-source voltage) equals the V_{DD} voltage. This feature offers designers flexibility in selecting the proper MOSFETs for a given application. Different MOSFETs require different V_{GS} characteristics for optimum R_{DSON} performance. Typically, the higher the gate voltage (up to 16V), the lower the R_{DSON} achieved. For example, as shown in Figure 10, a NTMSF4899NF MOSFET can be driven to the ON state with a gate voltage of 5.5V but R_{DSON} is 5.2mΩ. If driven to 10V, R_{DSON} is 4.1mΩ – a decrease of 20%.

In low-current applications, the losses due to R_{DSON} are minimal, but in high-current motor drive applications such as power tools, the difference in R_{DSON} can lower the efficiency, reducing run time.

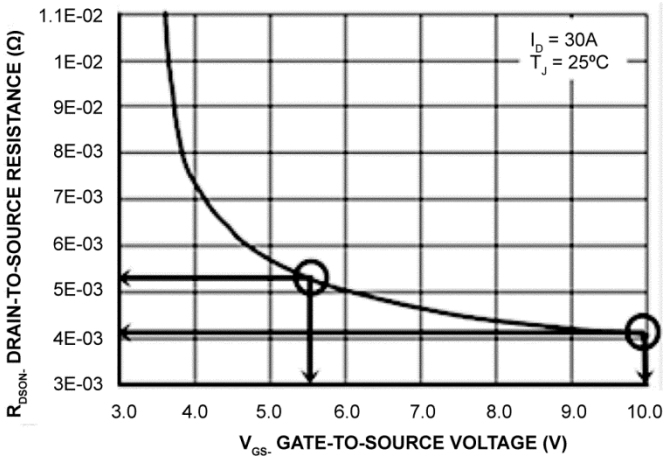


Figure 10. MOSFET R_{DSON} vs. V_{GS}

Overcurrent Protection Circuitry

The MIC4607 provides overcurrent protection for the motor driver circuitry. It consists of:

- A comparator that senses the voltage across a current-sense resistor
- A latch and timer that keep all gate drivers off during a fault
- An open-drain pin that pulls low during the fault.

If an overcurrent condition is detected, the FLT/ pin is pulled low and the gate drive outputs are latched off for a time that is determined by the DLY pin circuitry. After the delay circuitry times out, a high-going edge on any of the LI pins (for the MIC4607-1 version) or a low-going edge on any of the PWM pins (for the MIC4607-2 version) is required to reset the latch, de-assert the FLT/ pin and allow the gate drive outputs to switch.

For additional information, refer to the *Timing Diagrams* section as well as the *Functional Diagram* section.

ILIM

The ILIM+ and ILIM- pins provide a Kelvin-sensed circuit that monitors the voltage across an external current sense resistor. This resistor is typically connected between the source pins of all three low-side MOSFETs and power ground. If the peak voltage across this resistor exceeds the V_{ILIM+} threshold, it will cause all six outputs to latch off. Both pins should be shorted to VSS ground if the overcurrent features is not used.

DLY

A capacitor connected to the DLY pin determines the amount of time the gate drive outputs are latched off before they can be restarted.

During normal operation, the DLY pin is held low by an internal MOSFET. After an over-current condition is detected, the MOSFET turns off and the external capacitor is charged up by an internal current source. The outputs remain latched off until the DLY pin voltage reaches the V_{DLY+} threshold (typically 1.5V).

The delay time can be approximately calculated using Equation 1:

$$t_{DLY} = \frac{C_{DLY} \times V_{DLY-}}{I_{DLY}} \quad \text{Eq. 1}$$

Where:

C_{DLY} is the external capacitance on the DLY pin

I_{DLY} is the DLY pin current source (typically 0.44µA)

V_{DLY+} is the internal comparator threshold (typically 1.5V)

FLT/

This open-drain output is pulled low while the gate drive outputs are latched off after an over-current condition. It will de-assert once the DLY pin has reached the V_{DLY+} threshold and a rising edge occurs on any LI pin (for the MIC4607-1) or a falling edge on any PWM pin (MIC4607-2).

During normal operation, the internal pull-down MOSFET is of the pin is high impedance. A pull-up resistor must be connected to this pin.

Application Information

Adaptive Dead Time

For each phase, it is important that both MOSFETs of the same phase branch are not conducting at the same time or V_{IN} will be shorted to ground and current will "shoot through" the MOSFETs. Excessive shoot-through causes higher power dissipation in the MOSFETs, voltage spikes and ringing. The high switching current and voltage ringing generate conducted and radiated EMI.

Minimizing shoot-through can be done passively, actively or through a combination of both. Passive shoot-through protection can be achieved by implementing delays between the high and low gate drivers to prevent both MOSFETs from being on at the same time. These delays can be adjusted for different applications. Although simple, the disadvantage of this approach is that it requires long delays to account for process and temperature variations in the MOSFET and MOSFET driver.

Adaptive Dead Time monitors voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs on and off. This active approach adjusts the delays to account for some of the variations, but it too has its disadvantages. High currents and fast switching voltages in the gate drive and return paths can cause parasitic ringing to turn the MOSFETs back on even while the gate driver output is low. Another disadvantage is that the driver cannot monitor the gate voltage inside the MOSFET. Figure 11 shows an equivalent circuit of the high-side gate drive.

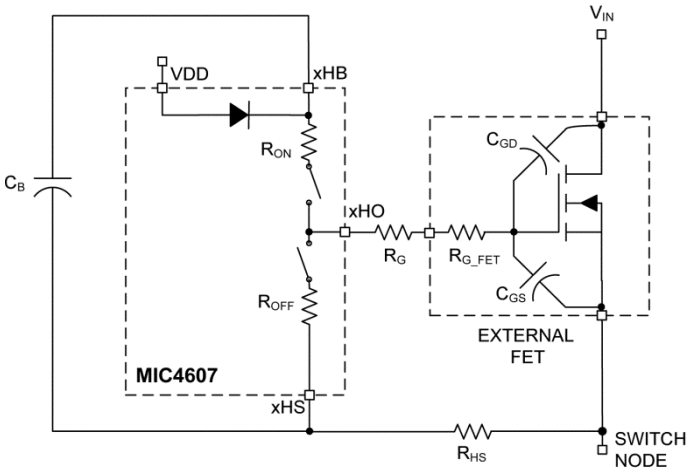


Figure 11. MIC4607 Driving an External MOSFET

The internal gate resistance (R_{G_FET}) and any external damping resistor (R_G) and HS pin resistor (R_{HS}), isolate the MOSFET's gate from the driver output. There is a delay between when the driver output goes low and the MOSFET turns off. This turn-off delay is usually specified in the MOSFET data sheet. This delay increases when an external damping resistor is used.

The MIC4607 uses a combination of active sensing and passive delay to ensure that both MOSFETs are not on at the same time. Figure 12 illustrates how the adaptive dead-time circuitry works.

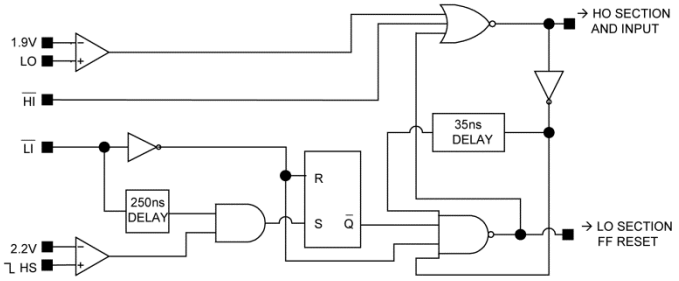


Figure 12. Adaptive Dead-Time Logic Diagram

For the MIC4607-2, a high level on the xPWM pin causes $\overline{HI}$ to go low and $\overline{LI}$ to go high. This causes the xLO pin to go low. The MIC4607 monitors the xLO pin voltage and prevents the xHO pin from turning on until the voltage on the xLO pin reaches the V_{LOOFF} threshold. After a short delay, the MIC4607 drives the xHO pin high. Monitoring the xLO voltage eliminates any excessive delay due to the MOSFET driver's turn-off time and the short delay accounts for the MOSFET turn-off delay as well as letting the xLO pin voltage settle out. If an external resistor is used between the xLO output and the MOSFET gate, it must be made small enough to prevent excessive voltage drop across the resistor during turn-off. Figure 13 illustrates using a diode (D_{LS}) and resistor (R_{LS2}) in parallel with the gate resistor to prevent a large voltage drop between the xLO pin and MOSFET gate voltages during turn-off.

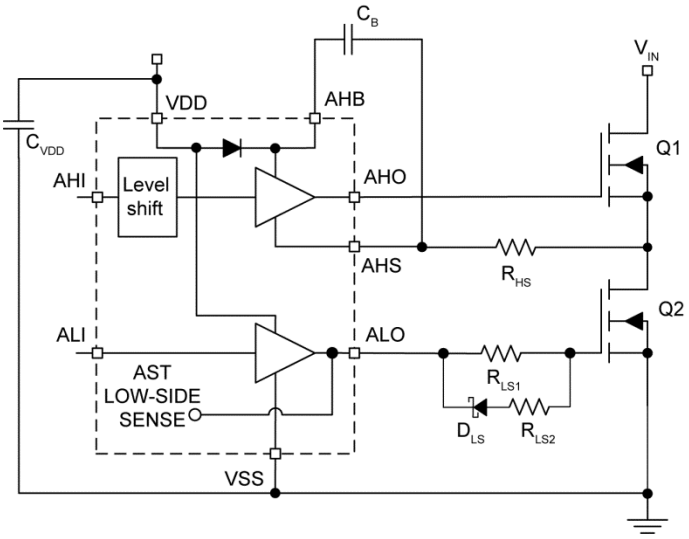


Figure 13. Low-Side Drive Gate Resistor Configuration

A low on the xPWM pin causes $\overline{HI}$ to go high and $\overline{LI}$ to go low. This causes the xHO pin to go low after a short delay (t_{HOOFF}). Before the xLO pin can go high, the voltage on the switching node (xHS pin) must have dropped to 2.2V. Monitoring the switch voltage instead of the xHO pin voltage eliminates timing variations and excessive delays due to the high side MOSFET turn-off. The xLO driver turns on after a short delay (t_{LOON}). Once the xLO driver is turned on, it is latched on until the xPWM signal goes high. This prevents any ringing or oscillations on the switch node or xHS pin from turning off the xLO driver. If the xPWM pin goes low and the voltage on the xHS pin does not cross the V_{SWTH} threshold, the xLO pin will be forced high after a short delay (t_{SWTO}), insuring proper operation.

The internal logic circuits also insure a "first on" priority at the inputs. If the xHO output is high, the xLI pin is inhibited. A high signal or noise glitch on the xLI pin has no effect on the xHO or xLO outputs until the xHI pin goes low. Similarly, xLO being high holds xHO low until xLI and xLO are low.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure that the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width can result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is determined by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned back on.

Although the adaptive dead-time circuit in the MIC4607 prevents the driver from turning both MOSFETs on at the same time, other factors outside of the anti-shoot-through circuit's control can cause shoot-through. Other factors include ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

The scope photo in Figure 14 shows the dead time (<20ns) between the high- and low-side MOSFET transitions as the low-side driver switches off while the high-side driver transitions from off to on.

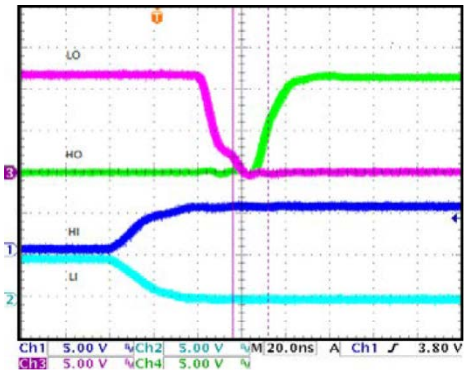


Figure 14. Adaptive Dead-Time LO (LOW) to HO (HIGH)

Table 1 contains truth tables for the MIC4607-1 (independent TTL inputs) and Table 2 is for the MIC4607-2 (PWM inputs) that details the "first on" priority as well as the failsafe delay (t_{SWTO}).

Table 1. MIC4607-1 Truth Table

xLI	xHI	xLO	xHO	Comments
0	0	0	0	Both outputs off.
0	1	0	1	xHO will not go HIGH until xLO falls below 1.9V.
1	0	1	0	xLO will be delayed an extra 250ns if xHS never falls below 2.2V.
1	1	X	X	First ON stays on until input of same goes LOW.

Table 2. MIC4607-2 Truth Table

xPWM	xLO	xHO	Comments
0	1	0	xLO will be delayed an extra 250ns if xHS never falls below 2.2V.
1	0	1	xHO will not go HIGH until xLO falls below 1.9V.

HS Node Clamp

A resistor/diode clamp between the switching node and the HS pin is necessary to clamp large negative glitches or pulses on the HS pin.

Figure 15 shows the Phase A section high-side and low-side MOSFETs connected to one phase of the three phase motor. There is a brief period of time (dead time) between switching to prevent both MOSFETs from being on at the same time. When the high-side MOSFET is conducting during the on-time state, current flows into the motor. After the high-side MOSFET turns off, but before the low-side MOSFET turns on, current from the motor flows through the body diode in parallel with the low-side MOSFET. Depending upon the turn-on time of the body diode, the motor current, and circuit parasitics, the initial negative voltage on the switch node can be several volts or more. The forward voltage drop of the body diode can be several volts, depending on the body diode characteristics and motor current.

Even though the HS pin is rated for negative voltage, it is good practice to clamp the negative voltage on the HS pin with a resistor and possibly a diode to prevent excessive negative voltage from damaging the driver. Depending upon the application and amount of negative voltage on the switch node, a 3Ω resistor is recommended. If the HS pin voltage exceeds 0.7V, a diode between the xHS pin and ground is recommended. The diode reverse voltage rating must be greater than the high-voltage input supply (V_{IN}). Larger values of resistance can be used if necessary.

Adding a series resistor in the switch node limits the peak high-side driver current during turn-off, which affects the switching speed of the high-side driver. The resistor in series with the HO pin may be reduced to help compensate for the extra HS pin resistance.

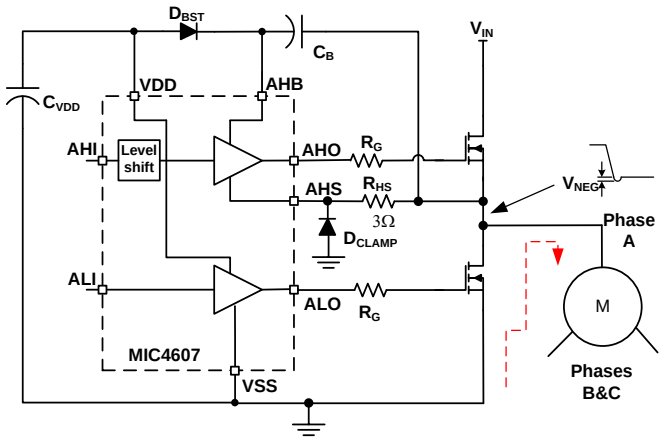


Figure 15. Negative HS Pin Voltage

Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the bootstrap capacitor (C_B) multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by:

$$I_{F(AVE)} = Q_{GATE} \times f_S \quad \text{Eq. 1}$$

Where:

Q_{GATE} = Total gate charge at $V_{HB} – V_{HS}$.

f_S = Gate drive switching frequency.

The average power dissipated by the forward voltage drop of the diode equals:

$$P_{DIODE\,FWD} = I_{F(AVE)} \times V_F \quad \text{Eq. 2}$$

Where:

V_F = Diode forward voltage drop.

There are three phases in the MIC4607. The power dissipation for each of the bootstrap diodes must be calculated and summed to obtain the total bootstrap diode power dissipation for the package.

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 3µA at a reverse voltage of 85V at 125°C. Power dissipation due to reverse leakage is typically much less than 1mW and can be ignored.

An optional external bootstrap diode may be used instead of the internal diode (Figure 16). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the VDD supply voltage. The above equations can be used to calculate power dissipation in the external diode; however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as:

$$P_{DIODE_{REV}} = I_R \times V_{REV} \times (1 - D) \quad \text{Eq. 3}$$

Where:
I_R = Reverse current flow at V_{REV} and T_J.

V_{REV} = Diode reverse voltage.

D = Duty cycle = $t_{ON} \times f_S$.

The on-time is the time the high-side switch is conducting. In most topologies, the diode is reverse biased during the switching cycle off-time.

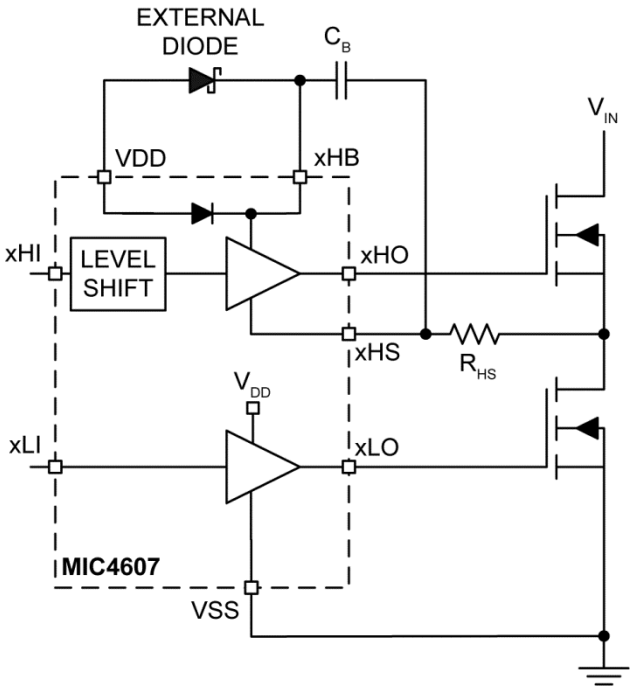


Figure 16. Optional External Bootstrap Diode

Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 17 shows a simplified equivalent circuit of the MIC4607 driving an external high-side MOSFET.

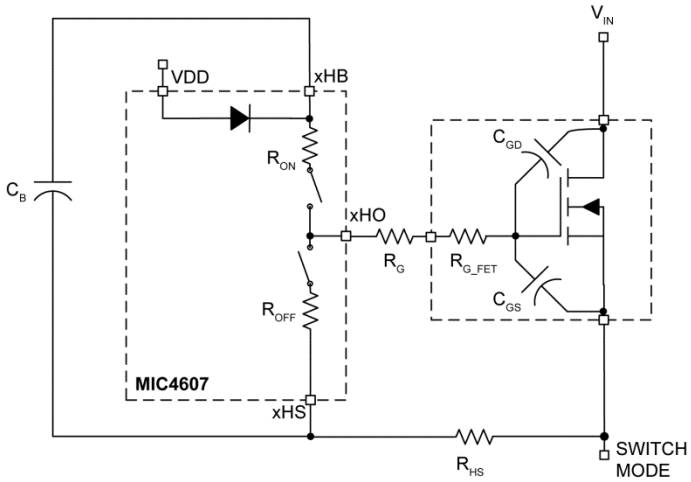


Figure 17. MIC4607 Driving an External High-Side MOSFET

Dissipation during the External MOSFET Turn-On

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G and R_{G_FET}. R_{ON} is the on resistance of the upper driver MOSFET in the MIC4607. R_G is the series resistor (if any) between the driver and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET and is typically listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_FET}.

The effective capacitances of C_{GD} and C_{GS} are difficult to calculate because they vary non-linearly with I_D, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge versus VGS. Figure 18 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^2$$

but

$$Q = C \times V \qquad \text{Eq. 4}$$

so,

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$

Where:
C_{ISS} = Total gate capacitance of the MOSFET.

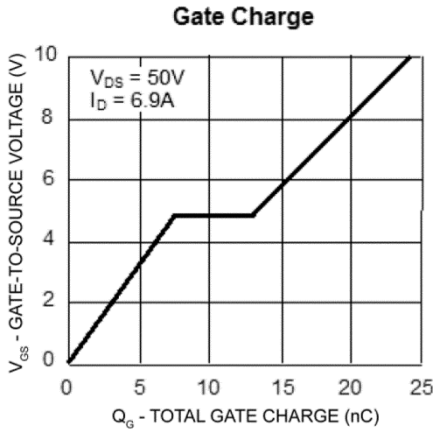


Figure 18. Typical Gate Charge vs. V_{GS}

The same energy is dissipated by R_{OFF}, R_G, and R_{G_FET} when the driver IC turns the MOSFET off. Assuming R_{ON} is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is:

$$E_{DRIVER} = Q_G \times V_{GS}$$

and

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S \qquad \text{Eq. 5}$$

Supply Current Power Dissipation

Power is dissipated in the input and control sections of the MIC4607, even if there is no external load. Current is still drawn from the VDD and HB pins for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The V_{DD} and V_{HB} currents are proportional to operating frequency and the V_{DD} and V_{HB} voltages. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4607 due to supply current is:

$$P_{DISS_{SUPPLY}} = V_{DD} \times I_{DD} + V_{HB} \times I_{HB} \qquad \text{Eq. 6}$$

Values for I_{DD} and I_{HB} are found in the EC table and the typical characteristics graphs.

Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4607 is equal to the power dissipation caused by driving the external MOSFETs, the supply currents and the internal bootstrap diodes.

$$P_{DISS_{TOTAL}} = P_{DISS_{SUPPLY}} + P_{DISS_{DRIVE}} + P_{DIODE} \qquad \text{Eq. 7}$$

Where:
E_{DRIVER} = Energy dissipated per switching cycle.

P_{DRIVER} = Power dissipated per switching cycle.

Q_G = Total gate charge at V_{GS}.

V_{GS} = Gate-to-source voltage on the MOSFET.

f_S = Switching frequency of the gate drive circuit.

The power dissipated in the driver equals the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting $R_{ON} = R_{OFF}$, the power dissipated in the driver due to driving the external MOSFET is:

$$P_{DISS_{DRIVER}} = P_{DRIVER} \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}} \quad \text{Eq. 8}$$

There are six MOSFETs driven by the MIC4607. The power dissipation for each of the drivers must be calculated and summed to obtain the total driver diode power dissipation for the package.

In some cases, the high-side FET of one phase may be pulsed at a frequency, f_S, while the low-side FET of the other phase is kept continuously on. Since the MOSFET gate is capacitive, there is no driver power if the FET is not switched. The operation of all driver outputs must be considered to accurately calculate power dissipation.

The die temperature can be calculated after the total power dissipation is known.

$$T_J = T_A + P_{DISS_{TOTAL}} \times \theta_{JA} \quad \text{Eq. 9}$$

Where:

T_A = Maximum ambient temperature.

T_J = Junction temperature (°C).

$P_{DISS_{TOTAL}}$ = Total power dissipation of the MIC4607.

θ_{JA} = Thermal resistance from junction to ambient air.

Other Timing Considerations

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low-side (VDD) and high-side (xHB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from xHB to xHS has two functions: it provides decoupling for the high-side circuitry and also provides current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1µF is required for C_B (xHB to xHS capacitors) and 1µF for the VDD capacitor, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the VDD and VSS pins. The bypass capacitor (C_B) for the xHB supply pin must be located as close as possible between the xHB and xHS pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the "Grounding, Component Placement and Circuit Layout" sub-section for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus V_{GS} voltage. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{HB}} \quad \text{Eq. 10}$$

Where:

Q_{GATE} = Total gate charge at V_{HB}.

ΔVHB = Voltage drop at the HB pin.

If the high-side MOSFET is not switched but held in an on state, the voltage in the bootstrap capacitor will drop due to leakage current that flows from the HB pin to ground. This current is specified in the EC table. In this case, the value of C_B is calculated as:

$$C_B \geq \frac{I_{HBS} \times t_{ON}}{\Delta V_{HB}} \quad \text{Eq. 11}$$

Where:
I_{HBS} = Maximum xHB pin leakage current.

t_{ON} = maximum high-side FET on-time.

The larger value of C_B from Equation 10 or Equation 11 should be used.

Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4607 driver require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

Figure 19 shows the critical current paths of the high- and low-side driver when their outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the xHB pin and out the xHO pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor C_B. The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor CB must be placed close to the xHB and xHS pins. This capacitor not only provides all the energy for turn-on but it must also keep xHB pin noise and ripple low for proper operation of the high-side drive circuitry.

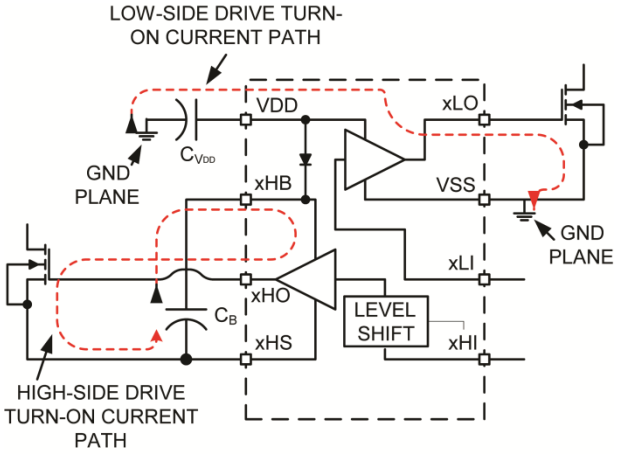


Figure 19. Turn-On Current Paths

Figure 20 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_B.

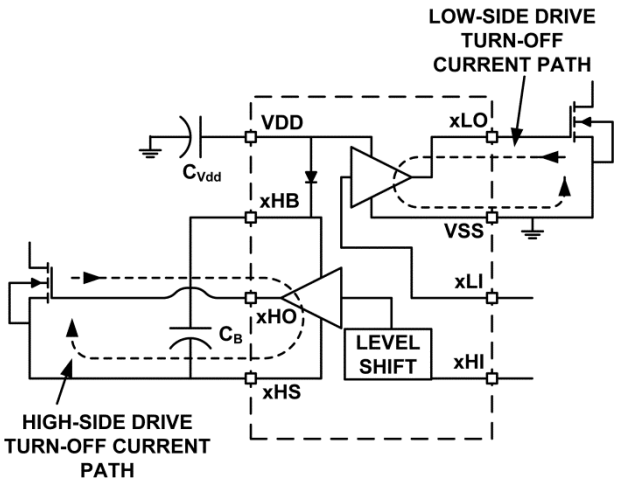


Figure 20. Turn-Off Current Paths

Motor Applications

Figure 21 illustrates an automotive motor application. The 12V battery input voltage can see peaks as high as 60V during a load dump event. The 85V-rated MIC4607drives 6 MOSFETs that provide power to the BLDC motor.

A current-sense resistor senses the peak motor current. The voltage across this resistor is monitored by the OC circuit in the MIC4607, which provides overcurrent protection for the application. The 120V rating of the MIC5281 series of LDOs provide input surge voltage protection, while regulating the battery voltage down to 3.3V and 10V – 12V for the microcontroller and gate driver respectively. This circuit can also be used for power tool applications, where the battery voltage carries high-voltage peaks and surges.

Figure 22 is a block diagram for a 24V motor drive application. The regulated 24V bus allows the use of lower input voltage LDOs, such as the MIC5239-3.3 and MIC5234. This circuit configuration can be used in industrial applications.

Figure 22 illustrates an off-line motor application. Adding an off-line power supply to the front end allow the MIC4607 to be used in applications such as blenders and other small white goods as well as ceiling fan applications. The circuit consists of an MIC38C44 based AC/DC power supply, that is used to generate 24VDC to power a BLDC motor. The MIC4607 drives the six MOSFETs that provide power to the motor.

The MIC4607 can also be used in low and mid-voltage inverter applications. Figure 24 shows how power generated by a spinning (or breaking) motor can be used to generate DC power to a load or provide power for battery-charging applications.

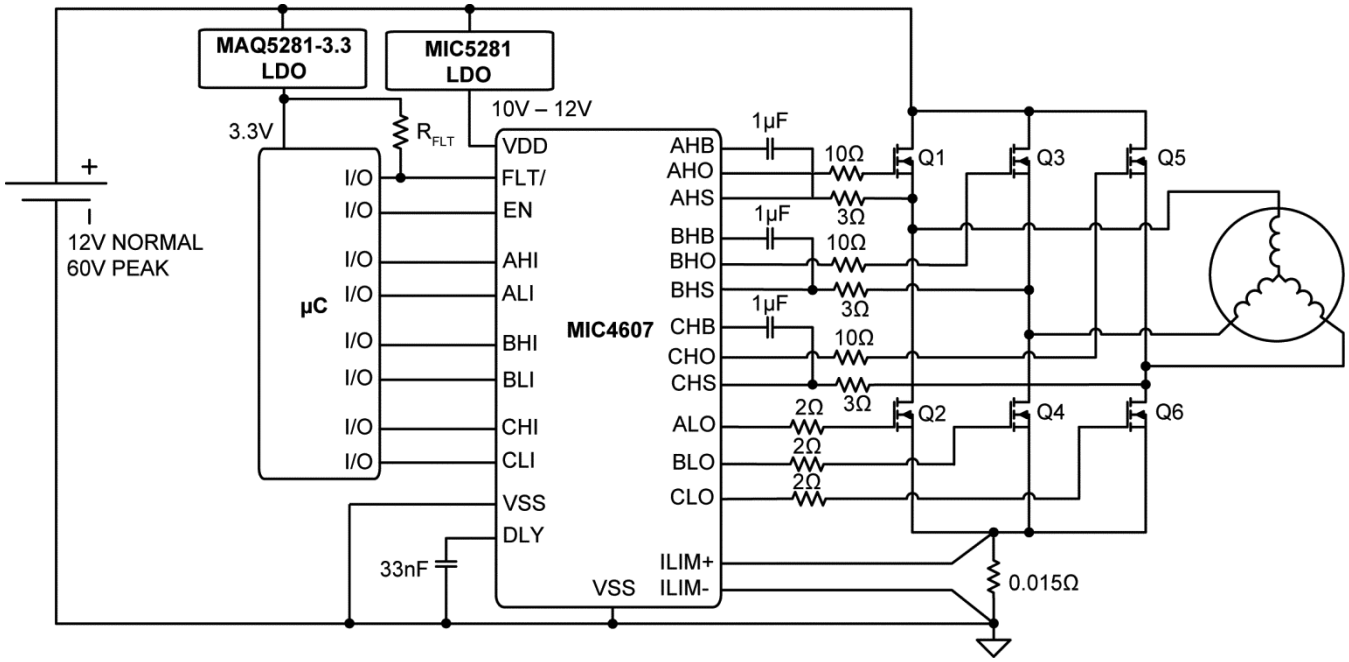


Figure 21. Automotive or Power Tool Application

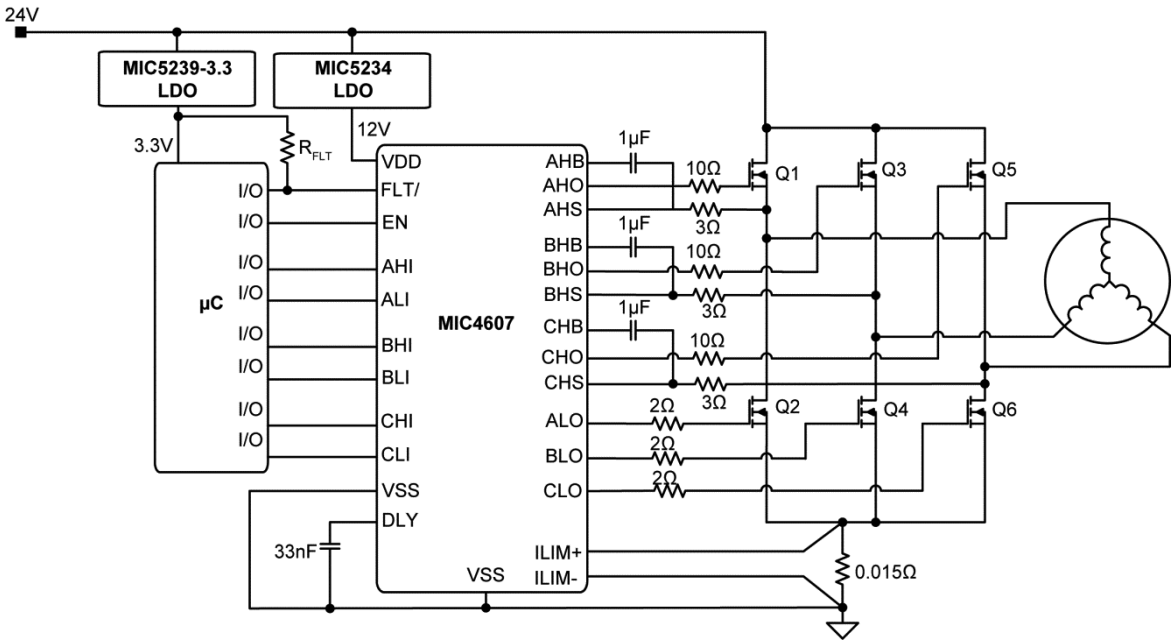


Figure 22. Industrial Motor Driver

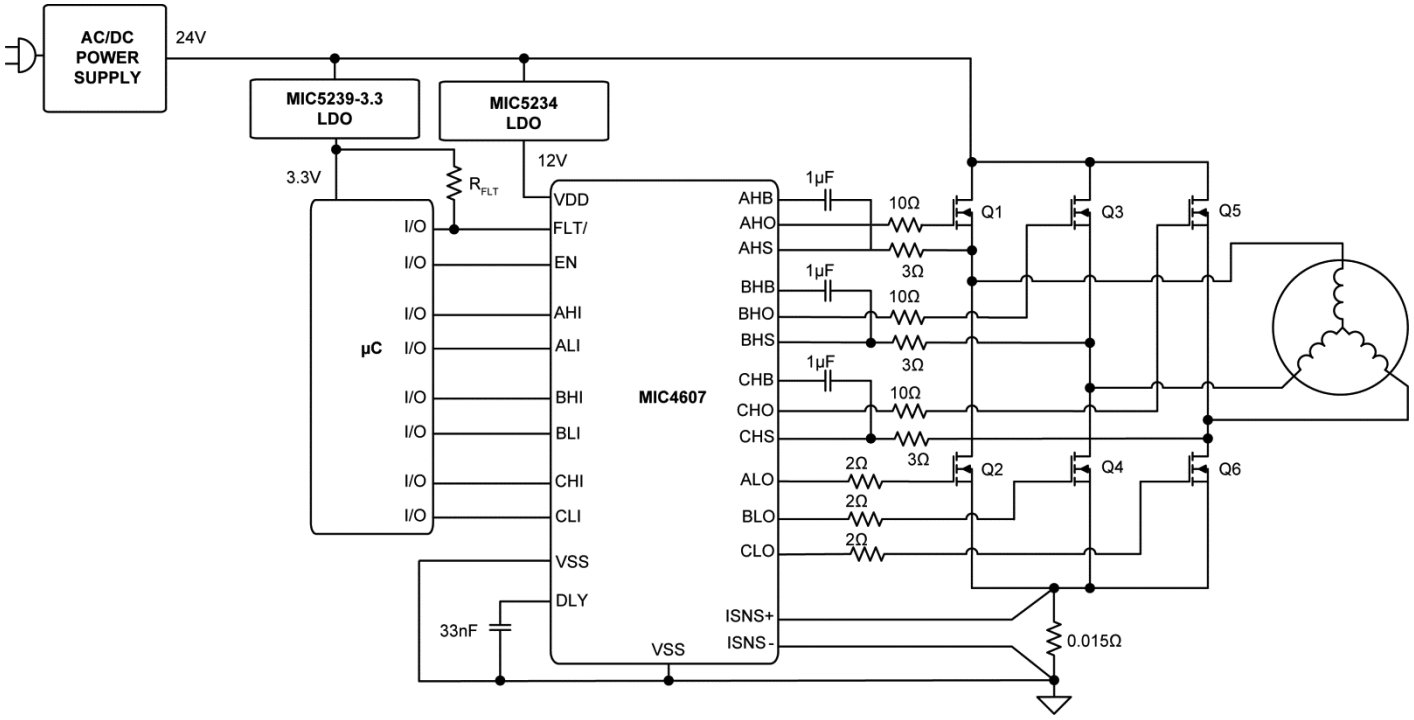


Figure 23. Blender Motor Drive Application Diagram

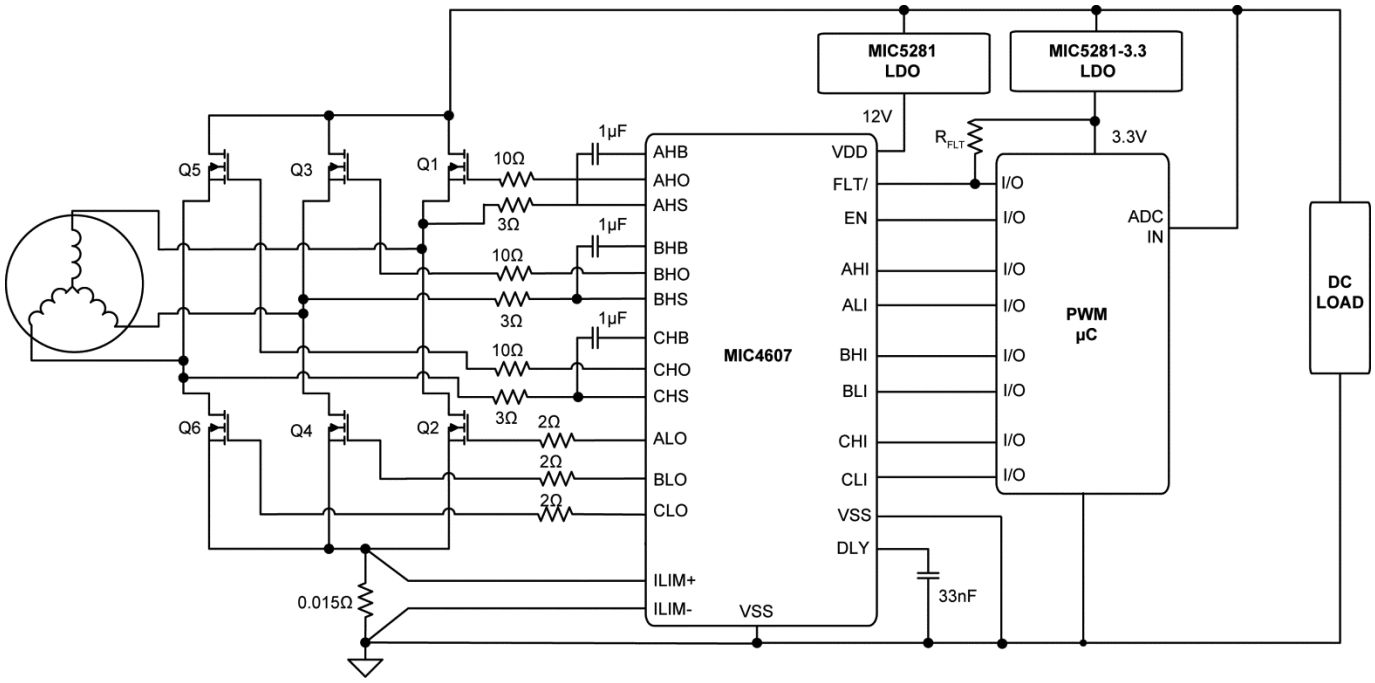
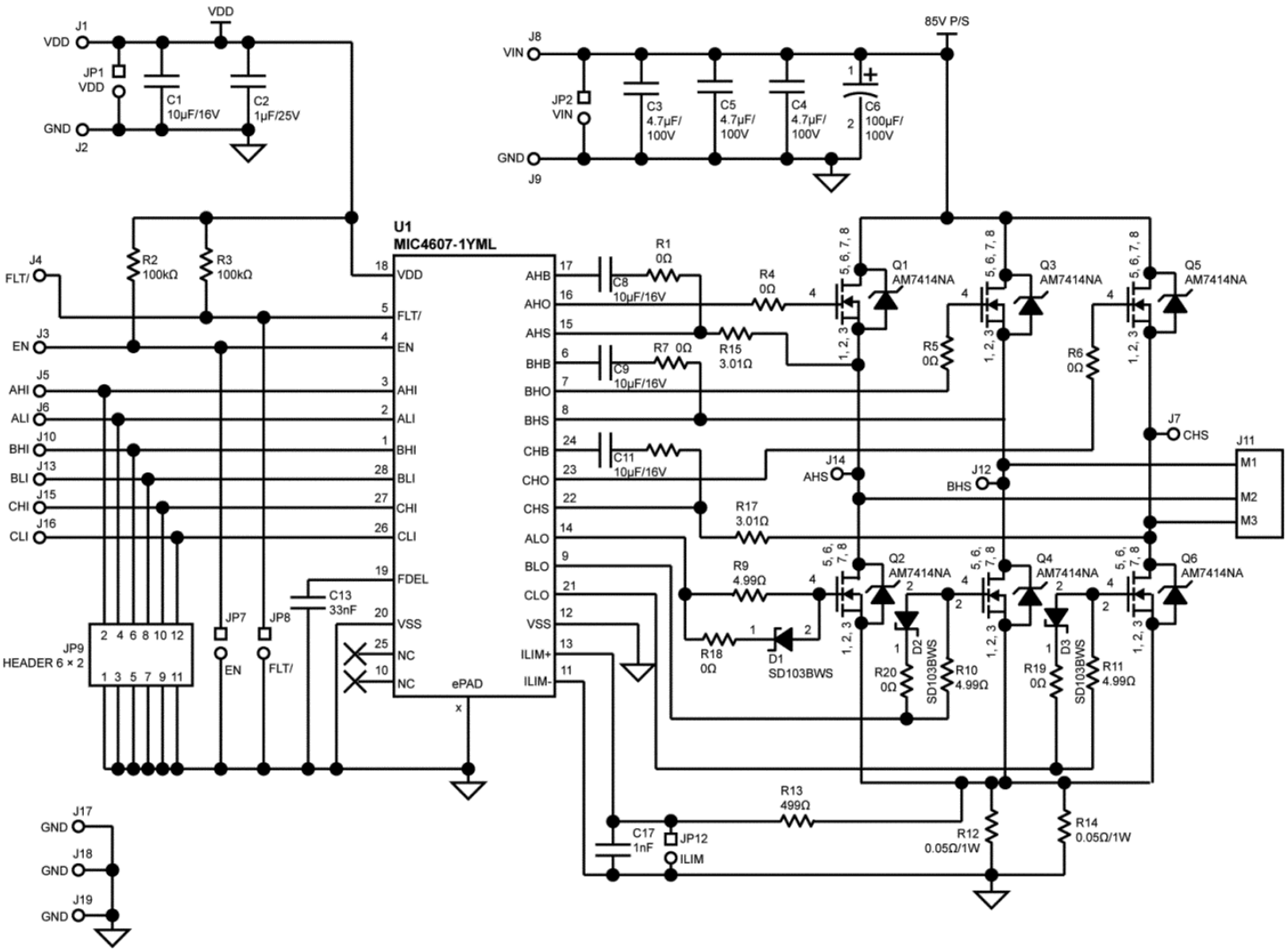


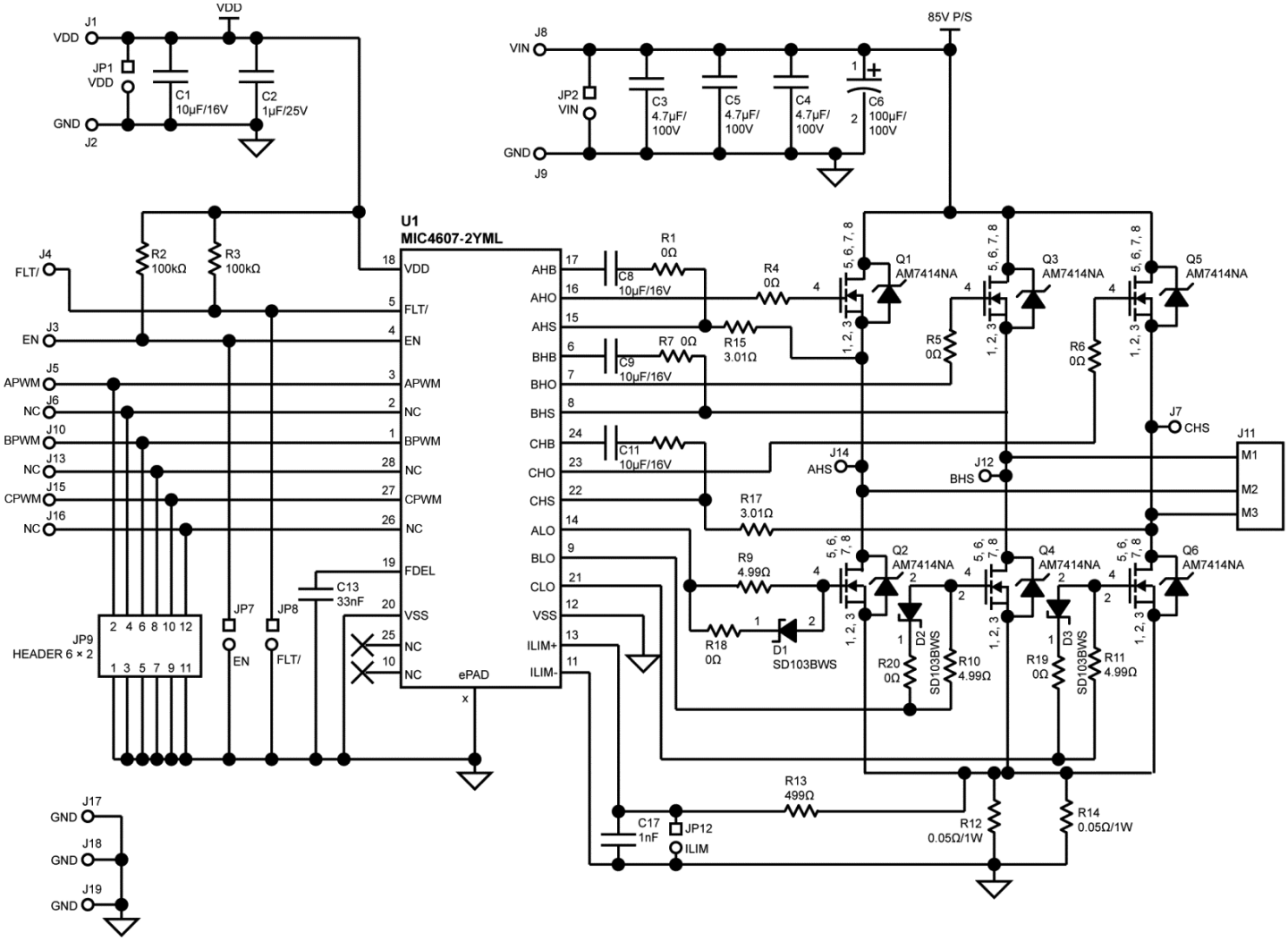
Figure 24. Three-Phase Synchronous Rectification

Typical Application Schematic (MIC4607-1 Version, HI/LI Inputs)



MIC4607–1 Version, HI/LI Inputs

Typical Application Schematic (Continued) (MIC4607-2 Version, PWM Inputs)



MIC4607-2 Version, PWM Inputs

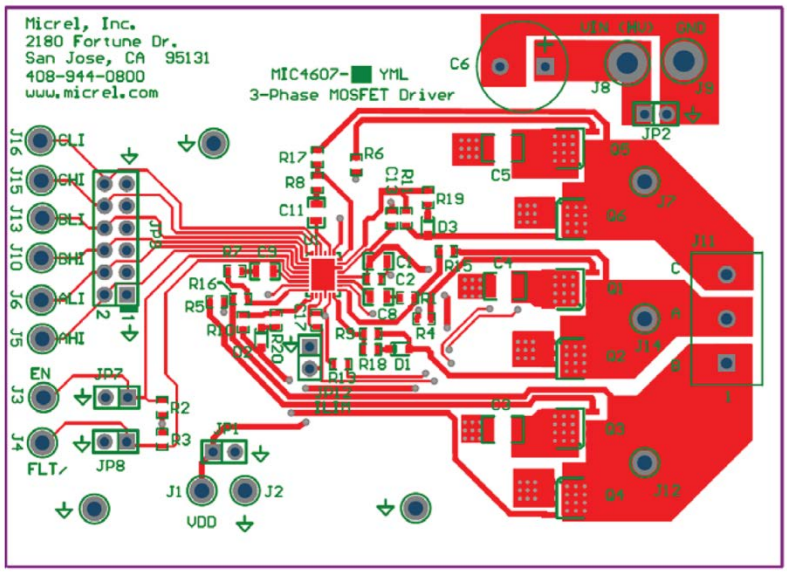
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C8, C9, C11	0805YD106MAT2A	AVX[8]	10µF Ceramic Capacitor, 16V, X5R, Size 0805	4
C2	06033D105MAT2A	AVX	1µF Ceramic Capacitor, 25V, X5R, Size 0603	1
C3, C4, C5	C3225X7S2A475M200AB	TDK[9]	4.7µF Ceramic Capacitor, 100V, X7S, Size 1210	3
C6	B41858-C9107-M000	TDK	100µF Aluminum Electrolytic Capacitor, 100V	1
C13	06035C333MAT2A	AVX	33nF Ceramic Capacitor, 50V, X7R, Size 0603	1
C17	06035C102MAT2A	AVX	1nF Ceramic Capacitor, 50V, X7R, Size 0603	1
Q1, Q2, Q3, Q4, Q5, Q6	AM7414NA	Analog Power[10]	N-Channel MOSFET, 100V	6
R1, R4, R5, R6, R7, R8, R18, R19, R20	CRCW06030000FRT1	Vishay[11]	0Ω, Size 0603	9
R9, R10, R11	CRCW06034R99FRT1	Vishay	4.99Ω, 1%, Size 0603	3
R13	CRCW06034990FRT1	Vishay	499Ω, 1%, Size 0603	1
R2, R3	CRCW06031003FRT1	Vishay	100kΩ, 1%, Size 0603	2
R12, R14	ERJ-L14KF50MU	Panasonic[12]	0.05Ω, 1W, Size 1210	2
R15, R16, R17	CRCW06033R01FRT1	Vishay	3.01Ω, 1%, Size 0603	3
D1, D2, D3	SD103BWS	Diodes, Inc.[13]	Schottky Diode, 30V, 350mA, SOD-323	3
U1	**MIC4607-1YML**	**Micrel, Inc.[14]**	**85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection**	**1**
	MIC4607-2YML			

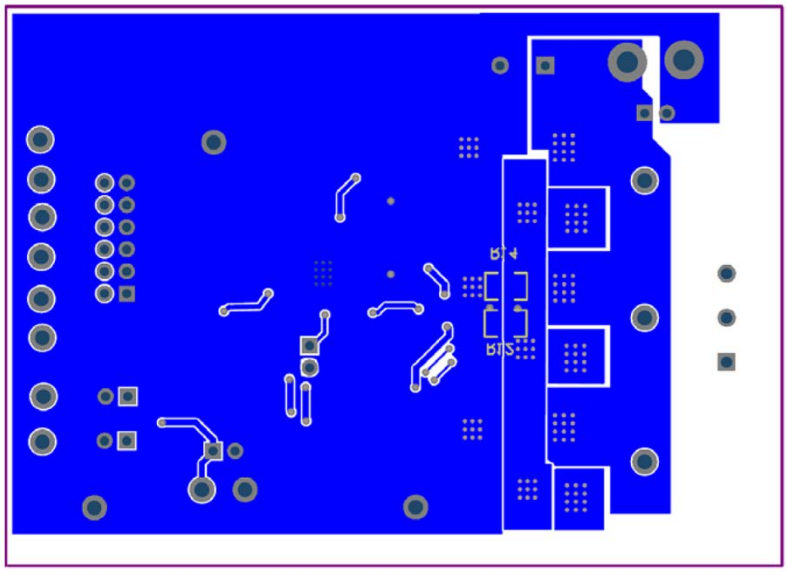
Notes:

8. AVX: www.avx.com.
9. TDK: www.tdk.com.
10. Analog Power: www.analogpowerinc.com.
11. Vishay: www.vishay.com.
12. Panasonic: www.industrial.panasonic.com.
13. Diodes, Inc.: www.diodes.com.
14. **Micrel, Inc.:** www.micrel.com.

PCB Layout Recommendations

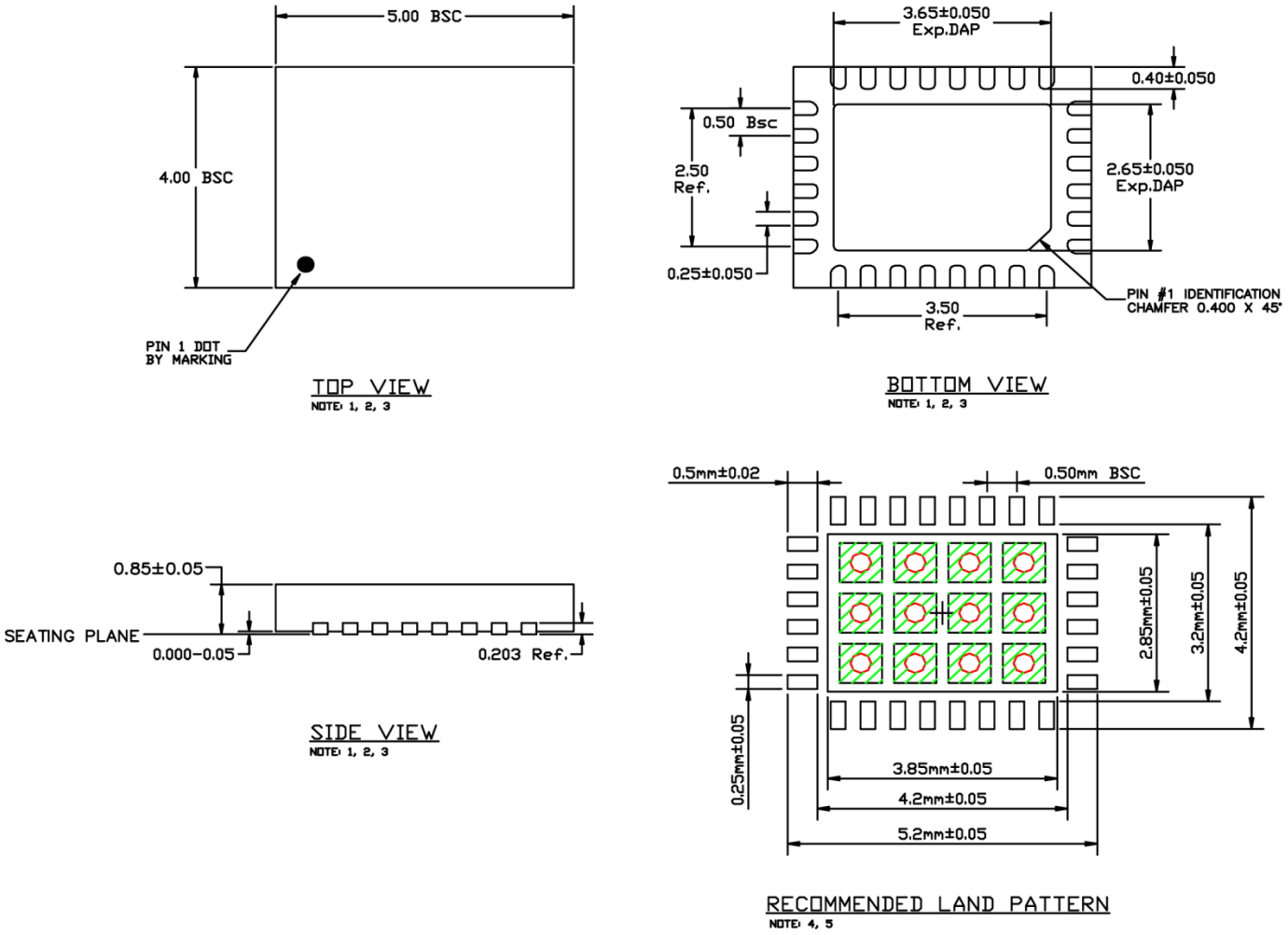


Top Layer



Bottom Layer

Package Information and Recommended Land Pattern[15]



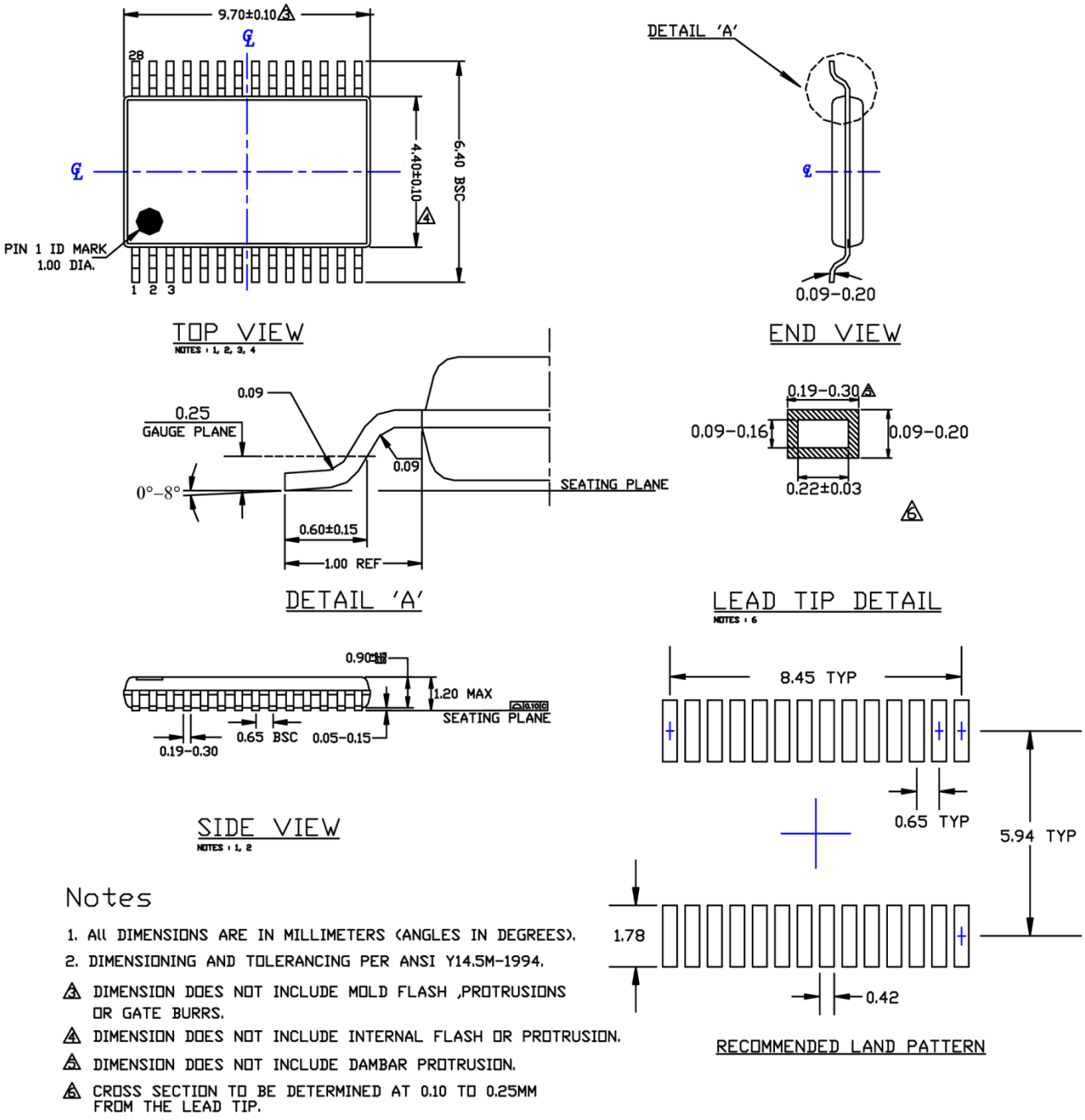
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. 0.91mm Pitch.
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.71mmx0.71mm IN SIZE. 0.20mm Gap.

28-Pin 4mm × 5mm QFN (ML)

Note:

15. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Land Pattern[15] (Continued)



Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH ,PROTRUSIONS OR GATE BURRS.
4. DIMENSION DOES NOT INCLUDE INTERNAL FLASH OR PROTRUSION.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
6. CROSS SECTION TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.

28-Pin TSSOP (TS)

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