MT9P111PACSTCH-GEVB

MT9P111 Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Demo 3 system. Test points and jumpers on the board provide access to the clock, I/Os, and other miscellaneous signals.

Features

- Clock Input
  - Default – 27 MHz Crystal Oscillator
  - Optional Demo 3 Controlled MClk
- Two Wire Serial Interface
  - Selectable Base Address
- Parallel Interface
- MIPI Interface
- ROHS Compliant

Block Diagram

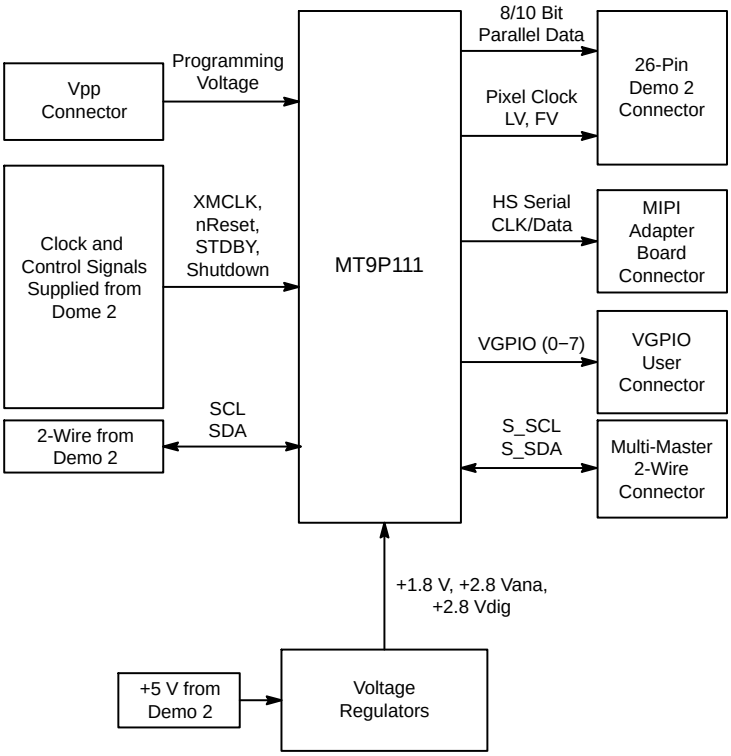
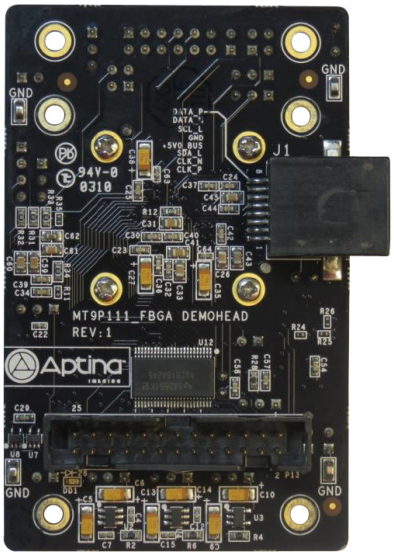


Figure 2. Block Diagram of MT9P111PACSTCH−GEVB

Top View



Bottom View

Figure 1. MT9P111 Evaluation Board

Top View

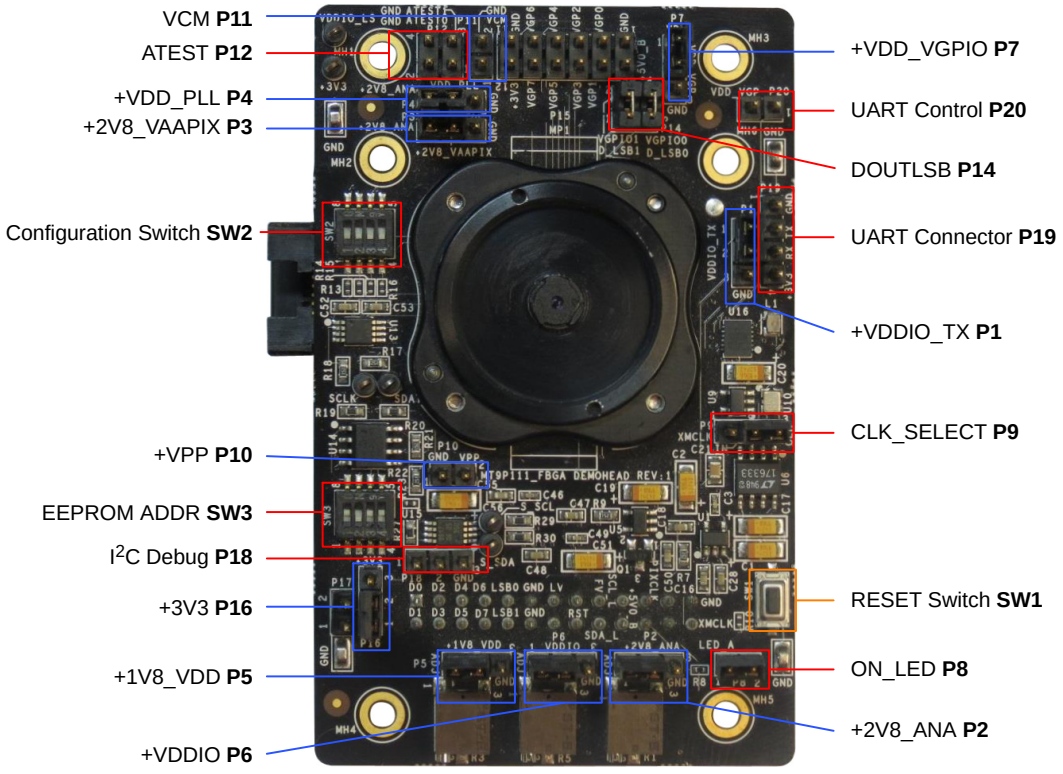


Figure 3. Top View of the Board with Default Jumpers

Bottom View

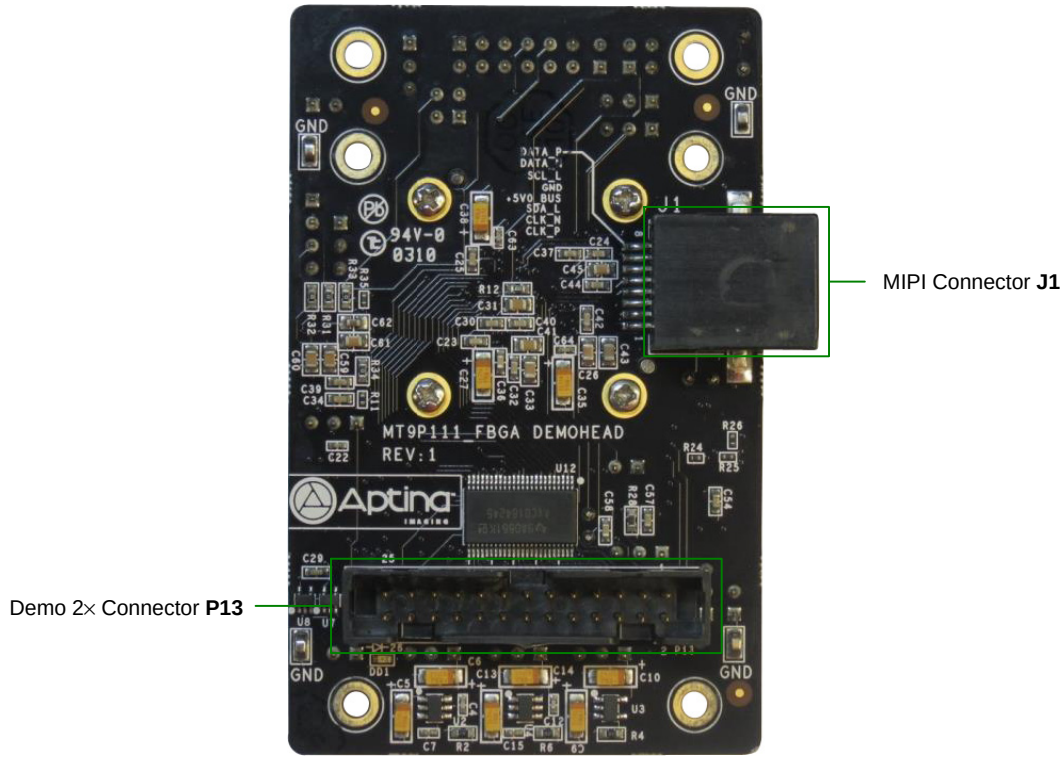


Figure 4. Bottom View of the Board

Jumper Pin Location

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.

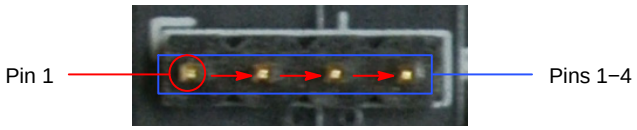


Figure 5. Pin Locations for a Single Jumper. Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right

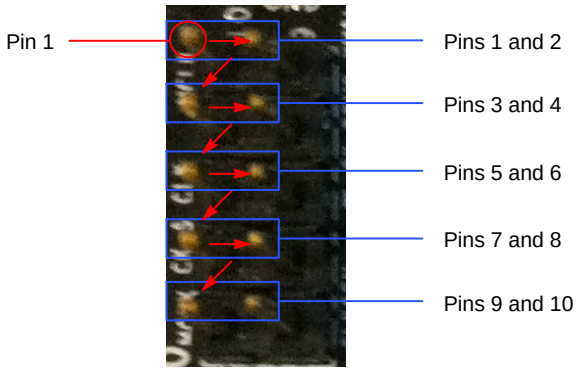


Figure 6. Pin Locations and Assignments of Grouped Jumpers. Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture

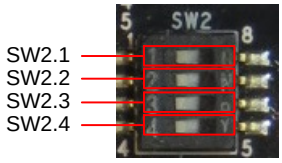


Figure 7. Switches of Configuration Switch SW2 in Their Default Positions. TEST(SW2.1), SADDR(SW2.2), STDBY(SW2.3), and SHUTDOWN(SW2.4) are All Off by Default

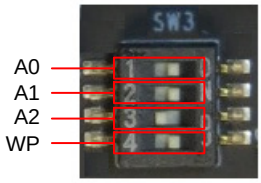


Figure 8. EEPROM Switches in Their Default Positions. The First Switch (A0) of SW3 is ON, the Second Switch (A1) is ON, the Third Switch (A2) is OFF, and the Fourth Switch (WP) is ON

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

Jumper/Header No.	Jumper/Header Name	Pins	Description
P1	+VDDIO_TX	1−2 (Default)	Connects to On-Board +VDDIO_TX Power Supply
		2−3	External Power Supply Connection
P2	+VAA	1−2 (Default)	Connects to On-Board +2V8_ANA Power Supply
		2−3	External Power Supply Connection
P3	+VAAPIX	1−2 (Default)	Connects to On-Board +2V8_ANA Power Supply
		2−3	External Power Supply Connection
P5	+1V8_VDD	1−2 (Default)	Connects to On-Board +1V8_VDD Power Supply
		2−3	External Power Supply Connection
P6	+VDDIO	1−2 (Default)	Connects to On-Board +VDDIO Power Supply
		2−3	External Power Supply Connection
P7	+VDD_VGPIO	1−2 (Default)	Connects to On-Board +VDDIO Power Supply
		2−3	External Power Supply Connection
P8	ON_LED	1−2 (Default)	Connects LED to Power Supply
		Open	LED Off
P9	CLK_SELECT	2−3 (Default)	On-Board 27 MHz Oscillator
		1−2	Connects to XMCLK from Demo2X Board
P10	+VPP	Open (Default)	External Connection of +VPP Power Supply for OTPM
P11	+VCM	Open (Default)	For Connection to External +VCM Power Supply
P12	ATEST	Open (Default)	For Debug/Test
P14	DOUTLSB	1−2, 3−4 (Default)	DOUTLSB[1:0] are Used
		Open	DOUTLSB[1:0] are Not Used
P16	+3V3	2−3 (Default)	Connects to On-Board +3V3 Power Supply
		1−2	External Power Supply Connection
P18	I^2C Debug	Open (Default)	For Debug/Test
P20	UART Control	Open (Default)	UART Shutdown
		1−2	UART Active
SW1	RESET	N/A	When Pushed, 400 ms Reset Signal will be Sent to MT9P017
SW2	Configuration Switch	SW2.1 OFF (Default)	Normal Operation
		SW2.1 ON	Test Mode
		SW2.2 OFF (Default)	I^2C Address set to 0x78
		SW2.2 ON	I^2C Address set to 0x7A
		SW2.3 OFF (Default)	Normal Operation
		SW2.3 ON	Low Power State
		SW2.4 OFF (Default)	Normal Operation
		SW2.4 ON	Lowest Power State
SW3	EEPROM ADDR	A0 ON, A1 ON, A2 OFF, WP ON (Default)	EEPROM Address Set to 0xA8
		A0 OFF, A1 OFF, A2 OFF, WP ON	EEPROM Address Set to 0xAC
		A0 ON, A1 OFF, A2 ON, WP ON	EEPROM Address Set to 0xA4
		A0 ON, A1 ON, A2 ON, WP ON	EEPROM Address Set to 0xA0

Interfacing to ON Semiconductor Demo 2× Baseboard

The ON Semiconductor Demo 2× baseboard has a similar 26-pin connector which mates with P13 of the headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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